Isolated No Opto-Coupler Flyback Controller with Active PFC

FEATURES

- **Isolated PFC Flyback with Minimum Number of External Components**
- **V_{IN} and V_{OUT} Limited Only by External Components**
- **Active Power Factor Correction**
- **Low Harmonic Distortion**
- **No Opto-Coupler Required**
- **Constant-Current and Constant-Voltage Regulation**
- Accurate Regulated Voltage and Current (±5% Typical)
- Energy Star Compliant (<0.5W No Load Operation)
- Thermally Enhanced 16-lead MSOP Package

APPLICATIONS

- Offline 5W to 100W+ Applications
- High DC V_{IN} Isolated Applications
- Offline Bus Converter (12V, 24V or 48V Outputs)

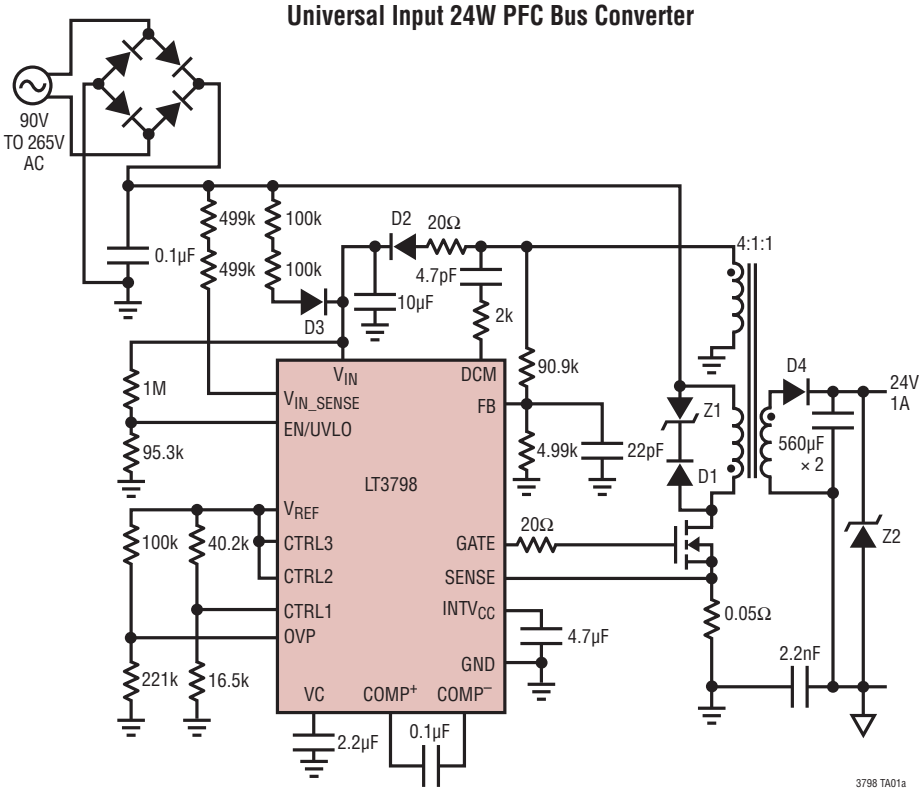
DESCRIPTION

The LT®3798 is a constant-voltage/constant-current isolated flyback controller that combines active power factor correction (PFC) with no opto-coupler required for output voltage feedback into a single-stage converter. A LT3798 based design can achieve a power factor of greater than 0.97 by actively modulating the input current, allowing compliance with most Harmonic Current Emission requirements.

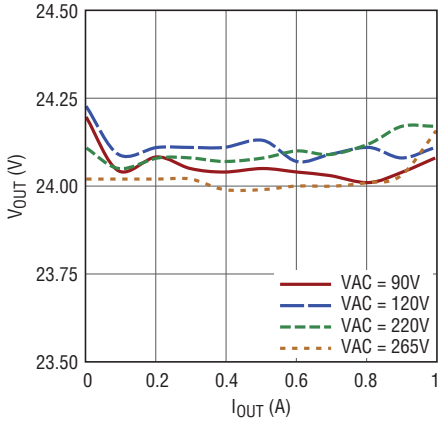
The LT3798 is well suited for a wide variety of off-line applications. The input range can be scaled up or down, depending mainly on the choice of external components. Efficiencies higher than 86% can be achieved with output power levels up to 100W. In addition, the LT3798 can easily be designed into high DC input applications.

TYPICAL APPLICATION

Universal Input 24W PFC Bus Converter



V_{OUT} vs I_{OUT}

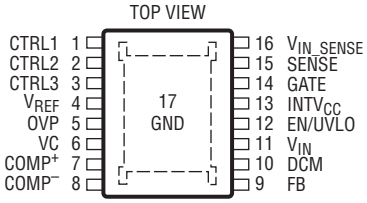


ABSOLUTE MAXIMUM RATINGS

(Note 1)

EN/UVLO.....30V
V_{IN}.....42V
$INTV_{CC}$.....12V
CTRL1, CTRL2, CTRL3.....4V
FB, V_{REF}, $COMP^+$.....3V
VC, OVP, $COMP^-$.....4V
SENSE.....0.4V
V_{IN_SENSE}.....1mA
DCM.....±3mA
Operating Temperature Range (Note 2)
LT3798E/LT3798I.....–40°C to 125°C
Storage Temperature Range.....–65°C to 150°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

θ_{JA} = 50°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3798EMSE#PBF	LT3798EMSE#TRPBF	3798	16-Lead Plastic MSOP	–40°C to 125°C
LT3798IMSE#PBF	LT3798IMSE#TRPBF	3798	16-Lead Plastic MSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 18V, $INTV_{CC}$ = 11V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage Range			10		38	V
V_{IN} Quiescent Current	$V_{EN/UVLO}$ = 0.2V $V_{EN/UVLO}$ = 1.5V, Not Switching		45	60 70	70	µA µA
V_{IN} Quiescent Current, $INTV_{CC}$ Overdriven	V_{INTVCC} = 11V			60		µA
V_{IN} Shunt Regulator Voltage	I = 1mA			40		V
V_{IN} Shunt Regulator Current Limit				8		mA
$INTV_{CC}$ Quiescent Current	$V_{EN/UVLO}$ = 0.2V $V_{EN/UVLO}$ = 1.5V, Not Switching		12.5 1.8	15.5 2.2	17.5 2.7	µA mA
EN/UVLO Pin Threshold	EN/UVLO Pin Voltage Rising	●	1.21	1.25	1.29	V
EN/UVLO Pin Hysteresis Current	EN/UVLO=1V		8	10	12	µA
V_{IN_SENSE} Threshold	Turn Off			27		µA
V_{REF} Voltage	0 µA Load 200µA Load	● ●	1.97 1.95	2.0 1.98	2.03 2.03	V V
CTRL1/CTRL2/CTRL3 Pin Bias Current	CTLR1/CTRL2/CTRL3 = 1V				±30	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 18V, $INTV_{CC}$ = 11V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SENSE Current Limit Threshold	V_{IN_SENSE} = 150µA		96	102	107	mV
Minimum SENSE Current Limit Threshold	V_{IN_SENSE} = 34µA			14		mV
Minimum SENSE Current Limit Threshold	V_{IN_SENSE} = 21µA			4		mV
SENSE Input Bias Current	Current Out of Pin, SENSE = 0V			15		µA
FB Voltage		●	1.22	1.25	1.28	V
FB voltage Line Regulation	10V < V_{IN} < 35V			0.01	0.03	%/V
FB Pin Bias Current	(Note 3), FB = 1V		4.05	4.25	4.4	µA
FB Error Amplifier Voltage Gain	$\Delta V_{VC}/\Delta V_{FB}$, CTRL1=1V, CTRL2=2V, CTRL3=2V			180		V/V
FB Error Amplifier Transconductance	ΔI = 5µA			170		UMHOS
Current Error Amplifier Voltage Gain	$\Delta V_{COMP}+/\Delta V_{COMP}–$, CTRL1 = 1V, CTRL2 = 2V, CTRL3 = 2V			100		V/V
Current Error Amplifier Transconductance	ΔI = 5µA			50		UMHOS
Current Loop Voltage Gain	$\Delta V_{CTRL}/\Delta V_{SENSE}$,1000pF Cap from $COMP^+$ to $COMP^–$			21		V/V
DCM Current Turn-On Threshold	Current Out of Pin			80		µA
Maximum Oscillator Frequency	$COMP^+$ = 0.95V, V_{IN_SENSE} = 150µA			150		kHz
Minimum Oscillator Frequency	$COMP^+$ = 0V, V_{FB} <V_{OVP}			4		kHz
Minimum Oscillator Frequency	$COMP^+$ = 0V, V_{FB} >V_{OVP}			0.5		kHz
Backup Oscillator Frequency				20		kHz
Linear Regulator						
$INTV_{CC}$ Regulation Voltage	No Load		9.8	10	10.4	V
Dropout (V_{IN}-$INTV_{CC}$)	I_{INTVCC} = –10mA, V_{IN} = 10V			500	900	mV
Current Limit	Below Undervoltage Threshold		12	25		mA
Current Limit	Above Undervoltage Threshold		80	120		mA
Gate Driver						
t_r GATE Driver Output Rise Time	C_L = 3300pF, 10% to 90%			18		ns
t_f GATE Driver Output Fall Time	C_L = 3300pF, 90% to 10%			18		ns
GATE Output Low (V_{OL})					0.01	V
GATE Output High (V_{OH})			$INTV_{CC}$- 50mV			V

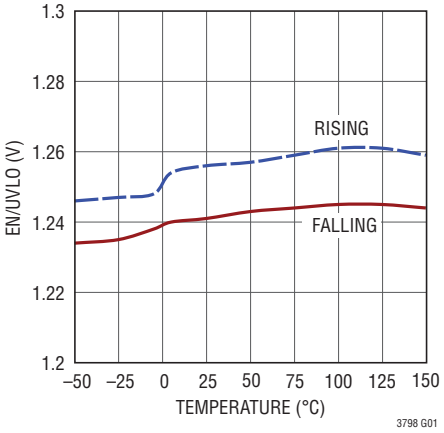
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3798E is guaranteed to meet specified performance from 0°C to 125°C junction temperature. Specification over the –40°C and 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The 3798I is guaranteed to meet specified performance from –40°C to 125°C operating junction temperature range.

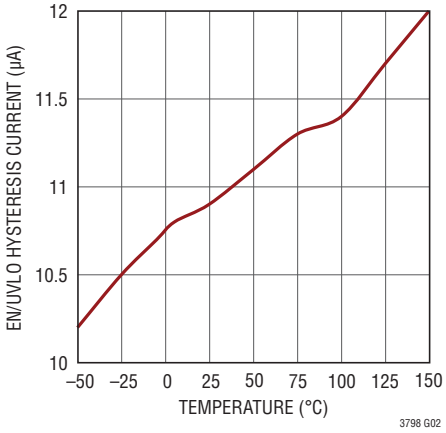
Note 3: Current flows out of the FB pin.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

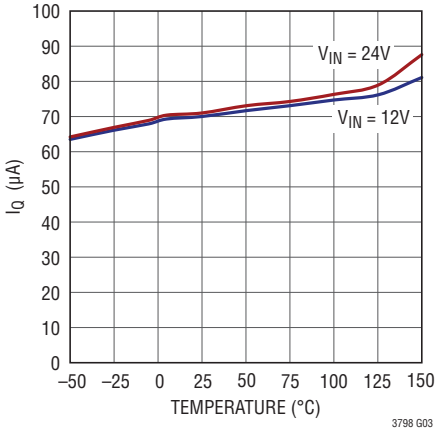
EN/UVLO Threshold vs Temperature



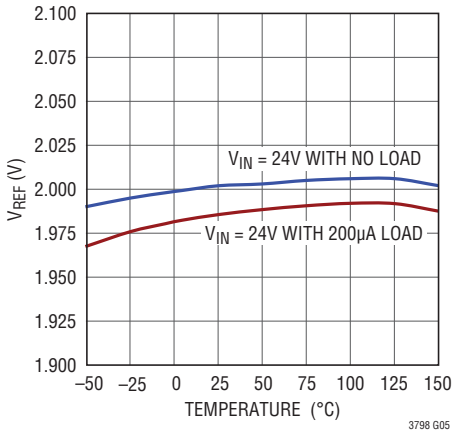
EN/UVLO Hysteresis Current vs Temperature



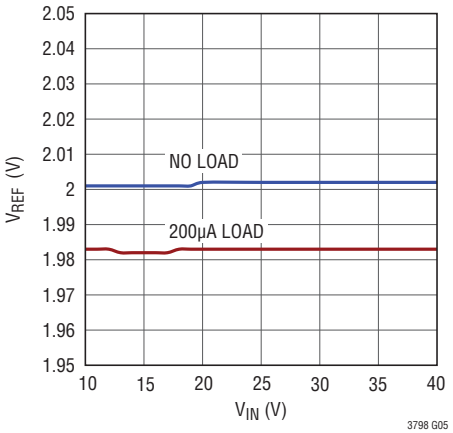
V_{IN} I_Q vs Temperature



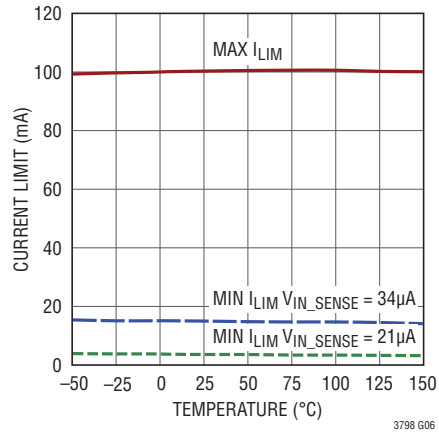
V_{REF} vs Temperature



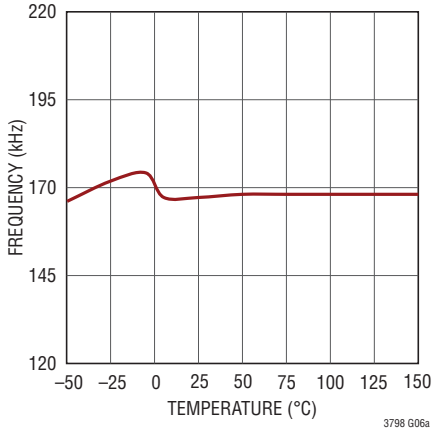
V_{REF} vs V_{IN}



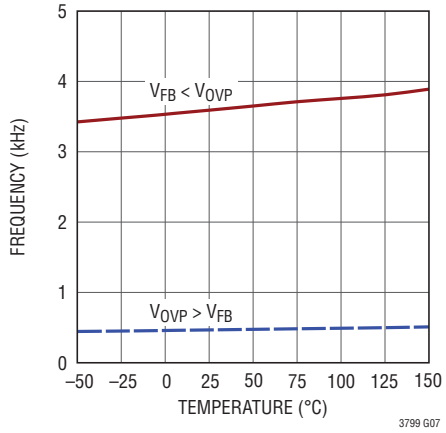
SENSE Current Limit Threshold vs Temperature



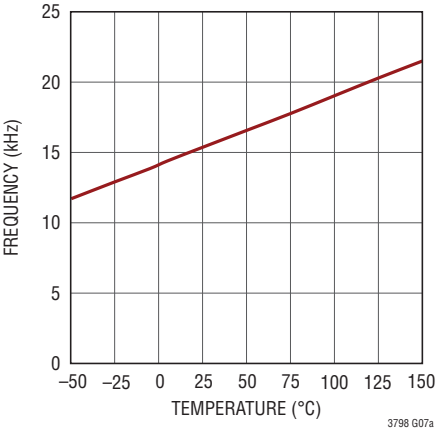
Maximum Oscillator Frequency vs Temperature



Minimum Oscillator Frequency vs Temperature

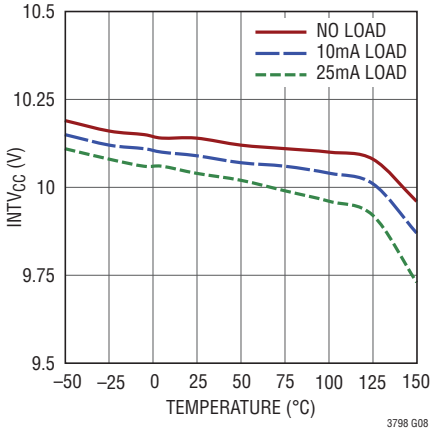


Backup Oscillator Frequency vs Temperature

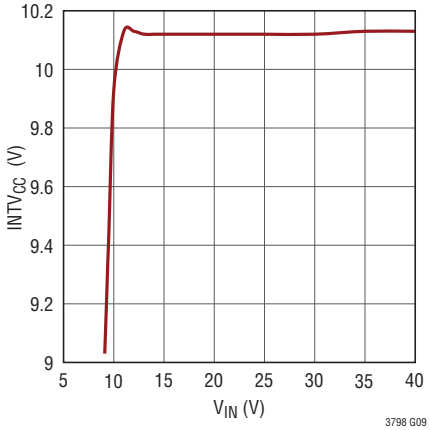


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

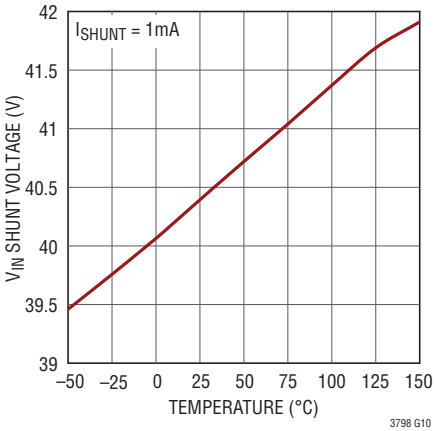
$INTV_{CC}$ vs Temperature



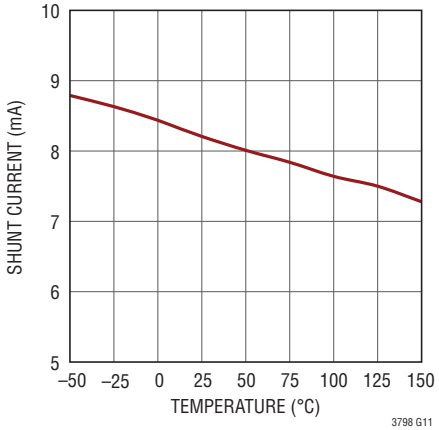
$INTV_{CC}$ vs V_{IN}



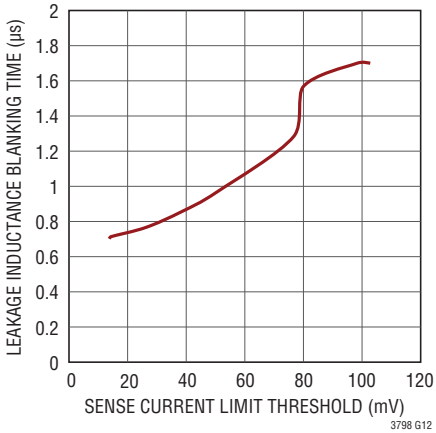
V_{IN} Shunt Voltage vs Temperature



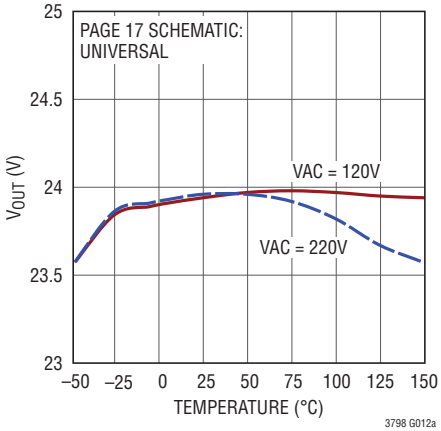
Maximum Shunt Current vs Temperature



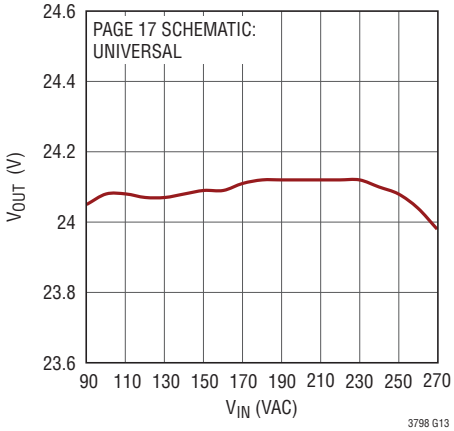
Leakage Inductance Blanking Time vs SENSE Current Limit Threshold



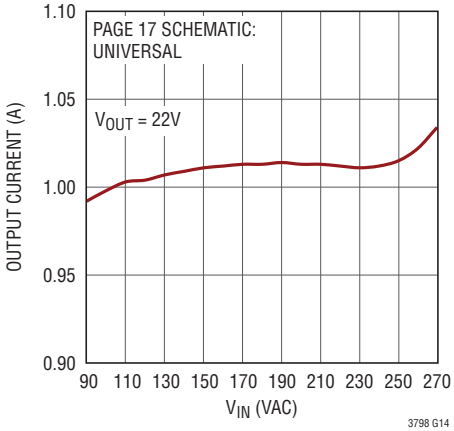
V_{OUT} vs Temperature



Output Voltage vs Input Voltage

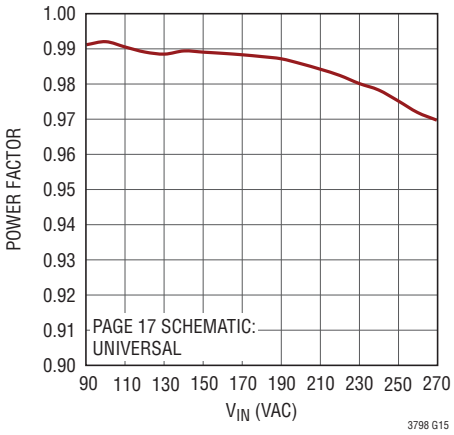


Output Current vs Input Voltage

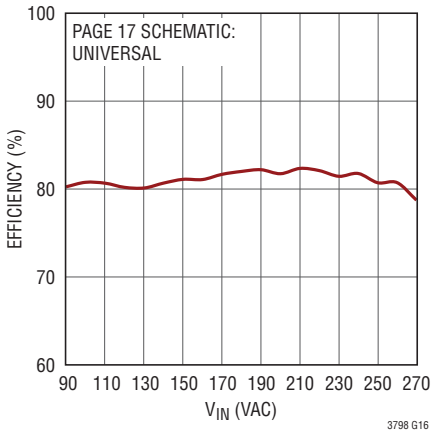


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Power Factor vs Input Voltage



Efficiency vs Input Voltage



PIN FUNCTIONS

CTRL1, CTRL2, CTRL3 (Pin 1, Pin 2, Pin 3): Current Output Adjustment Pins. These pins control the output current. The lowest value out of the three CTRL inputs is compared to negative input of the operational amplifier.

V_{REF} (Pin 4): Voltage Reference Output Pin. Typically 2V. This pin drives a resistor divider for the CTRL pin, either for analog dimming or for temperature limit/compensation of output load. Can supply up to 200µA.

OVP (Pin 5): Overvoltage Protection. This pin accepts a DC voltage to compare to the sample and hold's voltage output information. When output voltage information is above the OVP, the part divides the minimum switching frequency by 8, around 500Hz. This protects devices connected to the output. This also allows the part to operate with very little power consumption with no load to meet energy star requirements.

VC (Pin 6): Compensation Pin for Internal Error Amplifier. Connect a series RC from this pin to ground to compensate the switching regulator. A 100pF capacitor in parallel helps eliminate noise.

$COMP^+$, $COMP^-$ (Pin 7, Pin 8): Compensation Pins for Internal Error Amplifier. Connect a capacitor between these two pins to compensate the internal feedback loop.

FB (Pin 9): Voltage Loop Feedback Pin. FB is used to regulate the output voltage by sampling the third winding. If the converter is used in current mode, the FB pin will normally be at a voltage level lower than 1.25V, and will reach the steady state of 1.25V if it detects an open output condition.

DCM (Pin 10): Discontinuous Conduction Mode Detection Pin. Connect a capacitor and resistor in series with this pin to the third winding.

V_{IN} (Pin 11): Input Voltage. This pin supplies current to the internal start-up circuitry and to the $INTV_{CC}$ LDO. This pin must be locally bypassed with a capacitor. A 42V shunt regulator is internally connected to this pin.

EN/UVLO (Pin 12): Enable/Undervoltage Lockout. A resistor divider connected to V_{IN} is tied to this pin to program the minimum input voltage at which the LT3798 will turn on. When below 1.25V, the part will draw 60µA with most of the internal circuitry disabled and a 10µA hysteresis current will be pulled out of the EN/UVLO pin. When above 1.25V, the part will be enabled and begin to switch and the 10µA hysteresis current is turned off.

$INTV_{CC}$ (Pin 13): Regulated Supply for Internal Loads and GATE Driver. Supplied from V_{IN} and regulates to 10V (typical). $INTV_{CC}$ must be bypassed with a 4.7µF capacitor placed close to the pin.

PIN FUNCTIONS

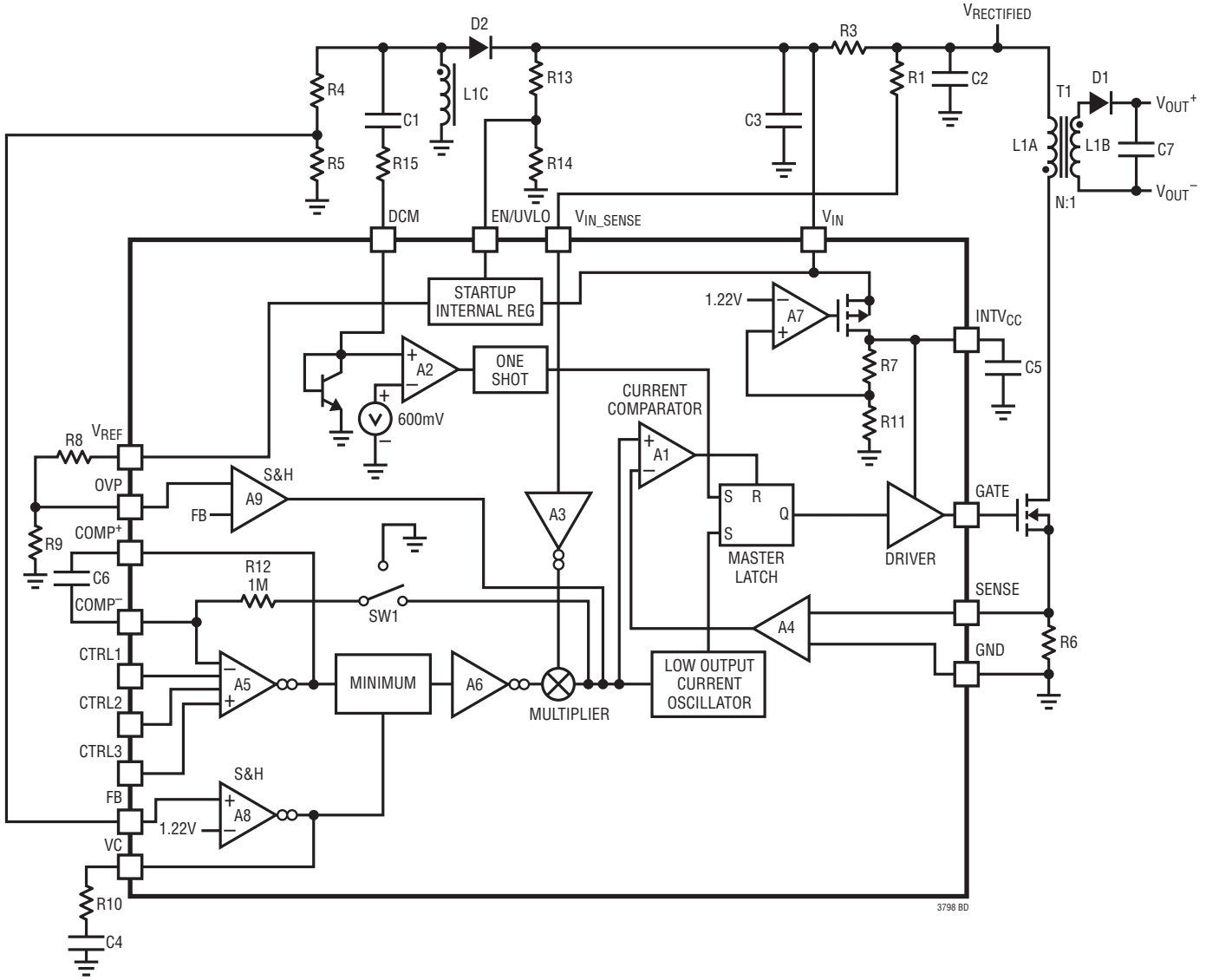
GATE (Pin 14): N-Channel FET Gate Driver Output. Switches between $INTV_{CC}$ and GND. Driven to GND during shutdown state and stays high during low voltage states.

SENSE (Pin 15): The Current Sense Input for the Control Loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor, R_{SENSE}, in the source of the NFET. The negative terminal of the current sense resistor should be connected to the GND plane close to the IC.

V_{IN_SENSE} (Pin 16): Line Voltage Sense Pin. The pin is used for sensing the AC line voltage to perform power factor correction. Connect a resistor in series with the line voltage to this pin. If no PFC is needed, connect this pin to $INTV_{CC}$ with a 25k resistor.

GND (Exposed Pad Pin 17): Ground. The exposed pad of the package provides both electrical contact to ground and good thermal contact to the printed circuit board. The exposed pad must be soldered to the circuit board for proper operation.

BLOCK DIAGRAM



OPERATION

The LT3798 is a current mode switching controller IC designed specifically for generating a constant current/constant voltage supply in an isolated flyback topology. The special problem normally encountered in such circuits is that information relating to the output voltage and current on the isolated secondary side of the transformer must be communicated to the primary side in order to maintain regulation. Historically, this has been done with an opto-isolator. The LT3798 uses a novel method of using the external MOSFETs peak current information from the sense resistor to calculate the output current of a flyback converter without the need of an opto-coupler.

Active power factor correction is becoming a requirement for offline power supplies and the power levels are decreasing. A power factor of one is achieved if the current drawn is proportional to the input voltage. The LT3798 modulates the peak current limit with a scaled version of the input voltage. This technique can provide power factors of 0.97 or greater.

The Block Diagram shows an overall view of the system. The external components are in a flyback topology configuration. The third winding senses the output voltage and also supplies power to the part in steady-state operation. The V_{IN} pin supplies power to an internal LDO that generates 10V at the $INTV_{CC}$ pin. The novel control circuitry consists of two error amplifiers, a minimum circuit, a multiplier, a transmission gate, a current comparator, a low output current oscillator and a master latch, which will be explained in the following sections. The part also features a sample-and-hold to sample the output voltage from the third winding. A comparator is used to detect discontinuous conduction mode (DCM) with a cap connected to the third winding. The part features a 1.9A gate driver.

The LT3798 is designed for both off-line and DC applications. The EN/UVLO and a resistor divider can be configured for a micropower hysteretic start-up. In the Block Diagram, R3 is used to stand off the high voltage supply voltage. The internal LDO starts to supply current to the $INTV_{CC}$ when V_{IN} is above 2.5V. The V_{IN} and $INTV_{CC}$ capacitors are charged by the current from R3. When V_{IN} exceeds the turn-on threshold and $INTV_{CC}$ is in regulation at 10V, the part begins to switch. The V_{IN} hysteresis is set by the EN/UVLO resistor divider. The third winding provides power to V_{IN} when its voltage is higher than the V_{IN} voltage. A voltage shunt is provided for fault protection and can sink 8mA of current when V_{IN} is over 40V.

During a typical cycle, the gate driver turns the external MOSFET on and a current flows through the primary winding. This current increases at a rate proportional to the input voltage and inversely proportional to the magnetizing inductance of the transformer. The control loop determines the maximum current and the current comparator turns the switch off when the current level is reached. When the switch turns off, the energy in the core of the transformer flows out the secondary winding through the output diode, D1. This current decreases at a rate proportional to the output voltage. When the current decreases to zero, the output diode turns off and voltage across the secondary winding starts to oscillate from the parasitic capacitance and the magnetizing inductance of the transformer. Since all windings have the same voltage across them, the third winding rings too. The capacitor connected to the DCM pin, C1, trips the comparator A2, which serves as a dv/dt detector, when the ringing occurs. This timing information is used to calculate the output current and will be described below. The dv/dt detector waits for the ringing waveform to reach its minimum value and then the switch turns back on. This switching behavior is similar to zero volt switching and minimizes the amount of energy lost when the switch is turned back on and improves efficiency as much as 5%. Since this part operates on the edge of continuous conduction mode and discontinuous conduction mode, the operating mode is called critical conduction mode (or boundary conduction mode).

Primary Side Control Loops

The LT3798 achieves constant current/constant voltage operation by using two separate error amplifiers. These two amplifiers are then fed to a circuit that outputs the lower voltage of the two, shown as the "minimum" block in the Block Diagram. This voltage is converted to a current before being fed into the multiplier.

OPERATION

Primary Side Current Control Loop

The CTRL1/CTRL2/CTRL3 pins control the output current of the flyback controller. To simplify the loop, let's assume the V_{IN_SENSE} pin is held at a constant voltage above 1V eliminating the multiplier from the control loop. The error amplifier, A5, is configured as integrator with the external capacitor C6. The COMP+ node voltage is converted to a current into the multiplier with the V/I converter, A6. Since A7's output is constant, the output of the multiplier is proportional to A6 and can be ignored. The output of the multiplier controls the peak current with its connection to the current comparator, A1. The output of the multiplier is also connected to the transmission gate, SW1, and to a 1M resistor. The transmission gate, SW1, turns on when the secondary current flows to the output capacitor. This is called the flyback period when the output diode D1 is on. The current through the 1M resistor gets integrated by A5. The lowest CTRL input is equal to the negative input of A5 in steady state.

A current output regulator normally uses a sense resistor in series with the output current and uses a feedback loop to control the peak current of the switching converter. In this isolated case, the output current information is not available so instead the LT3798 calculates it using the information available on the primary side of the transformer. The output current may be calculated by taking the average of the output diode current. As shown in Figure 1, the diode current is a triangle waveform with a base of the flyback time and a height of the peak secondary winding current. In a flyback topology, the secondary winding current is N times the primary winding current, where N_{PS} is the primary to secondary winding ratio. Instead of taking the area of the triangle, let's think of it as a pulse width modulation (PWM) waveform. During the flyback time, the average current is half the peak secondary winding current and zero during the rest of the cycle. The equation to express the output current is:

$$I_{OUT} = 0.5 \bullet I_{PK} \bullet N_{PS} \bullet D$$

where D is equal to the percentage of the cycle that the flyback time represents. The LT3798 has access to the primary winding current, the input to the current comparator, and when the flyback time starts and ends. Now the output current can be calculated by averaging a PWM

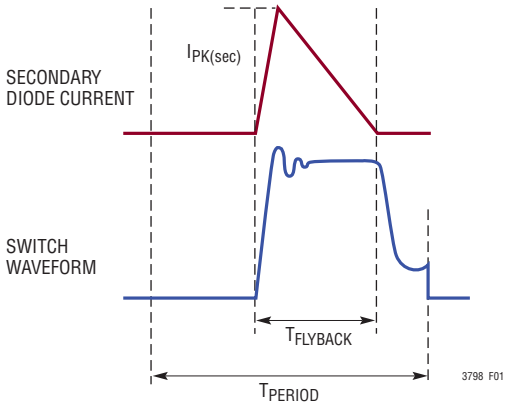


Figure 1. Secondary Diode Current and Switch Waveforms

waveform with a height of the current limit and a duty cycle of the flyback time over the entire cycle. In the feedback loop described above, the input to the integrator is such a waveform. The integrator adjusts the peak current until calculated output current equals the control voltage. If the calculated output current is low compared to the control pin, the error amplifier increases the voltage on the COMP+ node thus increasing the current comparator input.

Primary Side Voltage Control

The output voltage is available through the third winding on the primary side. A resistor divider attenuates the output voltage for the voltage error amplifier. A sample-and-hold circuit samples the attenuated output voltage and feeds it to the error amplifier. The output of the error amplifier is the VC pin. This node needs a capacitor to compensate the output voltage control loop.

Power Factor Correction

When the V_{IN_SENSE} voltage is connected to a resistor divider of the supply voltage, the current limit is proportional to the supply voltage. The minimum of the two error amplifier outputs is multiplied with the V_{IN_SENSE} pin voltage. If the LT3798 is configured with a fast control loop, slower changes from the V_{IN_SENSE} pin would not interfere with the current limit or the output current. The COMP+ pin would adjust to the changes of the V_{IN_SENSE}. The only way for the multiplier to function is to set the control loop to be an order of magnitude slower than the fundamental frequency of the V_{IN_SENSE} signal. In an offline case, the

OPERATION

fundamental frequency of the supply voltage is 120Hz so the control loop unity gain frequency needs to be set less than approximately 12Hz. Without a large amount of energy storage on the secondary side, the output current will be affected by the supply voltage changes, but the DC component of the output current will be accurate. For DC input or non-PFC AC input applications, connect a 25k resistor from V_{IN_SENSE} to $INTV_{CC}$ instead of the AC line voltage.

Startup

The LT3798 uses a hysteretic start-up to operate from high offline voltages. A resistor connected to the supply voltage protects the part from high voltages. This resistor is connected to the V_{IN} pin on the part and bypassed with a capacitor. When the resistor charges the V_{IN} pin to a turn-on voltage set with the EN/UVLO resistor divider and the $INTV_{CC}$ pin is at its regulation point, the part begins to switch. The resistor cannot provide power for the part in steady state, but relies on the capacitor to start-up the part, then the third winding begins to provide power to the V_{IN} pin along with the resistor. An internal voltage clamp is attached to the V_{IN} pin to prevent the resistor current from allowing V_{IN} to go above the absolute maximum voltage of the pin. The internal clamp is set at 40V and is capable of 8mA(typical) of current at room temperature.

Setting the V_{IN} Turn-On and Turn-Off Voltages

A large voltage difference between the V_{IN} turn-on voltage and the V_{IN} turn-off voltage is preferred to allow time for the third winding to power the part. The EN/UVLO sets these two voltages. The pin has a 10µA current sink when the pins voltage is below 1.25V and 0µA when above 1.25V. The V_{IN} pin connects to a resistor divider as shown in Figure 2. The UVLO threshold for V_{IN} rising is:

$$V_{IN(UVLO,RISING)} = \frac{1.25V \bullet (R1+R2)}{R2} + 10\mu A \bullet R1$$

The UVLO Threshold for V_{IN} Falling is:

$$V_{IN(UVLO,FALLING)} = \frac{1.25V \bullet (R1+R2)}{R2}$$

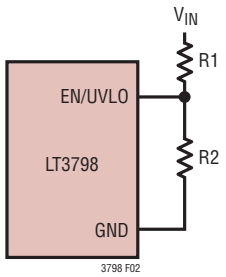


Figure 2. Undervoltage Lockout (UVLO)

Programming Output Voltage

The output voltage is set using a resistor divider from the third winding to the FB pin. From the Block Diagram, the resistors R4 and R5 form a resistor divider from the third winding. The FB also has an internal current source that compensates for the diode drop. This current source causes an offset in the output voltage that needs to be accounted for when setting the output voltage. The output voltage equation is:

$$V_{OUT} = V_{BG}\,(R4+R5)/(N_{ST} \bullet R5) - (V_F + (R4 \bullet I_{TC})/N_{ST})$$

where V_{BG} is the internal reference voltage, N_{ST} is the winding ratio between the secondary winding and the third winding, V_F is the forward drop of the output rectifying diode, and I_{TC} is the internal current source for the FB pin.

The temperature coefficient of the diode's forward drop needs to be the opposite of the term, $(R4 \bullet I_{TC})/N_{ST}$. By taking the partial derivative with respect to temperature, the value of R4 is found to be the following:

$$R4 = N_{ST}(1/(\delta I_{TC}/\delta T)(\delta V_F/\delta T))$$

$$\delta I_{TC}/\delta T = 12.4nA/°C$$

$$I_{TC} = 4.25\mu A$$

where $\delta I_{TC}/\delta T$ is the partial derivative of the I_{TC} current source, and $\delta V_F/\delta T$ is the partial derivative of the forward drop of the output rectifying diode.

With R4 set with the above equation, the resistor value for R5 is found using the following:

$$R5 = (V_{BG} \bullet R4)/(N_{ST}(V_{OUT}+V_F)+R4 \bullet I_{TC}-V_{BG})$$

OPERATION

Programming Output Current

The maximum output current depends on the supply voltage and the output voltage in a flyback topology. With the V_{IN_SENSE} pin connected to 100µA current source and a DC supply voltage, the maximum output current is determined at the minimum supply voltage, and the maximum output voltage using the following equation:

$$I_{OUT(MAX)} = 2 \bullet (1-D) \bullet \frac{N_{PS}}{42 \bullet R_{SENSE}}$$

where

$$D = \frac{V_{OUT} \bullet N_{PS}}{V_{OUT} \bullet N_{PS} + V_{IN}}$$

The maximum control voltage to achieve this maximum output current is 2V • (1-D).

It is suggested to operate at 95% of these values to give margin for the part's tolerances.

When designing for power factor correction, the output current waveform is going to have a half sine wave squared shape and will no longer be able to provide the above currents. By taking the integral of a sine wave squared over half a cycle, the average output current is found to be half the value of the peak output current. In this case, the recommended maximum average output current is as follows:

$$I_{OUT(MAX)} = 2 \bullet (1-D) \bullet \frac{N_{PS}}{42 \bullet R_{SENSE}} \bullet 47.5\%$$

where

$$D = \frac{V_{OUT} \bullet N_{PS}}{V_{OUT} \bullet N_{PS} + V_{IN}}$$

The maximum control voltage to achieve this maximum output current is (1-D) • 47.5%.

For control voltages below the maximum, the output current is equal to the following equation:

$$I_{OUT} = CTRL \bullet \frac{N_{PS}}{42 \bullet R_{SENSE}}$$

The V_{REF} pin supplies a 2V reference voltage to be used with the control pins. To set an output current, a resistor divider is used from the 2V reference to one of the control pins. The following equation sets the output current with a resistor divider:

$$R1 = R2\left(\frac{2N_{PS}}{42 \bullet I_{OUT} \bullet R_{SENSE}} - 1\right)$$

where R1 is the resistor connected to the V_{REF} pin and the CTRL pin and R2 is the resistor connected to the CTRL pin and ground.

Setting V_{IN_SENSE} Resistor

The V_{IN_SENSE} resistor sets the current feeding the internal multiplier that modulates the current limit for power factor correction. At the maximum line voltage, V_{MAX}, the current is set to 360µA. Under this condition, the resistor value is equal to (V_{MAX}/360µA).

For DC input or non-PFC AC input applications, connect a 25k resistor from V_{IN_SENSE} to $INTV_{CC}$ instead of the AC line voltage.

Critical Conduction Mode Operation

Critical conduction mode is a variable frequency switching scheme that always returns the secondary current to zero with every cycle. The LT3798 relies on boundary mode and discontinuous mode to calculate the critical current because the sensing scheme assumes the secondary current returns to zero with every cycle. The DCM pin uses a fast current input comparator in combination with a small capacitor to detect dv/dt on the third winding. To eliminate false tripping due to leakage inductance ringing, a blanking time of between 600ns and 2µs is applied after the switch turns off, depending on the current limit shown in the Leakage Inductance Blanking Time vs SENSE Current Limit Threshold curve in the Typical Performance Characteristics section. The detector looks for 80µA of current through the DCM pin due to falling voltage on the third winding when the secondary diode turns off. This detection is important since the output current is calculated using this comparator's output. This is not the optimal time to turn the switch on because the switch voltage is still close to $V_{IN} + V_{OUT} \bullet N_{PS}$ and would waste all the energy stored in the parasitic capacitance on the switch node. Discontinuous ringing begins when the secondary current reaches zero and the energy in the parasitic capacitance on the switch node transfers

OPERATION

to the input capacitor. This is a second-order network composed of the parasitic capacitance on the switch node and the magnetizing inductance of the primary winding of the transformer. The minimum voltage of the switch node during this discontinuous ring is $V_{IN} – V_{OUT} • N_{PS}$. The LT3798 turns the switch back on at this time, during the discontinuous switch waveform, by sensing when the slope of the switch waveform goes from negative to positive using the dv/dt detector. This switching technique may increase efficiency by 5%.

Sense Resistor Selection

The resistor, R_{SENSE}, between the source of the external N-channel MOSFET and GND should be selected to provide an adequate switch current to drive the application without exceeding the current limit threshold.

For applications without power factor correction, select a resistor according to:

$$R_{SENSE} = \frac{2(1-D)N_{PS}}{I_{OUT} • 42} • 95\%$$

where

$$D = \frac{V_{OUT} • N_{PS}}{V_{OUT} • N_{PS} + V_{IN}}$$

For applications with power factor correction, select a resistor according to:

$$R_{SENSE} = \frac{2(1-D)N_{PS}}{I_{OUT} • 42} • 47.5\%$$

where

$$D = \frac{V_{OUT} • N_{PS}}{V_{OUT} • N_{PS} + V_{IN}}$$

Minimum Current Limit

The LT3798 features a minimum current limit of approximately 18% of the peak current limit. This is necessary when operating in critical conduction mode since low current limits would increase the operating frequency to a very high frequency. The output voltage sensing circuitry needs a minimum amount of flyback waveform time to sense the output voltage on the third winding. The time needed is 350ns. The minimum current limit allows the use of smaller transformers since the magnetizing primary inductance does not need to be as high to allow proper time to sample the output voltage information.

To help improve crossover distortion of the line input current, a second minimum current limit of 6% becomes active when the V_{IN_SENSE} current is lower than 27µA. Since the off-time becomes very short with this lower minimum current limit, the sample-and-hold is deactivated.

Universal Input

The LT3798 operates over the universal input voltage range of 90VAC to 265VAC. In the Typical Performance Characteristics section, the Output Voltage vs V_{IN} and the Output Current vs V_{IN} graphs, show the output voltage and output current line regulation for the first application picture in the Typical Applications section.

Selecting Winding Turns Ratio

Boundary mode operation gives a lot of freedom in selecting the turns ratio of the transformer. We suggest to keep the duty cycle low, lower N_{PS}, at the maximum input voltage since the duty cycle will increase when the AC waveform decreases to zero volts. A higher N_{PS} increases the output current while keeping the primary current limit constant. Although this seems to be a good idea, it comes at the expense of a higher RMS current for the secondary-side diode which might not be desirable because of the primary side MOSFET's superior performance as a switch. A higher N_{PS} does reduce the voltage stress on the secondary-side diode while increasing the voltage stress on the primary-side MOSFET. If switching frequency at full output load is kept constant, the amount of energy delivered per cycle by the transformer also stays constant regardless of the N_{PS}. Therefore, the size of the transformer remains the same at practical N_{PS}'s. Adjusting the turns ratio is a good way to find an optimal MOSFET and diode for a given application.

OPERATION

Switch Voltage Clamp Requirement

Leakage inductance of an offline transformer is high due to the extra isolation requirement. The leakage inductance energy is not coupled to the secondary but goes into the drain node of the MOSFET. This is problematic since 400V and higher rated MOSFETs cannot always handle this energy by avalanching. Therefore the MOSFET needs protection. A transient voltage suppressor (TVS) and diode are recommended for all offline application and connected, as shown in Figure 3. The TVS device needs a reverse breakdown voltage greater than $(V_{OUT} + V_F) \bullet N_{PS}$ where V_{OUT} is the output voltage of the flyback converter, V_F is the secondary diode forward voltage, and N_{PS} is the turns ratio. An RCD clamp can be used in place of the TVS clamp.

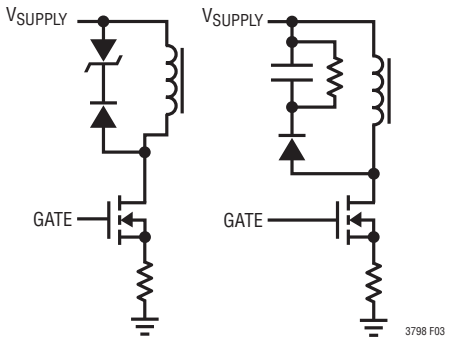


Figure 3. TVS & RCD Switch Voltage Clamps

In addition to clamping the spike, in some designs where short circuit protection is desired, it will be necessary to decrease the amount of ringing by using an RC snubber. Leakage inductance ringing is at its worst during a short circuit condition, and can keep the converter from cycling on and off by peak charging the bias capacitor. On/off cycling is desired to keep power dissipation down in the output diode. Alternatively, a heat sink can be used to manage diode temperature.

The recommended approach for designing an RC snubber is to measure the period of the ringing at the MOSFET drain when the MOSFET turns off without the snubber and then add capacitance—starting with something in the range of 100pF—until the period of the ringing is 1.5 to 2 times longer. The change in period will determine the value of the parasitic capacitance, from which the parasitic inductance can be determined from the initial period, as well. Similarly, initial values can be estimated using stated switch capacitance and transformer leakage inductance. Once the value of the drain node capacitance and inductance is known, a series resistor can be added to the snubber capacitance to dissipate power and critically dampen the ringing. The equation for deriving the optimal series resistance using the observed periods (t_{PERIOD}, and $t_{PERIOD(SNUBBED)}$) and snubber capacitance ($C_{SNUBBER}$) is below, and the resultant waveforms are shown in Figure 4.

$$C_{PAR} = \frac{C_{SNUBBER}}{\left(\frac{t_{PERIOD(SNUBBED)}}{t_{PERIOD}}\right)^2 - 1}$$

$$L_{PAR} = \frac{t_{PERIOD}^2}{C_{PAR} \bullet 4\pi^2}$$

$$R_{SNUBBER} = \sqrt{\frac{L_{PAR}}{C_{PAR}}}$$

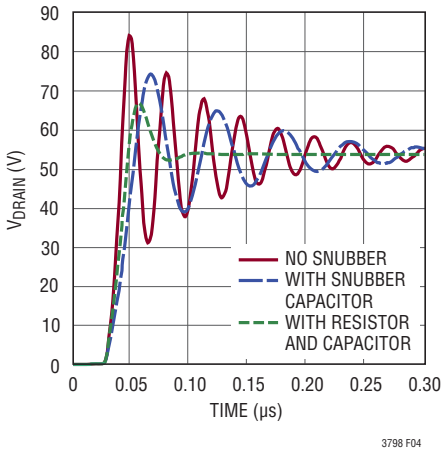


Figure 4. Observed Waveforms at MOSFET Drain when Iteratively Implementing an RC Snubber

Note that energy absorbed by a snubber will be converted to heat and will not be delivered to the load. In high voltage or high current applications, the snubber may need to be sized for thermal dissipation. To determine the power dissipated in the snubber resistor from capacitive losses, measure the drain voltage immediately before the MOSFET turns on and use the following equation relating that

OPERATION

voltage and the MOSFET switching frequency to determine the expected power dissipation:

$$P_{SNUBBER} = f_{SW} \bullet C_{SNUBBER} \bullet V_{DRAIN}^2/2$$

Decreasing the value of the capacitor will reduce the dissipated power in the snubber at the expense of increased peak voltage on the MOSFET drain, while increasing the value of the capacitance will decrease the overshoot.

Transformer Design Considerations

Transformer specification and design is a critical part of successfully applying the LT3798. In addition to the usual list of caveats dealing with high frequency isolated power supply transformer design, the following information should be carefully considered. Since the current on the secondary side of the transformer is inferred by the current sampled on the primary, the transformer turns ratio must be tightly controlled to ensure a consistent output current.

A tolerance of ±5% in turns ratio from transformer to transformer could result in a variation of more than ±5% in output regulation. Fortunately, most magnetic component manufacturers are capable of guaranteeing a turns ratio tolerance of 1% or better. Linear Technology has worked with several leading magnetic component manufacturers to produce predesigned flyback transformers for use with the LT3798. Table 1 shows the details of several of these transformers.

Loop Compensation

The voltage feedback loop is a traditional GM error amplifier. The loop cross-over frequency is set much lower than twice the line frequency for PFC to work properly.

The current output feedback loop is an integrator configuration with the compensation capacitor between the negative input and output of the operational amplifier. This is a one-pole system therefore a zero is not needed in the compensation. For offline applications with PFC, the crossover should be set an order of magnitude lower than the line frequency of 120Hz or 100Hz. In a typical application, the compensation capacitor is 0.1µF.

In non-PFC applications, the crossover frequency may be increased to improve transient performance. The desired crossover frequency needs to be set an order of magnitude below the switching frequency for optimal performance.

Table 1. Predesigned Transformers—Typical Specifications, Unless Otherwise Noted

TRANSFORMER PART NUMBER	SIZE (L × W × H)	L_{PRI} (µH)	N_{PSA} (N_P:N_S:N_A)	R_{PRI} (mΩ)	R_{SEC} (mΩ)	MANUFACTURER	TARGET APPLICATION (V_{OUT}/I_{OUT})
JA4429	21.1mm × 21.1mm × 17.3mm	400	1:0.24:0.24	252	126	Coilcraft	22V/1A
7508110210	15.75mm × 15mm × 18.5mm	2000	6.67:1:1.67	5100	165	Würth Elektronik	10V/0.4A
750813002	15.75mm × 15mm × 18.5mm	2000	20:1.0:5.0	6100	25	Würth Elektronik	3.8V/1.1A
750811330	43.2mm × 39.6mm × 30.5mm	300	6:1.0:1.0	150	25	Würth Elektronik	18V/5A
750813144	16.5mm × 18mm × 18mm	600	4:1:0.71	2400	420	Würth Elektronik	28V/0.5A
750813134	16.5mm × 18mm × 18mm	600	8:1:1.28	1850	105	Würth Elektronik	14V/1A
750811291	31mm × 31mm × 25mm	400	1:1:0.24	550	1230	Würth Elektronik	85V/0.4A
750813390	43.18mm × 39.6mm × 30.48mm	100	1:1:0.22	150	688	Würth Elektronik	90V/1A
750811290	31mm × 31mm × 25mm	460	1:1:0.17	600	560	Würth Elektronik	125V/0.32A
X-11181-002	23.5mm × 21.4mm × 9.5mm	500	72:16:10	1000	80	Premo	30V/0.5A
750811248	31mm × 31mm × 25mm	300	4:1.0:1.0	280	25	Würth Elektronik	24V/2A
S001621	25mm × 22.2mm × 16mm	820	16:1.0:4.0	1150	10	Renco	5V/4A
750312872	43.2mm × 39.6mm × 30.5mm	14	1:1:0.8	11	11	Würth Elektronik	28V/4A

OPERATION

MOSFET and Diode Selection

With a strong 1.9A gate driver, the LT3798 can effectively drive most high voltage MOSFETs. A low Qg MOSFET is recommended to maximize efficiency. In most applications, the $R_{DS(ON)}$ should be chosen to limit the temperature rise of the MOSFET. The drain of the MOSFET is stressed to $V_{OUT} \bullet N_{PS} + V_{IN}$ during the time the MOSFET is off and the secondary diode is conducting current. But in most applications, the leakage inductance voltage spike exceeds this voltage. The voltage of this stress is determined by the switch voltage clamp. Always check the switch waveform with an oscilloscope to make sure the leakage inductance voltage spike is below the breakdown voltage of the MOSFET. A transient voltage suppressor and diode are slower than the leakage inductance voltage spike, therefore causing a higher voltage than calculated.

The secondary diode stress may be as much as $V_{OUT} + 2 \bullet V_{IN}/N_{PS}$ due to the anode of the diode ringing with the secondary leakage inductance. An RC snubber in parallel with the diode eliminates this ringing, so that the reverse voltage stress is limited to $V_{OUT} + V_{IN}/N_{PS}$. With a high N_{PS} and output current greater than 3A, the I_{RMS} through the diode can become very high and a low forward drop Schottky is recommended.

Discontinuous Mode Detection

The discontinuous mode detector uses AC-coupling to detect the ringing on the third winding. A 22pF capacitor with a 30k resistor in series is recommended in most designs. Depending on the amount of leakage inductance ringing, an additional current may be needed to prevent false tripping from the leakage inductance ringing. A resistor from $INTV_{CC}$ to the DCM pin adds this current. Up to an additional 100µA of current may be needed in some cases. The DCM pin is roughly 0.7V, therefore the resistor value is selected using the following equation:

$$R = \frac{10V - 0.7V}{I}$$

where I is equal to the additional current into the DCM pin.

Power Factor Correction/Harmonic Content

The LT3798 attains high power factor and low harmonic content by making the peak current of the main power switch proportional to the line voltage by using an internal multiplier. A power factor of >0.97 is easily attainable for most applications by following the design equations in this data sheet. With proper design, LT3798 applications can easily meet most harmonic standards.

Operation Under Light Output Loads

The LT3798 detects output overvoltage conditions by looking at the voltage on the third winding. The third winding voltage is proportional to the output voltage when the main power switch is off and the secondary diode is conducting current. Sensing the output voltage requires delivering power to the output. When the output current is very low, this periodic delivery of output current can exceed the load current. The OVP pin sets the output overvoltage threshold. When the output of the sample-and-hold is above this voltage, the minimum switching frequency is divided by 8 as shown in Figure 5. This OVP threshold needs to be set above 1.35V and should be set out of the way of output voltage transients. The output clamp point is set with the following formula:

$$V_{OUT} = V_{OVP}(R4 + R5)/(N_{ST} \bullet R5) - (V_F + (R4 \bullet I_{TC})/N_{ST})$$

The V_{OVP} pin voltage may be provided by a resistor divider from the V_{REF} pin. This frequency division greatly reduces the output current delivered to the output but a Zener or resistor is required to dissipate the remaining output current. The Zener diode's voltage needs to be 5% higher than the output voltage set by the resistor divider connected to the FB pin. Multiple Zener diodes in series may be needed for higher output power applications to keep the Zener's temperature within the specification.

OPERATION

Protection from Shorted Output Conditions

During a shorted output condition as shown in Figure 6, the LT3798 operates at the minimum operating frequency. In normal operation, the third winding provides power to the IC, but the third winding voltage is zero during a shorted condition. This causes the part's V_{IN} UVLO to shutdown switching. The part starts switching again when V_{IN} has reached its turn-on voltage.

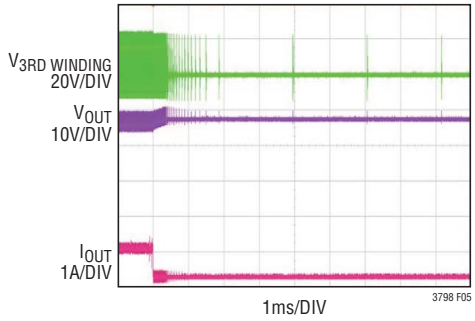


Figure 5. Switching Waveforms When Output Open-Circuits or at Very Light Load Conditions

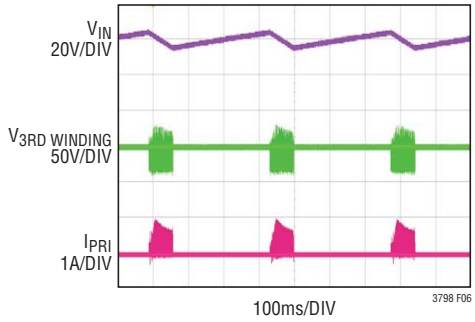


Figure 6. Switching Waveforms When Output Short-Circuits

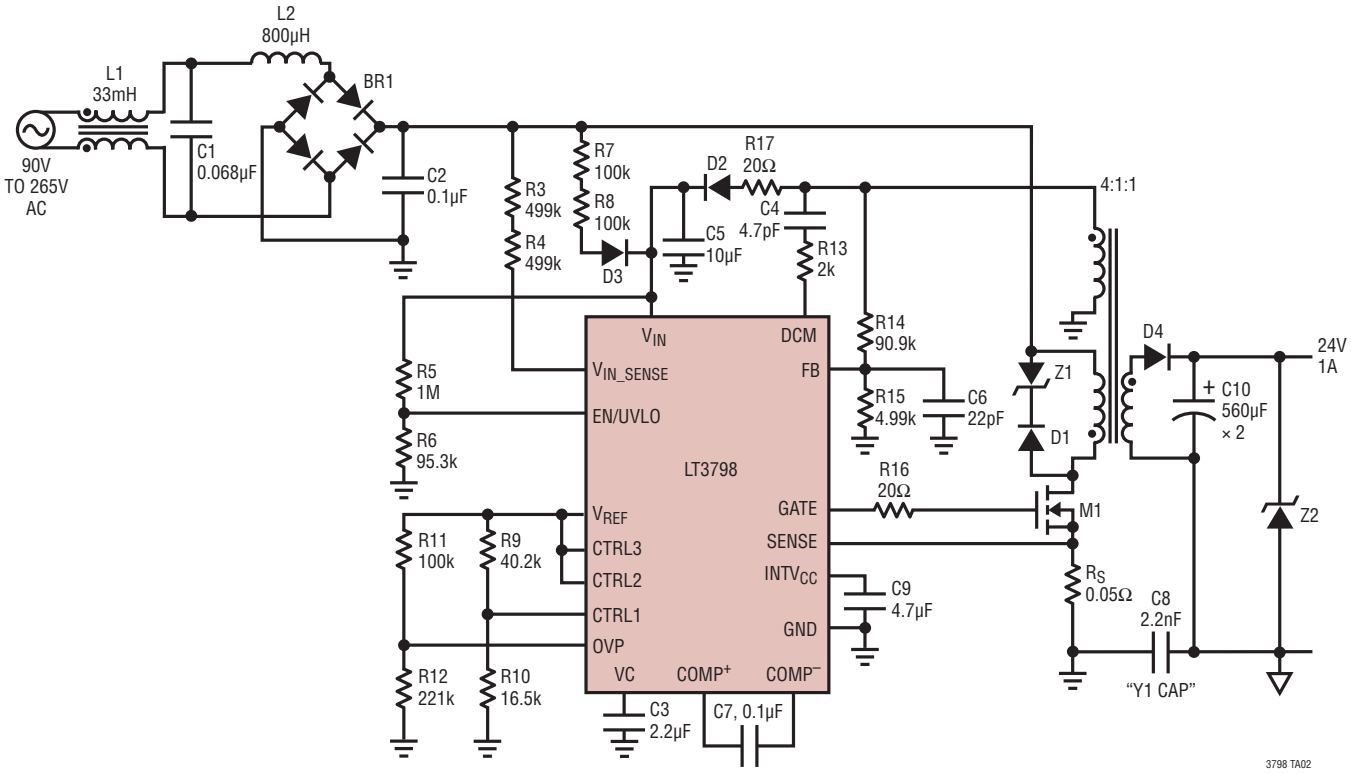
Usage with DC Input Voltage

The LT3798 is flexible enough to operate well from low voltage to very high voltage DC input voltage applications. When the supply voltage is less than 40V, the startup resistor is not needed and the part's V_{IN} can be connected directly to the supply voltage. The startup sequence for voltages higher than 40V is the same as what is described for high voltage offline supply voltages.

The loop compensation component values can be chosen to provide faster loop response since the LT3798 does not have to provide PFC for the slow 50Hz/60Hz AC input voltage. For DC input applications, connect a 25k resistor from V_{IN_SENSE} to $INTV_{CC}$.

TYPICAL APPLICATIONS

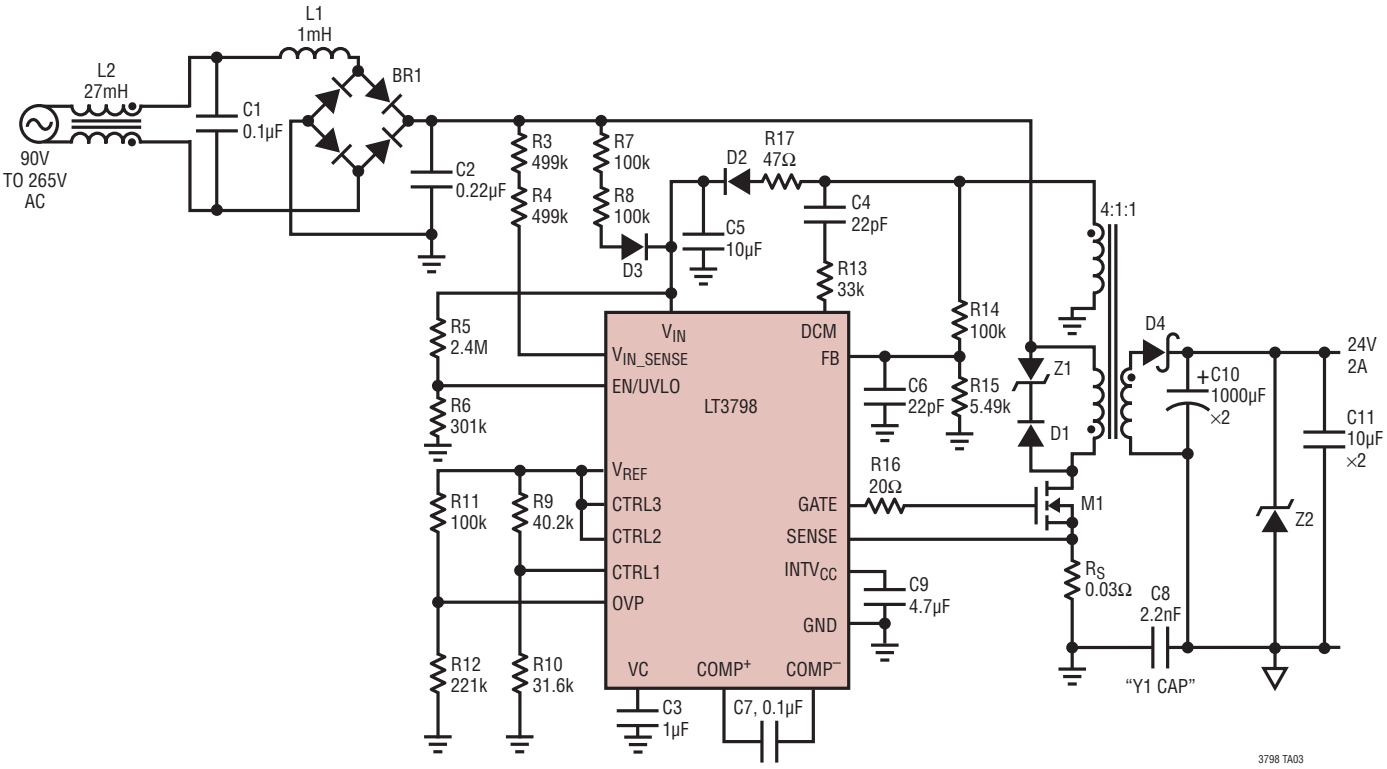
Universal Input 24W PFC Bus Converter



BR1: DIODES, INC. HD06
C8: VISHAY 440LD22-R
D1: CENTRAL SEMICONDUCTOR CMR1U-06M
D2, D3: DIODES INC. BAV20W
D4: CENTRAL SEMICONDUCTOR CMR1U-02M
M1: FAIRCHILD FDPF15N65
T1: COILCRAFT JA4429-AL
Z1: FAIRCHILD SMBJ170A
Z2: CENTRAL SEMICONDUCTOR CMZ5937B

TYPICAL APPLICATIONS

Universal Input 48W PFC Application

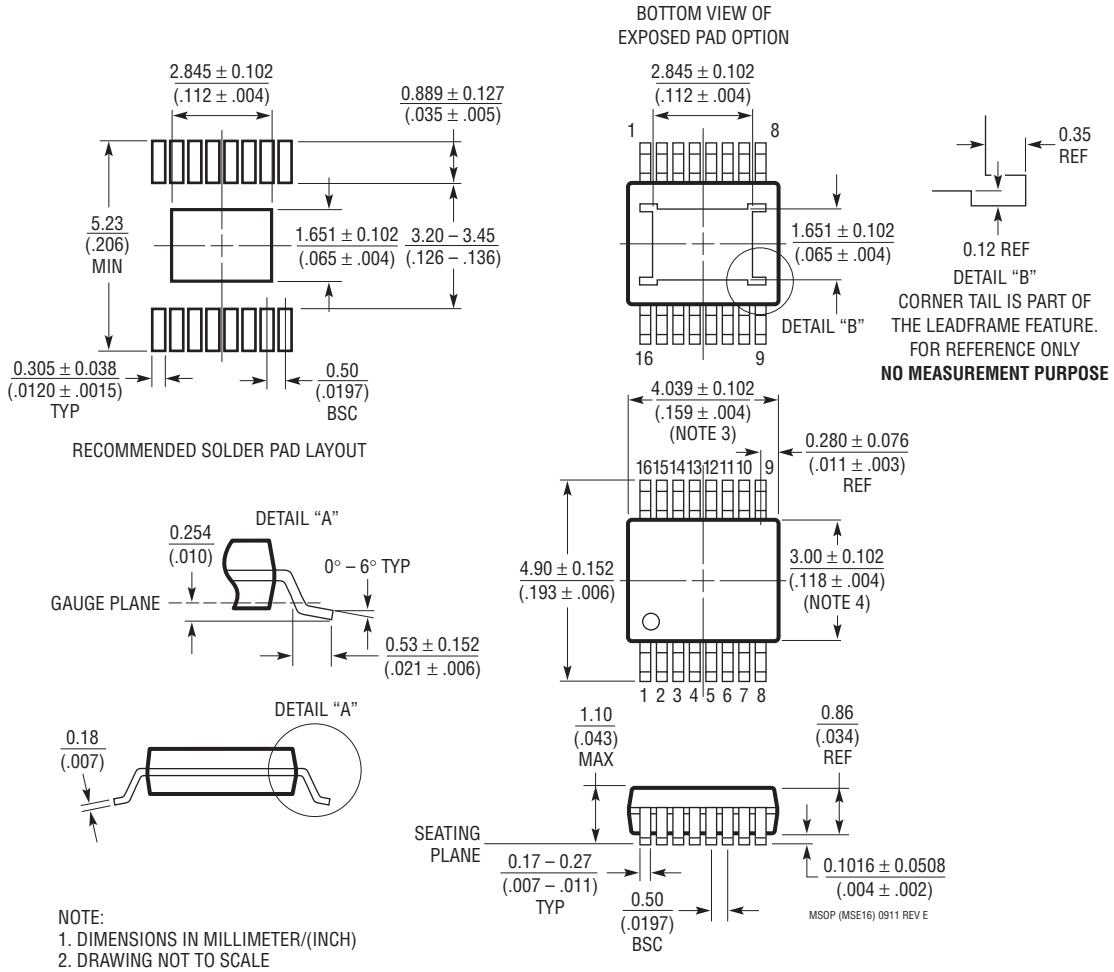


BR1: DIODES, INC. HD06
C8: VISHAY 440LD22-R
C11: MURATA GRM32ER7YA106KA12L
D1: CENTRAL SEMICONDUCTOR CMR1U-06M
D2, D3: DIODES INC. BAV20W
D4: DIODES INC. SBR20A200CTB
M1: INFINEON IPB60R165CP
T1: WÜRTH ELEKTRONIK 750811248
Z1: FAIRCHILD SMBJ170A
Z2: CENTRAL SEMICONDUCTOR CMZ5937B

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

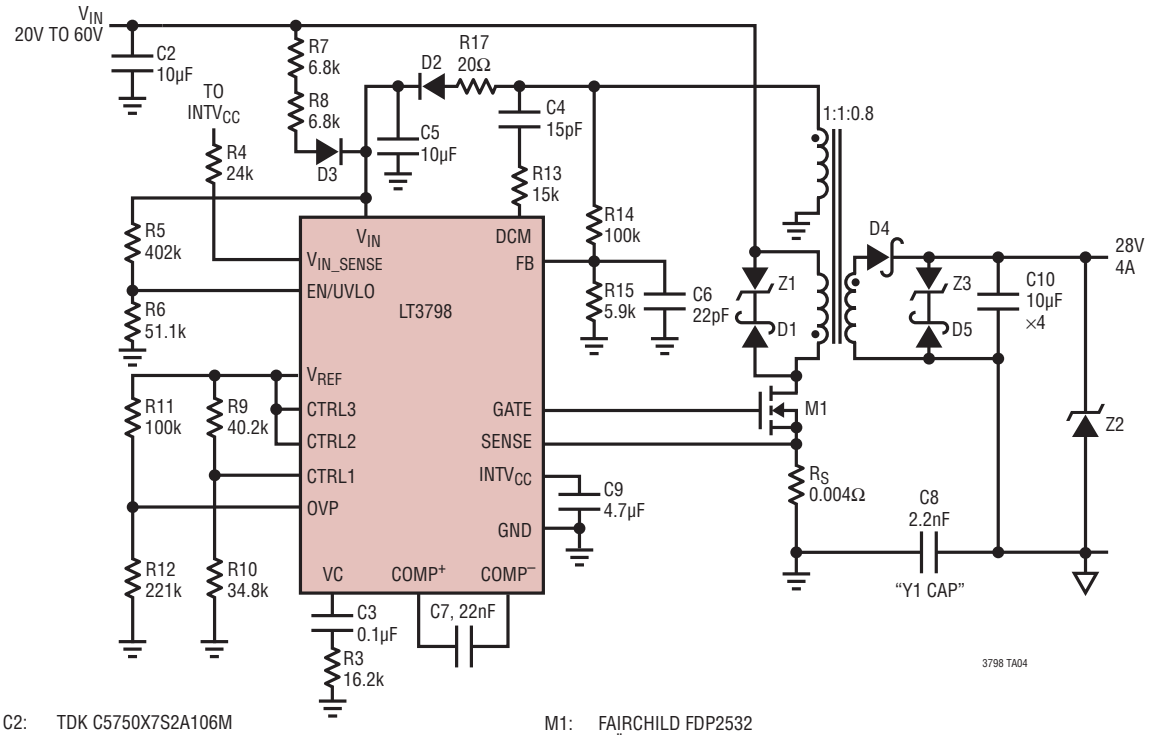
MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev E)



NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

TYPICAL APPLICATION

112W Wide DC Input Industrial Power Supply



C2: TDK C5750X7S2A106M
C8: VISHAY 440LD22-R
C10: MURATA GRM32ER7YA106KA12L
D1: DIODES INC. DFLS1150
D2, D3: DIODES INC. BAV20W
D4: ON SEMICONDUCTOR MBR20200CT
D5: DIODES INC. DFLS2100
M1: FAIRCHILD FDP2532
T1: WÜRTH ELEKTRONIK 750312872
Z1: DIODES INC. SMCJ60A
Z2: CENTRAL SEMICONDUCTOR CMZ59398
Z3: FAIRCHILD SMBJ170A

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3799/LT3799-1	Offline Isolated Flyback LED Controller with Active PFC	No Opto-Coupler Required, TRIAC Dimmable, V_{IN} and V_{OUT} Limited Only by External Components, MSOP-16E
LT3748	100V Isolated Flyback Controller	5V ≤ V_{IN} ≤ 100V, No Opto Flyback , MSOP-16 with High Voltage Spacing
LT3573/LT3574/LT3575	40V Isolated Flyback Converters	Monolithic No-Opto Flybacks with Integrated 1.25A/0.65A/2.5A Switch
LT3511/LT3512	100V Isolated Flyback Converters	Monolithic No-Opto Flybacks with Integrated 240mA/420mA Switch
LT3757/LT3758	40V/100V Flyback/Boost Controllers	Universal Controllers with Small Package and Powerful Gate Drive
LT3957/LT3958	40V/100V Flyback/Boost Converters	Monolithic with Integrated 5A/3.3A Switch
LTC3803/LTC3803-3/LTC3803-5	200kHz/300kHz Flyback Controllers	V_{IN} and V_{OUT} Limited Only by External Components
LTC3805/LTC3805-5	Adjustable Frequency Flyback Controllers	V_{IN} and V_{OUT} Limited Only by External Components

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