

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## General Description

The MAX97220\_ is a differential input DirectDrive® line driver/headphone amplifier. This device is capable of driving line level loads with 3VRMS into 1kΩ with a 5V supply and 2VRMS into 600Ω loads from a 3.3V supply. A headphone load is capable of being driven with 125mW into 32Ω with a 5V supply. The IC is offered with an internally fixed 6dB gain or an externally set gain through external resistors. The external gain setting nodes can also be used to configure filters for set-top box applications. The IC has exceptional THD+N over the full audio bandwidth.

Two versions of the IC are available with different turn-on times ( $t_{ON}$ ). The A and C versions for headphone applications feature a  $t_{ON}$  of 5.5ms while the B and D versions, intended for set-top-box applications, feature a 130ms  $t_{ON}$ . An on-chip charge pump inverts the power-supply input, creating a negative rail. The output stage of the amplifier is powered between the positive input supply and the output of the charge pump. The bipolar supplies bias the output about ground, eliminating the need for large, distortion-introducing output coupling capacitors. The IC powers on and off without clicks or pops.

The IC is available in a 3mm x 3mm x 0.8mm, 16-pin TQFN and is specified over the extended -40°C to +85°C temperature range.

## Applications

Simple Multimedia Interfaces  
Set-Top Boxes  
Blu-ray™ and DVD Players  
LCD Televisions  
Prosumer Audio Devices

## Features

- ◆ Output Power 125mW into 32Ω with a 5V Supply
- ◆ 3VRMS Output Drive into 1kΩ with a 5V Supply
- ◆ 2VRMS Output Drive into 600Ω with a 3.3V Supply
- ◆ Fully Differential Inputs
- ◆ Fixed or Externally Adjustable Gain with No Clicks or Pops
- ◆ Wide 2.5V to 5.5V Operating Range
- ◆ DirectDrive Outputs Eliminate DC-Blocking Capacitors
- ◆ Flat THD+N, Better Than 90dB in the Audio Band
- ◆ 18-Bit SNR Performance, 112dB
- ◆ Footprint Compatible with the MAX9722

## Ordering Information

PART	PIN-PACKAGE	TOP MARK	GAIN SET	TURN-ON TIME (ms)
MAX97220AETE+	16 TQFN-EP*	+AIF	External	5.5
MAX97220BETE+	16 TQFN-EP*	+AIG	External	130
MAX97220CETE+	16 TQFN-EP*	+AIH	+6dB	5.5
MAX97220DETE+	16 TQFN-EP*	+AII	+6dB	130

**Note:** All devices operate over the -40°C to +85°C temperature range.

+Denotes a lead(Pb)-free/RoHS-compliant package.

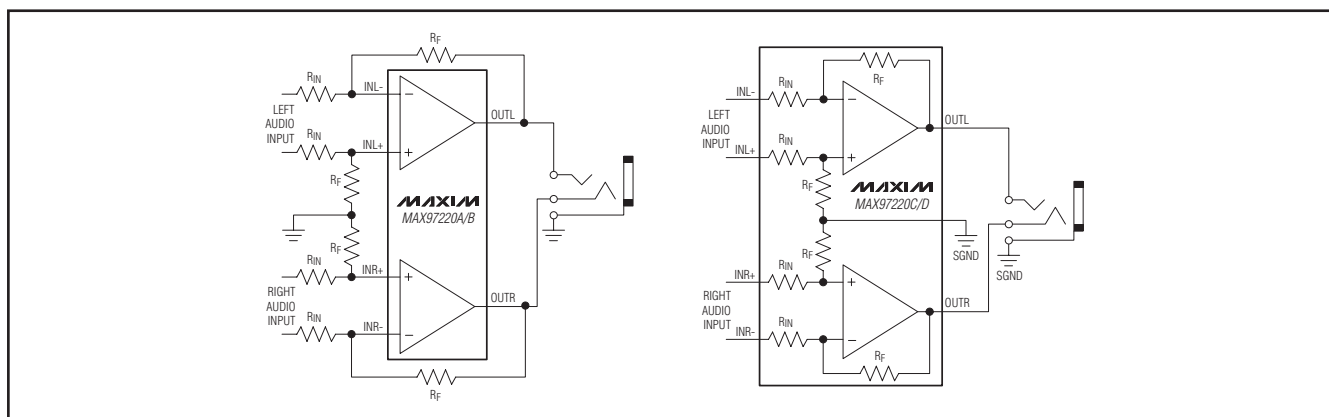
\*EP = Exposed pad.

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Blu-ray is a trademark of the Blu-ray Disc Association.

Functional Diagrams appear at end of data sheet.

## Simplified Block Diagrams



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## ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to PGND.)

SVDD, SVDD2, and PVDD	-0.3V to +6V
PVSS and BIAS	-6V to +0.3V
SGND	-0.3V to +0.3V
INL-, INL+, INR-, and INR+ (A and B)	-V <sub>SVDD</sub> /2 to +V <sub>SVDD</sub> /2
INL-, INL+, INR-, and INR+ (C and D)	(-0.75 x V <sub>SVDD</sub> ) to (+0.75 x V <sub>SVDD</sub> )
OUTL and OUTR	-4.5V to +4.5V
SHDN	-0.3V to +6V
C1P	-0.3V to (V <sub>PVDD</sub> + 0.3V)
C1N	(V <sub>PVSS</sub> - 0.3V) to +0.3V

OUT_ Short Circuit to PGND	Continuous
OUT_ Short Circuit to PVDD	Continuous
Short Circuit Between OUTL and OUTR	Continuous
Continuous Current Into/Out of All Pins	20mA
Continuous Power Dissipation (T <sub>A</sub> = +70°C) (Multilayer Board)	
TQFN (derate 20.8mW/°C above +70°C)	1666.7mW
Junction Temperature	+150°C
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C
Soldering Temperature (reflow)	+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN

Junction-to-Ambient Thermal Resistance ( $\theta_{JA}$ ) .....48°C/W

Junction-to-Case Thermal Resistance ( $\theta_{JC}$ ) .....7°C/W

**Note 1:** Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to [www.maxim-ic.com/thermal-tutorial](http://www.maxim-ic.com/thermal-tutorial).

## ELECTRICAL CHARACTERISTICS

(V<sub>PVDD</sub> = V<sub>SVDD</sub> = V<sub>SVDD2</sub> = 5V, V<sub>PGND</sub> = V<sub>SGND</sub> = 0V, C<sub>BIAS</sub> = 0.1µF, C1 = C2 = 1µF, R<sub>IN</sub> = 20kΩ, R<sub>F</sub> = 20kΩ (MAX97220A/MAX97220B), typical values tested at T<sub>A</sub> = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
<b>GENERAL</b>							
Supply Voltage Range	PVDD, SVDD_	Guaranteed by PSRR test		2.5		5.5	V
Quiescent Supply Current	IPVDD	No load, T <sub>A</sub> = +25°C	A version		5.5	7	mA
		No load, T <sub>A</sub> = +25°C	B/C/D versions		5	9	
		No load, V <sub>PVDD</sub> = V <sub>SVDD_</sub> = 3.3V			5		
Undervoltage Lockout	UVLO	PVDD falling				2.35	V
Shutdown Supply Current	IPVDD_SD	SHDN = 0, T <sub>A</sub> = +25°C			1	10	µA
Turn-On Time	t <sub>ON</sub>	Shutdown to full operation time	A/C versions	4.8	5.5	6.3	ms
			B/D versions	117	130	143	
<b>AMPLIFIERS</b>							
Input Resistance	R <sub>IN</sub>	C/D versions only		7.4	10	12.7	kΩ
Output Signal Attenuation in Shutdown		V <sub>SHDN</sub> = 0V, R <sub>L</sub> = 10kΩ	A/B versions	76			dB
			C/D versions	71			
Gain	A <sub>v</sub>	C/D versions only		5.5	6	6.5	dB
Output Offset Voltage	V <sub>OS</sub>	Unity gain, T <sub>A</sub> = +25°C				350	µV
Input Common-Mode Voltage Range	V <sub>CM</sub>	Voltage at IN+ and IN-	A/B versions	-0.5 x V <sub>PVDD</sub>		+0.5 x V <sub>PVDD</sub>	V
			C/D versions	-0.75 x V <sub>PVDD</sub>		+0.75 x V <sub>PVDD</sub>	
Maximum Differential Input Signal	V <sub>DIFF</sub>	(Note 4)				PVDD	V <sub>P</sub>

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## ELECTRICAL CHARACTERISTICS (continued)

(VPVDD = VSVDD = VSVDD2 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 20kΩ, RF = 20kΩ (MAX97220A/MAX97220B), typical values tested at TA = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS	
Power-Supply Rejection Ratio	PSRR	VPVDD = VSVDD_ = 2.5V to 5.5V	A/B versions	74	90		dB	
		VPVDD = VSVDD_ = 2.5V to 5.5V	C/D versions	73	90			
		fIN = 217Hz, 200mVp-p ripple				78		
		fIN = 10kHz, 200mVp-p ripple				63		
Common-Mode Rejection Ratio	CMRR	-VPVDD/2 ≤ VCM ≤ +VPVDD/2	A/B versions	70	86		dB	
		-0.75 x VPVDD ≤ VCM ≤ +0.75 x VPVDD	C/D versions	45	60			
Output Voltage Swing	VOUT	1kHz, 600Ω load, THD+N < 0.1%		3			VRMS	
		1kHz, RL = 600Ω load, VPVDD = VSVDD_ = 3.3V, THD+N < 0.1%			2.15			
		1kHz, RL = 10kΩ load, THD+N < 0.1%				3.5		
Output Power	POUT	RL = 16Ω, THD+N = 1%		40	110		mW	
		RL = 32Ω, THD+N = 1%				125		
Total Harmonic Distortion Plus Noise	THD+N	1kHz, 22Hz to 22kHz BW, VOUT = 3VRMS, RL = 10kΩ			103		dB	
		10kHz, 22Hz to 22kHz BW, VOUT = 3VRMS, RL = 10kΩ			90			
		1kHz, 22Hz to 22kHz BW, VOUT = 2VRMS, RL = 600Ω		80	105			
		10kHz, 22Hz to 30kHz BW, VOUT = 2VRMS, RL = 600Ω			94			
		1kHz, 22Hz to 22kHz BW, POUT = 20mW, RL = 32Ω				0.0035		%
Signal-to-Noise Ratio	SNR	A/B versions	VOUT = 3VRMS, THD+N = 0.1%, A-weighted, RIN = RF = 10kΩ, RL = 1kΩ		112.5		dB	
			VOUT = 2VRMS, VPVDD = 3.3V, THD+N = 0.1%, A-weighted, RIN = RF = 10kΩ, RL = 600Ω		109			
		C/D versions	VOUT = 3VRMS, THD+N = 0.1%, A-weighted, RL = 1kΩ		106			
			VOUT = 2VRMS, VPVDD = 3.3V, THD+N = 0.1%, A-weighted, RL = 600Ω		103			

MAX97220A-MAX97220D

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## ELECTRICAL CHARACTERISTICS (continued)

(VPVDD = VSVDD = VSVDD2 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 20kΩ, RF = 20kΩ (MAX97220A/MAX97220B), typical values tested at TA = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Output Noise Voltage	VN	A/B versions	A-weighted, RIN = RF = 10kΩ		7		μV
		C/D versions	A-weighted		14		
Crosstalk	XTALK	A/B versions	1kHz, VOUT = 3VRMS, RL = 10kΩ		-125		dB
			10kHz, VOUT = 3VRMS, RL = 10kΩ		-108		
			1kHz, VOUT = 2VRMS, RL = 600Ω, VPVDD = VSVDD_ = 3.3V		-123		
			10kHz, VOUT = 2VRMS, RL = 600Ω, VPVDD = VSVDD_ = 3.3V		-104		
			1kHz, POUT = 20mW, RL = 32Ω		-102		
			10kHz, POUT = 20mW, RL = 32Ω		-82		
		C/D versions	1kHz, VOUT = 2VRMS, RL = 10kΩ		100		
			10kHz, VOUT = 2VRMS, RL = 10kΩ		98		
			1kHz, VOUT = 2VRMS, RL = 600Ω		100		
			10kHz, VOUT = 2VRMS, RL = 600Ω		96		
			1kHz, POUT = 20mW, RL = 32Ω		95		
			1kHz, POUT = 20mW, RL = 16Ω		92		
Maximum Capacitive Load Drive	CL			470		pF	
External Feedback Resistor Range	RF	A/B versions		4.7	20	100	kΩ
Oscillator Frequency	fOSC			450	500	550	kHz

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## ELECTRICAL CHARACTERISTICS (continued)

(VPVDD = VSVD2 = VSVD1 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 20kΩ, RF = 20kΩ (MAX97220A/MAX97220B), typical values tested at TA = +25°C, unless otherwise noted.) (Notes 2 and 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Click-and-Pop Level (Note 5)	KCP	32 samples per second, A-weighted, RL = 10kΩ, unity gain	Into shutdown		-70	dBV
			Out of shutdown		-70	
		32 samples per second, A-weighted, RL = 32Ω, unity gain	Into shutdown		-76	
			Out of shutdown		-76	
<b>LOGIC INPUT (<math>\overline{\text{SHDN}}</math>)</b>						
$\overline{\text{SHDN}}$ Input Logic-High	V <sub>IH</sub>		1.4			V
$\overline{\text{SHDN}}$ Input Logic-Low	V <sub>IL</sub>				0.4	V
$\overline{\text{SHDN}}$ Input Leakage Current High	I <sub>IH</sub>	TA = +25°C			1	μA
$\overline{\text{SHDN}}$ Input Leakage Current Low	I <sub>IL</sub>	TA = +25°C			1	μA

**Note 2:** 100% production tested at TA = +25°C. Specifications over temperature limits are guaranteed by design.

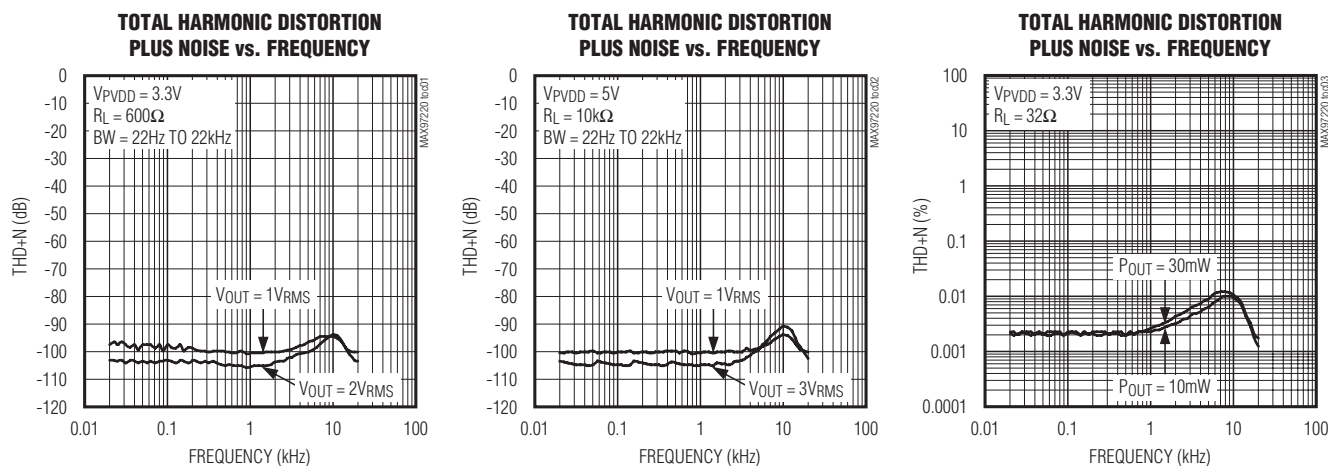
**Note 3:** Dynamic specifications are taken over 2.5V to 5.5V supply range. Inputs AC-coupled to PGND.

**Note 4:** The maximum differential input signal does not cause any excess distortion due to violation of the common-mode input range.

**Note 5:** Test performed with a resistive load connected to PGND. Mode transitions are controlled by  $\overline{\text{SHDN}}$ . KCP level is calculated as 20 x log (peak voltage during mode transition, no input signal).

## Typical Operating Characteristics

(VPVDD = VSVD2 = VSVD1 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 10kΩ, RF = 10kΩ, unless otherwise noted.)

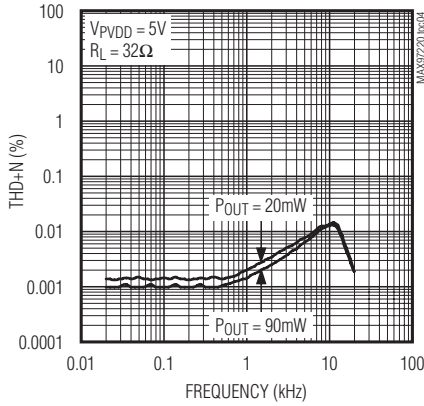


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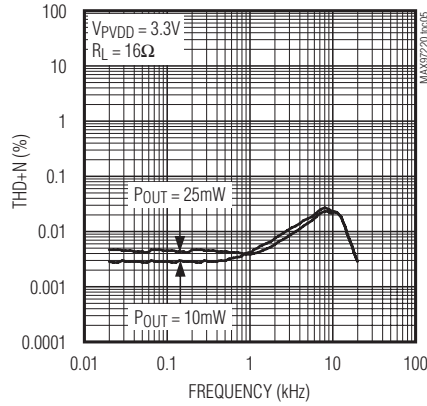
## Typical Operating Characteristics (continued)

( $V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$ ,  $V_{PGND} = V_{SGND} = 0V$ ,  $C_{BIAS} = 0.1\mu F$ ,  $C_1 = C_2 = 1\mu F$ ,  $R_{IN} = 10k\Omega$ ,  $R_F = 10k\Omega$ , unless otherwise noted.)

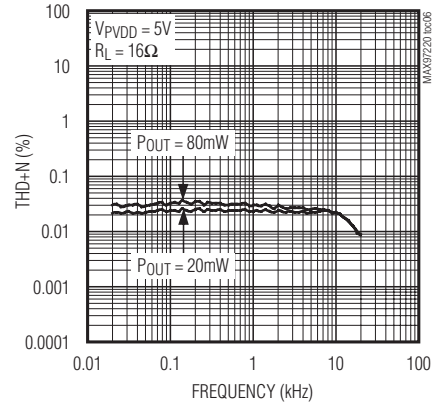
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY**



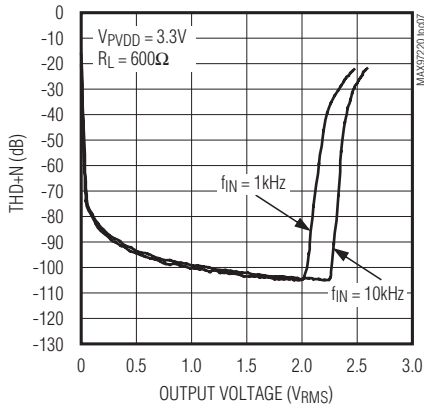
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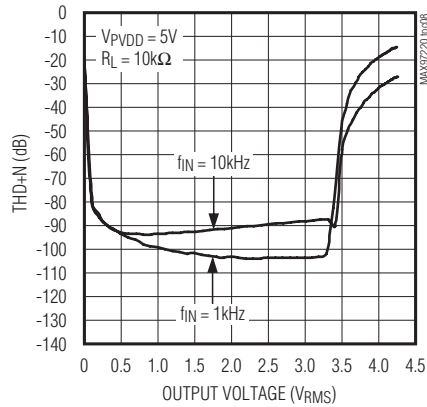
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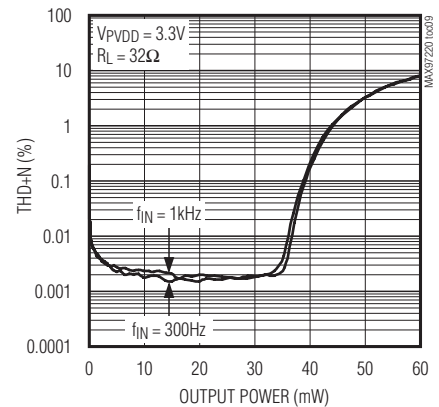
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT VOLTAGE**



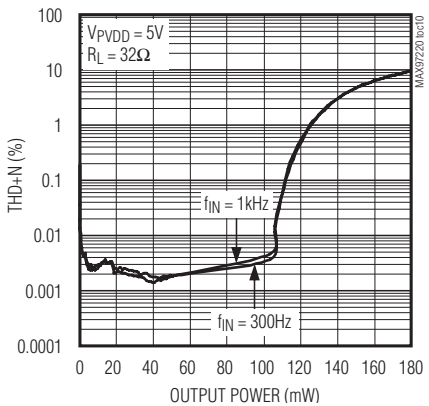
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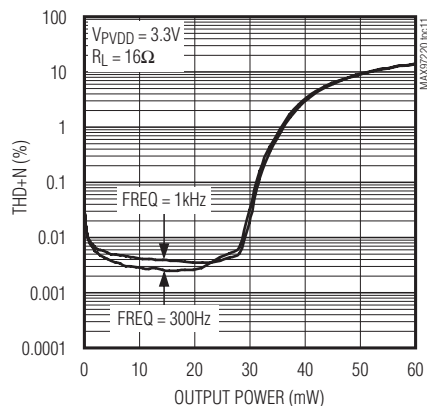
**TOTAL HARMONIC DISTORTION PLUS NOISE vs. OUTPUT POWER**



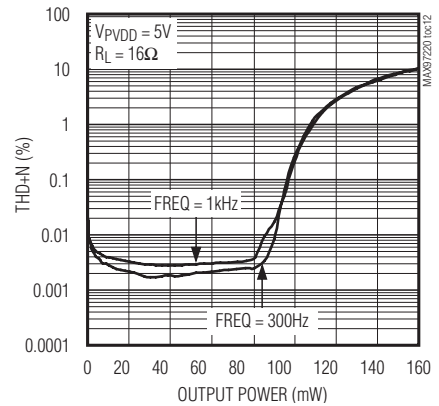
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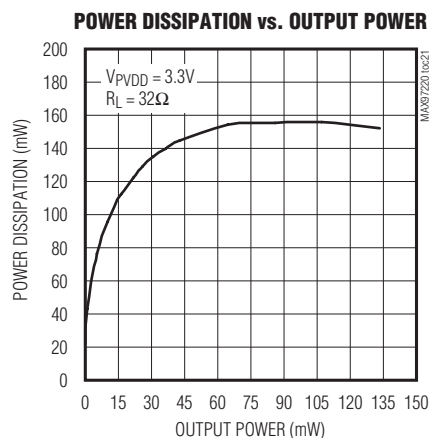
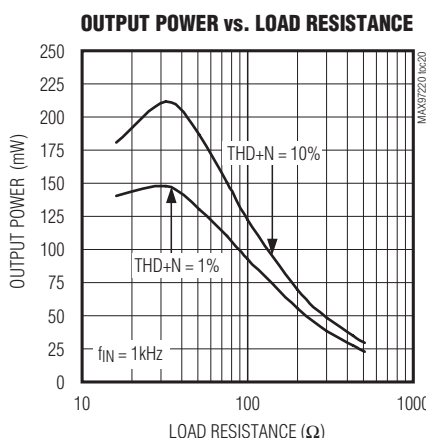
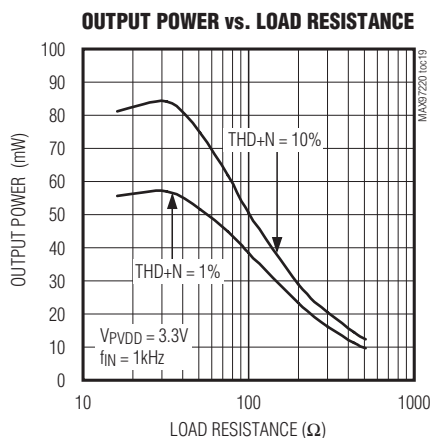
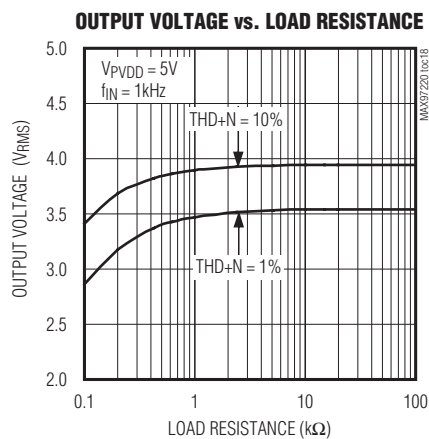
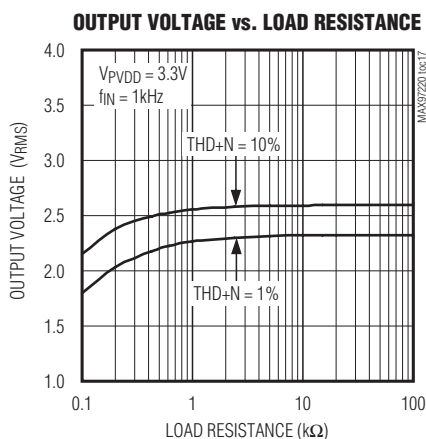
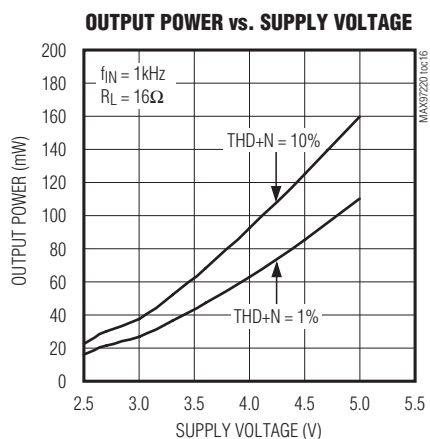
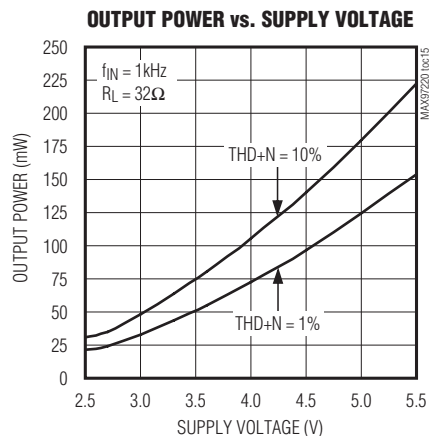
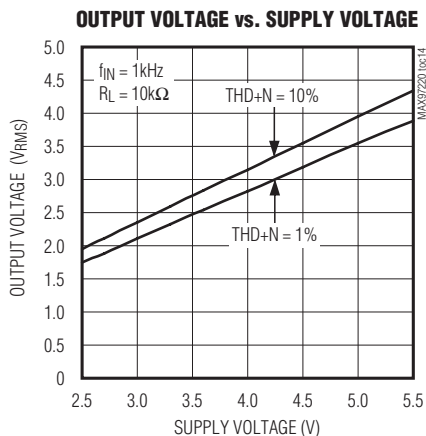
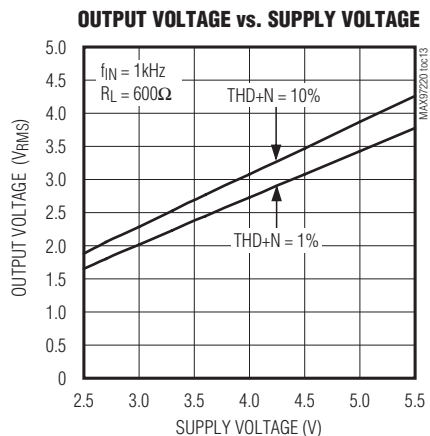


# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Typical Operating Characteristics (continued)

( $V_{PVDD} = V_{SVDD} = V_{SVDD2} = 5V$ ,  $V_{PGND} = V_{SGND} = 0V$ ,  $C_{BIAS} = 0.1\mu F$ ,  $C_1 = C_2 = 1\mu F$ ,  $R_{IN} = 10k\Omega$ ,  $R_F = 10k\Omega$ , unless otherwise noted.)

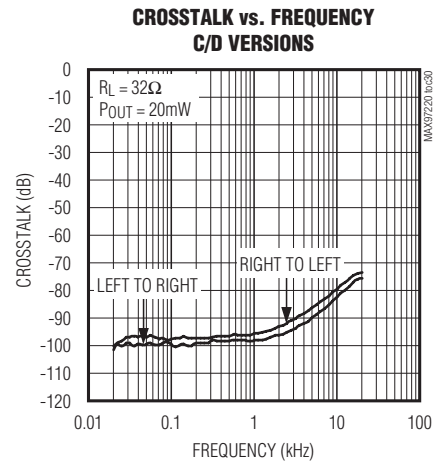
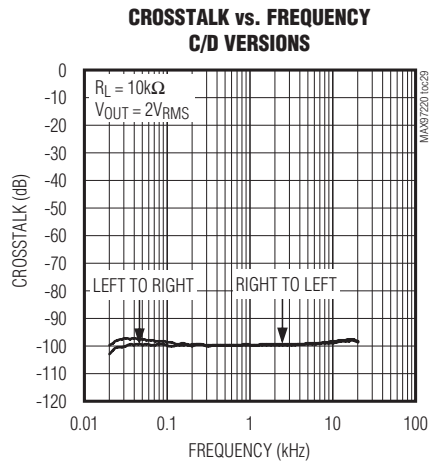
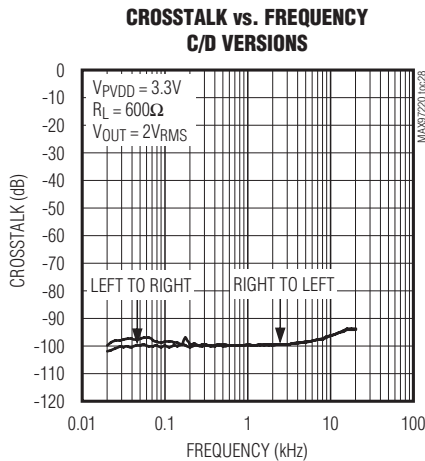
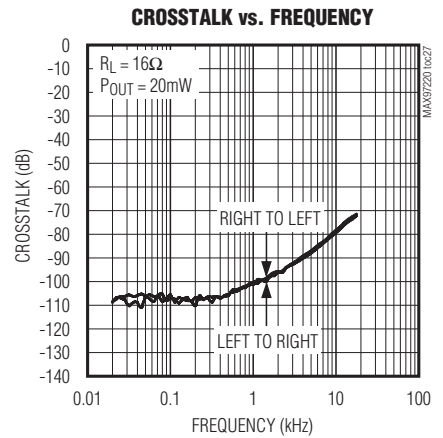
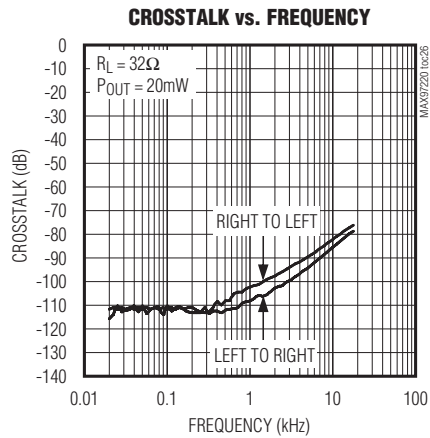
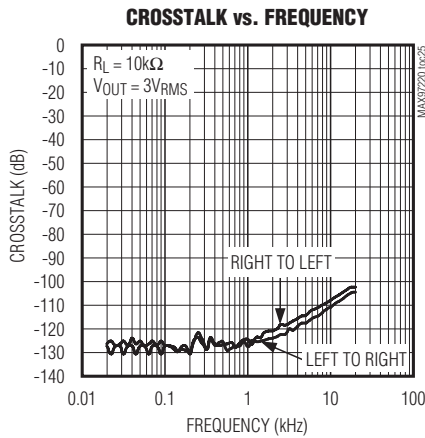
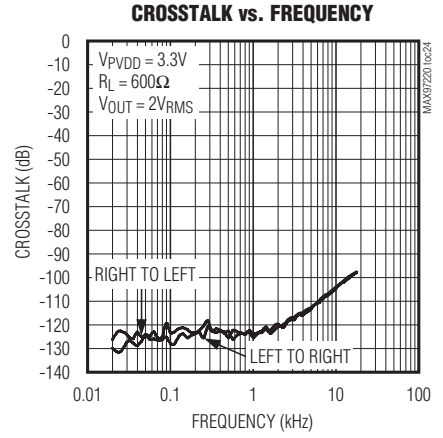
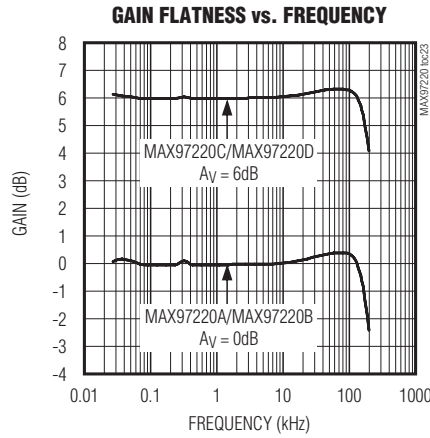
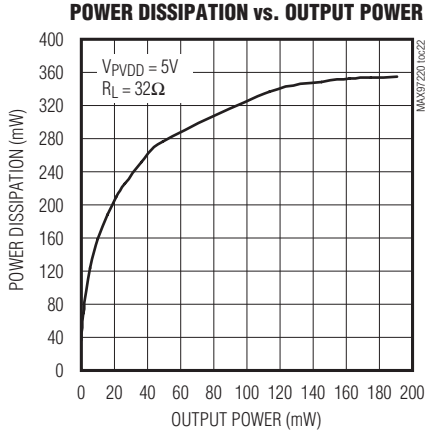
MAX97220A-MAX97220D



# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Typical Operating Characteristics (continued)

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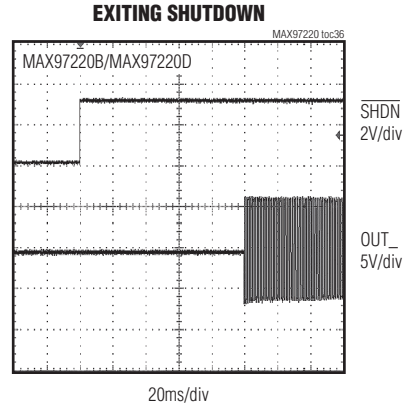
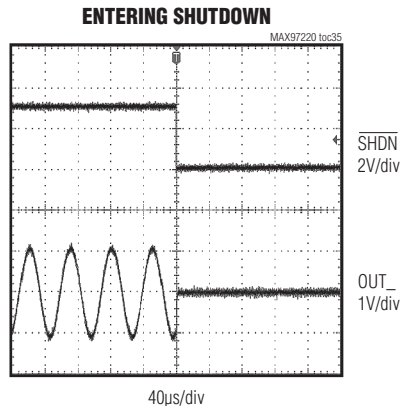
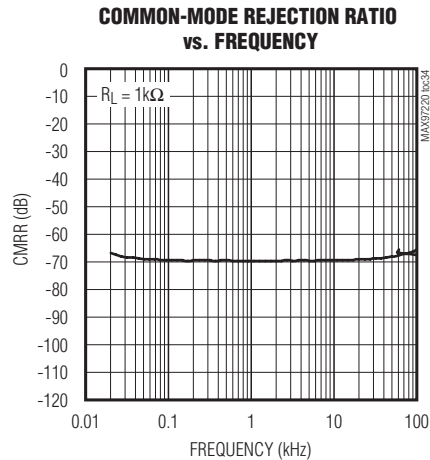
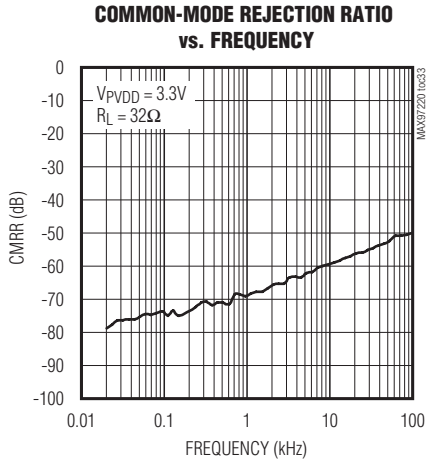
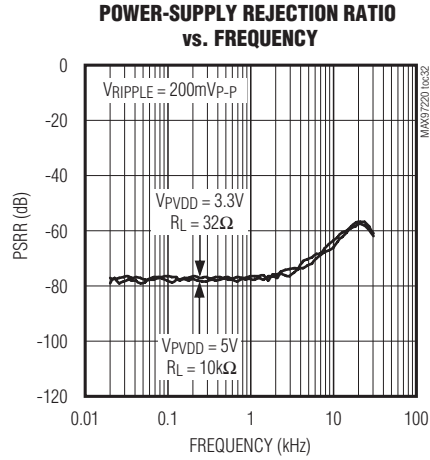
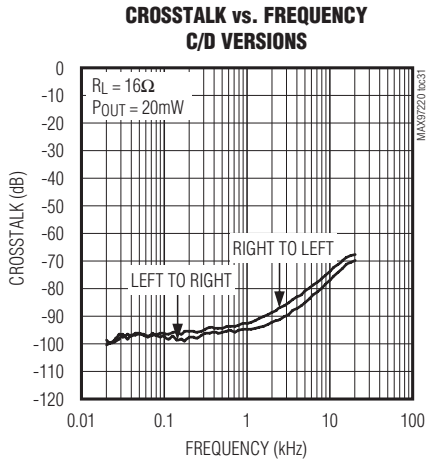


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## Typical Operating Characteristics (continued)

(VPVDD = VSVDD = VSVDD2 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 10kΩ, RF = 10kΩ, unless otherwise noted.)

MAX97220A-MAX97220D

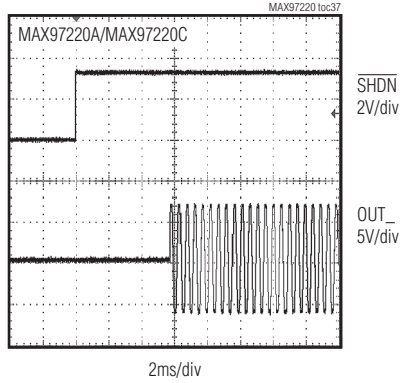


# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

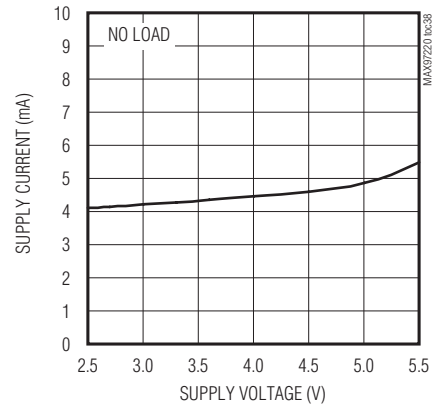
## Typical Operating Characteristics (continued)

(VPVDD = VSVDD = VSVDD2 = 5V, VPGND = VSGND = 0V, CBIAS = 0.1μF, C1 = C2 = 1μF, RIN = 10kΩ, RF = 10kΩ, unless otherwise noted.)

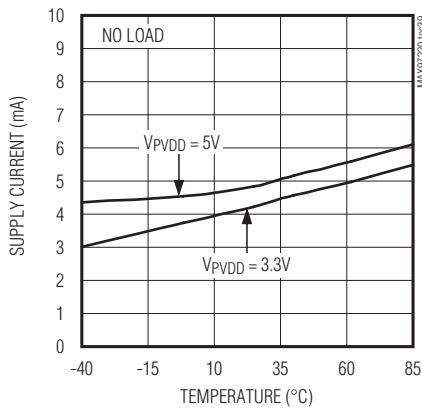
**EXITING SHUTDOWN**



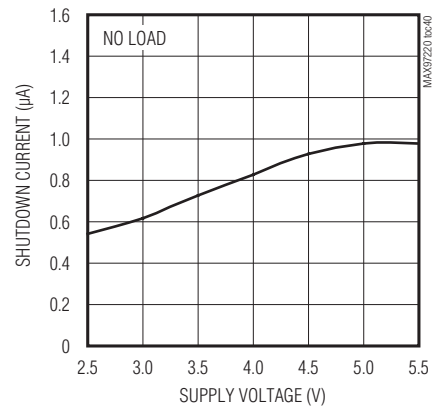
**SUPPLY CURRENT vs. SUPPLY VOLTAGE**



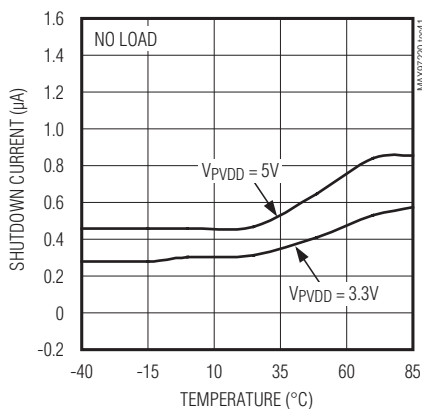
**SUPPLY CURRENT vs. TEMPERATURE**



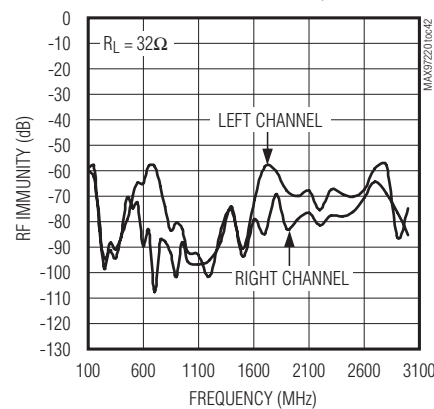
**SHUTDOWN CURRENT vs. SUPPLY VOLTAGE**



**SHUTDOWN CURRENT vs. TEMPERATURE**

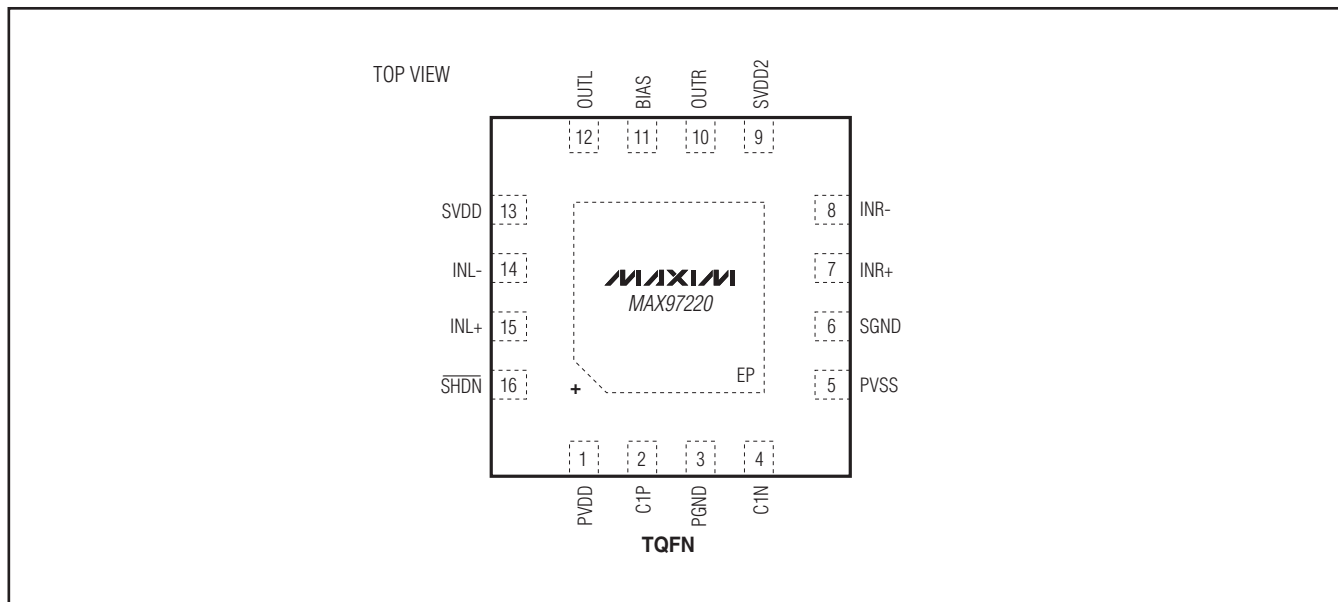


**RF IMMUNITY vs. FREQUENCY**



# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Pin Configuration



**MAX97220A-MAX97220D**

## Pin Description

PIN	NAME	FUNCTION
1	PVDD	Charge-Pump Power-Supply Input. Bypass to PGND with 1 $\mu$ F.
2	C1P	Positive Flying Capacitor Connection. Connect a 1 $\mu$ F capacitor between C1P and C1N.
3	PGND	Power Ground. Connect PGND and SGND together at the system ground plane.
4	C1N	Negative Flying Capacitor Connection. Connect a 1 $\mu$ F capacitor between C1P and C1N.
5	PVSS	Negative Charge-Pump Output. Bypass to PGND with 1 $\mu$ F.
6	SGND	Signal Ground. Connect PGND and SGND together at the system ground plane.
7	INR+	Right Positive Polarity Input
8	INR-	Right Negative Polarity Input
9	SVDD2	Signal Path Power-Supply Input. Bypass to PGND with 1 $\mu$ F. Connect directly to PVDD.
10	OUTR	Right DirectDrive Output
11	BIAS	Internal Supply Node. Bypass to PGND with 0.1 $\mu$ F.
12	OUTL	Left DirectDrive Output
13	SVDD	Signal Path Power-Supply Input. Bypass to PGND with 1 $\mu$ F. Connect directly to PVDD.
14	INL-	Left Negative Polarity Input
15	INL+	Left Positive Polarity Input
16	SHDN	Active-Low Shutdown. Drive SHDN high for normal operation.
—	EP	Exposed Pad. Electrically connect to PGND or leave unconnected.

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Detailed Description

The MAX97220\_ is a fully differential input line driver/headphone amplifier for set-top boxes, LCD TV, and home theater applications where audio fidelity is of primary importance. Power consumption of the amplifier is reduced while maintaining high SNR and THD+N performance. The MAX97220A/MAX97220B require external input and feedback resistors to set amplifier gain. The MAX97220C/MAX97220D feature internal input and feedback resistors for a set gain of +6dB. Output swings of  $3V_{RMS}$  with a 5V supply and  $2V_{RMS}$  with a 3.3V supply are perfect for line driver applications.

High fidelity is maintained through the differential input connection. An output noise voltage of  $7\mu V_{RMS}$  allows for 112dB SNR when powered from 5V and 109dB SNR when powered from 3.3V. The IC has better than 90dB THD+N across the entire audio bandwidth.

The MAX97220\_ operates from a single supply ranging from 2.5V to 5.5V. An on-chip charge pump inverts the positive supply (PVDD), creating an equal magnitude negative supply (PVSS). The headphone amplifiers

operate from bipolar supplies with their outputs biased about PGND (Figure 1). The benefit of this PGND bias is that the amplifier outputs do not have a DC component, typically  $PVDD/2$ . The large DC-blocking capacitors required with conventional headphone amplifiers are unnecessary, thus conserving board space, reducing system cost, and improving frequency response. Output power of 125mW into  $32\Omega$  is achievable from a 5V supply. The device features an undervoltage lockout that prevents operation from an insufficient power supply and click-and-pop suppression that eliminates audible transients on startup and shutdown.

## Differential Input

The IC can be configured as differential or pseudo-differential input amplifiers (Figures 2 and 3), making it compatible with all codecs. A differential input offers improved noise immunity over a single-ended input. In devices such as cellular phones, high-frequency signals from the RF transmitter can couple into the amplifier's input traces. The signals appear at the amplifier's inputs as common-mode noise. A differential input amplifier amplifies the difference of the two inputs while signals common to both inputs are cancelled. Configured differentially, the gain of the MAX97220A/MAX97220B is set by:

$$A_v = R_F/R_{IN}$$

The common-mode rejection ratio (CMRR) is limited by the external resistor matching, and if used, input capacitor matching at low frequencies. For example, the worst-case variation of 1% tolerant resistors results in 40dB CMRR, while 0.1% resistors result in 60dB CMRR. For best matching, use resistor arrays.

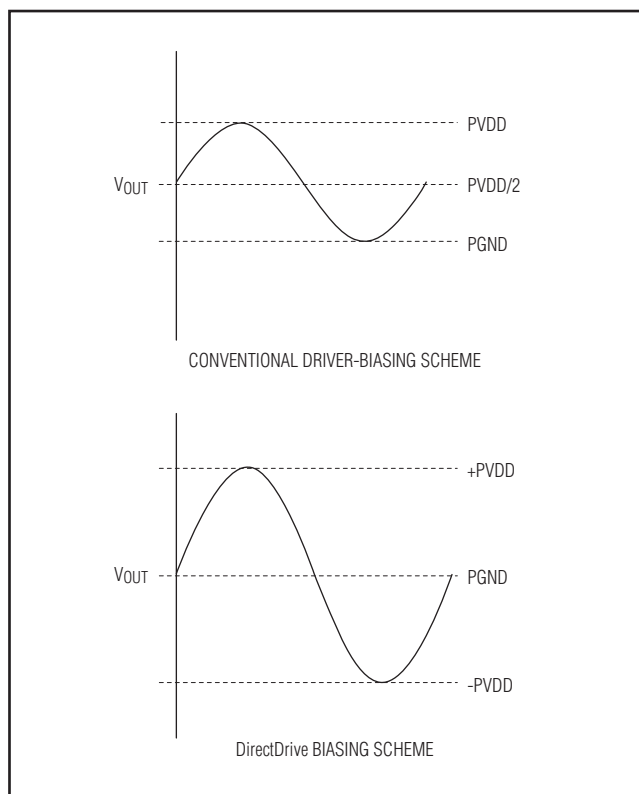


Figure 1. Conventional Driver Output Waveform vs. MAX97220\_ Output Waveform

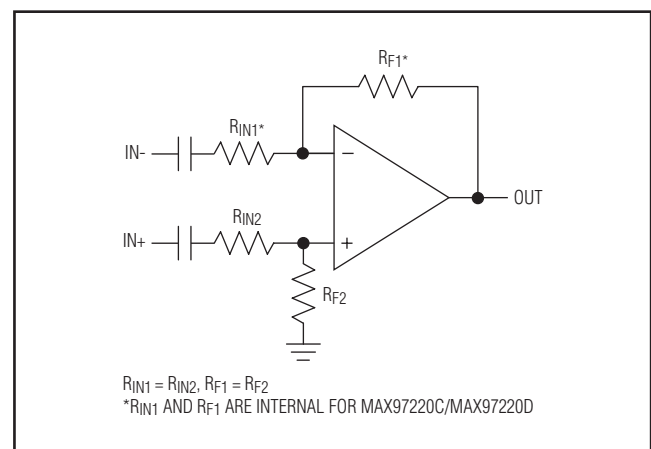


Figure 2. Differential Input Configuration

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

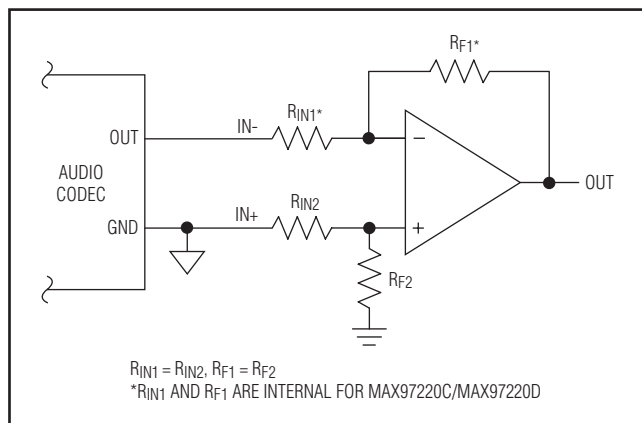


Figure 3. Pseudo-Differential Input Configuration

## DirectDrive

Conventional single-supply headphone amplifiers have their outputs biased about a nominal DC voltage (typically half the supply) for maximum dynamic range. Large coupling capacitors are needed to block this DC bias from the headphone. Without these capacitors, a significant amount of DC current flows to the headphone, resulting in unnecessary power dissipation and possible damage to both the headphone and the headphone amplifier.

Maxim's patented DirectDrive architecture uses a charge pump to create an internal negative supply voltage, allowing the IC's outputs to be biased about PGND. With no DC component, there is no need for the large DC-blocking capacitors. Instead of two large (220 $\mu$ F, typ) tantalum capacitors, the IC charge pump requires two small ceramic capacitors, conserving board space, reducing cost, and improving the frequency response of the headphone amplifier.

## Input Filter

In addition to the cost and size disadvantages of DC-blocking capacitors required by conventional headphone amplifiers, these capacitors limit the amplifier's low-frequency response and can distort the audio signal.

If input capacitors are used, input capacitor  $C_{IN}$ , in conjunction with internal input resistor  $R_{IN}$ , forms a highpass

filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2\pi R_{IN} C_{IN}}$$

Setting  $f_{-3dB}$  too high affects the low-frequency response of the amplifier. Use capacitors with adequately low voltage coefficients, such as X7R ceramic capacitors with a high voltage rating. Capacitors with higher voltage coefficients result in increased distortion at low frequencies.

## BIAS Capacitor

Bypass BIAS with a 0.1 $\mu$ F capacitor to PGND. Do not connect external loads to BIAS.

## Charge Pump

The MAX97220\_ features a low-noise charge pump. The 500kHz switching frequency is well beyond the audio range and, thus, does not interfere with the audio signals. The switch drivers feature a controlled switching speed that minimizes noise generated by turn-on and turn-off transients. By limiting the switching speed of the charge pump, the di/dt noise caused by the parasitic bond wire and trace inductance is minimized. The IC requires a 1 $\mu$ F flying capacitor between C1P and C1N and a 1 $\mu$ F hold capacitor from PVSS to PGND.

## Click-and-Pop Suppression

The IC features Maxim's industry-leading click-and-pop suppression circuitry. When entering shutdown, the amplifier outputs are high impedance to ground. This scheme minimizes the energy present in the audio band.

## Shutdown

The IC features a 1 $\mu$ A low-power shutdown mode that reduces power consumption. When the active-low shutdown mode is entered, the device's internal bias circuitry is disabled, the amplifier outputs go high impedance, and BIAS is driven to PGND. The MAX97220A/MAX97220B inputs are driven to PGND.

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Applications Information

### MAX9722 Compatibility

The MAX97220\_ is compatible with the footprint of the MAX9722. BIAS on the MAX97220\_ is in the same position as SVSS. On the MAX9722, SVSS is connected to PVSS. For the MAX97220\_, there is only one charge-pump output that doubles as the amplifier's negative power-supply input. The connection of negative charge-pump output and amplifier negative power-supply input is internal on the MAX97220\_ and external on the MAX9722.

To implement a PCB that is compatible with both the MAX9722 and MAX97220\_, put a capacitor pad from BIAS/SVSS (MAX97220\_/MAX9722 pin 11) to PGND. Also, place a 0Ω resistor pad from BIAS/SVSS (MAX97220\_/MAX9722 pin 11) to PVSS (pin 5 on both parts). Install the 0Ω resistor when the MAX9722 is used and leave the resistor out of circuit when the MAX97220\_ is used (Figure 4).

### Power Dissipation

While driving a headphone load, the IC dissipates a significant amount of power. The maximum power dissipation is given in the Continuous Power Dissipation of the *Absolute Maximum Ratings* section or can be calculated by the following equation:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where  $T_{J(MAX)}$  is +150°C,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the reciprocal of the derating factor in °C/W as specified in the *Absolute Maximum Ratings* section.

Since the IC is a stereo amplifier, the total maximum internal power dissipation for a given  $V_{DD}$  and load is given by the following equation:

$$P_{D(MAX)} = \frac{4V_{DD}^2}{\pi^2 R_L}$$

If the internal power dissipation for a given application exceeds the maximum allowed for a given package, reduce power dissipation by decreasing supply voltage, ambient temperature, input signal, or gain, or by increasing load impedance.

The TQFN package features an exposed thermal pad on its underside. This pad lowers the package's thermal impedance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to PGND or an isolated plane.

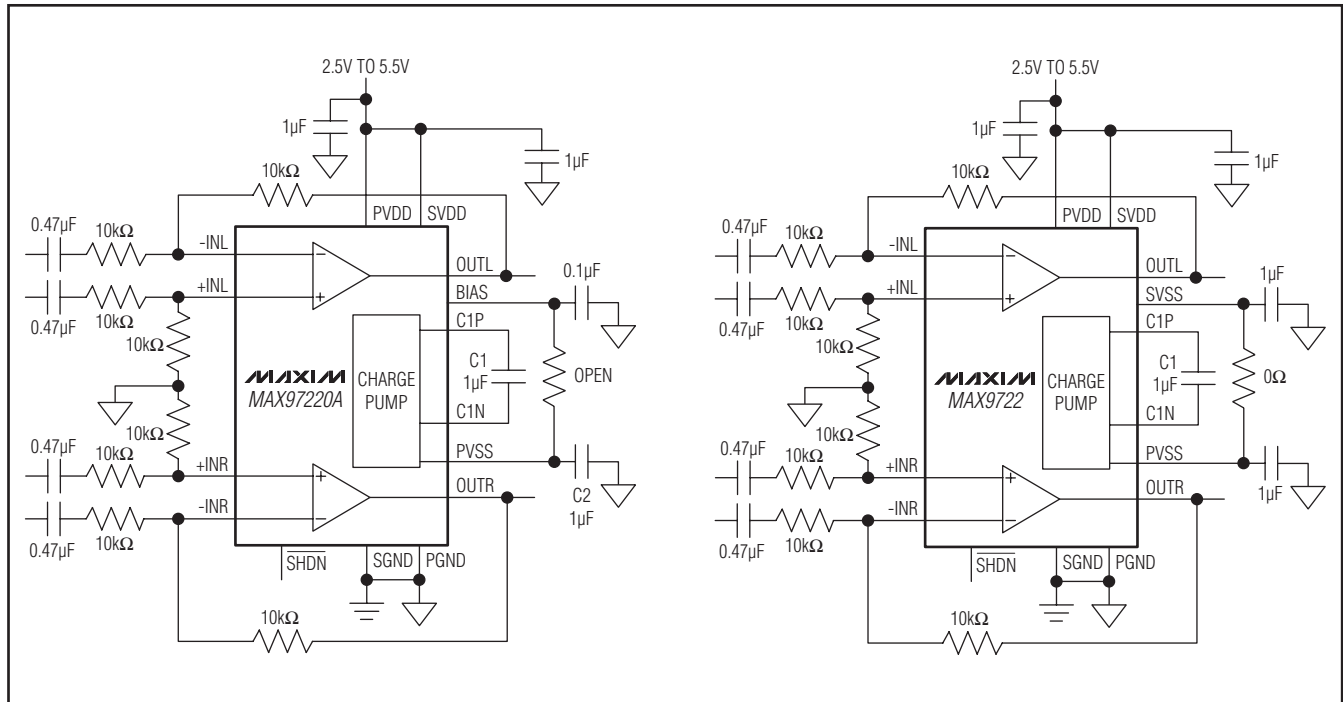


Figure 4. MAX97220A vs. MAX9722 PCB Layout

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

Thermal-overload protection limits total power dissipation in the IC. When the junction temperature exceeds +160°C, the thermal protection circuitry disables the amplifier. Operation returns to normal once the die cools by 15°C.

## Charge-Pump Capacitor Selection

Use capacitors with an ESR less than 100mΩ for optimum performance. Low-ESR ceramic capacitors minimize the output resistance of the charge pump. For best performance over the extended temperature range, select capacitors with an X7R dielectric.

## Flying Capacitor (C1)

The value of the flying capacitor (C1) affects the charge pump's load regulation and output resistance. A C1 value that is too small degrades the device's ability to provide sufficient current drive, which leads to a loss of output voltage. Increasing the value of C1 improves load regulation and reduces the charge-pump output resistance to an extent. Above 1μF, the on-resistance of the switches and the ESR of C1 and C2 dominate.

## Hold Capacitor (C2)

The hold capacitor value and ESR directly affect the ripple at PVSS. Use a low-ESR 1μF capacitor for C2.

## Amplifier Gain

The gain of the MAX97220C/MAX97220D is internally set at 6dB where all gain-setting resistors are integrated into the device. The internally set gain, in combination with DirectDrive, results in a headphone amplifier that requires only tiny 1μF capacitors to complete the amplifier circuit.

The gain of the MAX97220A/MAX97220B amplifier is set externally as shown in Figure 5. The gain is:

$$A_V = -R_F/R_{IN}$$

Choose feedback resistor values between the 4.7kΩ and 100kΩ range.

## Supply Bypassing

Proper power-supply bypassing ensures low-noise, low-distortion performance. Connect a 1μF ceramic capacitor from PVDD to PGND and a 1μF ceramic capacitor from SVDD to PGND. Add additional bulk capacitance as required by the application. Locate the bypass capacitor as close as possible to the device.

## PCB Layout and Grounding

Good PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and route heat away from the device. Good grounding improves audio performance, and prevents any digital switching noise from coupling into the audio.

Connect PGND and SGND together at a single point on the PCB. Connect all components associated with the charge pump (C1 and C2) to the PGND plane. Connect PVDD and SVDD together at the device. Place capacitors C1 and C2 as close as possible to the device. Ensure the PCB layout is partitioned so that the large switching currents in the ground plane do not return through SGND and the traces and components in the audio signal path. Refer to the MAX97220 Evaluation Kit for layout guidelines.

The IC is inherently designed for excellent RF immunity. For best performance, add ground fills around all signal traces on top or bottom PCB planes. Also, ensure a solid ground plane is used in multilayer PCB designs.

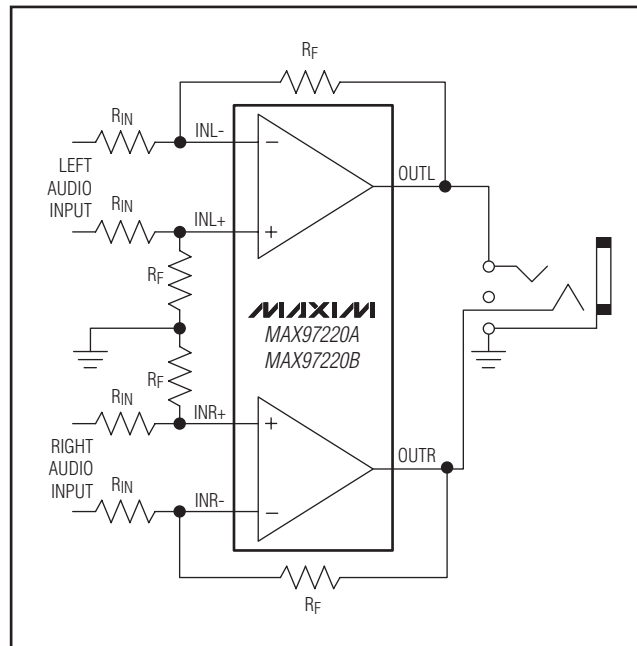
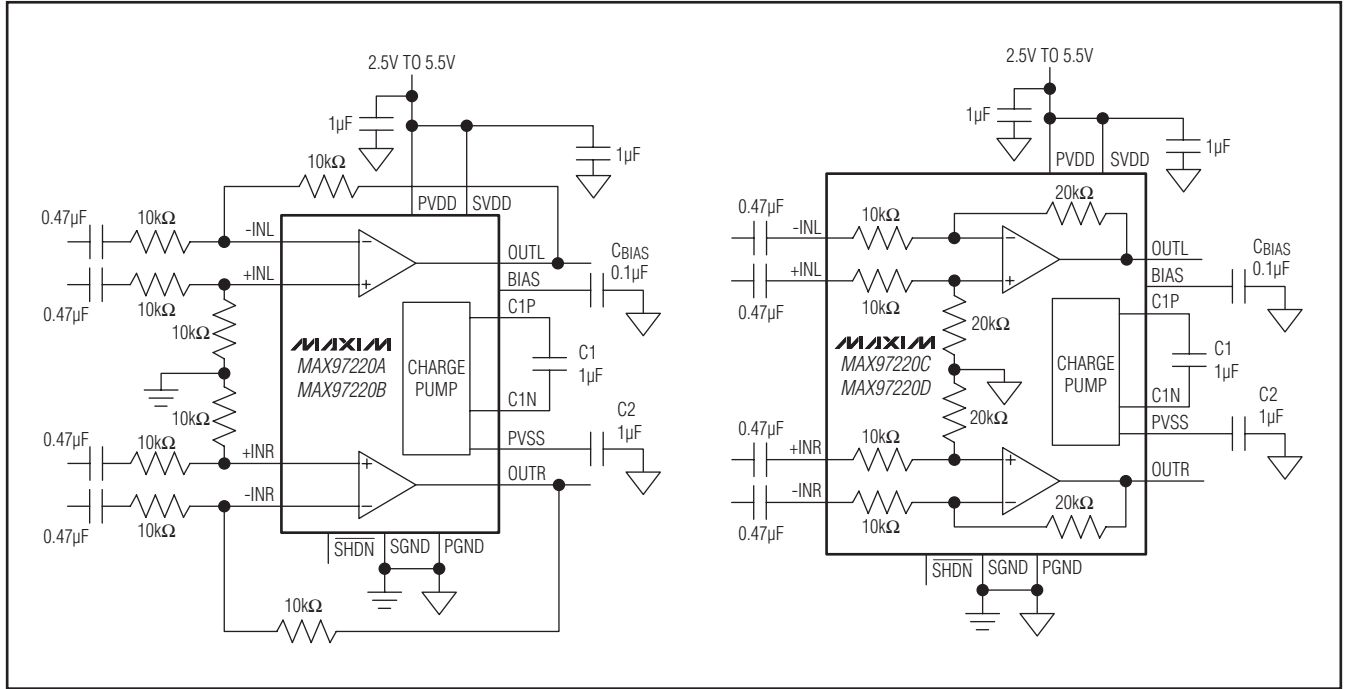


Figure 5. Setting the MAX97220A/MAX97220B Gain

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Functional Diagrams



## Chip Information

PROCESS: BiCMOS



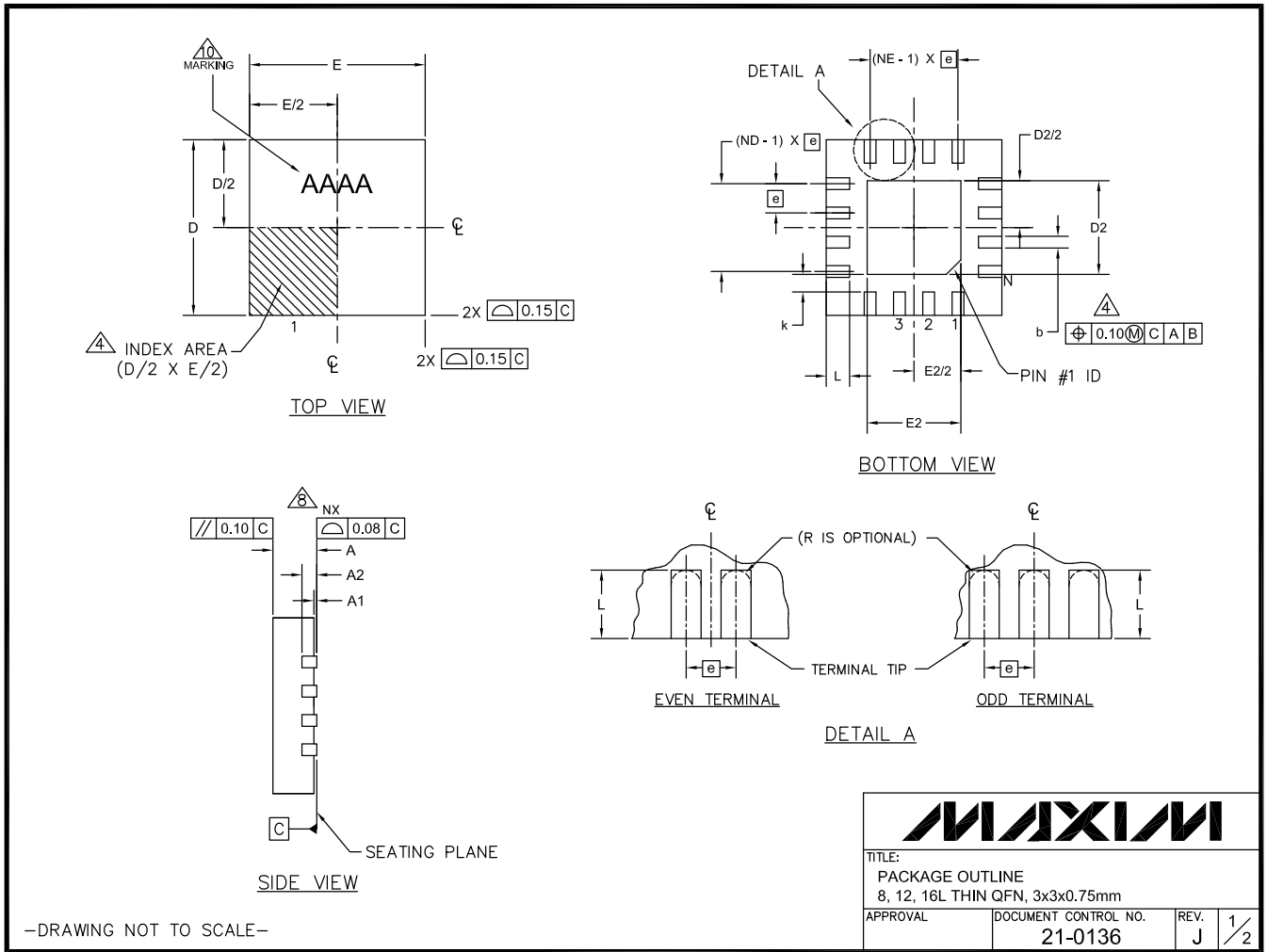
# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Package Information

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
16 TQFN	T1633-4	<a href="#">21-0136</a>	<a href="#">90-0031</a>

**MAX97220A-MAX97220D**



# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Package Information (continued)

For the latest package outline information and land patterns (footprints), go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages). Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.


PKG	8L 3x3			12L 3x3			16L 3x3		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
b	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30
D	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
E	2.90	3.00	3.10	2.90	3.00	3.10	2.90	3.00	3.10
e	0.65 BSC.			0.50 BSC.			0.50 BSC.		
L	0.35	0.55	0.75	0.45	0.55	0.65	0.30	0.40	0.50
N	8			12			16		
ND	2			3			4		
NE	2			3			4		
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF		
k	0.25	-	-	0.25	-	-	0.25	-	-

PKG. CODES	D2			E2			PIN ID	JEDEC
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.		
TQ833-1	0.25	0.70	1.25	0.25	0.70	1.25	0.35 x 45°	WEEC
T1233-1	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-3	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1233-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-1
T1633-2	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633F-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633FH-3	0.65	0.80	0.95	0.65	0.80	0.95	0.225 x 45°	WEED-2
T1633-4	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2
T1633-5	0.95	1.10	1.25	0.95	1.10	1.25	0.35 x 45°	WEED-2

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.20 mm AND 0.25 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220 REVISION C.
10. MARKING SHOWN IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
12. WARPAGE NOT TO EXCEED 0.10mm.
13. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND Pb FREE (+) PARTS.

-DRAWING NOT TO SCALE-

		
TITLE: PACKAGE OUTLINE 8, 12, 16L THIN QFN, 3x3x0.75mm		
APPROVAL	DOCUMENT CONTROL NO. 21-0136	REV. J 2/2

# Differential Input DirectDrive Line Drivers/Headphone Amplifiers

## Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	1/11	Initial release	—
1	10/11	Added top marks to <i>Ordering Information</i> , added B/C/D versions to Quiescent Supply Current, Output Signal Attenuation in Shutdown, and Power-Supply Rejection Ratio in the <i>Electrical Characteristics</i> table	2, 3

MAX97220A-MAX97220D

Maxim cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim product. No circuit patent licenses are implied. Maxim reserves the right to change the circuitry and specifications without notice at any time.

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