**SANYO** *SANYO Semiconductors*

# DATA SHEET

An ON Semiconductor Company

**Bi-CMOS integrated circuit**

# LV8415CB — Blurring correction driver IC for DSC
# H bridge × 2ch driver

## Overview

LV8415CB is blurring correction driver IC for DSC.

## Functions

- Actuator driver (saturation drive H bridge) × 2ch
- Constant current hall bias circuit × 2ch
- With built-in for PWM signal generation logic circuit × 2ch
- 8bitDAC for hall amplifier offset adjustment × 2ch
- Two systems in power supply ($V_M$: for actuator, $V_{CC}$)
- With built-in low voltage malfunction prevention circuit

- Hall Amplifier × 2ch
- General-purpose amplifier × 2ch
- 8bitDAC for hall bias × 2ch
- Three line serial input
- With built-in thermal protection circuit

## Specifications

### Maximum Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage 1 | $V_M$ max | | 6 | V |
| Supply voltage 2 | $V_{CC}$ max | | 6 | V |
| Output peak current | $I_O$ peak | OUT1 to 2 (t ≤ 10msec, duty ≤ 20%) | 600 | mA |
| Output current | $I_O$ max | OUT1 to 2 | 350 | mA |
| Hall bias current | $I_{HB}$ max | | 5 | mA |
| Allowable power dissipation | Pd max | On a specified board * | 1 | W |
| Operating temperature | Topr | | -20 to +85 | °C |
| Storage temperature | Tstg | | -55 to +150 | °C |

\* Specified board: 40.0mm×50.0mm×0.8mm, Four layers fiberglass epoxy circuit board.

### Allowable Operating Ratings at Ta = 25°C

| Parameter | Symbol | Conditions | Ratings | Unit |
|---|---|---|---|---|
| Supply voltage range 1 | $V_M$ | | 2.7 to 5.5 | V |
| Supply voltage range 2 | $V_{CC}$ | | 2.7 to 5.5 | V |
| Logic input voltage | $V_{IN}$ | | 0 to $V_{CC}$+0.3 | V |

# LV8415CB

**Electrical Characteristics** at Ta = 25°C, $V_{CC}$ = 3.3V, $V_M$ = 5.0V

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Current consumption when standing by | $I_{CCO}$ | ST = "L" | | | 1.0 | μA |
| VM current consumption | $I_M$ | $V_M$ = 5.0V, ST = "H", no load | | | 10 | μA |
| $V_{CC}$ current consumption | $I_{CC}$ | ST = "H", no load | | 2 | 3.2 | mA |
| $V_{CC}$ low voltage cutting voltage | VTHVCC | | 2.1 | 2.4 | 2.6 | V |
| Low voltage hysteresis voltage | VTHHYS | | 100 | 150 | 200 | mV |
| Thermal shutdown temperature | TSD | Design guarantee | 155 | 175 | 195 | °C |
| Thermal hysteresis width | ΔTSD | Design guarantee | 15 | 35 | 55 | °C |
| **H bridge output (OUT1-2)** | | | | | | |
| Output on resistance | Ronu | $I_O$ = 100mA, Upper-side on resistance | | 0.7 | 0.98 | Ω |
| | Rond | $I_O$ = 100mA, Under-side on resistance | | 0.5 | 0.7 | Ω |
| Output leakage current | $I_O$ leak | | | | 1 | μA |
| Diode forward voltage | VD | ID = -100mA | | 0.7 | | V |
| **Operational amplifier (OP-AMP1-4)** | | | | | | |
| Input offset voltage | OP_VIO | | | ±1 | ±5 | mV |
| Input offset current | OP_IIO | | | ±5 | ±50 | nA |
| Input bias current | OP_IB | | | 30 | 250 | nA |
| Equal phase input voltage range | VICM | | 0 | | $V_{CC}$ | V |
| Equal phase signal removal ratio | CMR | | 60 | 80 | | dB |
| Large amplitude voltage range | VG | $R_L$ = 20kΩ, VIN = 1mV(open loop gain) | 1 | 10 | | V/mV |
| Output voltage range | $V_OH$ | $R_L$ = 20kΩ | $V_{CC}$-0.2 | | | V |
| | $V_{OL}$ | $R_L$ = 20kΩ | | | 0.2 | V |
| Power supply change removal ratio | SVR | | 65 | 85 | | dB |
| Output current (sink/source) | OP_IO | | 1 | 2 | | mA |
| **Hall bias (HB1-2)** | | | | | | |
| Output current | IHB | RHG = 1kΩ, VHBIN = 1.0V | 0.95 | 1.00 | 1.05 | mA |
| Output saturation voltage | VSATHB | $I_{HB}$ = 1mA | $V_{CC}$-0.2 | | | V |
| **Standard voltage** | | | | | | |
| Standard voltage | VREF | | 1.60 | 1.65 | 1.70 | V |
| Standard voltage load characteristic | VRref | $I_{REF}$ = 100μA | 1.60 | 1.65 | 1.70 | V |
| **Internal CLK frequency for PWM drive** | | | | | | |
| CLK frequency | Fclk | | 13.5 | 15 | 17.25 | MHz |
| **Control pin (ST, SCLK, DATA, STB)** | | | | | | |
| Built-in pull-down resistance | Rin | | 50 | 100 | 200 | kΩ |
| Input current | $I_{IN}L$ | $V_{IN}$ = 0V | | | 1.0 | μA |
| | $I_{IN}H$ | $V_{IN}$ = 3.3V | 20 | 33 | 50 | μA |
| Input "L" level voltage | $V_{IN}L$ | | | | 1.0 | V |
| Input "H" level voltage | $V_{IN}H$ | | 2.5 | | | V |

## Package Dimensions

unit : mm (typ)

3397

TOP VIEW

2.47

2.47

SIDE VIEW

BOTTOM VIEW

0.235

0.4

0.235

0.4

A
B
C
D
E
F

6 5 4 3 2 1

∅0.245

SIDE VIEW

0.69 MAX

0.175

SANYO : WLP32(2.47X2.47)

### Pd max - Ta

Specified circuit board:
$40.0 \times 50.0 \times 0.8 mm^3$
Four layer glass epoxy board

1.2

1.0

0.8

0.6

0.4

0.2

0

0.52

Allowable power dissipation, Pd max – W

-30    0    30    60    90    120

Ambient temperature, Ta – °C
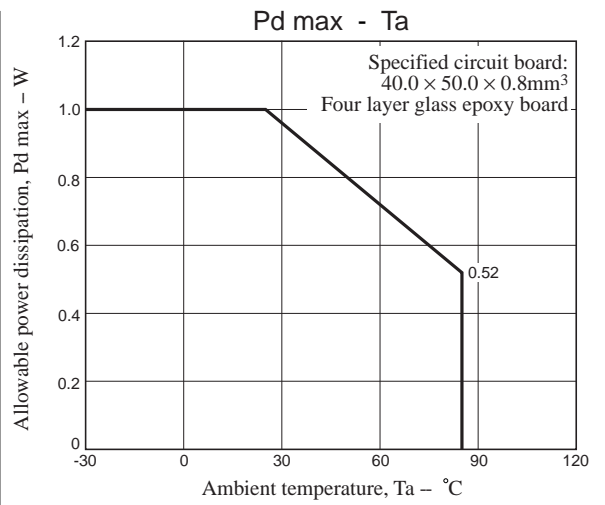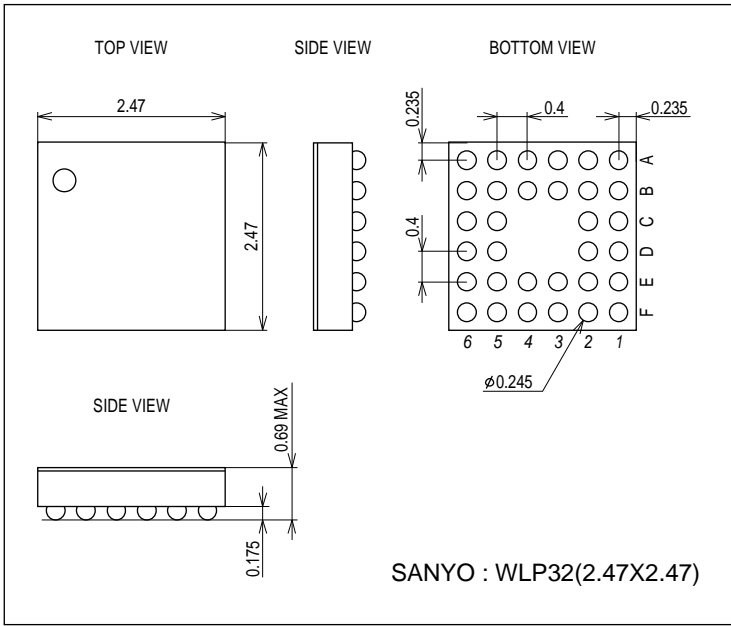
## Pin Assignment
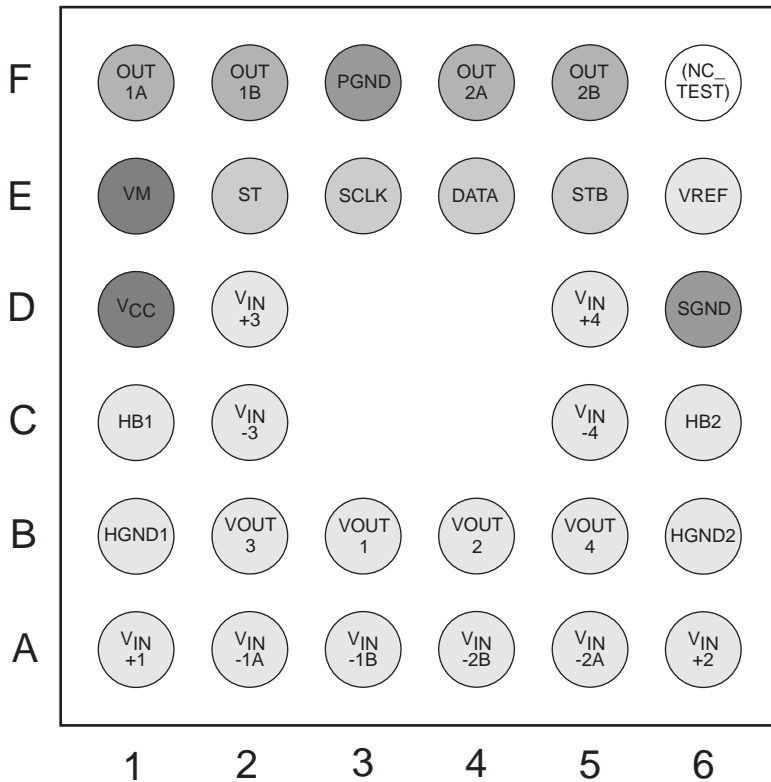
(NC_TEST) is pin only for the test.
Please NC_TESTpin connect GND line.

| | 1 | 2 | 3 | 4 | 5 | 6 |
|---|---|---|---|---|---|---|
| F | OUT 1A | OUT 1B | PGND | OUT 2A | OUT 2B | (NC_TEST) |
| E | VM | ST | SCLK | DATA | STB | VREF |
| D | $V_{CC}$ | $V_{IN}+3$ | | | $V_{IN}+4$ | SGND |
| C | HB1 | $V_{IN}-3$ | | | $V_{IN}-4$ | HB2 |
| B | HGND1 | VOUT 3 | VOUT 1 | VOUT 2 | VOUT 4 | HGND2 |
| A | $V_{IN}+1$ | $V_{IN}-1A$ | $V_{IN}-1B$ | $V_{IN}-2B$ | $V_{IN}-2A$ | $V_{IN}+2$ |

Power supply pin

GND pin

Output pin

Logic control pin

Analog control pin

Ball side view

## Pin function

| Pin No. | Pin name | Pin function | Equivalent Circuit |
|---------|----------|--------------|--------------------|
| E2<br>E3<br>E4<br>E5 | ST<br>SCLK<br>DATA<br>STB | Input pin.<br>High level 2V to ($V_{CC}$ = 3.3V)<br>Low level 0 to 0.5V ($V_{CC}$ = 3.3V) | |
| F1<br>F2<br>F4<br>F5<br>E1<br>F3 | OUT1A<br>OUT1B<br>OUT2A<br>OUT2B<br>VM<br>PGND | Output pin. (PWM output)<br>VM : POWER – Power supply pin.<br>PGND : POWER – GND pin. | |
| D1<br>D6 | $V_{CC}$<br>SGND | Signal system power supply pin<br>Signal system GND pin | |
| C1<br>B1<br>C6<br>B6 | HB1<br>HGND1<br>HB2<br>HGND2 | HB1, 2 pin<br>Hall bias source pin<br>HGND1, 2 pin<br>Hall bias current setting pin | |
| A1<br>A2<br>A3<br>A6<br>A5<br>A4 | $V_{IN}+1$<br>$V_{IN}-1A$<br>$V_{IN}-1B$<br>$V_{IN}+2$<br>$V_{IN}-2A$<br>$V_{IN}-2B$ | Hall amplifier input pin<br>$V_{IN}+$ Hall amplifier+ input pin<br>$V_{IN}-A$ Hall amplifier- input pin<br>$V_{IN}-B$ LPF formation pin<br>(The filter is formed for the noise removal.) | |
| B3<br>B4 | VOUT1<br>VOUT2 | Hall amplifier output pin.<br>VOUT1 : Hall amplifier 1ch output pin.<br>VOUT2 : Hall amplifier 2ch output pin. | |

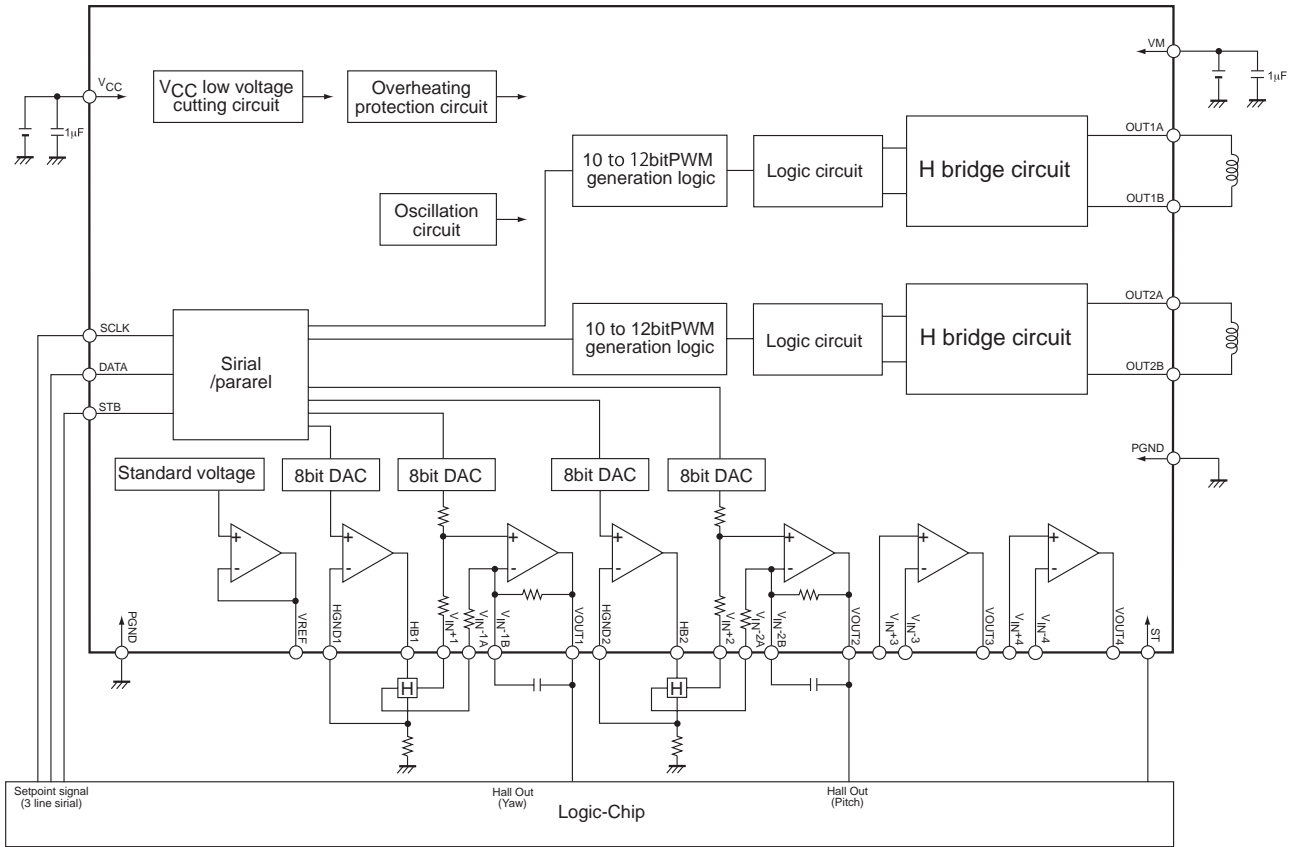# LV8415CB

| Pin No. | Pin name | Pin function | Equivalent Circuit |
|---------|----------|--------------|--------------------|
| D2<br>C2<br>D5<br>C5 | $V_{IN}+3$<br>$V_{IN}-3$<br>$V_{IN}+4$<br>$V_{IN}+4$ | General purpose amplifier input pin.<br>$V_{IN}+3$ : 3ch general purpose amplifier+ input pin<br>$V_{IN}-3$ : 3ch general purpose amplifier- input pin<br>$V_{IN}+4$ : 4ch general purpose amplifier+ input pin<br>$V_{IN}-4$ : 4ch general purpose amplifier- input pin |  |
| B2<br>B5 | VOUT3<br>VOUT4 | General purpose amplifier output pin.<br>VOUT3 : 3ch general purpose amplifier output pin<br>VOUT4 : 4ch general purpose amplifier output pin |  |
| E6 | VREF | Internal standard voltage pin<br>$V_{CC}/2$ output |  |
| F6 | NC-TEST | N.C. pin<br>TEST pin<br>Please NC_TEST pin connect GND line. |  |

## Block Diagram

**3 line serial communication electrical Characteristics at Ta = 25°C, $V_{CC}$ = 3.3V, $V_M$ = 5.0V**

| Parameter | Symbol | Conditions | Ratings | | | Unit |
|---|---|---|---|---|---|---|
| | | | min | typ | max | |
| Serial data forwarding pin | | | | | | |
| Logic pin input current | $I_{IN}L$ | $V_{IN}$=0V(SCLK, DATA, STB) | | | 1.0 | μA |
| | $I_{IN}H$ | $V_{IN}$=3.3V(SCLK, DATA, STB) | | 33 | 50 | V |
| Input "H" level voltage | $V_{IN}H$ | SCLK, DATA, STB | 2.5 | | | V |
| Input "L" level voltage | $V_{IN}L$ | SCLK, DATA, STB | | | 1.0 | μs |
| Minimum SCLK "H" pulse width | $T_{SC}H$ | | 0.1 | | | μs |
| Minimum SCLK "L" pulse width | $T_{SC}L$ | | 0.1 | | | μs |
| STB regulation time | Tlat | | 0.1 | | | μs |
| Minimum STB pulse width | Tlatw | | 0.1 | | | μs |
| Data set-up time | Tds | | 0.1 | | | μs |
| Data hold time | Tdh | | 0.1 | | | μs |
| maximum CLK frequency | Fclk | | | | 4 | MHz |
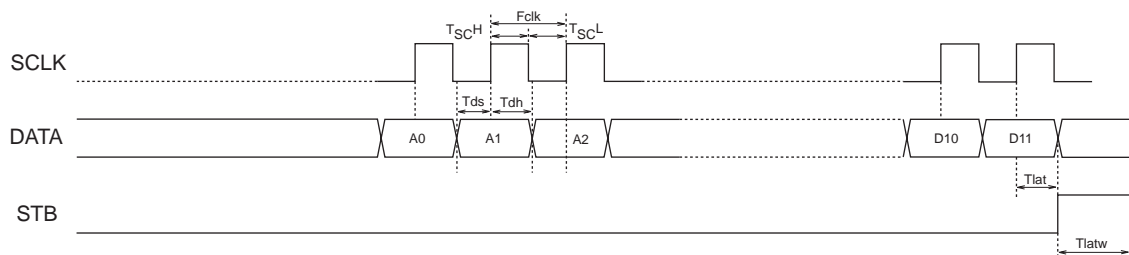
Serial data timing condition

Serial data input timing chart
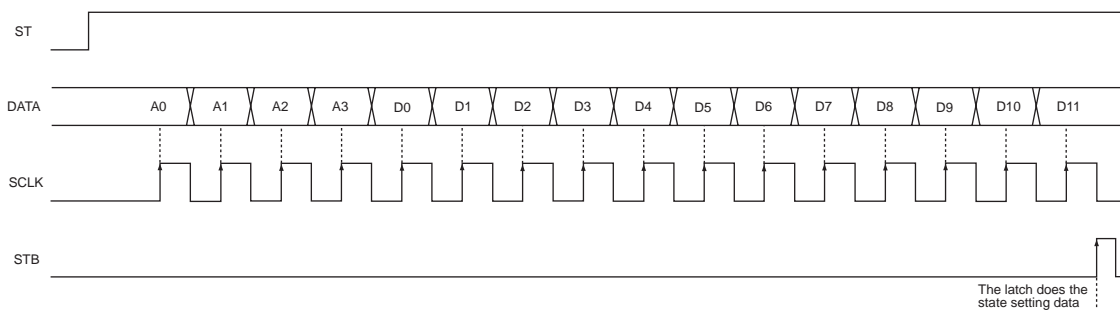
It inputs it from A0 in order of D11. The data transfer is done by the rising edge, and after all data transfers, the latch does all data to SCLK by the STB signal standing up. The STB signal accepts and the internal logic of IC doesn't accept the SCLK signal during "H".

Serial logic map

PWMh - bridge relation serial map

| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | D8 | D9 | D10 | D11 | Setting mode | Set content | Remarks |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 100% | |
| | | | | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 511/512 × 100% | |
| | | | | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 510/512 × 100% | Reverse |
| | | | | | | | | | | | | | | | | | … | |
| | | | | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | 2/512 × 100% | |
| | | | | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | 1/512 × 100% | |
| | | | | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1ch PWM Duty set | 0% | Middle point |
| | | | | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 1/512 × 100% | |
| | | | | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 2/512 × 100% | |
| | | | | | | | | | | | | | | | | | … | Normal rotation |
| | | | | * | * | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 509/512 × 100% | |
| | | | | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 510/512 × 100% | |
| | | | | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 511/512 × 100% | |
| 1 | 0 | 0 | 0 | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 100% | |
| | | | | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 511/512 × 100% | |
| | | | | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | | 510/512 × 100% | Reverse |
| | | | | | | | | | | | | | | | | | … | |
| | | | | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | 2/512 × 100% | |
| | | | | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | 1/512 × 100% | |
| | | | | * | * | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 2ch PWM Duty set | 0% | Middle point |
| | | | | * | * | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 1/512 × 100% | |
| | | | | * | * | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | 2/512 × 100% | |
| | | | | | | | | | | | | | | | | | … | Normal rotation |
| | | | | * | * | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 509/512 × 100% | |
| | | | | * | * | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 510/512 × 100% | |
| | | | | * | * | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | | 511/512 × 100% | |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 0V | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 1/255 × VREF | |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 2/255 × VREF | |
| | | | | | | | | | | | | * | * | * | * | 1ch hall bias set (8bit DAC) | … | |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | 253/255 × VREF | |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | 254/255 × VREF | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | VREF | |
| 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 0V | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 1/255 × VREF | |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 2/255 × VREF | |
| | | | | | | | | | | | | * | * | * | * | 2ch hall bias set (8bit DAC) | … | |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | 253/255 × VREF | |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | 254/255 × VREF | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | VREF | |
| 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 0V | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | $1/255 × V_{CC}$ | |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 1ch hall amplifier offset adjustment (8bit DAC) | $2/255 × V_{CC}$ | |
| | | | | | | | | | | | | * | * | * | * | | … | |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $253/255 × V_{CC}$ | |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $254/255 × V_{CC}$ | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $V_{CC}$ | |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | 0V | |
| | | | | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | | $1/255 × V_{CC}$ | |
| | | | | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | * | * | * | * | 2ch hall amplifier offset adjustment (8bit DAC) | $2/255 × V_{CC}$ | |
| | | | | | | | | | | | | * | * | * | * | | … | |
| | | | | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $253/255 × V_{CC}$ | |
| | | | | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $254/255 × V_{CC}$ | |
| | | | | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | * | * | * | * | | $V_{CC}$ | |

The PWMh-bridge driver's ON/OFF operation is done with the ST pin.

# LV8415CB

Hall amplifier gain setting range

Hall amplifier relation serial map

| Input | | | | | | | | Setting mode | Hall amplifier magnification |
| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 | | ()Inside: Resistance |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1ch hall amplifier gain setting ( "3" Resistance ÷ "2" Resistance) | 10 (36k//3.6k) |
| | | | | 1 | 0 | 0 | 0 | | 20 (72k//3.6k) |
| | | | | 0 | 1 | 0 | 0 | | 40 (144k//3.6k) |
| | | | | 1 | 1 | 0 | 0 | | 50 (180k//3.6k) |
| | | | | 0 | 0 | 1 | 0 | | 60 (216k//3.6k) |
| | | | | 1 | 0 | 1 | 0 | | 70 (252k//3.6k) |
| | | | | 0 | 1 | 1 | 0 | | 90 (324k//3.6k) |
| | | | | 1 | 1 | 1 | 0 | | 100 (360k//3.6k) |
| | | | | 0 | 0 | 0 | 1 | | 110 (396k//3.6k) |
| | | | | 1 | 0 | 0 | 1 | | 120 (432k//3.6K) |
| | | | | 0 | 1 | 0 | 1 | | 140 (504k//3.6k) |
| | | | | 1 | 1 | 0 | 1 | | 150 (540k//3.6k) |
| | | | | 0 | 0 | 1 | 1 | | 160 (570k//3.6k) |
| | | | | 1 | 0 | 1 | 1 | | 170 (612k//3.6k) |
| | | | | 0 | 1 | 1 | 1 | | 190 (684k//3.6k) |
| | | | | 1 | 1 | 1 | 1 | | 200 (720k//3.6k) |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 2ch hall amplifier gain setting ( "3" Resistance ÷ "2" Resistance) | 10 (36k//3.6k) |
| | | | | 1 | 0 | 0 | 0 | | 20 (72k//3.6k) |
| | | | | 0 | 1 | 0 | 0 | | 40 (144k//3.6k) |
| | | | | 1 | 1 | 0 | 0 | | 50 (180k//3.6k) |
| | | | | 0 | 0 | 1 | 0 | | 60 (216k//3.6k) |
| | | | | 1 | 0 | 1 | 0 | | 70 (252k//3.6k) |
| | | | | 0 | 1 | 1 | 0 | | 90 (324k//3.6k) |
| | | | | 1 | 1 | 1 | 0 | | 100 (360k//3.6k) |
| | | | | 0 | 0 | 0 | 1 | | 110 (396k//3.6k) |
| | | | | 1 | 0 | 0 | 1 | | 120 (432k//3.6K) |
| | | | | 0 | 1 | 0 | 1 | | 140 (504k//3.6k) |
| | | | | 1 | 1 | 0 | 1 | | 150 (540k//3.6k) |
| | | | | 0 | 0 | 1 | 1 | | 160 (570k//3.6k) |
| | | | | 1 | 0 | 1 | 1 | | 170 (612k//3.6k) |
| | | | | 0 | 1 | 1 | 1 | | 190 (684k//3.6k) |
| | | | | 1 | 1 | 1 | 1 | | 200 (720k//3.6k) |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1ch hall amplifier offset resistance / input resistance ( "1" Resistance ÷ "2" Resistance) | 10 (36k//3.6k) |
| | | | | 1 | 0 | 0 | 0 | | 20 (72k//3.6k) |
| | | | | 0 | 1 | 0 | 0 | | 40 (144k//3.6k) |
| | | | | 1 | 1 | 0 | 0 | | 50 (180k//3.6k) |
| | | | | 0 | 0 | 1 | 0 | | 60 (216k//3.6k) |
| | | | | 1 | 0 | 1 | 0 | | 70 (252k//3.6k) |
| | | | | 0 | 1 | 1 | 0 | | 90 (324k//3.6k) |
| | | | | 1 | 1 | 1 | 0 | | 100 (360k//3.6k) |
| | | | | 0 | 0 | 0 | 1 | | 110 (396k//3.6k) |
| | | | | 1 | 0 | 0 | 1 | | 120 (432k//3.6K) |
| | | | | 0 | 1 | 0 | 1 | | 140 (504k//3.6k) |
| | | | | 1 | 1 | 0 | 1 | | 150 (540k//3.6k) |
| | | | | 0 | 0 | 1 | 1 | | 160 (570k//3.6k) |
| | | | | 1 | 0 | 1 | 1 | | 170 (612k//3.6k) |
| | | | | 0 | 1 | 1 | 1 | | 190 (684k//3.6k) |
| | | | | 1 | 1 | 1 | 1 | | 200 (720k//3.6k) |
| 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 2ch hall amplifier offset resistance / input resistance ( "1" Resistance ÷ "2" Resistance) | 10 (36k//3.6k) |
| | | | | 1 | 0 | 0 | 0 | | 20 (72k//3.6k) |
| | | | | 0 | 1 | 0 | 0 | | 40 (144k//3.6k) |
| | | | | 1 | 1 | 0 | 0 | | 50 (180k//3.6k) |
| | | | | 0 | 0 | 1 | 0 | | 60 (216k//3.6k) |
| | | | | 1 | 0 | 1 | 0 | | 70 (252k//3.6k) |
| | | | | 0 | 1 | 1 | 0 | | 90 (324k//3.6k) |
| | | | | 1 | 1 | 1 | 0 | | 100 (360k//3.6k) |
| | | | | 0 | 0 | 0 | 1 | | 110 (396k//3.6k) |
| | | | | 1 | 0 | 0 | 1 | | 120 (432k//3.6K) |
| | | | | 0 | 1 | 0 | 1 | | 140 (504k//3.6k) |
| | | | | 1 | 1 | 0 | 1 | | 150 (540k//3.6k) |
| | | | | 0 | 0 | 1 | 1 | | 160 (570k//3.6k) |
| | | | | 1 | 0 | 1 | 1 | | 170 (612k//3.6k) |
| | | | | 0 | 1 | 1 | 1 | | 190 (684k//3.6k) |
| | | | | 1 | 1 | 1 | 1 | | 200 (720k//3.6k) |

General-purpose amplifier ON/OFF setting

| Input | | | | | | Setting mode | Set content | Remarks |
|---|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | D0 | D1 | | | |
| 0 | 0 | 1 | 1 | 0 | * | General-purpose | Stand-by | |
| | | | | 1 | * | amplifier 1 | Operate | |
| | | | | * | 0 | General-purpose | Stand-by | |
| | | | | * | 1 | amplifier 2 | Operate | |

PWM circuit accuracy setting

| Input | | | | | | Setting mode | Set content | Remarks |
|---|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | D0 | D1 | | | |
| 1 | 0 | 1 | 1 | 0 | 0 | | 10bit resolution | Initial value |
| | | | | 0 | 1 | PWM accuracy setting | 11bit resolution | |
| | | | | 1 | 0 | | 12bit resolution | |
| | | | | * | * | | - | |

PWM pulse width of moving

1ch (X axis side)

| Input [3:0] | | | | | | | | Setting mode | Moving pulse number |
|---|---|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | D0 | D1 | D2 | D3 | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1ch (X axis) side width of | 0 (Initialization) |
| | | | | 1 | 0 | 0 | 0 | moving | 1 |
| | | | | 0 | 1 | 0 | 0 | | 2 |
| | | | | 1 | 1 | 0 | 0 | | 3 |
| | | | | 0 | 0 | 1 | 0 | | 4 |
| | | | | 1 | 0 | 1 | 0 | | 5 |
| | | | | 0 | 1 | 1 | 0 | | 6 |
| | | | | 1 | 1 | 1 | 0 | | 7 |
| | | | | 0 | 0 | 0 | 1 | | 8 |
| | | | | 1 | 0 | 0 | 1 | | 9 |
| | | | | 0 | 1 | 0 | 1 | | 10 |
| | | | | 1 | 1 | 0 | 1 | | 11 |
| | | | | 0 | 0 | 1 | 1 | | 12 |
| | | | | 1 | 0 | 1 | 1 | | 13 |
| | | | | 0 | 1 | 1 | 1 | | 14 |
| | | | | 1 | 1 | 1 | 1 | | 15 |

Note : 1 pulse = 1CLK

2ch (Y axis side)

| Input [7:4] | | | | | | | | Setting mode | Moving pulse number |
|---|---|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | D4 | D5 | D6 | D7 | | |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 2ch (Y axis) side width of | 0 (Initialization) |
| | | | | 1 | 0 | 0 | 0 | moving | 1 |
| | | | | 0 | 1 | 0 | 0 | | 2 |
| | | | | 1 | 1 | 0 | 0 | | 3 |
| | | | | 0 | 0 | 1 | 0 | | 4 |
| | | | | 1 | 0 | 1 | 0 | | 5 |
| | | | | 0 | 1 | 1 | 0 | | 6 |
| | | | | 1 | 1 | 1 | 0 | | 7 |
| | | | | 0 | 0 | 0 | 1 | | 8 |
| | | | | 1 | 0 | 0 | 1 | | 9 |
| | | | | 0 | 1 | 0 | 1 | | 10 |
| | | | | 1 | 1 | 0 | 1 | | 11 |
| | | | | 0 | 0 | 1 | 1 | | 12 |
| | | | | 1 | 0 | 1 | 1 | | 13 |
| | | | | 0 | 1 | 1 | 1 | | 14 |
| | | | | 1 | 1 | 1 | 1 | | 15 |

Note : 1 pulse = 1CLK

The ON/OFF operation of the hall amplifier and the hall bias is done with the ST pin.

Note : An initial value of A0 to A3 = 1111 is a static test mode. Use it specifying data D0 for one.

TEST mode setting

| Input | | | | | Setting mode | Content | Remarks |
|---|---|---|---|---|---|---|---|
| A0 | A1 | A2 | A3 | D0 | | | |
| 1 | 1 | 1 | 1 | 0 | NC pin _ TEST mode | External CLK | It uses it by the shipment inspection. |
| | | | | 1 | | Internal CLK | Internal CLK operation |

Note : External CLK mode is for the shipment inspection. Use it with internal CLK. Use it after it internal CLK switches because default is external CLK mode.

Hall bias, Offset adjustment circuit configuration
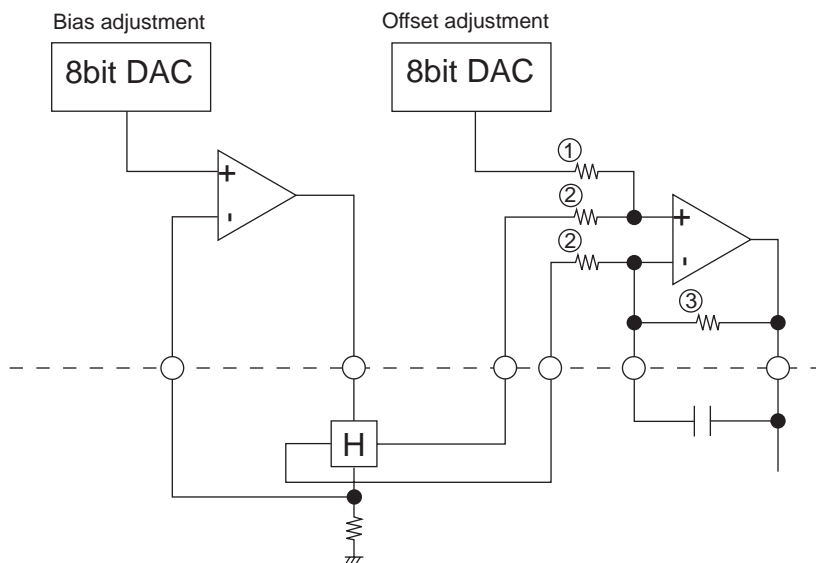


Hall amplifier, Hall bias equivalent circuit

About the gain adjustment

    The resistance ratio of "2" and "3" is adjusted in figure and the gain is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

About the Offset adjustment

    The resistance ratio of "1" and "2" is adjusted in figure and the Offset is set. Refer to the setting to the cereal map. The magnification can be set from ten by 200.

## Note in design

- Stand-by function
  IC becomes a stand-by state at ST = "L", and IC enters the state of operation at ST ="H". Moreover, the register in IC is reset as for ST = "L" at times.

- Hall bias
  The constant current output is built into for the hall element drive. The constant current value is set from detection resistance (RHG) connected from the HBIN pin impression voltage and the HGND pin between GND.

    Constant current value ($I_O$) = HBIN voltage ÷ Detection resistance
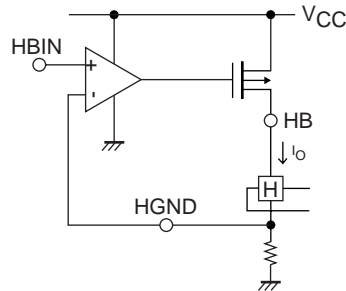


  Constant current value ($I_O$) becomes about 1mA when assuming HBIN pin impressed voltage =1.0V and detection resistance = 1 kΩ from the above-mentioned calculation type. Moreover, the HGND pin must connect with the HB pin, and connect the detection resistance of a large value as much as possible when you do not use the hall bias circuit.

- Operation amplifier
  Impress the bias to the $V_{IN+}$ pin, and compose the buffer by the connection to the VOUT pin in the $V_{IN-}$ pin in the operational amplifier not used.