GaN HEMT Pulsed Power Transistor
3.1 - 3.5 GHz, 30W Peak, 500us Pulse, 10% Duty Cycle

Production V1
23 Aug 11

Features

- GaN depletion mode HEMT microwave transistor
- Common source configuration
- Broadband Class AB operation
- Thermally enhanced Cu/Mo/Cu package
- RoHS Compliant
- +50V Typical Operation
- MTTF of 114 years (Channel Temperature < 200°C)

Application

- Civilian and Military Pulsed Radar

Product Description

The MAGX-003135-030L00 is a gold metalized matched Gallium Nitride (GaN) on Silicon Carbide RF power transistor optimized for civilian and military radar pulsed applications between 3100 - 3500 MHz. Using state of the art wafer fabrication processes, these high performance transistors provide high gain, efficiency, bandwidth, ruggedness over a wide bandwidth for today's demanding application needs. The MAGX-003135-030L00 is constructed using a thermally enhanced Cu/Mo/Cu flanged ceramic package which provides excellent thermal performance. High breakdown voltages allow for reliable and stable operation in extreme mismatched load conditions unparalleled with older semiconductor technologies.

Typical RF Performance

Freq. (MHz)	Pin (W Peak)	Pout (W Peak)	Gain (dB)	Eff (%)
3100	3	40	11.2	59.3
3300	3	40	11.2	57.7
3500	3	34	10.5	51.2

Typical RF performance measured in M/A-COM RF test fixture. Devices tested in common source Class-AB configuration as follows: Vdd=50V, Idq=130mA (pulsed), F=3.1-3.5GHz, Pulse=500us, Duty=10%.

Ordering Information

MAGX-003135-030L00	30W GaN Power Transistor
MAGX-003135-SB1PPR	Evaluation Fixture

• **North America** Tel: 800.366.2266 / Fax: 978.366.2266
• **Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
• **Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298
Visit www.macomtech.com for additional data sheets and product information.

Absolute Maximum Ratings Table (1, 2, 3)

Supply Voltage (Vdd)	+65V
Supply Voltage (Vgg)	-8 to 0V
Supply Current (Id1)	3000 mA
Input Power (Pin)	+30 dBm
Absolute Max. Junction/Channel Temp	200 ºC
MTTF (T_J<200°C)	114 years
Continuous Power Dissipation (Pdiss) at 85 ºC	27 W
Pulsed Power Dissipation (Pavg) at 85 ºC	65 W
Thermal Resistance, (Tchannel = 200 ºC) Pulsed 500uS, 10% Duty cycle	1.8 ºC/W
Operating Temp	-40 to +95C
Storage Temp	-65 to +150C
Mounting Temperature	See solder reflow profile
ESD Min. - Machine Model (MM)	50 V
ESD Min. - Human Body Model (HBM)	>250 V
MSL Level	MSL1

(1) Operation of this device above any one of these parameters may cause permanent damage.

(2) Channel temperature directly affects a device's MTTF. Channel temperature should be kept as low as possible to maximize lifetime.

(3) For saturated performance it recommended that the sum of (3*Vdd + abs(Vgg)) <175

Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
DC CHARACTERISTICS						
Drain-Source Leakage Current	V_{GS} = -8V, V_{DS} = 175V	I_{DS}	-	-	2.5	mA
Gate Threshold Voltage	V_{DS} = 5V, I_D = 6mA	$V_{GS\ (th)}$	-5	-3	-2	V
Forward Transconductance	V_{DS} = 5V, I_D = 1.5mA	G_M	1.0	-	-	S
DYNAMIC CHARACTERISTICS						
Input Capacitance	V_{DS} = 0v, V_{GS} = -8V, F = 1MHz	C_{ISS}	-	13.2	-	pF
Output Capacitance	V_{DS} = 50V, V_{GS} = -8V, F = 1MHz	C_{OSS}	-	5.6	-	pF
Reverse Transfer Capacitance	V_{DS} = 50V, V_{GS} = -8V, F = 1MHz	C_{RSS}	-	0.5	-	pF

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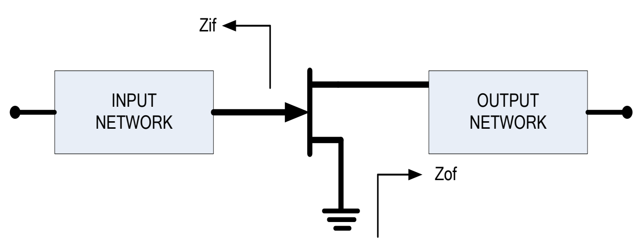
Electrical Specifications: T_C = 25 ± 5°C (Room Ambient)

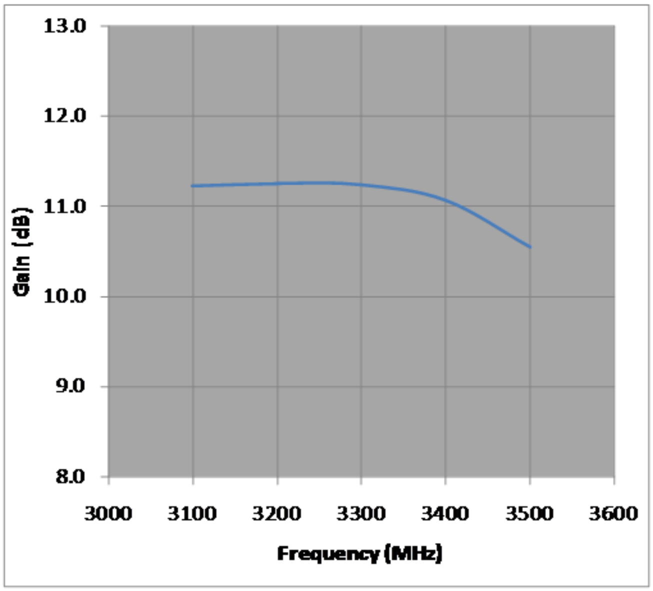
Parameter	Test Conditions	Symbol	Min	Typ	Max	Units
RF FUNCTIONAL TESTS *Vdd=50V, Idq=130mA (pulsed), F=3.1-3.5GHz, Pulse=500us, Duty=10%.*						
Output Power	Pin = 3W Peak	P_{OUT}	30 3	40 4	-	W Peak W Ave
Power Gain	Pout = 30W Peak	G_P	10.0	11.0	-	dB
Drain Efficiency	Pin = 3W Peak	η_D	50	55	-	%
Load Mismatch Stability	Pin = 3W Peak	VSWR-S	5:1	-		-
Load Mismatch Tolerance	Pin = 3W Peak	VSWR-T	10:1	-		-

Test Fixture Impedance

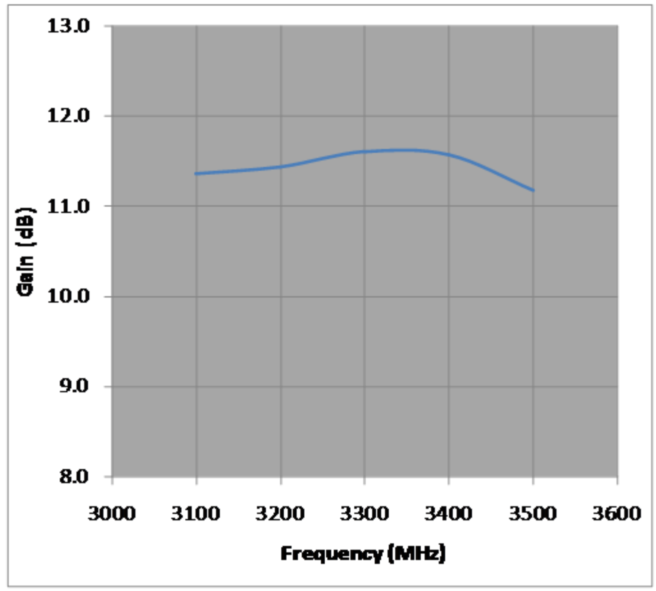
F (MHz)	Z_{IF} (Ω)	Z_{OF} (Ω)
3100	7.6 - j12.5	5.2 - j0.2
3300	7.5 - j11.4	6.0 + j0.2
3500	7.2 - j10.2	6.7 + j0.1



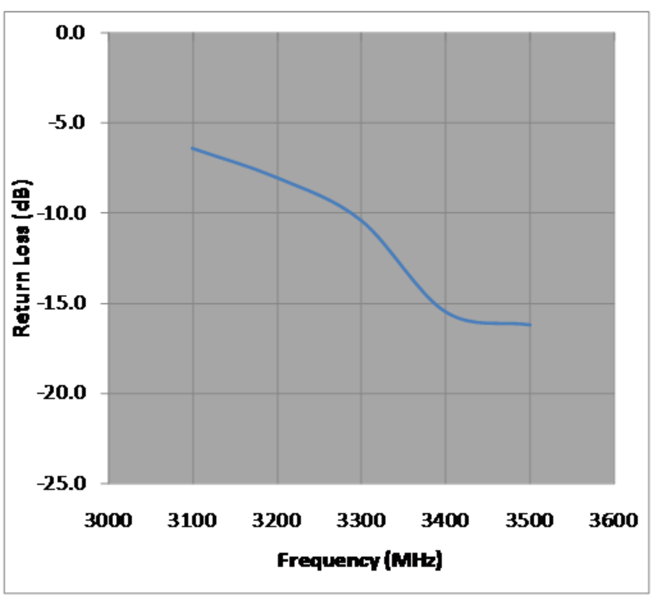
Gain vs. Frequency
50V Drain Bias, Idq=0.13A



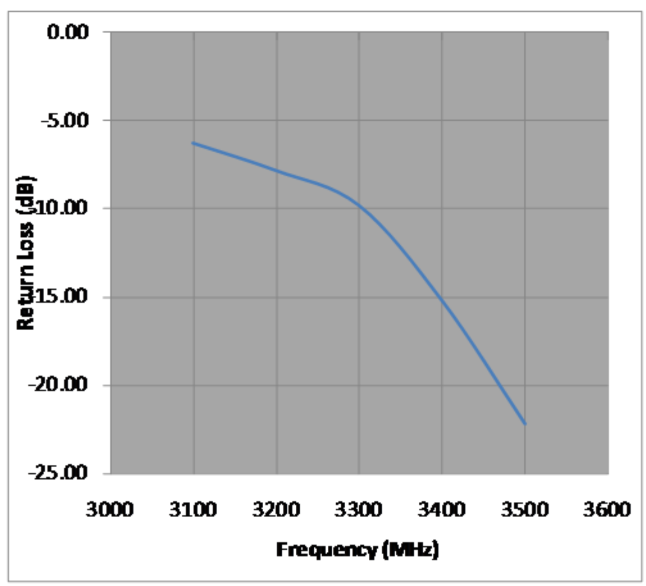
Gain vs. Frequency
65V Drain Bias, Idq=0.13A



Return Loss vs. Frequency
50V Drain Bias, Idq=0.13A



Return Loss vs. Frequency
65V Drain Bias, Idq=0.13A



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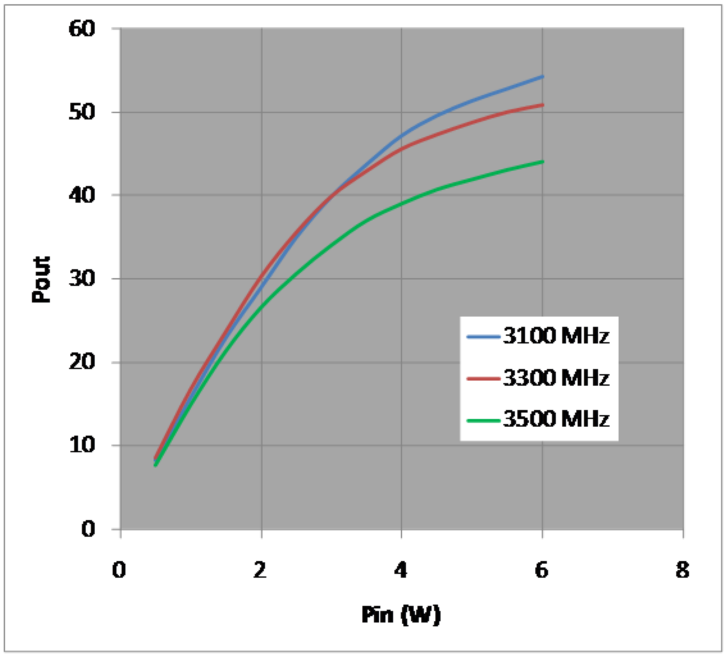
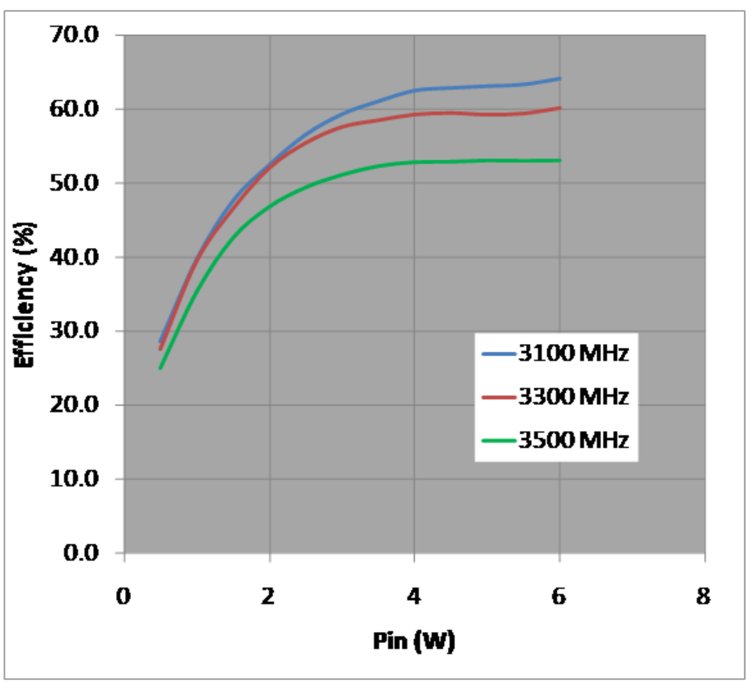
Output Power vs. Input Power
50V Drain Bias, Idq=0.13A



Drain Efficiency vs. Input Power
50V Drain Bias, Idq=0.13A



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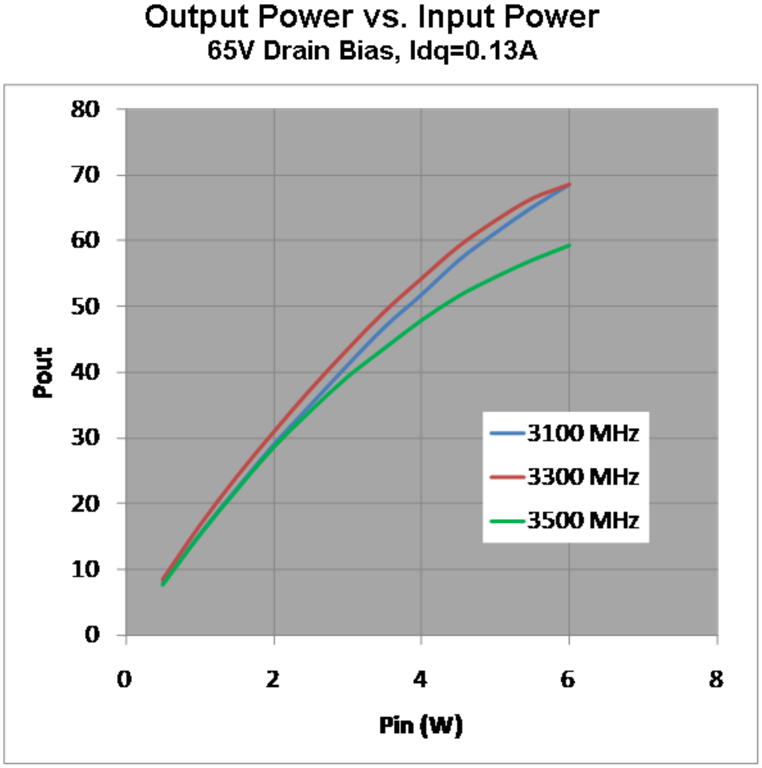
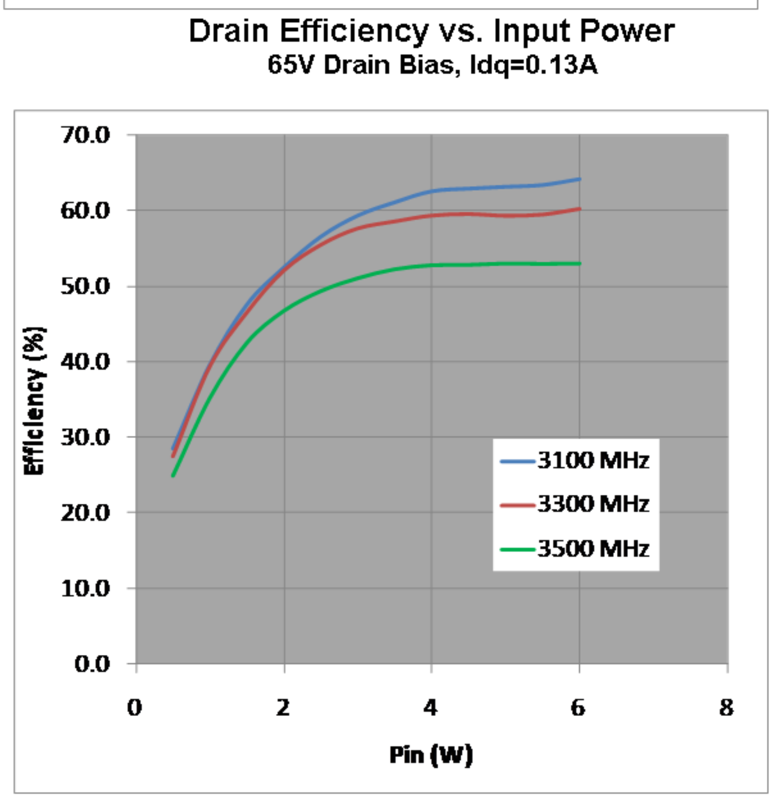

Output Power vs. Input Power
65V Drain Bias, Idq=0.13A
Pout
Pin (W)
0
2
4
6
8
10
20
30
40
50
60
70
80
3100 MHz
3300 MHz
3500 MHz


Drain Efficiency vs. Input Power
65V Drain Bias, Idq=0.13A
Efficiency (%)
Pin (W)
0.0
10.0
20.0
30.0
40.0
50.0
60.0
70.0
0
2
4
6
8
3100 MHz
3300 MHz
3500 MHz

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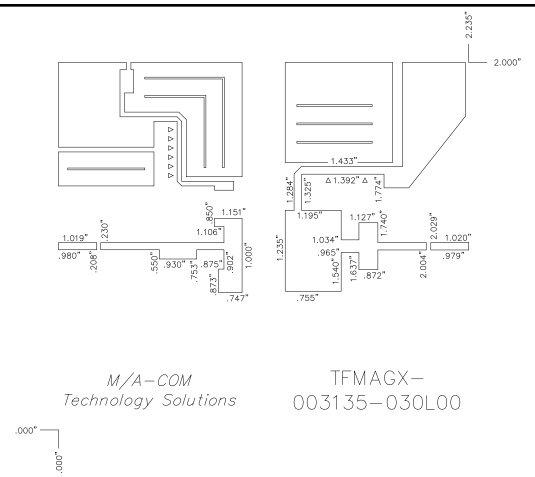
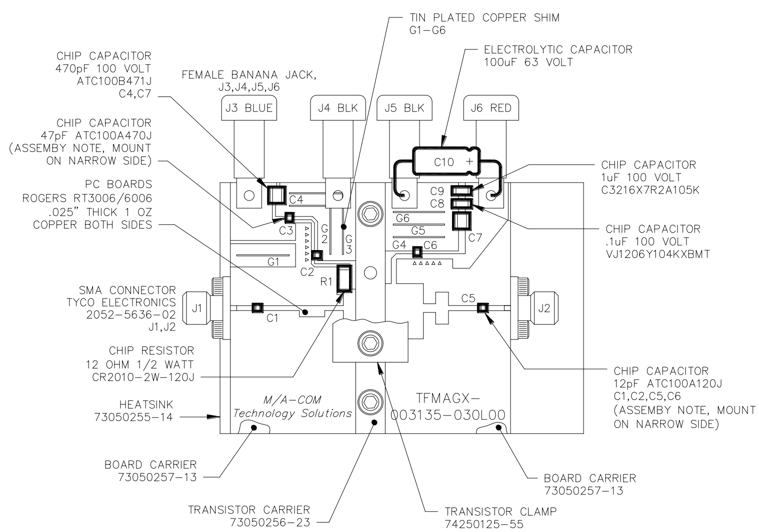
Test



CIRCUIT DIMENSIONS SCALE = 1:1

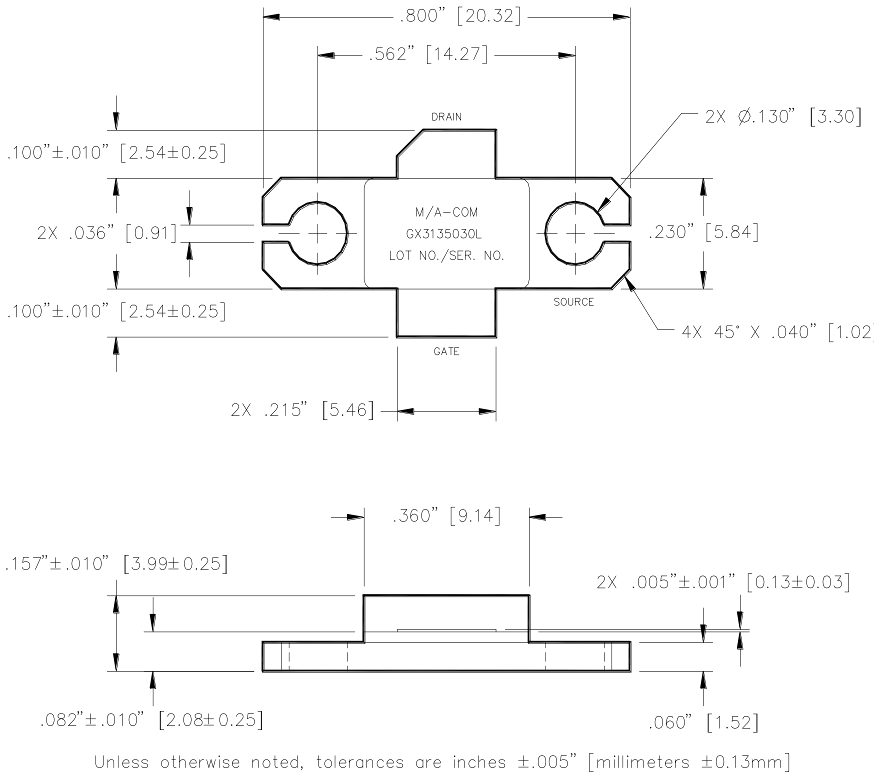
Note: A .dwg circuit drawing is available upon request

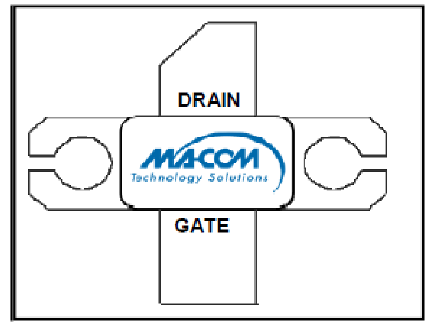
Test Fixture Assembly



ASSEMBLY VIEW

Outline Drawings





CORRECT DEVICE SEQUENCING

TURNING THE DEVICE ON

1. Set V_{GS} to the pinch-off (V_P), typically -5V
2. Turn on V_{DS} to nominal voltage (50V)
3. Increase V_{GS} until the I_{DS} current is reached
4. Apply RF power to desired level

TURNING THE DEVICE OFF

1. Turn the RF power off
2. Decrease V_{GS} down to V_P
3. Decrease V_{DS} down to 0V
4. Turn off V_{GS}

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