EN71NS032A0
Stacked Multi-Chip Product (MCP) Flash Memory and RAM
32 Megabit (2M x 16-bit) CMOS 1.8 Volt-only Burst Simultaneous Operation, Multiplexed Flash Memory and
16 Megabit (1M x 16-bit) Pseudo Static RAM

Distinctive Characteristics

MCP Features

- **Power supply voltage of 1.7V to 1.95V**
- **High performance**
  - 70 ns @ random access
  - 7 ns @ burst access (108MHz)
- **Package**
  - 6.2 x 7.7 x 1.0mm 56 ball BGA
- **Operating Temperature**
  - 25°C to +85°C

General Description

EN71NS032A0 is a product line of stacked Multi-Chip Product (MCP) packages and consists of:

- Burst Simultaneous Operation, Multiplexed NOR Flash Memory.
- Burst Mode, Multiplexed Pseudo SRAM.

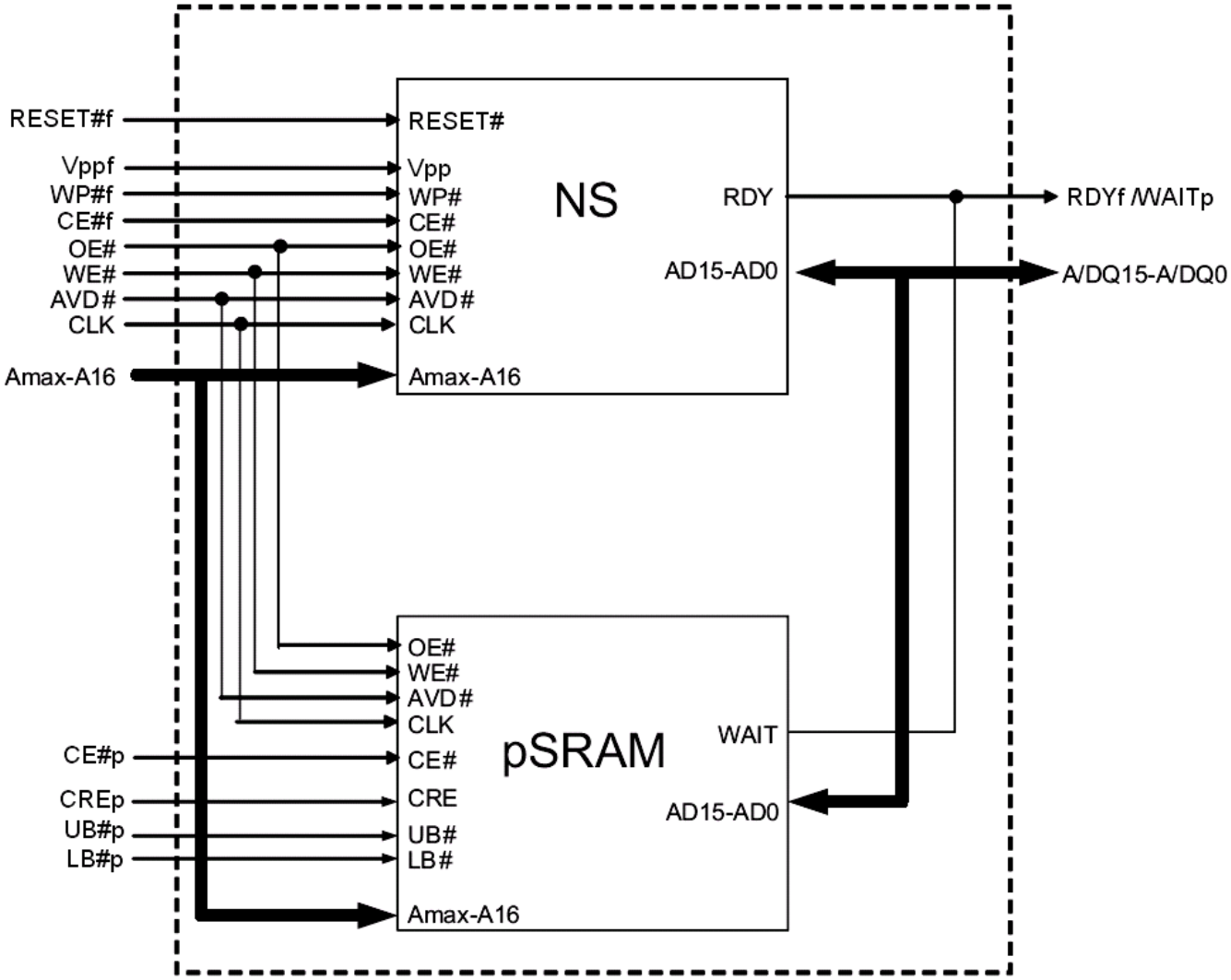
For detailed specifications, Please refer to the individual datasheets listed in the following table.

Device	Document
NOR Flash Memory	EN29NS032
Pseudo SRAM	ENPSS16

Flash Density	32Mb	**pSRAM density**	16Mb
Flash Access time	70ns at Async. Mode 7ns at Burst Read	**pSRAM Access time**	70ns at Async. Mode 7ns at Burst Read
Flash Burst mode max frequency	108MHz	**pSRAM Burst mode max frequency**	108MHz
Package	56-ball BGA		

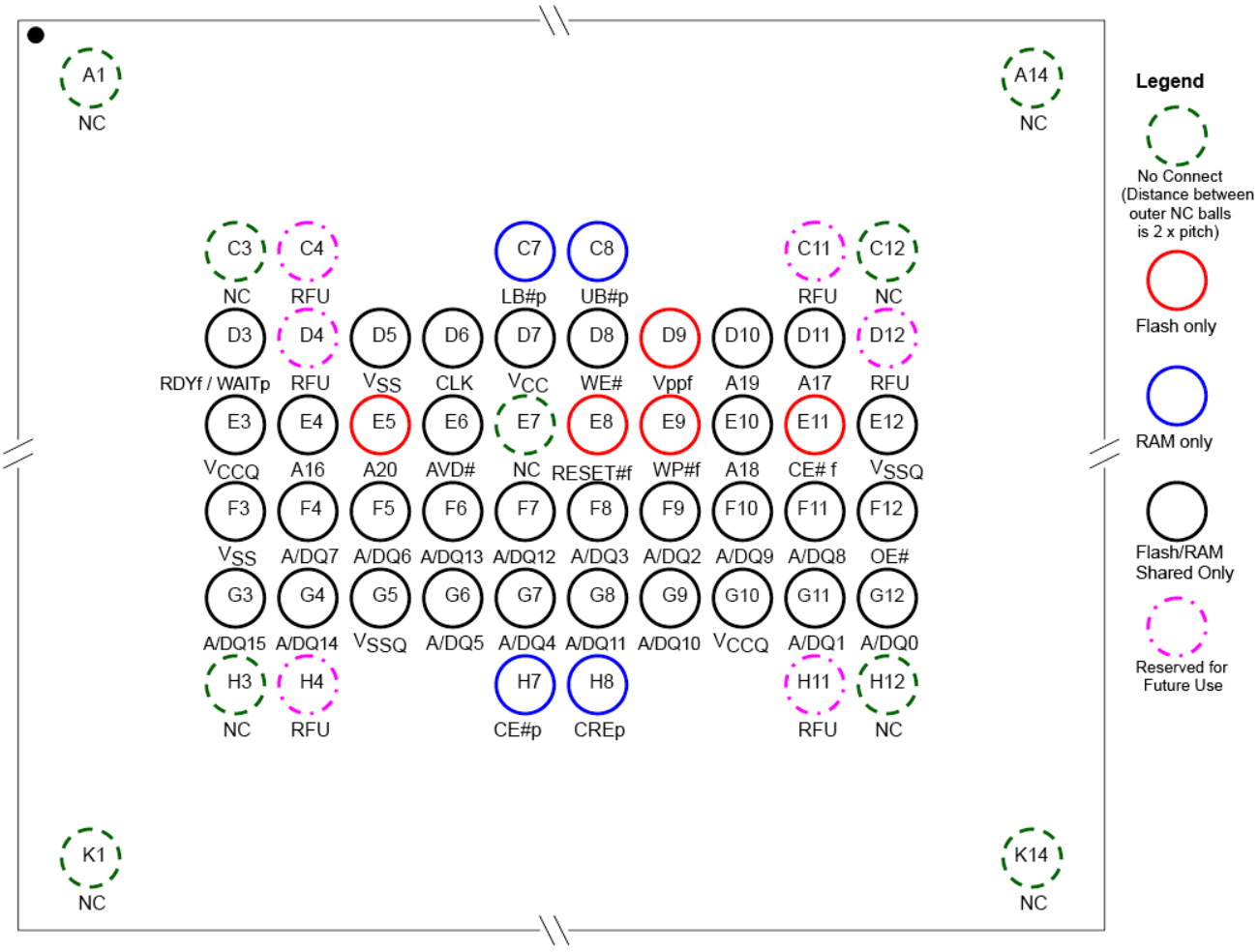
MCP Block Diagram

NOR FLASH + PSRAM DIAGRAM



Note: Amax = A20

Connection Diagram



MCP	Flash-only Addresses	Shared Addresses	Shared ADQ Pins
EN71NS032A0	A20	A19 – A16	ADQ15 – ADQ0

Pin Description

Symbol	Description	Flash	pSRAM
A20–A16	Address Inputs	●	●
ADQ15–ADQ0	Multiplexed Address/Data	●	●
OE#	Output Enable input. Asynchronous relative to CLK for the Burst mode.	●	●
WE#	Write Enable input.	●	●
VSSQ/VSS	Ground	●	●
VCCQ/VCC	Device Power Supply (1.7 V–1.95 V).	●	●
NC	Not Contact; pin not connected internally	●	●
RDYf/WAITp	Ready output; indicates the status of the Burst read. Flash Memory RDY (using default “Active HIGH” configuration) V_{OL} = data invalid, V_{OH} = data valid. Note: The default polarity for the pSRAM WAIT signal is opposite the default polarity of the Flash RDY signal. pSRAM WAIT (using default “Active HIGH” configuration) V_{OL} = data valid, V_{OH} = data invalid. To match polarities, change bit 10 of the pSRAM Bus Configuration Register to 0 (Active LOW WAIT). Alternately, change bit 10 of the Flash Configuration Register to 0 (Active LOW RDY)	●	●
CLK	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{OL} or V_{IH} while in asynchronous mode.	●	●
AVD#	Address Valid input. Indicates to device that the valid address is present on the address inputs. V_{IL} = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched on rising edge of CLK. V_{IH} = device ignores address inputs	●	●
RESET# f	Hardware reset input. V_{IL} = device resets and returns to reading array data	●	
WP#f	Hardware write protect input. V_{IL} = disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	●	
Vppf	Accelerated input. At Vpp , accelerates programming; automatically places device in Accelerated Program mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions. (Applying high voltage on MCP package is prohibited; otherwise, internal RAM may be damaged easily!)	●	
CE# p	Chip Enable Input for pSRAM.		●
CE# f	Chip Enable Input for Flash. Asynchronous relative to CLK for the Burst mode.	●	
CREp	Control register enable (pSRAM).		●
LB#p	Lower byte enable. DQ7~DQ0 (pSRAM)		●
UB#p	Upper byte enable. DQ15~DQ8 (pSRAM)		●
RFU	Reserved for Future Use		

Operating Mode (For Asynchronous mode)

Asynchronous Mode BCR[15]=1	Power	CLK	ADV#	CE#	OE#	WE#	CRE	UB#/ LB#	WAIT2	A/DQ[15:0]	Note
Read	Active	X	⌐¯¬	L	L	H	L	L	Low-z	Data out	4
Write	Active	X	⌐¯¬	L	X	L	L	L	High-z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	X	X	L	X	X	L	X	Low-z	X	4, 6
Configuration register write	Active	X	⌐¯¬	L	H	L	H	X	Low-z	High-z	
Configuration register read	Active	X	⌐¯¬	L	L	H	H	L	Low-z	Config. Reg.out	
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7

Operating Mode (For Synchronous Burst mode)

Burst Mode BCR[15]=0	Power	CLK	ADV#	CE#	OE#	WE#	CRE	UB#/ LB#	WAIT	A/DQ[15:0]	Note
Async read	Active	H or L	⌐¯¬	L	L	H	L	L	Low-z	Data out	4, 8
Async write	Active	H or L	⌐¯¬	L	X	L	L	L	High-z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-z	High-z	5, 6
No operation	Idle	H or L	X	L	X	X	L	X	Low-z	X	4, 6
Initial burst read	Active	⌐¯¬	L	L	X	H	L	L	Low-z	Address	4, 9
Initial burst write	Active	⌐¯¬	L	L	H	L	L	X	Low-z	Address	4, 9
Burst continue	Active	⌐¯¬	H	L	X	X	X	L	Low-z	Data out or Data in	4, 9
Configuration register write	Active	⌐¯¬	L	L	H	L	H	X	Low-z	High-z	9. 10
Configuration register read	Active	⌐¯¬	L	L	L	H	H	L	Low-z	Config. Reg.out	9, 10
DPD	Deep Power-down	L	X	H	X	X	X	X	High-z	High-z	7

Note:

1. With burst mode enabled, CLK must be static(HIGH or LOW) during asynchronous READs and asynchronous WRITEs and to achieve standby power during standby mode.
2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are enabled. When only LB# is in select mode, DQ[7:0] are enabled. When only UB# is in the select mode, DQ[15:8] are enabled.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device pins must be static (unswitched) in order to achieve standby current.
7. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.
8. When the BCR is configured for sync mode, sync READ and WRITE, and async READ and WRITE are supported by ENPSS16
9. Burst mode operation is initialized through the bus configuration register (BCR[15]).
10. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).
11. X=don't care. H=logic high. L=logic low.

Purpose

Eon Silicon Solution Inc. (hereinafter called “Eon”) is going to provide its products’ top marking on ICs with < cFeon > from January 1st, 2009, and without any change of the part number and the compositions of the ICs. Eon is still keeping the promise of quality for all the products with the same as that of Eon delivered before. Please be advised with the change and appreciate your kindly cooperation and fully support Eon’s product family.

Eon products’ Top Marking

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cFeon Top Marking Example:

cFeon

Part Number: XXXX-XXX
Lot Number: XXXXX
Date Code: XXXXX

For More Information

Please contact your local sales office for additional information about Eon memory solutions.

ORDERING INFORMATION

EN71NS 032 A0 - 7 DC W P

PACKAGING CONTENT
P = RoHS compliant

TEMPERATURE RANGE
W = Wireless (-25°C to +85°C)

PACKAGE
DC = 56-Ball BGA
0.50mm pitch, 6.2mm x 7.7mm package

BURST READ ACCESS TIME
7 = 108 MHz
9 = 83 MHz

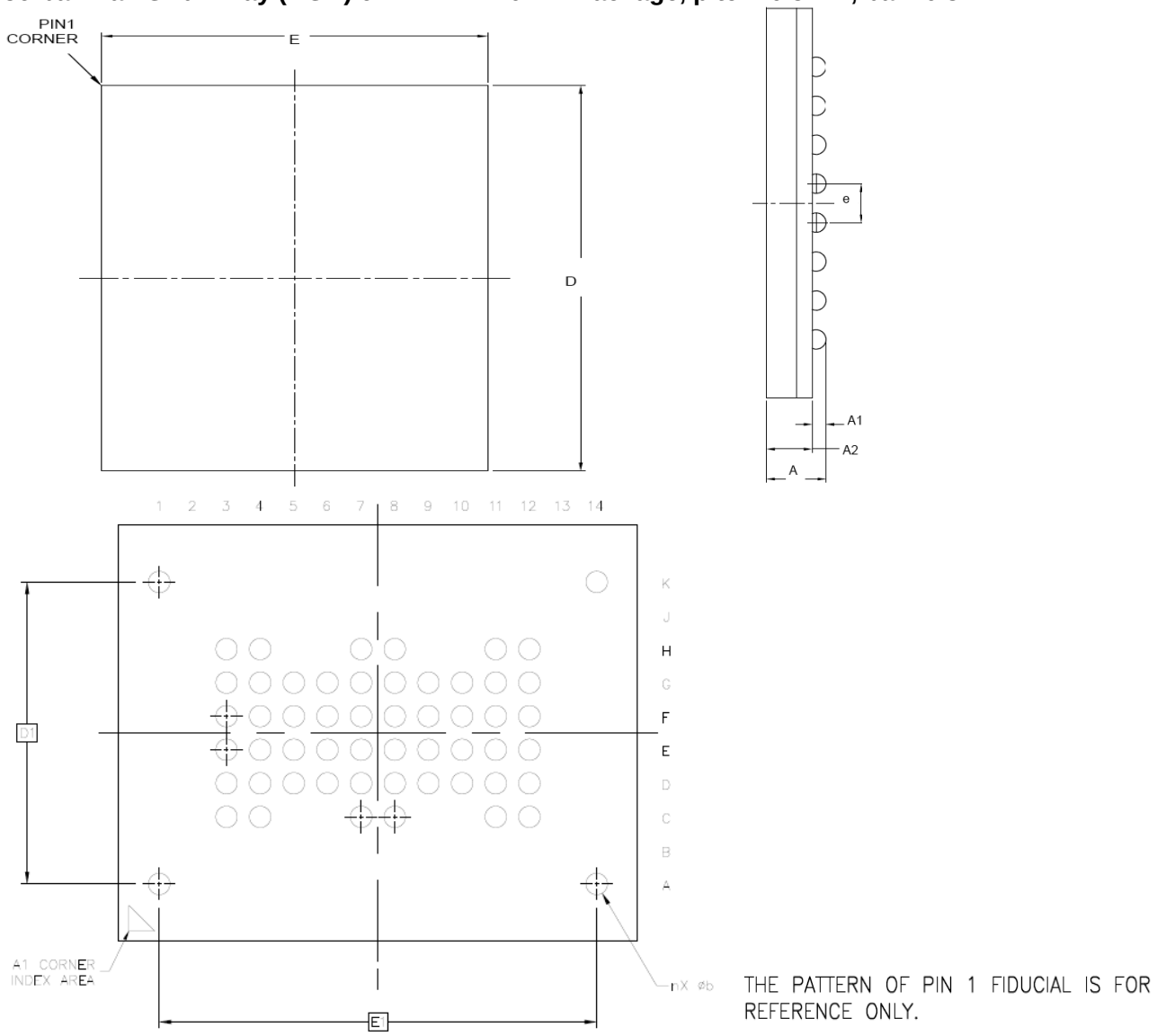
Pseudo SRAM density
A0 = 16Mb

DENSITY
032 = 32Megabit (2M x 16 Bit)

BASE PART NUMBER
EN = Eon Silicon Solution Inc.
71NS = Multi-chip Product (MCP)
1.8V Simultaneous Read/Write,
Burst-mode Multiplexed Flash and RAM

PACKAGE MECHANICAL

56-ball Ball Grid Array (BGA) 6.2 x 7.7 x 1.0mm Package, pitch: 0.5mm, ball: 0.3mm



SYMBOL	DIMENSION IN MM		
	MIN.	NOR	MAX
A	- - -	- - -	1.00
A1	0.16	- - -	0.26
A2		0.676	
D	6.10	6.20	6.30
E	7.60	7.70	7.80
D1		4.5 BSC	
E1		6.5 BSC	
e		0.5 BSC	
b	0.27	- - -	0.37

Note : 1. Coplanarity: 0.1 mm

Revisions List

Revision No	Description	Date
A	Initial Release	2010/10/13
B	Add BURST READ ACCESS TIME option of 9 = 83 MHz.	2011/07/05