

## Memory FRAM

# 128 K (16 K × 8) Bit I<sup>2</sup>C

## MB85RC128

### ■ DESCRIPTION

The MB85RC128 is a FRAM (Ferroelectric Random Access Memory) Stand-Alone chip in a configuration of 16,384 words × 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells.

The MB85RC128 adopts the two-wire serial interface.

Unlike SRAM, the MB85RC128 is able to retain data without using a data backup battery.

The read/write endurance of the nonvolatile memory cells used for the MB85RC128 has improved to be at least 10<sup>10</sup> cycles, significantly out performing Flash memory and E<sup>2</sup>PROM in the number.

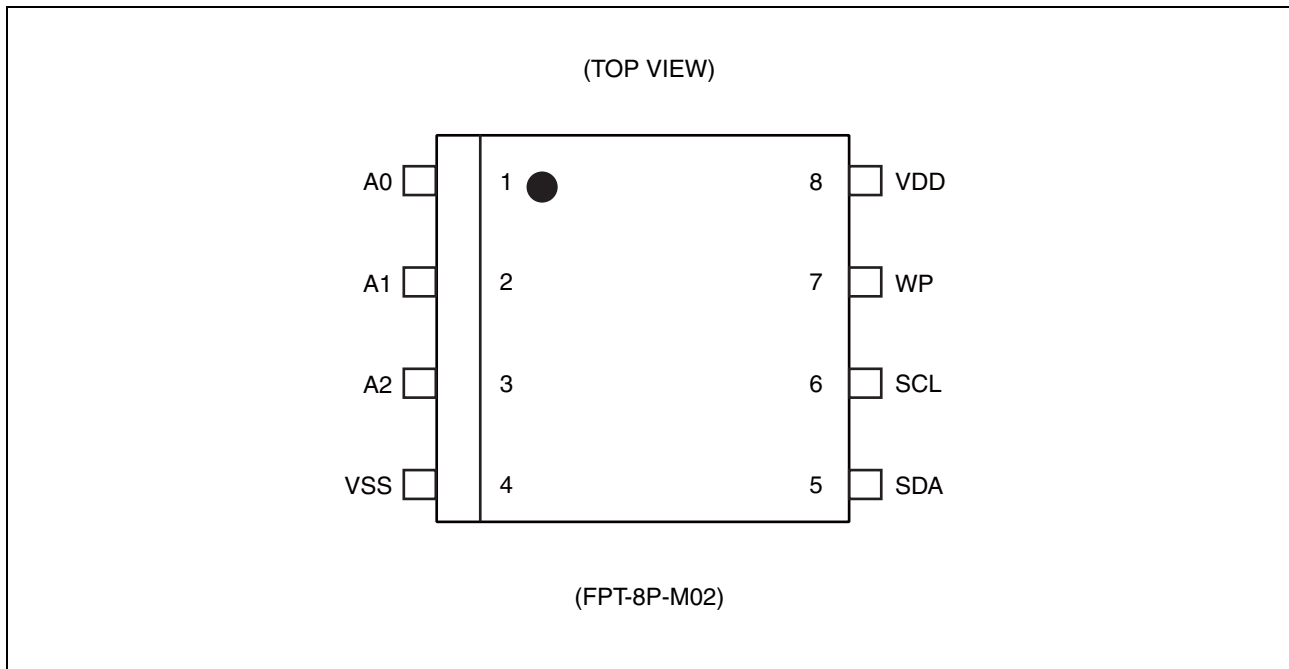
The MB85RC128 does not need a polling sequence after writing to the memory such as the case of Flash memory nor E<sup>2</sup>PROM.

### ■ FEATURES

- Bit configuration : 16,384 words × 8 bits
- Operating power supply voltage : 2.7 V to 3.6 V
- Operating frequency : 400 kHz (Max)
- Two-wire serial interface : I<sup>2</sup>C-bus specification ver. 2.1 compliant, supports Standard-mode/  
Fast-mode.  
Fully controllable by two ports: serial clock (SCL) and serial data (SDA).
- Operating temperature range : - 40 °C to +85 °C
- Data retention : 10 years ( + 75 °C)
- Read/write endurance : 10<sup>10</sup> times
- Package : Plastic / SOP, 8-pin (FPT-8P-M02)
- Low power consumption : Operating current 0.15 mA (Max: @400 kHz), Standby current 5 μA (Typ)

# MB85RC128

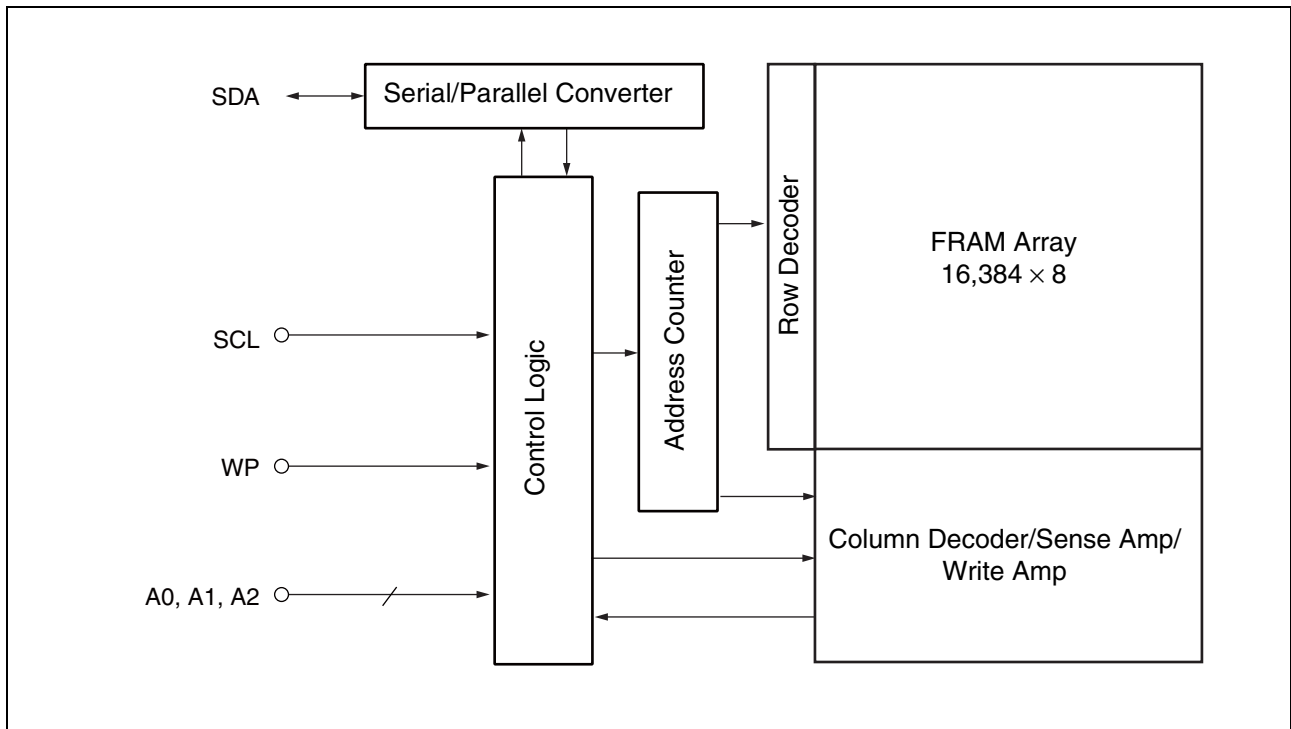
## ■ PIN ASSIGNMENT



## ■ PIN FUNCTIONAL DESCRIPTIONS

Pin Number	Pin Name	Functional Description
1 to 3	A0 to A2	Device Address pins The MB85RC128 can be connected to the same data bus up to 8 devices. Device addresses are used in order to identify each of the devices. Connect these pins to VDD pin or VSS pin externally. Only if the combination of VDD and VSS pins matches a device, an address and a code inputted from the SDA pin, the device operates. In the open pin state, A0, A1, and A2 pins are pulled-down and recognized as "L".
4	VSS	Ground pin
5	SDA	Serial Data I/O pin This is an I/O pin of serial data for performing bidirectional communication of address and writing or reading data of FRAM memory cell array. It is an open drain output that may be wired OR with other open drain or open collector signals on the bus, so a pull-up resistance is required to be connected to the external circuit.
6	SCL	Serial Clock pin This is a clock input pin for input/output serial data. Data is sampled on the rising edge of the clock and output on the falling edge.
7	WP	Write Protect pin When Write Protect pin is "H", writing operation is disabled. When Write Protect pin is "L", the entire memory region can be overwritten. Reading operation is always enabled regardless of the Write Protect pin input level. The Write Protect pin is pulled down internally to VSS pin, therefore if the Write Protect pin is open, the pin status is detected as "L" (write enabled).
8	VDD	Supply Voltage pin

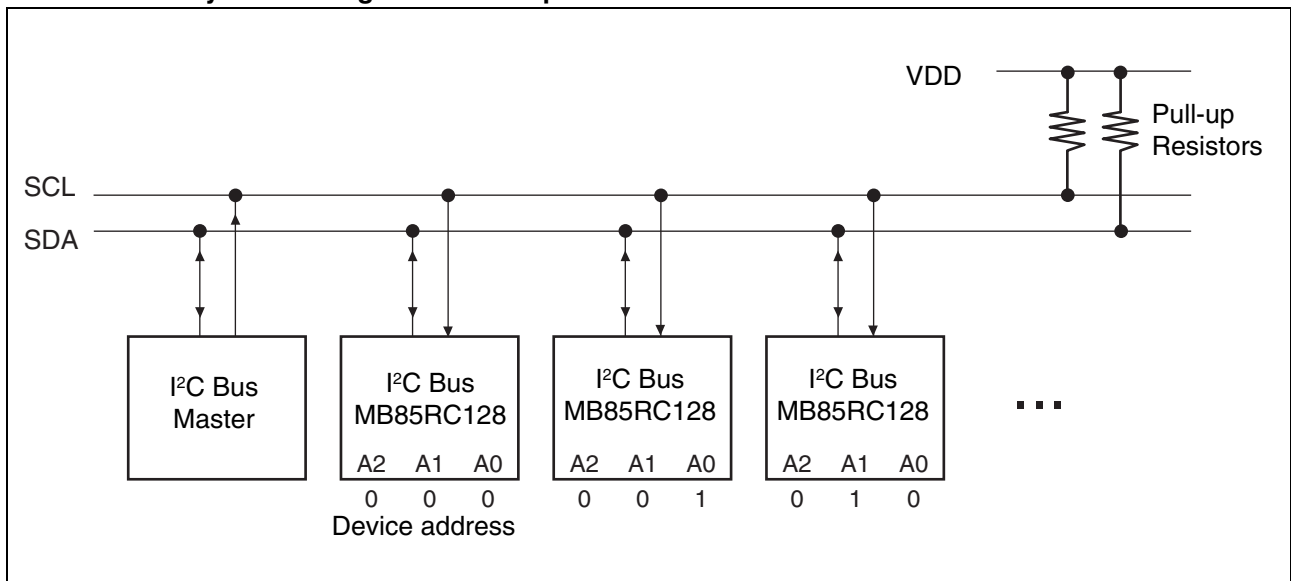
## ■ BLOCK DIAGRAM



## ■ I<sup>2</sup>C (Inter-Integrated Circuit)

The MB85RC128 has a two-wire serial interface, supports the I<sup>2</sup>C bus, and operates as a slave device. The I<sup>2</sup>C bus defines communication roles of “master” and “slave” devices, with the master side holding the authority to initiate control. Furthermore, a I<sup>2</sup>C bus connection is possible where a single master device is connected to multiple slave devices. In this case, it is necessary to assign a unique device address to the slave device, the master side starts communication after specifying the slave to communicate by addresses.

### ● I<sup>2</sup>C Interface System Configuration Example



## ■ I<sup>2</sup>C COMMUNICATION PROTOCOL

The I<sup>2</sup>C bus is a two wire serial interface that uses a bidirectional data bus (SDA) and serial clock (SCL). A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The SDA signal should change while SCL is Low. However, as an exception, when starting and stopping communication sequence, SDA is allowed to change while SCL is High.

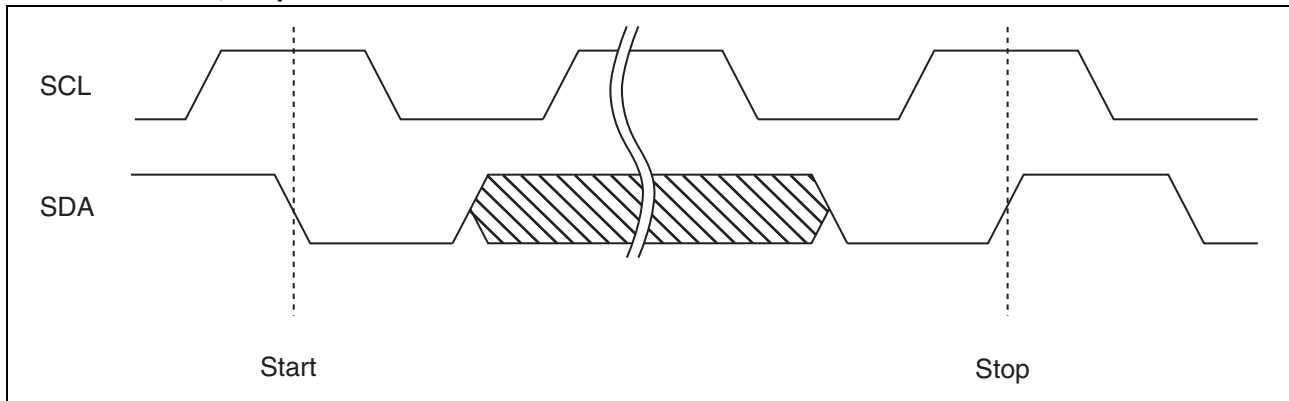
- Start Condition

To start read or write operations by the I<sup>2</sup>C bus, change the SDA input from High to Low while the SCL input is in the high state.

- Stop Condition

To stop the I<sup>2</sup>C bus communication, change the SDA input from Low to High while the SCL input is in the high state. In the reading operation, inputting the stop condition finishes reading and enters the standby state. In the writing operation, inputting the stop condition finishes inputting the rewrite data.

- Start Condition, Stop Condition



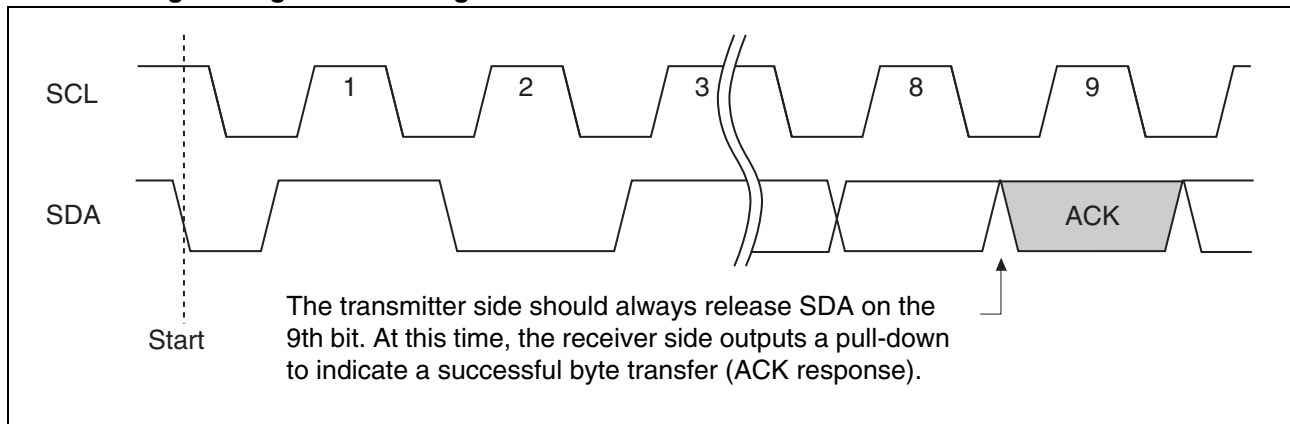
Note : The FRAM device does not need the programming wait time ( $t_{wc}$ ) after issuing the Stop Condition during the write operation.

## ■ ACKNOWLEDGE (ACK)

In the I<sup>2</sup>C bus, serial data including address or memory information is sent in units of 8 bits. The acknowledge signal indicates that every each 8 bits of the data is successfully sent and received. The information receiver side usually outputs “L” every time on the 9th SCL clock after each 8 bits are successfully transmitted. On the transmitter side, the bus is temporarily released to Hi-Z every time on this 9th clock to allow the acknowledge signal to be received and checked. During this Hi-Z-released period, the receiver side pulls the SDA line down to indicate “L” that the previous 8bits communication is successfully received.

If the information receiver side detects Stop condition before driving the acknowledge “L”, the read operation ends and the I<sup>2</sup>C bus enters the standby state. If Stop condition is not sent, nor does the transmitter detect the acknowledge “L”, the bus remains in the released state “H” without doing anything.

### • Acknowledge timing overview diagram



## ■ DEVICE ADDRESS WORD (Slave address)

Following the start condition, the bus master sends the 8bits device address word (Slave address) to start I<sup>2</sup>C communication. The device address word (8bits) consists of a device Type code (4bits), device address code (3bits), and a read/write code (1bit).

- Device Type Code (4bits)

The upper 4 bits of the device address word are a device type code that identifies the device type, and are fixed at “1010” for the MB85RC128.

- Device Address Code (3bits)

Following the device type code, the 3 bits of the device address code are input in order of A2, A1, and A0 pins. Each MB85RC128 is given a unique 3bits code on the device address pin (external hardware pin A2, A1, and A0). When the device address code is received by the slave device, the slave only responds if the hardware device address of which is equal to its unique 3bits code.

- Read/Write Code (1bit)

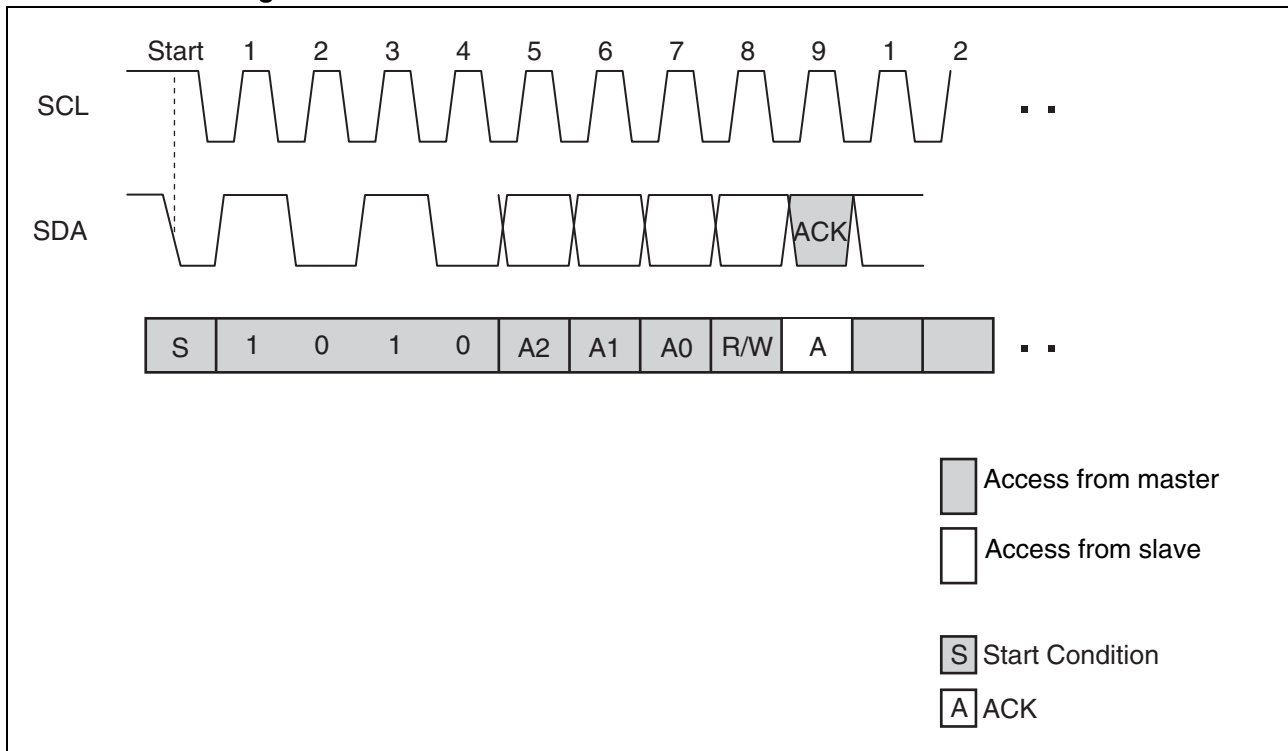
The 8th bit of the device address word is the R/W (read/write) code. When the R/W code is “L”, a write operation is enabled, and the R/W code is “H”, a read operation is enabled for the MB85RC128.

## ■ DATA STRUCTURE

In the I<sup>2</sup>C bus, the acknowledge “L” is output on the 9th bit after the 8 bits of the device and address word following the start condition. After confirming the acknowledge response at the slave, the I<sup>2</sup>C master outputs 8bits × 2 memory address to the I<sup>2</sup>C slave. When the memory address input ends, the slave again outputs the acknowledge “L”. After this operation, the I/O data follows in units of 8 bits, with the acknowledge “L” output after every 8bits.

It is determined by the R/W code whether the data line is driven by the master or the slave. For a write operation the slave will accept 8bits from the master then send an acknowledge. If the master detects the acknowledge, the master will transfer the next 8bits. For a read operation the slave will place 8bits on the I<sup>2</sup>C bus, then wait for an acknowledge from the master.

### • Data Structure Diagram



## ■ FRAM ACKNOWLEDGE -- POLLING NOT REQUIRED

The MB85RC128 performs write operations at the same speed as read operations, so any waiting time for an ACK polling\* does not occur. The write cycle takes no additional time.

\*: As to E<sup>2</sup>PROM, the Acknowledge Polling is performed as a progress check in the write programming step. It places NAK condition on the bus as of “not acknowledged” during the writing programming period. The busy status for the write programming is given from 9th ACK bit. That “done” condition is placed onto I<sup>2</sup>C bus by E<sup>2</sup>PROM I<sup>2</sup>C device and your program had to poll the bus in order to sense that condition.

## ■ WRITE PROTECT (WP)

The entire memory array can be write protected using the Write Protect pin. When the Write Protect is set to “H”, the entire memory map will be write protected. When the write protect pin is “L”, all addresses may be overwritten.

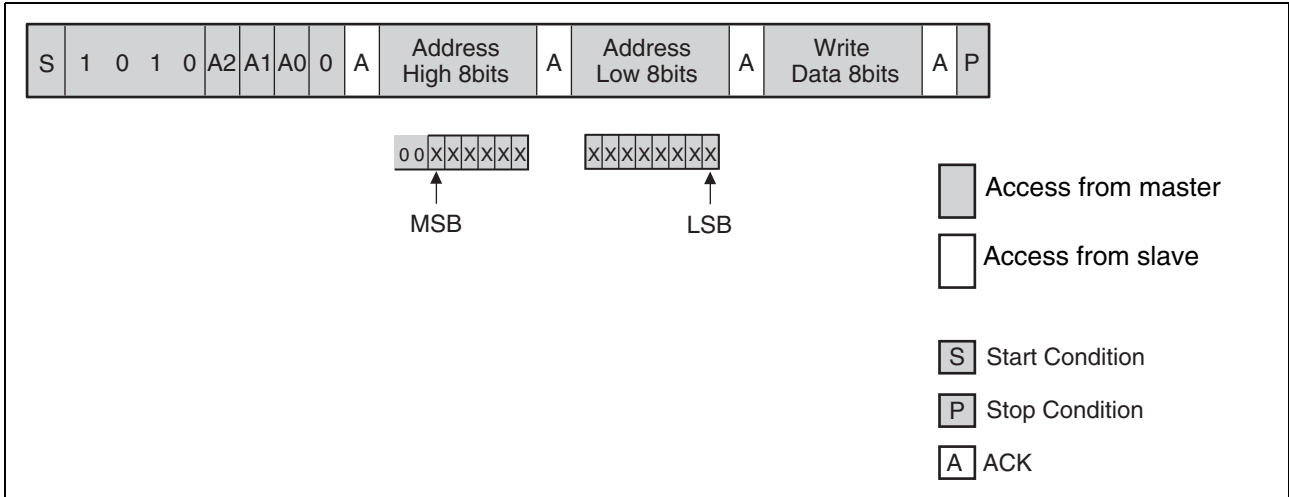
Note : The Write Protect pin is pulled down internally to VSS pin, therefore if the Write Protect pin is open, the pin status is detected as Low (write enabled).

# MB85RC128

## ■ COMMAND

### • Byte Write

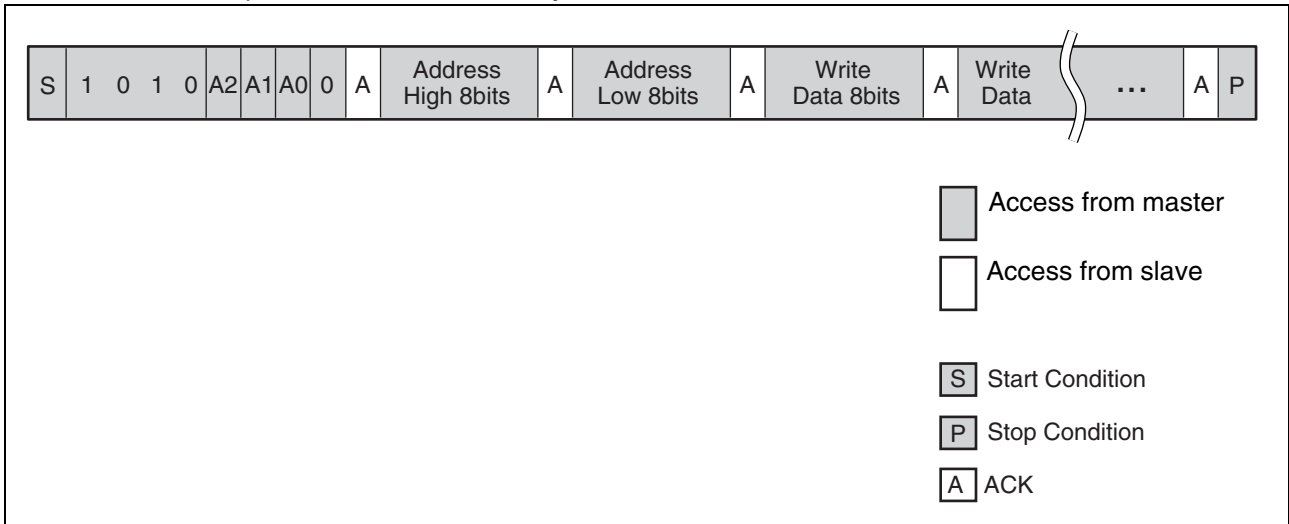
If the 8th bit of the device address word (R/W = 0) is sent following the start condition, the slave responds with an ACK. After this ACK, write addresses and data are sent in the same way, and the write ends by master, generating a stop condition at the end.



Note : In the MB85RC128, input "00" as the upper 2 bits of the MSB.

### • Page Write

If additional 8bits are sent after the same command as Byte Write, a page write is performed. If more bytes are sent than will fit up to the end of the address, the address rolls over to 0000h. Therefore, if more than 8KBytes are sent, the data is overwritten in order starting from the start of the FRAM memory address that was written first. Because FRAM performs write operations at bus speed, the data will be written to FRAM after the ACK response finishes immediately.

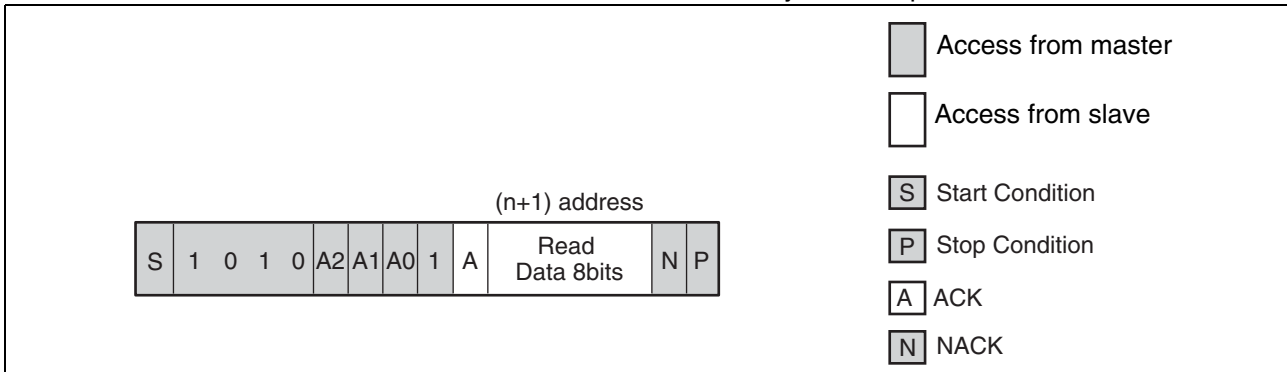


Note : It is not necessary to take a period for internal write programming cycles from the buffer to the memory after the stop condition is generated.



- Current Address Read

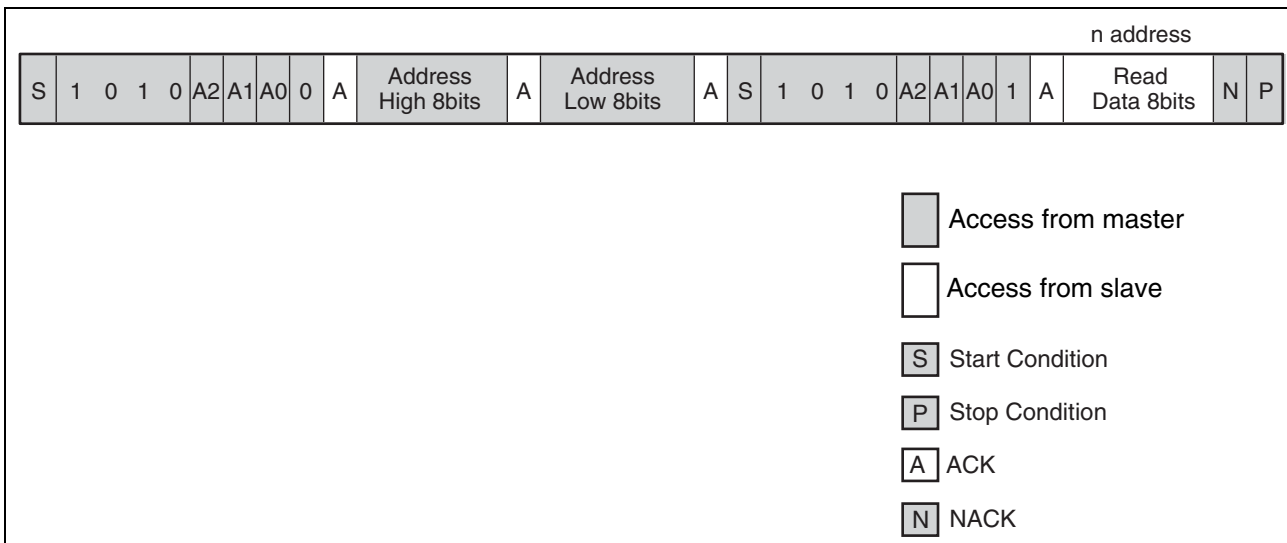
When the previous write or read operation finishes successfully up to the stop command and if the last accessed address is taken to be “n”, then the address at “n+1” is read by sending the following command unless turning the power off. If the end of the address range is reached internally, the address counter will roll over to 0000<sub>H</sub>. The current address is undefined immediately after the power is turned on.



- Random Read

The one byte of data at the address as saved in the buffer can be read out synchronously to SCL by specifying the address in the same way as for a write, and then issuing another start condition and sending the Control Byte (R/W = 1).

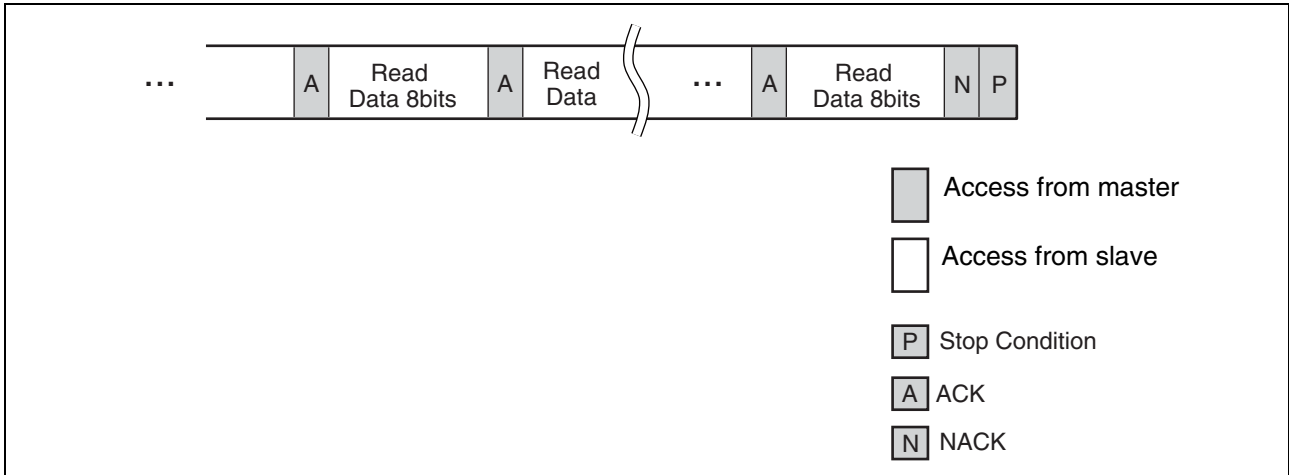
The final NACK is issued by the receiver that receives the data. In this case, this bit is issued by the master side.



# MB85RC128

- Sequential Read

Data can be received continuously following the control byte after specifying the address the same as for Random Read. If the read exceeds the end of address for the MB85RC128, the internal read address automatically rolls over to 0000<sub>H</sub>.



## ■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage*	$V_{CC}$	- 0.5	+4.0	V
Input pin voltage*	$V_{IN}$	- 0.5	$V_{CC} + 0.5 (\leq 4.0)$	V
Output pin voltage*	$V_{OUT}$	- 0.5	$V_{CC} + 0.5 (\leq 4.0)$	V
Ambient temperature	$T_A$	- 40	+ 85	°C
Storage temperature	$T_{stg}$	- 40	+ 125	°C

\* : These parameters are based on the condition that VSS is 0 V.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power supply voltage*	$V_{CC}$	2.7	3.3	3.6	V
“H” level input voltage*	$V_{IH}$	$V_{CC} \times 0.8$	—	$V_{CC} + 0.5 (\leq 4.0)$	V
“L” level input voltage*	$V_{IL}$	- 0.5	—	+ 0.6	V
Ambient temperature	$T_A$	- 40	—	+ 85	°C

\* : These parameters are based on the condition that VSS is 0 V.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

# MB85RC128

## ■ ELECTRICAL CHARACTERISTICS

### 1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input leakage current	$ I_{Li} $	SCL, SDA = 0 V to $V_{CC}$ A0, A1, A2, WP = 0 V or $V_{CC}$	—	—	1	$\mu A$
Output leakage current	$ I_{Lo} $	$V_{OUT} = 0 V$ to $V_{DD}$	—	—	1	$\mu A$
Operating power supply current	$I_{CC}$	SCL = 400 kHz	—	100	150	$\mu A$
Standby current	$I_{SB}$	SCL, SDA = $V_{CC}$ A0, A1, A2, WP = 0 V or $V_{CC}$	—	5	20	$\mu A$
“L” level output voltage	$V_{OL}$	$I_{OL} = 2 mA$	—	—	0.4	V

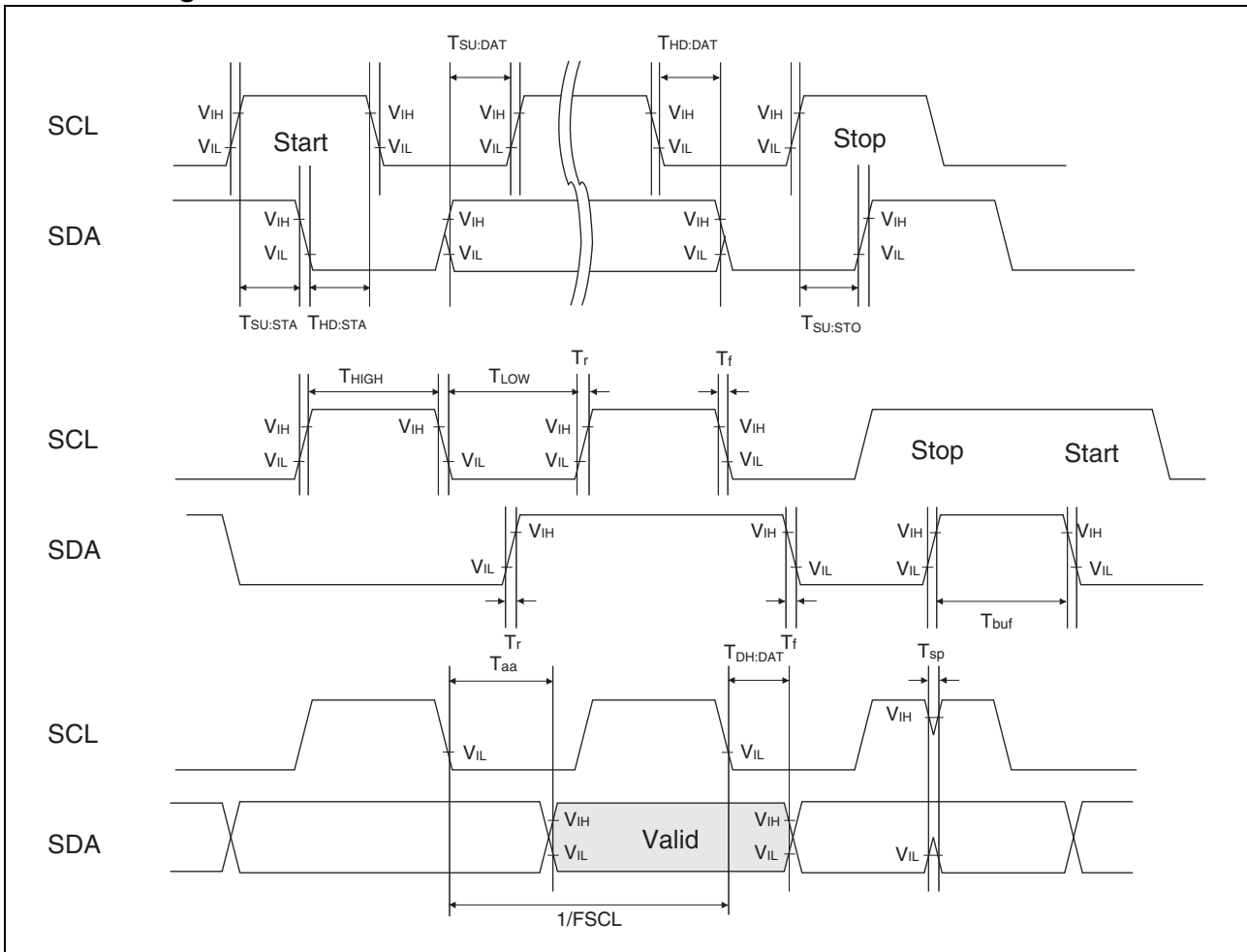
### 2. AC Characteristics

Parameter	Symbol	Value		Unit
		Min	Max	
SCL clock frequency	F <sub>SCL</sub>	0	400	kHz
Clock high time	$T_{HIGH}$	600	—	ns
Clock low time	$T_{LOW}$	1300	—	ns
SCL/SDA rise time	$T_r$	—	300	ns
SCL/SDA fall time	$T_f$	—	300	ns
Start condition hold	$T_{HD:STA}$	600	—	ns
Start condition setup	$T_{SU:STA}$	600	—	ns
SDA input hold	$T_{HD:DAT}$	0	—	ns
SDA input setup	$T_{SU:DAT}$	100	—	ns
SDA output hold	$T_{DH:DAT}$	0	—	ns
Stop condition setup	$T_{SU:STO}$	600	—	ns
SDA output access after SCL fall	$T_{AA}$	—	900	ns
Pre-charge time	$T_{BUF}$	1300	—	ns
Pulse width ignored (Input Filter on SCL and SDA)	$T_{SP}$	—	50	ns

AC characteristics were measured under the following measurement conditions.

- Power supply voltage : 2.7 V to 3.6 V
- Operating temperature : - 40 °C to + 85 °C
- Input voltage magnitude : 0.3 V to 2.7 V
- Input rise time : 5 ns
- Input fall time : 5 ns
- Input judge level :  $V_{CC}/2$
- Output judge level :  $V_{CC}/2$

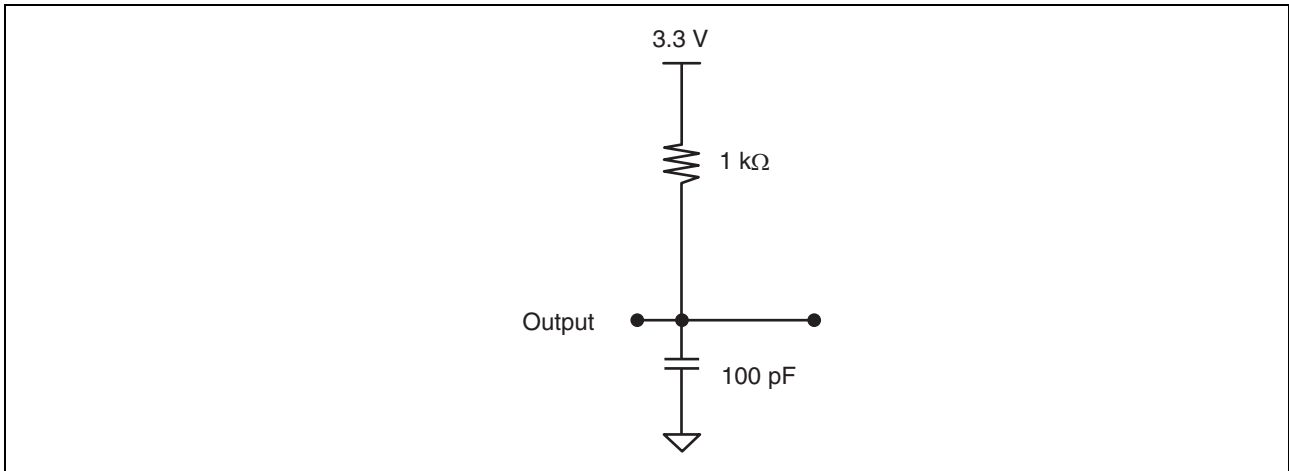
## 3. AC Timing Definitions



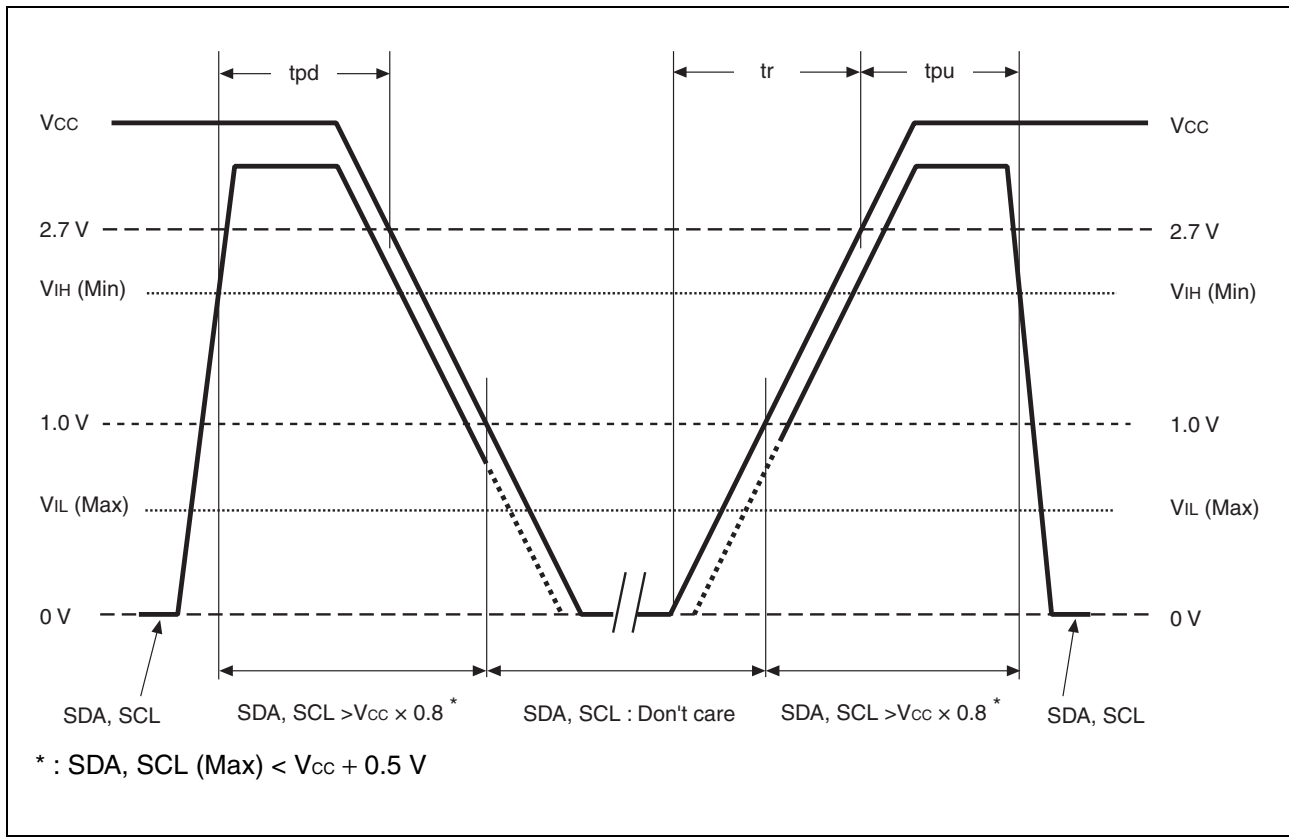
## 4. Pin capacitance

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
I/O capacitance	$C_{I/O}$	$V_{IN} = V_{OUT} = 0\text{ V}$ , $f = 1\text{ MHz}$ , $T_A = +25\text{ }^\circ\text{C}$	—	—	15	pF
Input capacitance	$C_{IN}$		—	—	15	pF

## 5. AC Test Load Circuit



## POWER ON SEQUENCE



Parameter	Symbol	Value		Unit
		Min	Max	
SDA, SCL level hold time during power down	tpd	85	—	ns
SDA, SCL level hold time during power up	tpu	85	—	ns
Power supply rise time	tr	10	—	$\mu s$

## NOTES ON USE

- Data written before performing IR reflow is not guaranteed.
- VDD pin is required to be rising from 0 V because turning the power on from an intermediate level may cause malfunctions, when the power is turned on.

During the access period from the start condition to the stop condition, keep the level of WP, A0, A1, and A2 pins to "H" or "L".

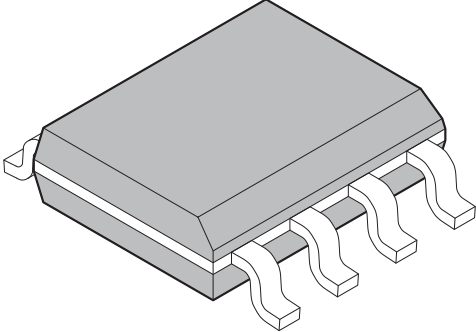
# MB85RC128

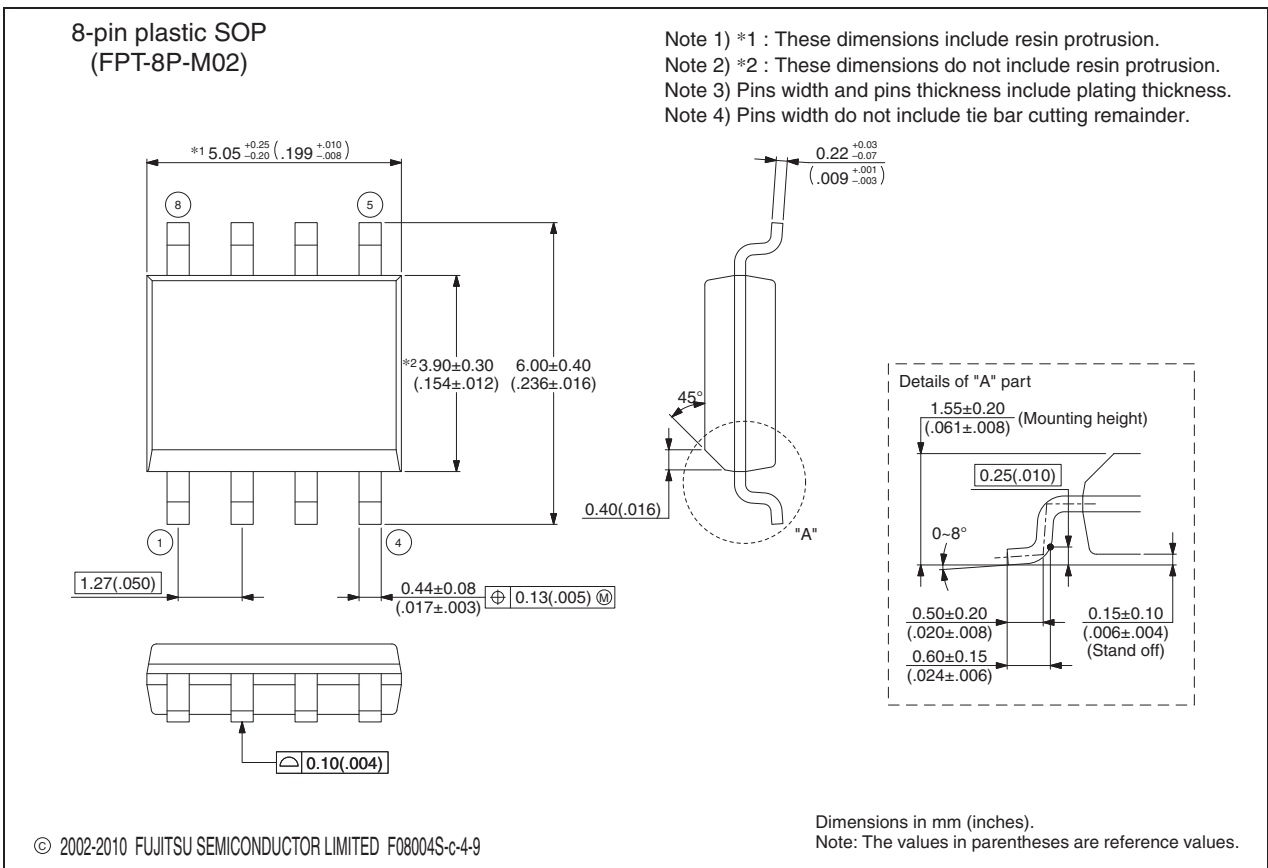
## ■ ORDERING INFORMATION

Part number	Package	Remarks
MB85RC128PNF-G-JNE1	8-pin, plastic SOP (FPT-8P-M02)	
MB85RC128PNF-G-JNERE1	8-pin, plastic SOP (FPT-8P-M02)	Embossed Carrier tape



## ■ PACKAGE DIMENSION

<p style="text-align: center;">8-pin plastic SOP</p>  <p style="text-align: center;">(FPT-8P-M02)</p>	Lead pitch	1.27 mm
	Package width × package length	3.9 mm × 5.05 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.75 mm MAX
	Weight	0.06 g



Please check the latest package dimension at the following URL.  
<http://edevice.fujitsu.com/package/en-search/>

**MEMO**

**MEMO**

## FUJITSU SEMICONDUCTOR LIMITED

Nomura Fudosan Shin-yokohama Bldg. 10-23, Shin-yokohama 2-Chome,  
Kohoku-ku Yokohama Kanagawa 222-0033, Japan

Tel: +81-45-415-5858

<http://jp.fujitsu.com/fsl/en/>

*For further information please contact:*

### North and South America

FUJITSU SEMICONDUCTOR AMERICA, INC.

1250 E. Arques Avenue, M/S 333

Sunnyvale, CA 94085-5401, U.S.A.

Tel: +1-408-737-5600 Fax: +1-408-737-5999

<http://us.fujitsu.com/micro/>

### Asia Pacific

FUJITSU SEMICONDUCTOR ASIA PTE. LTD.

151 Lorong Chuan,

#05-08 New Tech Park 556741 Singapore

Tel : +65-6281-0770 Fax : +65-6281-0220

<http://www.fujitsu.com/sg/services/micro/semiconductor/>

### Europe

FUJITSU SEMICONDUCTOR EUROPE GmbH

Pittlerstrasse 47, 63225 Langen, Germany

Tel: +49-6103-690-0 Fax: +49-6103-690-122

<http://emea.fujitsu.com/semiconductor/>

FUJITSU SEMICONDUCTOR SHANGHAI CO., LTD.

Rm. 3102, Bund Center, No.222 Yan An Road (E),

Shanghai 200002, China

Tel : +86-21-6146-3688 Fax : +86-21-6335-1605

<http://cn.fujitsu.com/fss/>

### Korea

FUJITSU SEMICONDUCTOR KOREA LTD.

902 Kosmo Tower Building, 1002 Daechi-Dong,

Gangnam-Gu, Seoul 135-280, Republic of Korea

Tel: +82-2-3484-7100 Fax: +82-2-3484-7111

<http://kr.fujitsu.com/fsk/>

FUJITSU SEMICONDUCTOR PACIFIC ASIA LTD.

10/F., World Commerce Centre, 11 Canton Road,

Tsimshatsui, Kowloon, Hong Kong

Tel : +852-2377-0226 Fax : +852-2376-3269

<http://cn.fujitsu.com/fsp/>

Specifications are subject to change without notice. For further information please contact each office.

### All Rights Reserved.

The contents of this document are subject to change without notice.

Customers are advised to consult with sales representatives before ordering.

The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU SEMICONDUCTOR device; FUJITSU SEMICONDUCTOR does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.

FUJITSU SEMICONDUCTOR assumes no liability for any damages whatsoever arising out of the use of the information.

Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU SEMICONDUCTOR or any third party or does FUJITSU SEMICONDUCTOR warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU SEMICONDUCTOR assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.

The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).

Please note that FUJITSU SEMICONDUCTOR will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.

Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.

The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department