74AUP2G79

Low-power dual D-type flip-flop; positive-edge trigger

Rev. 5 — 30 September 2010   **Product data sheet**

1. General description

The 74AUP2G79 provides the dual positive-edge triggered D-type flip-flop. Information on the data input (nD) is transferred to the nQ output on the LOW-to-HIGH transition of the clock pulse (nCP). The nD input must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation.

Schmitt trigger action at all inputs makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 0.8 V to 3.6 V.

This device ensures a very low static and dynamic power consumption across the entire V_{CC} range from 0.8 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing a damaging backflow current through the device when it is powered down.

2. Features and benefits

- Wide supply voltage range from 0.8 V to 3.6 V
- High noise immunity
- Complies with JEDEC standards:
  - JESD8-12 (0.8 V to 1.3 V)
  - JESD8-11 (0.9 V to 1.65 V)
  - JESD8-7 (1.2 V to 1.95 V)
  - JESD8-5 (1.8 V to 2.7 V)
  - JESD8-B (2.7 V to 3.6 V)
- ESD protection:
  - HBM JESD22-A114F Class 3A exceeds 5 000 V
  - MM JESD22-A115-A exceeds 200 V
  - CDM JESD22-C101E exceeds 1 000 V
- Low static power consumption; $I_{CC} = 0.9 \ \mu A$ (maximum)
- Latch-up performance exceeds 100 mA per JESD78 Class II
- Inputs accept voltages up to 3.6 V
- Low noise overshoot and undershoot < 10 % of V_{CC}
- I_{OFF} circuitry provides partial Power-down mode operation
- Multiple package options
- Specified from −40 °C to +85 °C and −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74AUP2G79DC	−40 °C to +125 °C	VSSOP8	plastic very thin shrink small outline package; 8 leads; body width 2.3 mm	SOT765-1
74AUP2G79GT	−40 °C to +125 °C	XSON8	plastic extremely thin small outline package; no leads; 8 terminals; body 1 × 1.95 × 0.5 mm	SOT833-1
74AUP2G79GF	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1 × 0.5 mm	SOT1089
74AUP2G79GD	−40 °C to +125 °C	XSON8U	plastic extremely thin small outline package; no leads; 8 terminals; UTLP based; body 3 × 2 × 0.5 mm	SOT996-2
74AUP2G79GM	−40 °C to +125 °C	XQFN8U	plastic extremely thin quad flat package; no leads; 8 terminals; UTLP based; body 1.6 × 1.6 × 0.5 mm	SOT902-1
74AUP2G79GN	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.2 × 1.0 × 0.35 mm	SOT1116
74AUP2G79GS	−40 °C to +125 °C	XSON8	extremely thin small outline package; no leads; 8 terminals; body 1.35 × 1.0 × 0.35 mm	SOT1203

4. Marking

Table 2. Marking codes

Type number	Marking code[1]
74AUP2G79DC	p79
74AUP2G79GT	p79
74AUP2G79GF	pP
74AUP2G79GD	p79
74AUP2G79GM	p79
74AUP2G79GN	pP
74AUP2G79GS	pP

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

Fig 1. Logic symbol

001aah811

Fig 2. IEC logic symbol

001aah812

74AUP2G79

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Product data sheet

Rev. 5 — 30 September 2010

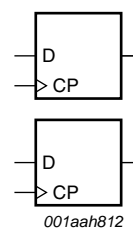**2 of 25**
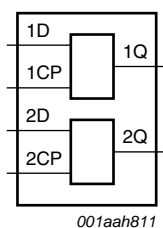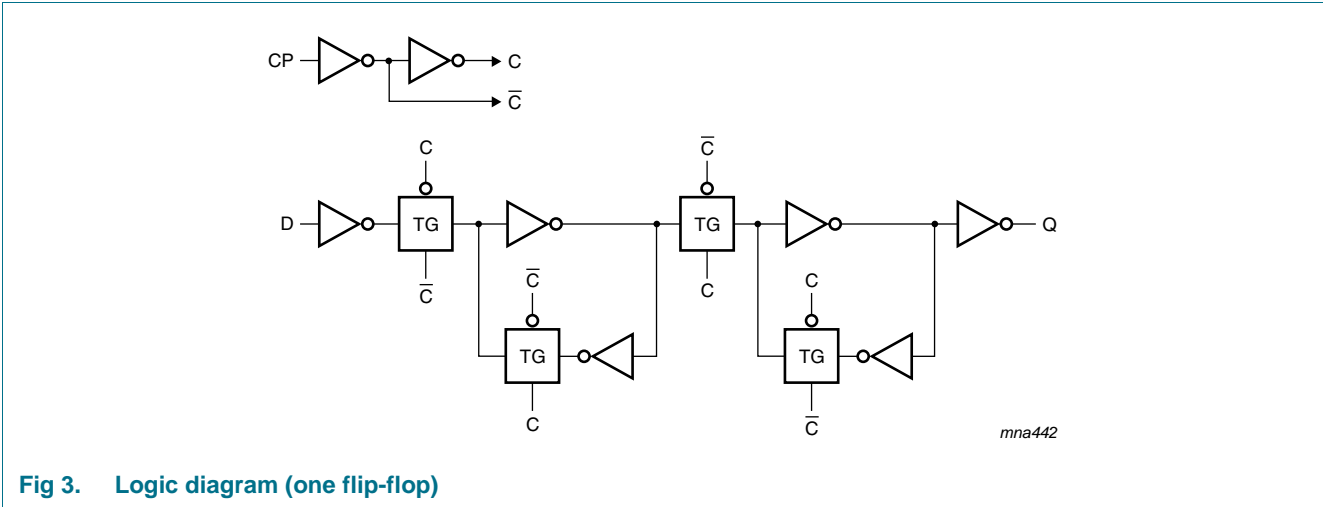
Fig 3.   Logic diagram (one flip-flop)

6.   Pinning information

6.1   Pinning
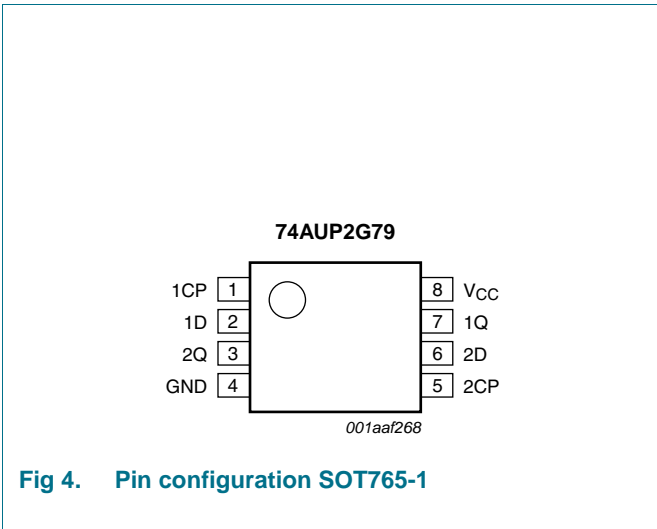
Fig 4.   Pin configuration SOT765-1

Transparent top view
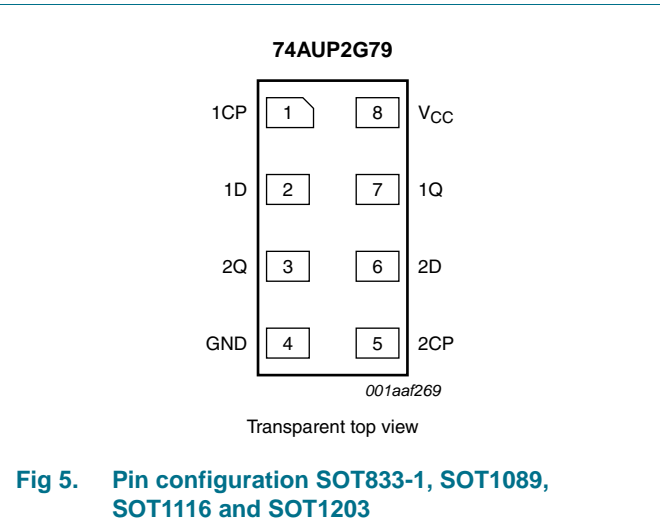
Fig 5.   Pin configuration SOT833-1, SOT1089, SOT1116 and SOT1203
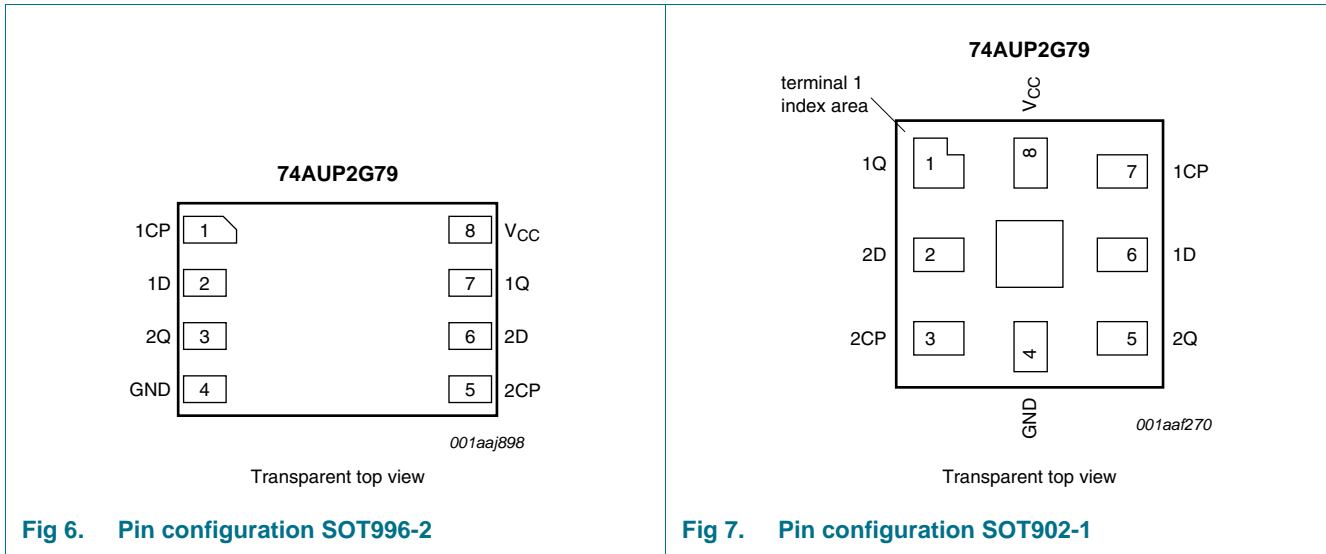
Fig 6.   Pin configuration SOT996-2

Fig 7.   Pin configuration SOT902-1

6.2 Pin description

Table 3.   Pin description

Symbol	Pin		Description
	SOT765-1, SOT833-1, SOT1089, SOT996-2, SOT1116 and SOT1203	SOT902-1	
1CP, 2CP	1, 5	7, 3	clock pulse input
1D, 2D	2, 6	6, 2	data input
GND	4	4	ground (0 V)
1Q, 2Q	7, 3	1, 5	data output
V_{CC}	8	8	supply voltage

7. Functional description

Table 4.   Function table[1]

Input		Output
nCP	nD	nQ
↑	L	L
↑	H	H
L	X	q

[1]   H = HIGH voltage level;

L = LOW voltage level;

↑ = LOW-to-HIGH CP transition;

X = don't care;

q = lower case letter indicates the state of referenced input, one set-up time prior to the LOW-to-HIGH CP transition.

74AUP2G79

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Product data sheet

Rev. 5 — 30 September 2010

4 of 25

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+4.6	V
I_{IK}	input clamping current	$V_I < 0$ V		−50	-	mA
V_I	input voltage		[1] −0.5		+4.6	V
I_{OK}	output clamping current	$V_O < 0$ V		−50	-	mA
V_O	output voltage	Active mode and Power-down mode	[1] −0.5		+4.6	V
I_O	output current	$V_O = 0$ V to V_{CC}		-	±20	mA
I_{CC}	supply current			-	50	mA
I_{GND}	ground current			−50	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +125 °C	[2]	-	250	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For VSSOP8 packages: above 110 °C the value of P_{tot} derates linearly with 8.0 mW/K.
For XSON8, XSON8U and XQFN8U packages: above 118 °C the value of P_{tot} derates linearly with 7.8 mW/K.

9. Recommended operating conditions

Table 6. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		0.8	3.6	V
V_I	input voltage		0	3.6	V
V_O	output voltage	Active mode	0	V_{CC}	V
		Power-down mode; $V_{CC} = 0$ V	0	3.6	V
T_{amb}	ambient temperature		−40	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 0.8$ V to 3.6 V	0	200	ns/V

10. Static characteristics

Table 7. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = 25 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 0.9 V to 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 V to 3.6 V	V_{CC} − 0.1	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	$0.75 \times V_{CC}$	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.11	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.32	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	2.05	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.9	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.72	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.31	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.31	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.31	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.44	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.31	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.44	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.1	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.2	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.2	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.5	µA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC}$ − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	40	µA
C_I	input capacitance	V_{CC} = 0 V to 3.6 V; V_I = GND or V_{CC}	-	0.6	-	pF
C_O	output capacitance	V_O = GND; V_{CC} = 0 V	-	1.3	-	pF

Table 7. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{amb} = −40 °C to +85 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.65 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 0.9 V 1.95 V	-	-	$0.35 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = −20 µA; V_{CC} = 0.8 V to 3.6 V	$V_{CC} - 0.1$	-	-	V
		I_O = −1.1 mA; V_{CC} = 1.1 V	$0.7 \times V_{CC}$	-	-	V
		I_O = −1.7 mA; V_{CC} = 1.4 V	1.03	-	-	V
		I_O = −1.9 mA; V_{CC} = 1.65 V	1.30	-	-	V
		I_O = −2.3 mA; V_{CC} = 2.3 V	1.97	-	-	V
		I_O = −3.1 mA; V_{CC} = 2.3 V	1.85	-	-	V
		I_O = −2.7 mA; V_{CC} = 3.0 V	2.67	-	-	V
		I_O = −4.0 mA; V_{CC} = 3.0 V	2.55	-	-	V
V_{OL}	LOW-level output voltage	V_I = V_{IH} or V_{IL}				
		I_O = 20 µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.1	V
		I_O = 1.1 mA; V_{CC} = 1.1 V	-	-	$0.3 \times V_{CC}$	V
		I_O = 1.7 mA; V_{CC} = 1.4 V	-	-	0.37	V
		I_O = 1.9 mA; V_{CC} = 1.65 V	-	-	0.35	V
		I_O = 2.3 mA; V_{CC} = 2.3 V	-	-	0.33	V
		I_O = 3.1 mA; V_{CC} = 2.3 V	-	-	0.45	V
		I_O = 2.7 mA; V_{CC} = 3.0 V	-	-	0.33	V
		I_O = 4.0 mA; V_{CC} = 3.0 V	-	-	0.45	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.5	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.5	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.6	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	0.9	µA
ΔI_{CC}	additional supply current	per pin; V_I = V_{CC} − 0.6 V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	50	µA

74AUP2G79

Product data sheet **Rev. 5 — 30 September 2010** 7 of 25

Table 7. **Static characteristics** *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{amb} = -40$ °C to +125 °C						
V_{IH}	HIGH-level input voltage	V_{CC} = 0.8 V	$0.75 \times V_{CC}$	-	-	V
		V_{CC} = 0.9 V to 1.95 V	$0.70 \times V_{CC}$	-	-	V
		V_{CC} = 2.3 V to 2.7 V	1.6	-	-	V
		V_{CC} = 3.0 V to 3.6 V	2.0	-	-	V
V_{IL}	LOW-level input voltage	V_{CC} = 0.8 V	-	-	$0.25 \times V_{CC}$	V
		V_{CC} = 0.9 V 1.95 V	-	-	$0.30 \times V_{CC}$	V
		V_{CC} = 2.3 V to 2.7 V	-	-	0.7	V
		V_{CC} = 3.0 V to 3.6 V	-	-	0.9	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = -20$ µA; V_{CC} = 0.8 V to 3.6 V	$V_{CC} - 0.11$	-	-	V
		$I_O = -1.1$ mA; V_{CC} = 1.1 V	$0.6 \times V_{CC}$	-	-	V
		$I_O = -1.7$ mA; V_{CC} = 1.4 V	0.93	-	-	V
		$I_O = -1.9$ mA; V_{CC} = 1.65 V	1.17	-	-	V
		$I_O = -2.3$ mA; V_{CC} = 2.3 V	1.77	-	-	V
		$I_O = -3.1$ mA; V_{CC} = 2.3 V	1.67	-	-	V
		$I_O = -2.7$ mA; V_{CC} = 3.0 V	2.40	-	-	V
		$I_O = -4.0$ mA; V_{CC} = 3.0 V	2.30	-	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}				
		$I_O = 20$ µA; V_{CC} = 0.8 V to 3.6 V	-	-	0.11	V
		$I_O = 1.1$ mA; V_{CC} = 1.1 V	-	-	$0.33 \times V_{CC}$	V
		$I_O = 1.7$ mA; V_{CC} = 1.4 V	-	-	0.41	V
		$I_O = 1.9$ mA; V_{CC} = 1.65 V	-	-	0.39	V
		$I_O = 2.3$ mA; V_{CC} = 2.3 V	-	-	0.36	V
		$I_O = 3.1$ mA; V_{CC} = 2.3 V	-	-	0.50	V
		$I_O = 2.7$ mA; V_{CC} = 3.0 V	-	-	0.36	V
		$I_O = 4.0$ mA; V_{CC} = 3.0 V	-	-	0.50	V
I_I	input leakage current	V_I = GND to 3.6 V; V_{CC} = 0 V to 3.6 V	-	-	±0.75	µA
I_{OFF}	power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V	-	-	±0.75	µA
ΔI_{OFF}	additional power-off leakage current	V_I or V_O = 0 V to 3.6 V; V_{CC} = 0 V to 0.2 V	-	-	±0.75	µA
I_{CC}	supply current	V_I = GND or V_{CC}; I_O = 0 A; V_{CC} = 0.8 V to 3.6 V	-	-	1.4	µA
ΔI_{CC}	additional supply current	per pin; $V_I = V_{CC} - 0.6$ V; I_O = 0 A; V_{CC} = 3.3 V [1]	-	-	75	µA

[1] One input at $V_{CC} - 0.6$ V, other input at V_{CC} or GND.

11. Dynamic characteristics

Table 8.   Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 8 [2]								
		V_{CC} = 0.8 V	-	19.7	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	2.6	5.5	11.0	2.4	12.9	2.4	14.2	ns
		V_{CC} = 1.4 V to 1.6 V	2.0	3.8	7.0	1.8	8.1	1.8	9.0	ns
		V_{CC} = 1.65 V to 1.95 V	1.7	3.1	5.4	1.5	6.4	1.5	7.1	ns
		V_{CC} = 2.3 V to 2.7 V	1.4	2.3	4.0	1.1	4.7	1.1	5.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.2	2.0	3.4	0.9	4.0	0.9	4.4	ns
f_{max}	maximum frequency	nCP; see Figure 9								
		V_{CC} = 0.8 V	-	53	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	203	-	170	-	170	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	347	-	310	-	300	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	435	-	400	-	390	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	550	-	490	-	480	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	619	-	550	-	510	-	MHz
C_L = 10 pF										
t_{pd}	propagation delay	nCP to nQ; see Figure 8 [2]								
		V_{CC} = 0.8 V	-	23.1	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	3.1	6.3	12.3	2.8	14.4	2.8	15.9	ns
		V_{CC} = 1.4 V to 1.6 V	2.5	4.4	8.1	2.2	9.5	2.2	10.5	ns
		V_{CC} = 1.65 V to 1.95 V	2.1	3.6	6.3	1.9	7.5	1.9	8.3	ns
		V_{CC} = 2.3 V to 2.7 V	1.8	2.8	4.7	1.5	5.6	1.5	6.2	ns
		V_{CC} = 3.0 V to 3.6 V	1.7	2.5	4.1	1.3	4.5	1.3	5.0	ns
f_{max}	maximum frequency	nCP; see Figure 9								
		V_{CC} = 0.8 V	-	52	-	-	-	-	-	MHz
		V_{CC} = 1.1 V to 1.3 V	-	192	-	150	-	150	-	MHz
		V_{CC} = 1.4 V to 1.6 V	-	324	-	280	-	230	-	MHz
		V_{CC} = 1.65 V to 1.95 V	-	421	-	310	-	250	-	MHz
		V_{CC} = 2.3 V to 2.7 V	-	486	-	370	-	360	-	MHz
		V_{CC} = 3.0 V to 3.6 V	-	550	-	410	-	360	-	MHz

Table 8. Dynamic characteristics …continued

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C$_L$ = 15 pF										
t$_{pd}$	propagation delay	nCP to nQ; see Figure 8 [2]								
		V$_{CC}$ = 0.8 V	-	26.6	-	-	-	-	-	ns
		V$_{CC}$ = 1.1 V to 1.3 V	3.5	7.1	13.6	3.2	15.6	3.2	17.2	ns
		V$_{CC}$ = 1.4 V to 1.6 V	2.8	5.0	9.2	2.5	10.7	2.5	11.8	ns
		V$_{CC}$ = 1.65 V to 1.95 V	2.4	4.1	7.1	2.2	8.5	2.2	9.4	ns
		V$_{CC}$ = 2.3 V to 2.7 V	2.2	3.2	5.4	1.9	6.3	1.9	7.0	ns
		V$_{CC}$ = 3.0 V to 3.6 V	2.0	2.9	4.5	1.6	5.0	1.6	5.5	ns
f$_{max}$	maximum frequency	nCP; see Figure 9								
		V$_{CC}$ = 0.8 V	-	50	-	-	-	-	-	MHz
		V$_{CC}$ = 1.1 V to 1.3 V	-	181	-	120	-	120	-	MHz
		V$_{CC}$ = 1.4 V to 1.6 V	-	301	-	190	-	160	-	MHz
		V$_{CC}$ = 1.65 V to 1.95 V	-	407	-	240	-	190	-	MHz
		V$_{CC}$ = 2.3 V to 2.7 V	-	422	-	300	-	270	-	MHz
		V$_{CC}$ = 3.0 V to 3.6 V	-	481	-	320	-	300	-	MHz
C$_L$ = 30 pF										
t$_{pd}$	propagation delay	nCP to nQ; see Figure 8 [2]								
		V$_{CC}$ = 0.8 V	-	36.8	-	-	-	-	-	ns
		V$_{CC}$ = 1.1 V to 1.3 V	4.7	9.3	17.3	4.2	23.3	4.2	25.6	ns
		V$_{CC}$ = 1.4 V to 1.6 V	3.8	6.4	11.8	3.3	14.3	3.3	15.7	ns
		V$_{CC}$ = 1.65 V to 1.95 V	3.3	5.3	9.4	3.0	11.3	3.0	12.4	ns
		V$_{CC}$ = 2.3 V to 2.7 V	3.0	4.3	7.0	2.7	8.5	2.7	9.4	ns
		V$_{CC}$ = 3.0 V to 3.6 V	2.8	3.9	5.8	2.6	7.2	2.6	7.9	ns
f$_{max}$	maximum frequency	nCP; see Figure 9								
		V$_{CC}$ = 0.8 V	-	28	-	-	-	-	-	MHz
		V$_{CC}$ = 1.1 V to 1.3 V	-	128	-	70	-	70	-	MHz
		V$_{CC}$ = 1.4 V to 1.6 V	-	206	-	120	-	110	-	MHz
		V$_{CC}$ = 1.65 V to 1.95 V	-	262	-	150	-	120	-	MHz
		V$_{CC}$ = 2.3 V to 2.7 V	-	269	-	190	-	170	-	MHz
		V$_{CC}$ = 3.0 V to 3.6 V	-	309	-	200	-	190	-	MHz

Low-power dual D-type flip-flop; positive-edge trigger

Table 8.   Dynamic characteristics …*continued*

Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.

| Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_L = 5 pF, 10 pF, 15 pF and 30 pF										
t_{su}	set-up time	HIGH; nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	3.4	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.8	-	1.5	-	1.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.5	-	1.0	-	1.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.4	-	0.7	-	0.7	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.4	-	0.6	-	0.6	-	ns
		LOW; nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	3.0	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	0.9	-	1.6	-	1.6	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	0.6	-	1.0	-	1.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.5	-	0.9	-	0.9	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.7	-	1.0	-	1.0	-	ns
t_h	hold time	nD to nCP; see Figure 9								
		V_{CC} = 0.8 V	-	−1.9	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	−0.6	-	0	-	0	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	−0.4	-	0	-	0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	−0.4	-	0	-	0	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	−0.4	-	0	-	0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	−0.3	-	0	-	0	-	ns
t_W	pulse width	HIGH or LOW; nCP; see Figure 9								
		V_{CC} = 0.8 V	-	5.6	-	-	-	-	-	ns
		V_{CC} = 1.1 V to 1.3 V	-	2.4	-	3.5	-	3.5	-	ns
		V_{CC} = 1.4 V to 1.6 V	-	1.3	-	2.0	-	2.0	-	ns
		V_{CC} = 1.65 V to 1.95 V	-	0.9	-	1.9	-	1.9	-	ns
		V_{CC} = 2.3 V to 2.7 V	-	0.7	-	2.0	-	2.0	-	ns
		V_{CC} = 3.0 V to 3.6 V	-	0.6	-	2.2	-	2.2	-	ns

Table 8. Dynamic characteristics …*continued*
*Voltages are referenced to GND (ground = 0 V); for test circuit see Figure 10.*

Symbol	Parameter	Conditions	25 °C			−40 °C to +85 °C		−40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	Min	Max	
C_{PD}	power dissipation capacitance	f = 1 MHz; [3] V_I = GND to V_{CC}								
		V_{CC} = 0.8 V	-	1.6	-	-	-	-	-	pF
		V_{CC} = 1.1 V to 1.3 V	-	1.7	-	-	-	-	-	pF
		V_{CC} = 1.4 V to 1.6 V	-	1.8	-	-	-	-	-	pF
		V_{CC} = 1.65 V to 1.95 V	-	1.9	-	-	-	-	-	pF
		V_{CC} = 2.3 V to 2.7 V	-	2.3	-	-	-	-	-	pF
		V_{CC} = 3.0 V to 3.6 V	-	2.7	-	-	-	-	-	pF

[1] All typical values are measured at nominal V_{CC}.

[2] t_{pd} is the same as t_{PLH} and t_{PHL}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz;

f_o = output frequency in MHz;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs.

12. Waveforms
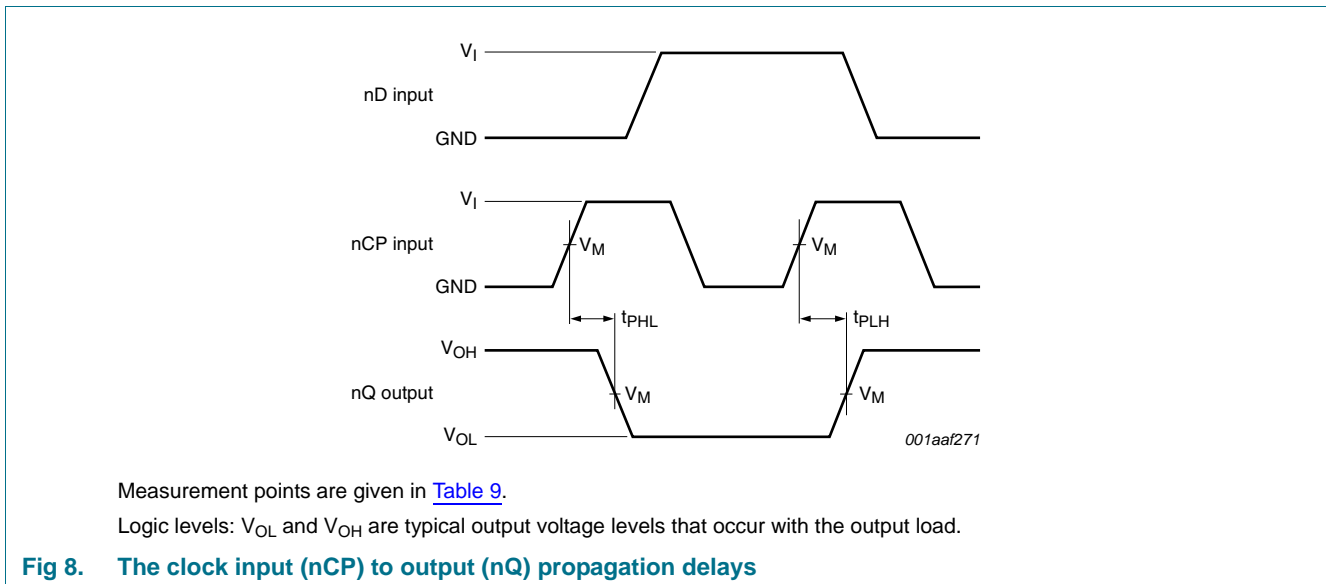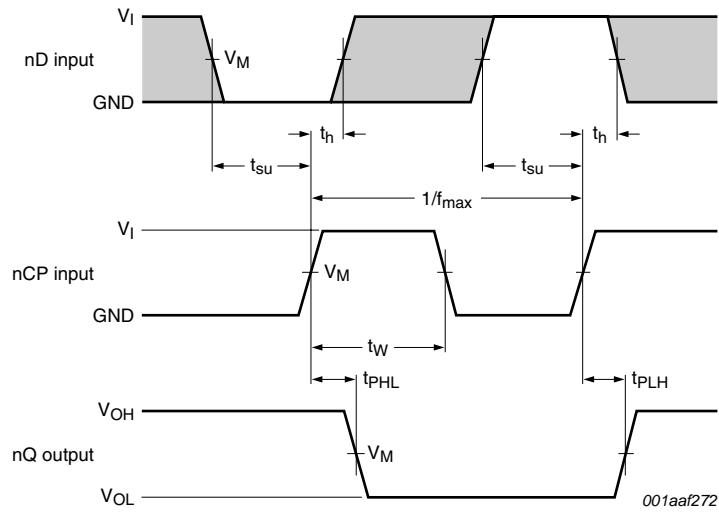
Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Fig 8. The clock input (nCP) to output (nQ) propagation delays

Measurement points are given in Table 9.

Logic levels: V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 9. **The clock input (nCP) to output (nQ) propagation delays, nCP clock pulse width, nD to nCP set-up times, nCP to nD hold times and the nCP maximum frequency**

Table 9. **Measurement points**

Supply voltage	Output	Input		
V_{CC}	V_M	V_M	V_I	$t_r = t_f$
0.8 V to 3.6 V	$0.5 \times V_{CC}$	$0.5 \times V_{CC}$	V_{CC}	≤ 3.0 ns

74AUP2G79

Product data sheet

Rev. 5 — 30 September 2010

13 of 25
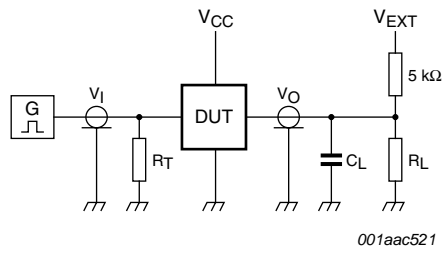
Test data is given in Table 10.

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 10. Test circuit for measuring switching times

Table 10.   Test data

Supply voltage	Load			V_{EXT}		
V_{CC}	C_L	R_L[1]	t_{PLH}, t_{PHL}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
0.8 V to 3.6 V	5 pF, 10 pF, 15 pF and 30 pF	5 kΩ or 1 MΩ	open	GND	$2 \times V_{CC}$

[1] For measuring enable and disable times R_L = 5 kΩ.
For measuring propagation delays, set-up and hold times and pulse width R_L = 1 MΩ.

13. Package outline

VSSOP8: plastic very thin shrink small outline package; 8 leads; body width 2.3 mm   SOT765-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(2)	e	HₑE	L	Lₚ	Q	v	w	y	Z(1)	θ
mm	1	0.15 / 0.00	0.85 / 0.60	0.12	0.27 / 0.17	0.23 / 0.08	2.1 / 1.9	2.4 / 2.2	0.5	3.2 / 3.0	0.4	0.40 / 0.15	0.21 / 0.19	0.2	0.13	0.1	0.4 / 0.1	8° / 0°

Notes
1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

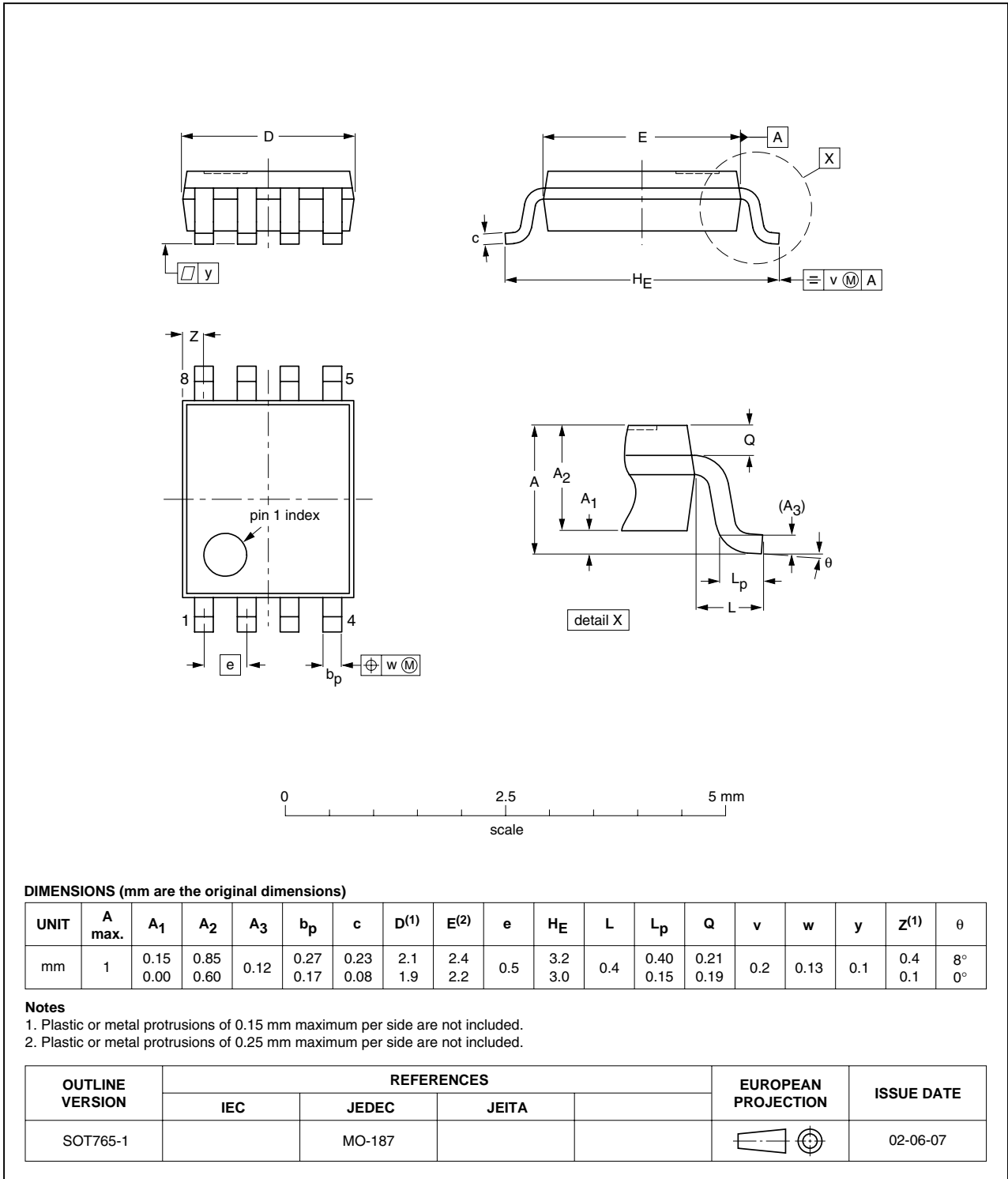| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT765-1		MO-187				02-06-07

Fig 11. Package outline SOT765-1 (VSSOP8)

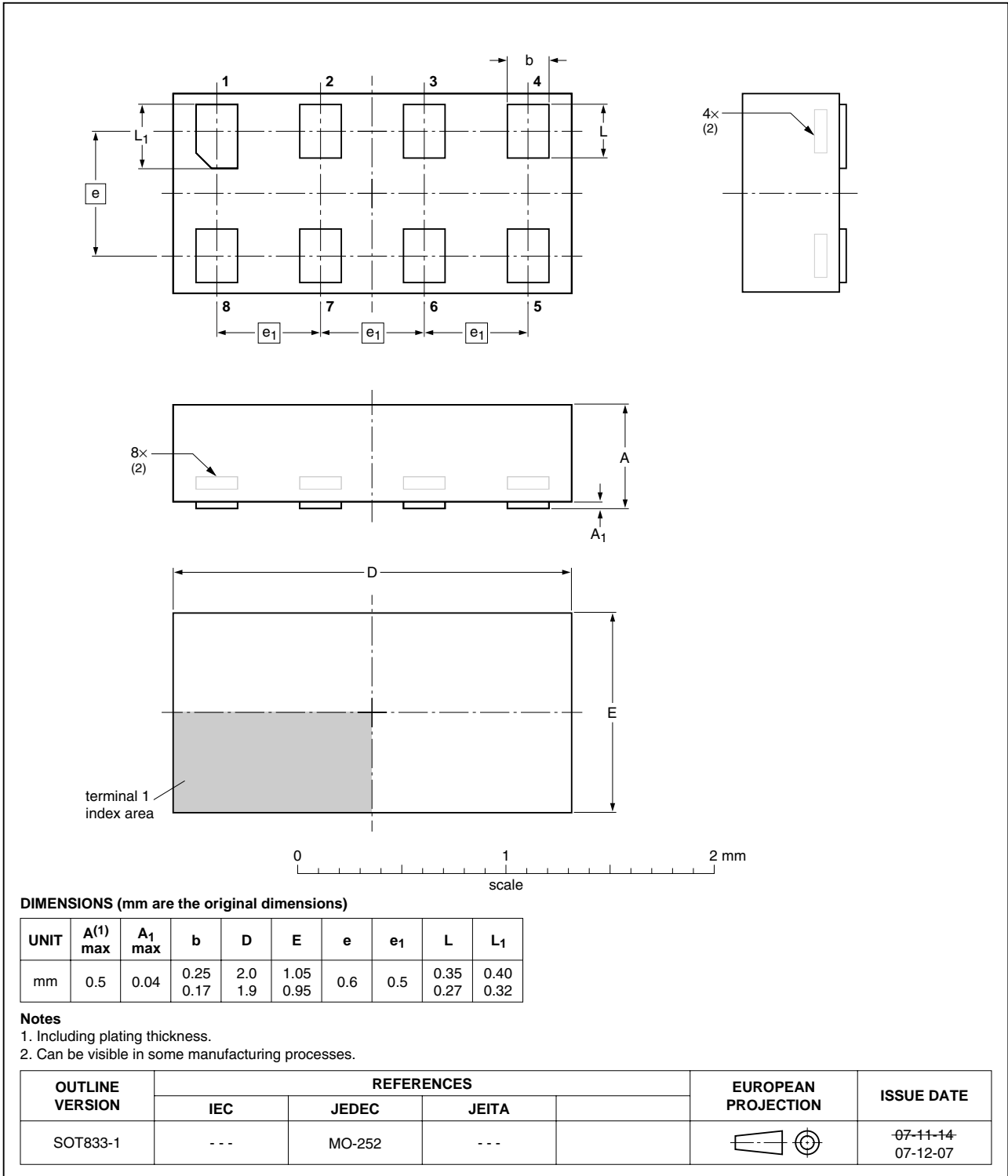XSON8: plastic extremely thin small outline package; no leads; 8 terminals; body 1 x 1.95 x 0.5 mm   SOT833-1

DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max	A₁ max	b	D	E	e	e₁	L	L₁
mm	0.5	0.04	0.25 0.17	2.0 1.9	1.05 0.95	0.6	0.5	0.35 0.27	0.40 0.32

Notes
1. Including plating thickness.
2. Can be visible in some manufacturing processes.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT833-1	- - -	MO-252	- - -			~~07-11-14~~ 07-12-07

Fig 12. Package outline SOT833-1 (XSON8)

XSON8: extremely thin small outline package; no leads;
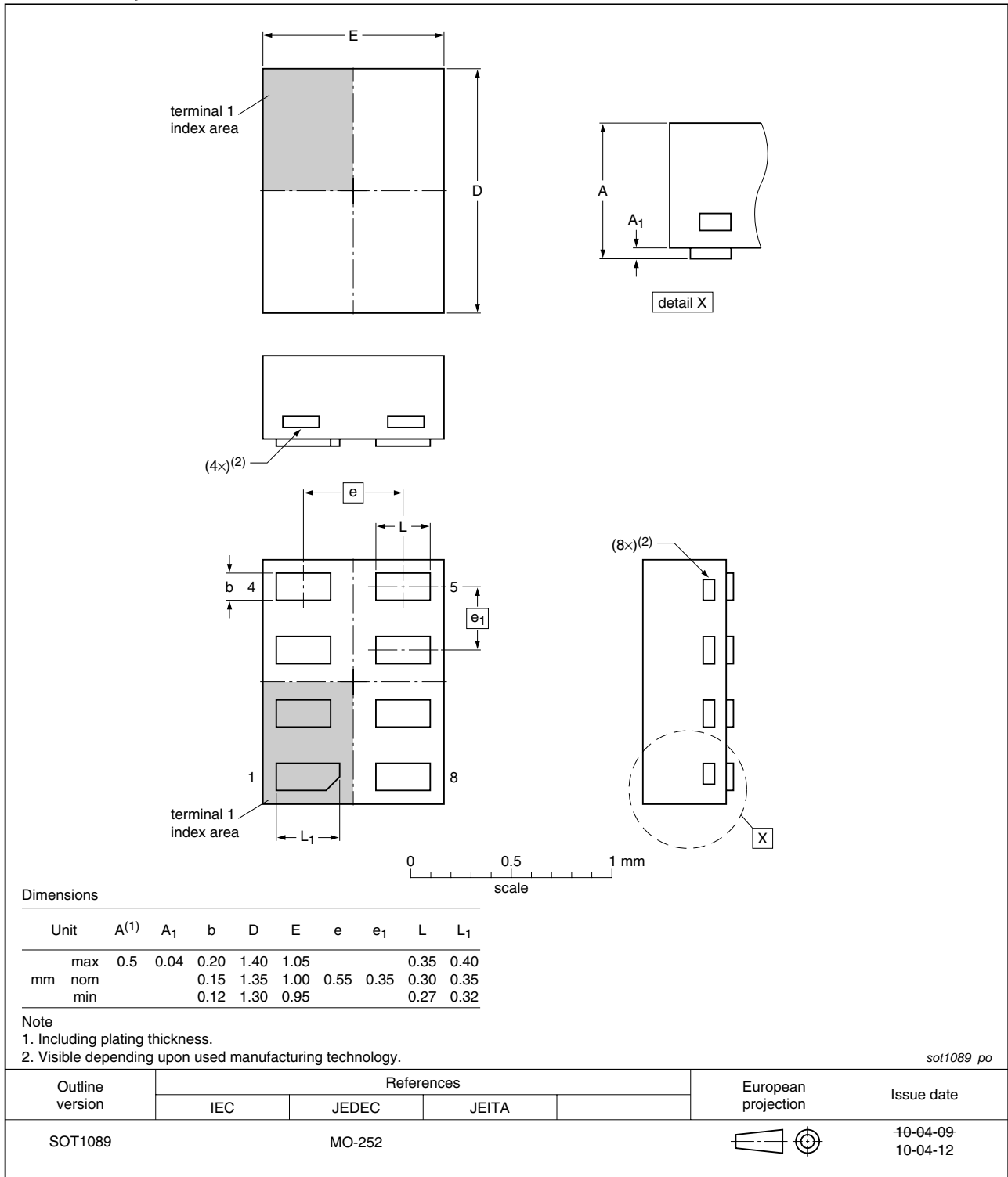8 terminals; body 1.35 x 1 x 0.5 mm

SOT1089

terminal 1
index area

E

D

A

A_1

detail X

$(4\times)^{(2)}$

e

L

b 4

5

e_1

$(8\times)^{(2)}$

1

8

terminal 1
index area

L_1

X

0   0.5   1 mm
scale

Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.5	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1089_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1089		MO-252				10-04-09 10-04-12

Fig 13. Package outline SOT1089 (XSON8)

XSON8U: plastic extremely thin small outline package; no leads;
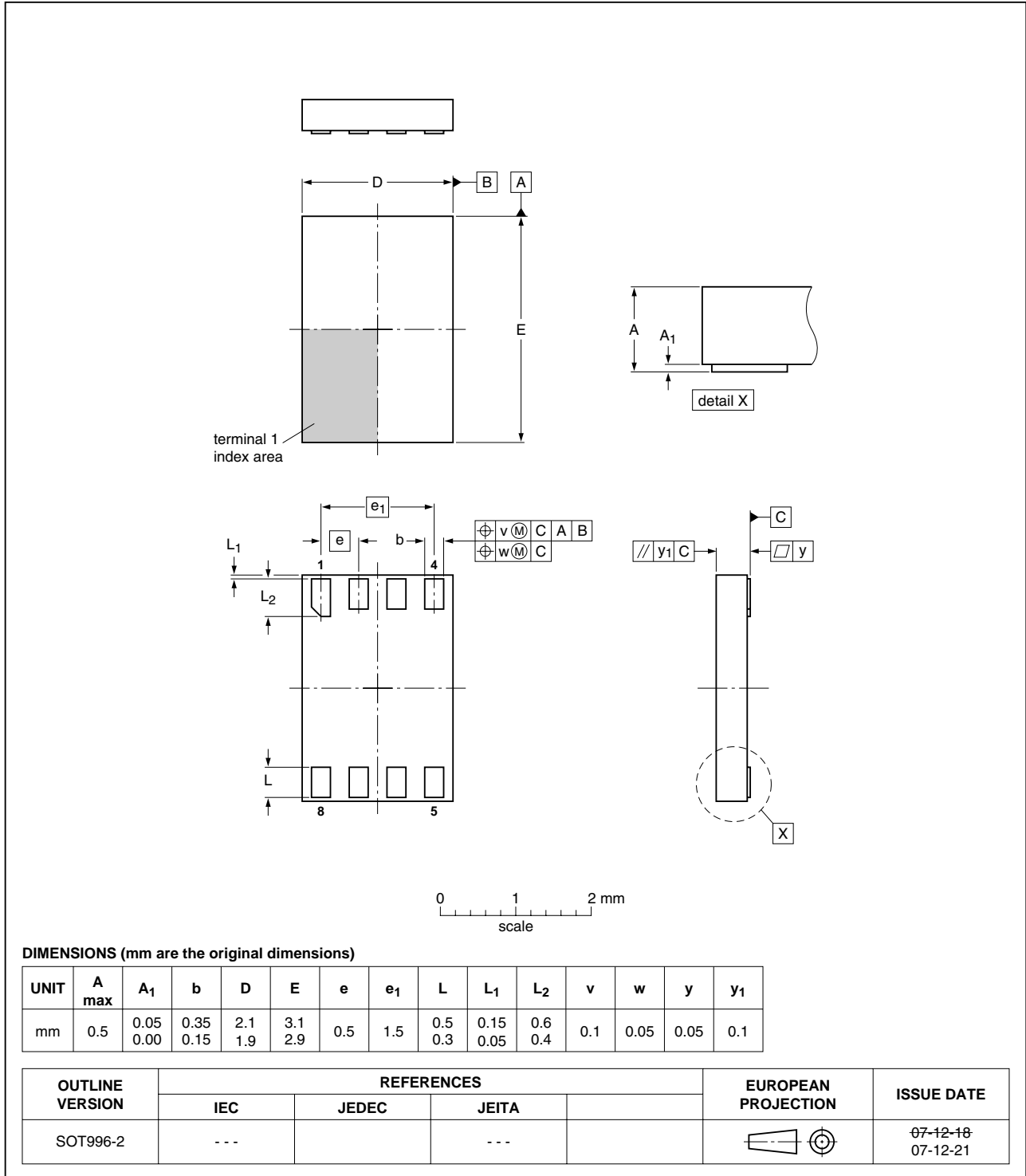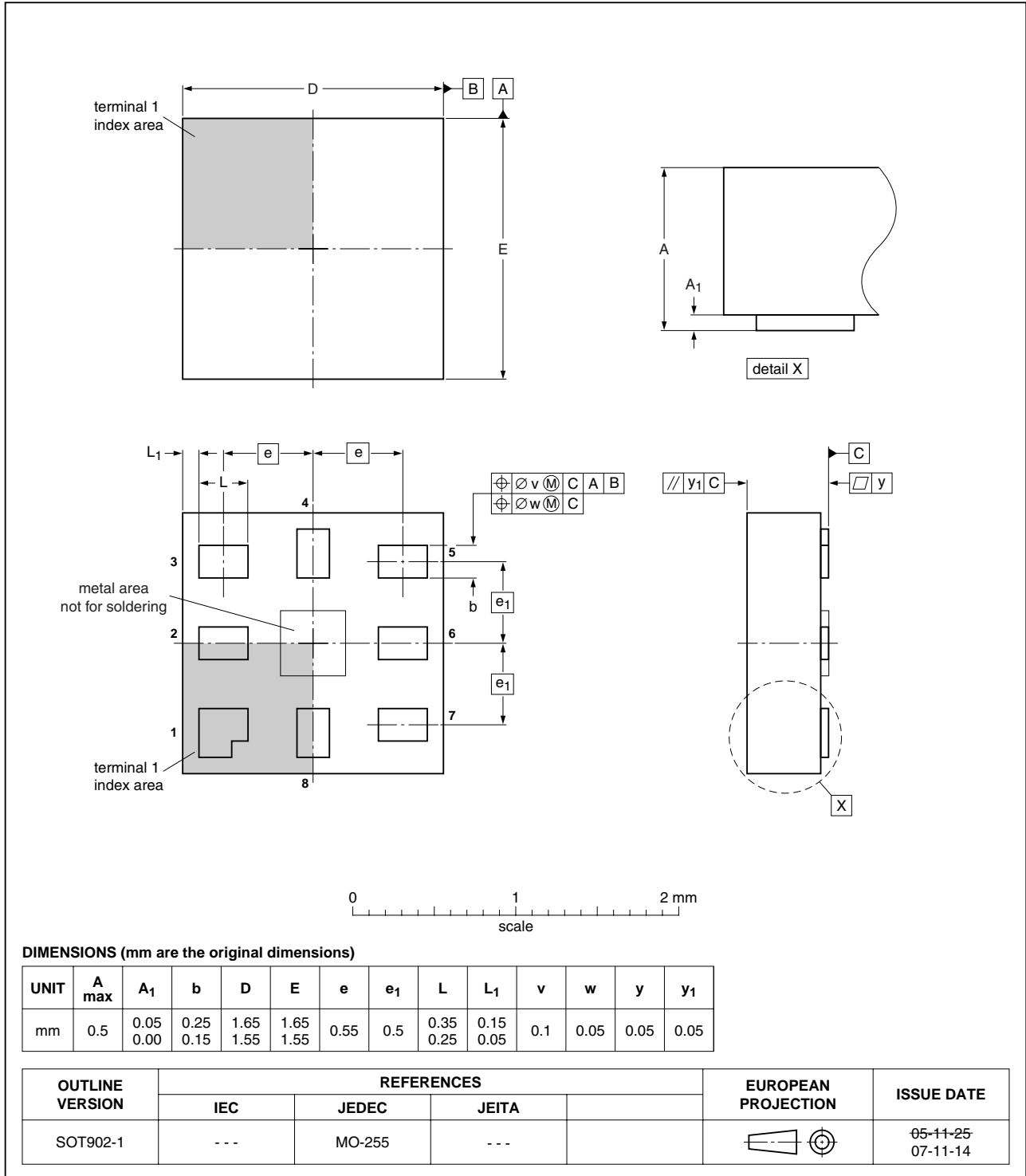**8 terminals; UTLP based; body 3 x 2 x 0.5 mm** SOT996-2

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A₁	b	D	E	e	e₁	L	L₁	L₂	v	w	y	y₁
mm	0.5	0.05 0.00	0.35 0.15	2.1 1.9	3.1 2.9	0.5	1.5	0.5 0.3	0.15 0.05	0.6 0.4	0.1	0.05	0.05	0.1

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT996-2	- - -		- - -		~~07-12-18~~ 07-12-21

Fig 14. Package outline SOT996-2 (XSON8U)

XQFN8U: plastic extremely thin quad flat package; no leads;
8 terminals; UTLP based; body 1.6 x 1.6 x 0.5 mm

SOT902-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	b	D	E	e	e_1	L	L_1	v	w	y	y_1
mm	0.5	0.05 0.00	0.25 0.15	1.65 1.55	1.65 1.55	0.55	0.5	0.35 0.25	0.15 0.05	0.1	0.05	0.05	0.05

OUTLINE VERSION	REFERENCES			EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA		
SOT902-1	- - -	MO-255	- - -		05-11-25 07-11-14

Fig 15. Package outline SOT902-1 (XQFN8U)

74AUP2G79

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Product data sheet **Rev. 5 — 30 September 2010** **19 of 25**

**XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.2 x 1.0 x 0.35 mm**   **SOT1116**

Dimensions	Unit	A[1]	A_1	b	D	E	e	e_1	L	L_1
	max	0.35	0.04	0.20	1.25	1.05			0.35	0.40
mm	nom			0.15	1.20	1.00	0.55	0.3	0.30	0.35
	min			0.12	1.15	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1116_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1116						~~10-04-02~~ 10-04-07
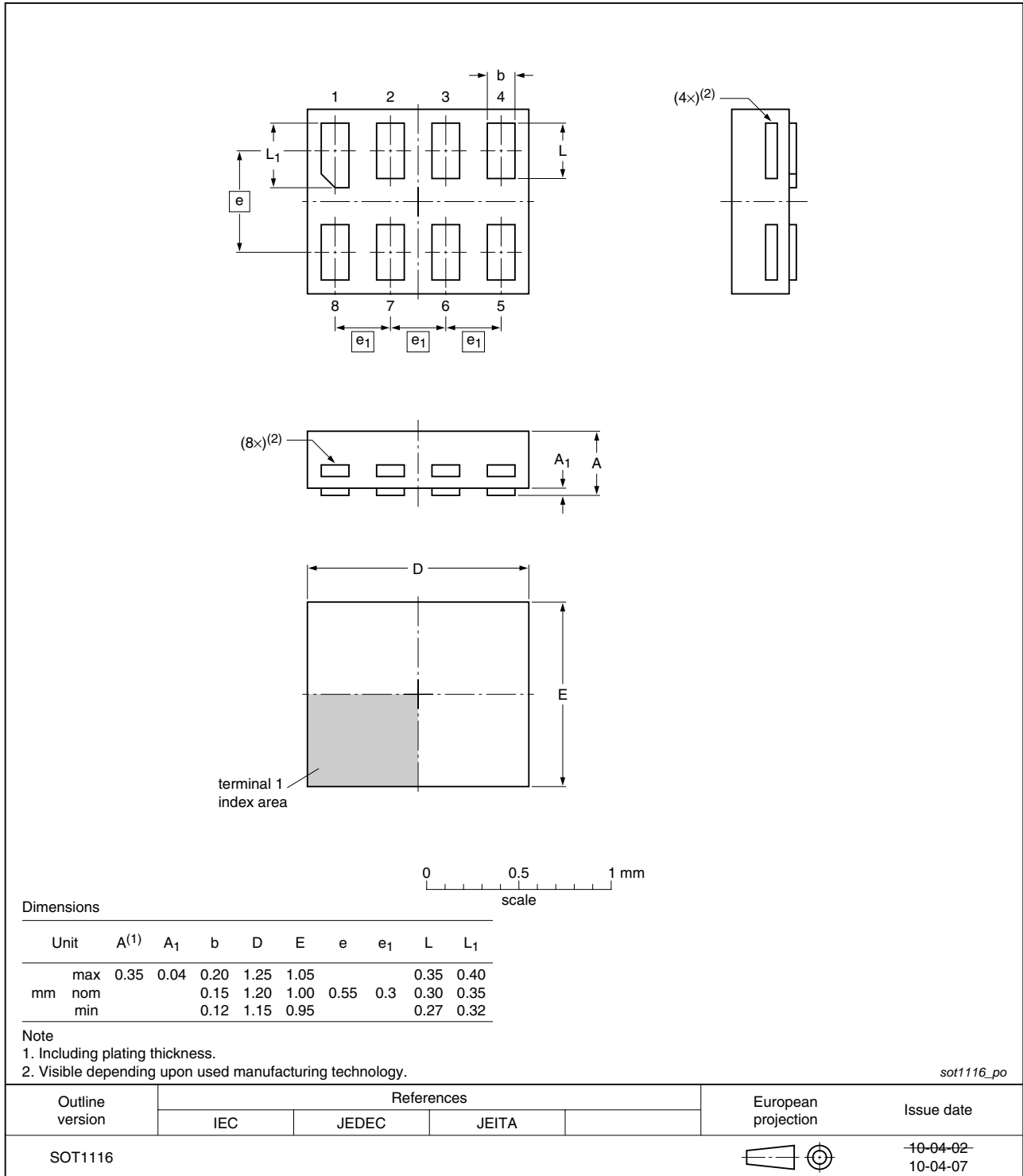
Fig 16. Package outline SOT1116 (XSON8)

XSON8: extremely thin small outline package; no leads;
8 terminals; body 1.35 x 1.0 x 0.35 mm

SOT1203

Dimensions

Unit		$A^{(1)}$	A_1	b	D	E	e	e_1	L	L_1
mm	max	0.35	0.04	0.20	1.40	1.05			0.35	0.40
	nom			0.15	1.35	1.00	0.55	0.35	0.30	0.35
	min			0.12	1.30	0.95			0.27	0.32

Note
1. Including plating thickness.
2. Visible depending upon used manufacturing technology.

sot1203_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1203						~~10-04-02~~ 10-04-06
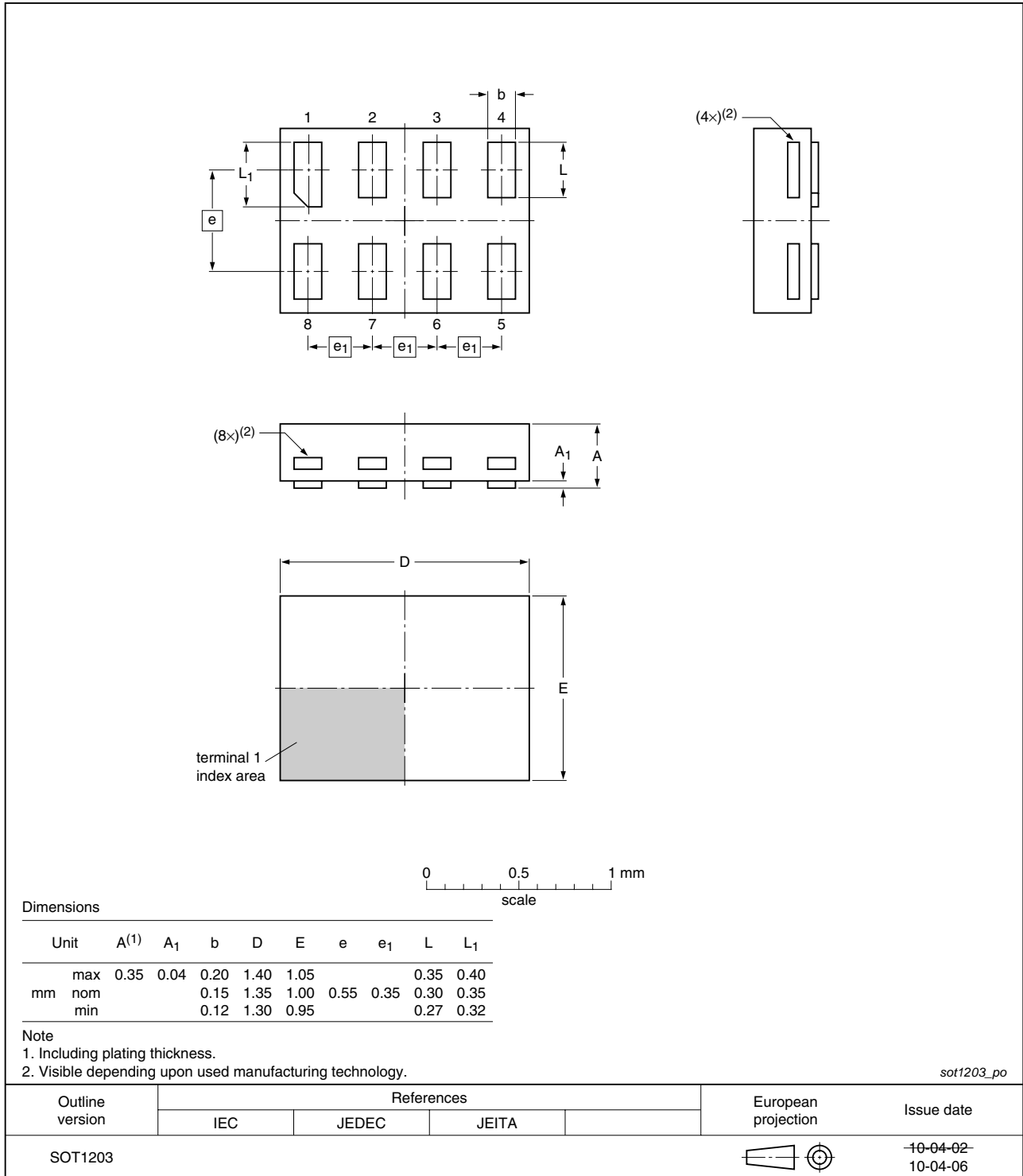
Fig 17. Package outline SOT1203 (XSON8)

74AUP2G79

Product data sheet

Rev. 5 — 30 September 2010

21 of 25

14. Abbreviations

Table 11.   Abbreviations

Acronym	Description
CDM	Charged Device Model
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

15. Revision history

Table 12.   Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AUP2G79 v.5	20100930	Product data sheet	-	74AUP2G79 v.4
Modifications:	• Added type number 74AUP2G79GF (SOT1089/XSON8 package). • Added type number 74AUP2G79GN (SOT1116/XSON8 package). • Added type number 74AUP2G79GS (SOT1203/XSON8 package).			
74AUP2G79 v.4	20090630	Product data sheet	-	74AUP2G79 v.3
74AUP2G79 v.3	20090401	Product data sheet	-	74AUP2G79 v.2
74AUP2G79 v.2	20080319	Product data sheet	-	74AUP2G79 v.1
74AUP2G79 v.1	20061006	Product data sheet	-	-

74AUP2G79

Product data sheet

Rev. 5 — 30 September 2010

22 of 25

NXP Semiconductors

74AUP2G79

Low-power dual D-type flip-flop; positive-edge trigger

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

16.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

16.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use in automotive applications — This NXP Semiconductors product has been qualified for use in automotive applications. The product is not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

74AUP2G79

All information provided in this document is subject to legal disclaimers. © NXP B.V. 2010. All rights reserved.

Product data sheet

Rev. 5 — 30 September 2010

23 of 25

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

16.4   Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

17. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

74AUP2G79

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2010. All rights reserved.

Product data sheet

Rev. 5 — 30 September 2010

24 of 25

18. Contents