Synchronizing dual J–$\overline{K}$ positive edge-triggered flip-flop with metastable immune characteristics

74F50109

FEATURE

- Metastable immune characteristics
- Output skew guaranteed less than 1.5ns
- High source current (I_{OH} = 15mA) ideal for clock driver applications
- Pinout compatible with 74F109
- See 74F5074 for synchronizing dual D-type flip-flop
- See 74F50728 for synchronizing cascaded D-type flip-flop
- See 74F50729 for synchronizing dual D-type flip-flop with edge-triggered set and reset

TYPE	TYPICAL f_{max}	TYPICAL SUPPLY CURRENT(TOTAL)
74F50109	150MHz	22mA

ORDERING INFORMATION

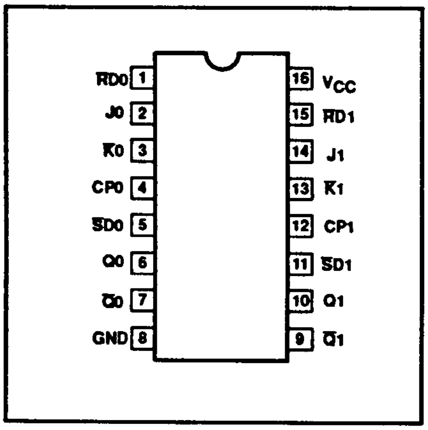
DESCRIPTION	ORDER CODE
	COMMERCIAL RANGE V_{CC} = 5V ±10%, T_{amb} = 0°C to +70°C
16–pin plastic DIP	N74F50109N
16–pin plastic SO	N74F50109D

INPUT AND OUTPUT LOADING AND FAN OUT TABLE

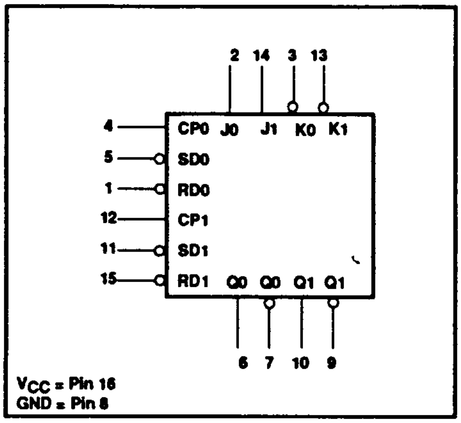
PINS	DESCRIPTION	74F (U.L.) HIGH/ LOW	LOAD VALUE HIGH/ LOW
J0, J1	J inputs	1.0/0.417	20µA/250µA
$\overline{K}$0, $\overline{K}$1	K inputs	1.0/0.417	20µA/250µA
CP0, CP1	Clock inputs (active rising edge)	1.0/0.033	20µA/20µA
$\overline{S}$D0, $\overline{S}$D1	Set inputs (active low)	1.0/0.033	20µA/20µA
$\overline{R}$D0, $\overline{R}$D1	Reset inputs (active low)	1.0/0.033	20µA/20µA
Q0, Q1, $\overline{Q}$0, $\overline{Q}$1	Data outputs	750/33	15mA/20mA

NOTE: One (1.0) FAST unit load is defined as: 20µA in the high state and 0.6mA in the low state.

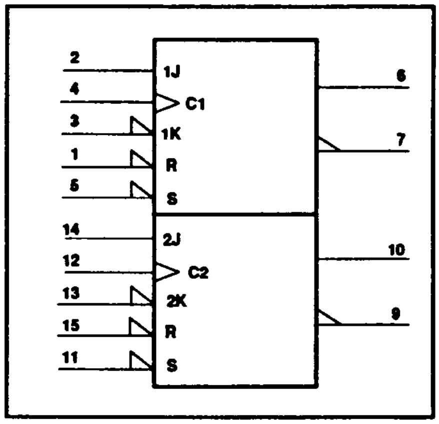
PIN CONFIGURATION



LOGIC SYMBOL



IEC/IEEE SYMBOL



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DESCRIPTION

The 74F50109 is a dual positive edge-triggered JK-type flip-flop featuring individual J, $\overline{K}$, clock, set, and reset inputs; also true and complementary outputs.

Set ($\overline{SD}$) and reset ($\overline{RD}$) are asynchronous active low inputs and operate independently of the clock (CP) input.

The J and $\overline{K}$ are edge–triggered inputs which control the state changes of the flip–flops as described in the function table.
The J and $\overline{K}$ inputs must be stable just one setup time prior to the low–to–high transition of the clock for guaranteed propagation delays. The J$\overline{K}$ design allows operation as a D flip–flop by tying J and $\overline{K}$ inputs together.
The 74F50109 is designed so that the outputs can never display a metastable state due to setup and hold time violations. If setup time and hold time are violated the propagation delays may be extended beyond the specifications but the outputs will not glitch or display a metastable state. Typical metastability parameters for the 74F50109 are: $\tau \cong$ 135ps and $\tau \cong$ 9.8 X 10^6 sec where τ represents a function of the rate at which a latch in a metastable state resolves that condition and T_0 represents a function of the measurement of the propensity of a latch to enter a metastable state.

METASTABLE IMMUNE CHARACTERISTICS

Signtetics uses the term 'metastable immune' to describe characteristics of some of the products in its FAST family. Specifically the 74F50XXX family presently consist of 4 products which displays metastable immune characteristics. This term means that the outputs will not glitch or display an output anomaly under any circumstances including setup and hold time violations.

This claim is easily verified on the 74F5074. By running two independent signal generators (see Fig. 1) at nearly the same frequency (in this case 10MHz clock and 10.02 MHz data) the device–under–test can be often be driven into a metastable state. If the Q output is then used to trigger a digital scope set to infinite persistence the $\overline{Q}$ output will build a waveform.0 An experiment was run by continuously operating the devices in the region where metastability will occur.

When the device–under–test is a 74F74 (which was not designed with metastable immune characteristics) the waveform will appear as in Fig. 2.

Fig. 2 shows clearly that the $\overline{Q}$ output can vary in time with respect to the Q trigger point. This also implies that the Q or $\overline{Q}$ output waveshapes may be distorted. This can be verified on an analog scope with a charge plate CRT. Perhaps of even greater interest are the dots running along the 3.5V volt line in the upper right hand quadrant. These show that the $\overline{Q}$ output did not change state even though the Q output glitched to at least 1.5 volts, the trigger point of the scope.

When the device–under–test is a metastable immune part, such as the 74F5074, the waveform will appear as in Fig. 3. The 74F5074 $\overline{Q}$ output will appear as in Fig. 3. The 74F5074 Q output will not vary with respect to the Q trigger point even when the a part is driven into a metastable state. Any tendency towards internal metastability is resolved by Philips Components–Signetics patented circuitry. If a metastable event occurs within the flop the only outward manifestation of the event will be an increased clock–to–Q/$\overline{Q}$ propagation delay.

This propagation delay is, of course, a function of the metastability characteristics of the part defined by τ and T_0.

The metastability characteristics of the 74F5074 and related part types represent state–of–the–art TTL technology.

After determining the T_0 and t of the flop, calculating the mean time between failures (MTBF) is simple. Suppose a designer wants to use the 74F50729 for synchronizing asynchronous data that is arriving at 10MHz (as measured by a frequency counter), has a clock frequency of 50MHz, and has decided that he would like to sample the output of the 74F50109 10 nanoseconds after the clock edge. He simply plugs his number into the equation below:

$$MTBF = e^{(t'/\tau)} / T_0 f_C f_I$$

In this formula, f_C is the frequency of the clock, f_I is the average input event frequency, and t' is the time after the clock pulse that the output is sampled (t' < h, h being the normal propagation delay). In this situation the f_I will be twice the data frequency of 20 MHz because input events consist of both of low and high transitions. Multiplying f_I by f_C gives an answer of 10^{15} Hz^2. From Fig. 4 it is clear that the MTBF is greater than 10^{10} seconds. Using the above formula MTBF is 1.51 X 10^{10} seconds or about 480 years.

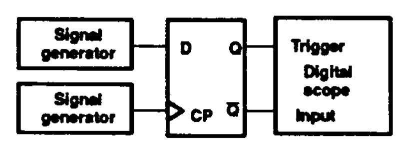


Figure 20. Test setup

COMPARISON OF METASTABLE IMMUNE AND NON–IMMUNE CHARACTERISTICS

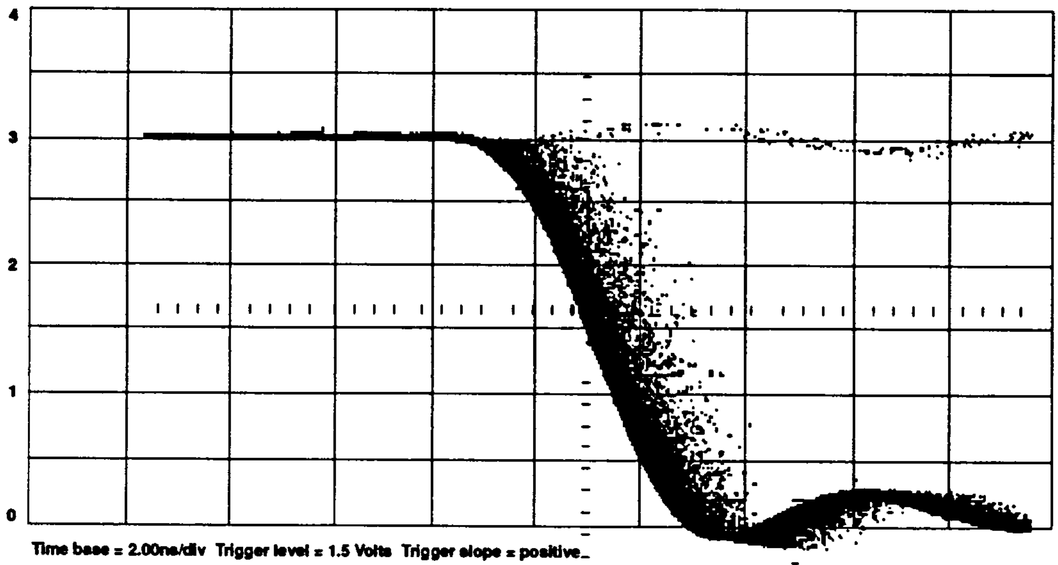


Figure 21. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

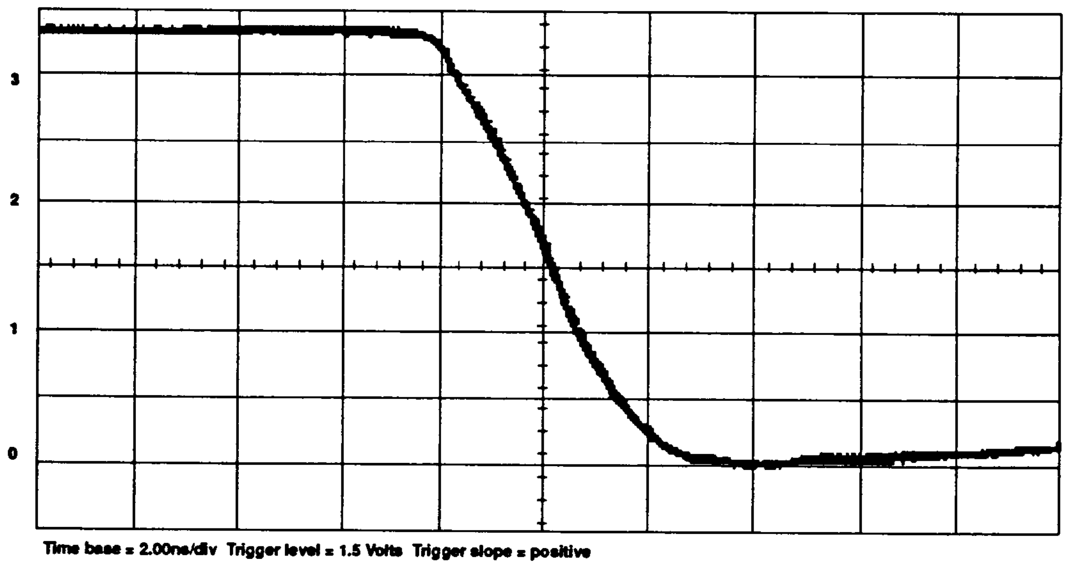


Figure 22. 74F74 $\overline{Q}$ output triggered by Q output, Setup and Hold times violated

MEAN TIME BETWEEN FAILURES (MTBF) VERSUS t'

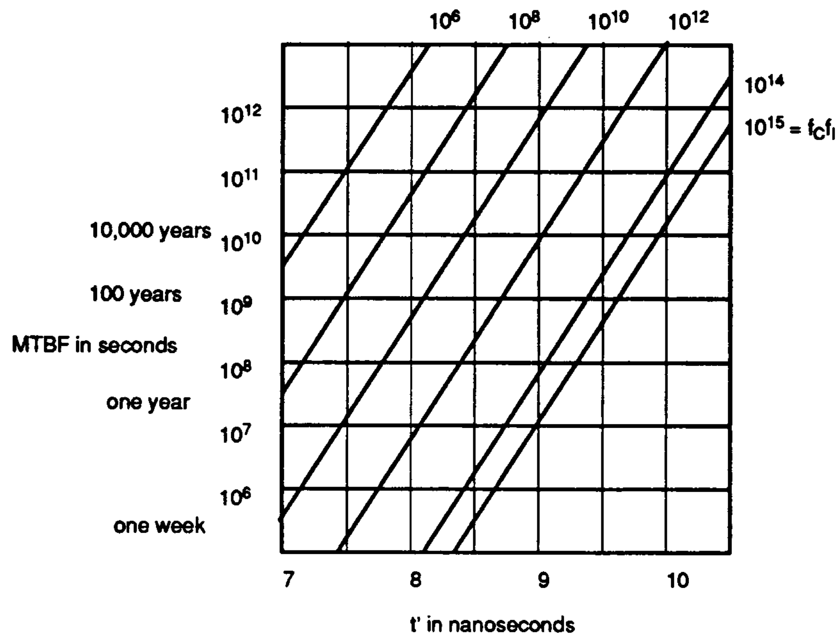


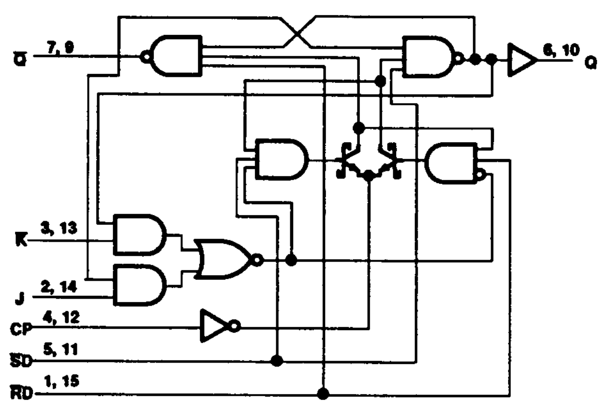
Figure 23.

NOTE: V_{CC} = 5V, T_{amb} = 25°C, τ =135ps, To = 9.8 X 10^8 sec

TYPICAL VALUES FOR τ AND T_0 AT VARIOUS V_{CC}S AND TEMPERATURES

	T_{amb} = 0°C		T_{amb} = 25°C		T_{amb} = 70°C	
V_{CC}	τ	T_0	τ	T_0	τ	T_0
5.5V	125ps	1.0 X 10^9 sec	138ps	5.4 X 10^6 sec	160ps	1.7 X 10^5 sec
5.0V	115ps	1.3 X 10^{10} sec	135ps	9.8 X 10^6 sec	167ps	3.9 X 10^4 sec
4.5V	115ps	3.4 X 10^{13} sec	132ps	5.1 X 10^8 sec	175ps	7.3 X 10^4 sec

LOGIC DIAGRAM



FUNCTION TABLE

INPUTS					OUTPUTS		OPERATING MODE
S̄D	R̄D	CP	J	K̄	Q	Q̄	
L	H	X	X	X	H	L	Asynchronous set
H	L	X	X	X	L	H	Asynchronous reset
L	L	X	X	X	H	H	Undetermined*
H	H	↑̸	X	X	q	q̄	Hold
H	H	↑	h	l	q̄	q	Toggle
H	H	↑	h	h	H	L	Load "1" (set)
H	H	↑	l	l	L	H	Load "0" (reset)
H	H	↑	l	h	q	q̄	Hold 'no change'

NOTES:
1. H = High–voltage level
2. h = High–voltage level one setup time prior to low–to–high clock transition
3. L = Low–voltage level
4. l = Low–voltage level one setup time prior to low–to–high clock transition
5. q = Lower case indicate the state of the referenced output prior to the low–to–high clock transition
6. X = Don't care
7. ↑ = Low–to–high clock transition
8. ↑̸ = Not low–to–high clock transition
9. * = Both outputs will be high if both S̄D and R̄D go low simultaneously

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limit set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	–0.5 to +7.0	V
V_{IN}	Input voltage	–0.5 to +7.0	V
I_{IN}	Input current	–30 to +5	mA
V_{OUT}	Voltage applied to output in high output state	–0.5 to V_{CC}	V
I_{OUT}	Current applied to output in low output state	40	mA
T_{amb}	Operating free air temperature range	0 to +70	°C
T_{stg}	Storage temperature range	–65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High–level input voltage	2.0			V
V_{IL}	Low–level input voltage			0.8	V
I_{IK}	Input clamp current			–18	mA
I_{OH}	High–level output current			–1	mA
I_{OL}	Low–level output current			20	mA
T_{amb}	Operating free air temperature range	0		+70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						MIN	TYP[2]	MAX	
V_{OH}	High–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OH} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN		±5%V_{CC}	2.7	3.4		V
V_{OL}	Low–level output voltage		V_{CC} = MIN, V_{IL} = MAX,	I_{OL} = MAX	±10%V_{CC}		0.30	0.50	V
			V_{IH} = MIN		±5%V_{CC}		0.30	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V					100	µA
I_{IH}	High–level input current		V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low–level input current	Jn, $\overline{K}$n	V_{CC} = MAX, V_I = 0.5V					-250	µA
		CPn, $\overline{S}$Dn, $\overline{R}$Dn	V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX			-60		-150	mA
I_{CC}	Supply current[4] (total)		V_{CC} = MAX				22	32	mA

NOTES:
3. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
4. All typical values are at V_{CC} = 5V, T_{amb} = 25°C.
5. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
6. Measure I_{CC} with the clock input grounded and all outputs open, then with Q and $\overline{Q}$ outputs high in turn.

AC ELECTRICAL CHARACTERISTICS

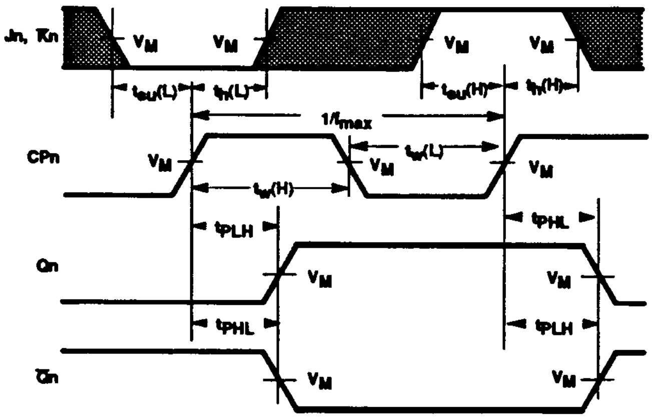
SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	Waveform 1	130	150		90		ns
t_{PLH} t_{PHL}	Propagation delay CPn to Qn or $\overline{Q}$n	Waveform 1	2.0 2.0	3.8 3.8	6.0 6.0	2.0 2.0	6.5 6.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{S}$Dn, $\overline{R}$Dn to Qn or $\overline{Q}$n	Waveform 2	3.5 3.5	5.5 5.5	8.0 8.0	3.0 3.0	8.5 8.5	ns
$t_{sk(o)}$	Output skew[1, 2]	Waveform 4			1.5		1.5	ns

NOTES:
1. | t_{PN} actual – t_{PM} actual| for any output compared to any other output where N and M are either LH or HL.
2. Skew times are valid only under same test conditions (temperature, V_{CC}, loading, etc.,).

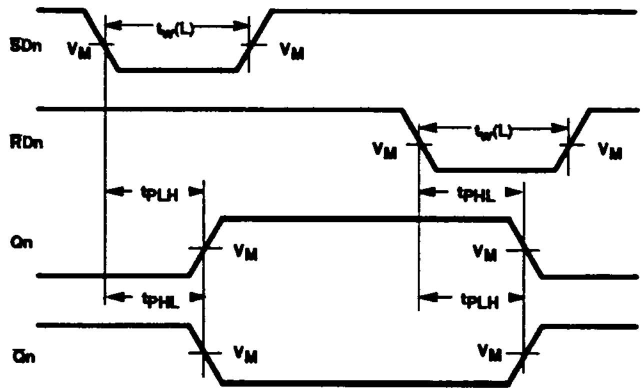
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_{amb} = +25°C V_{CC} = +5.0V C_L = 50pF, R_L = 500Ω			T_{amb} = 0°C to +70°C V_{CC} = +5.0V ± 10% C_L = 50pF, R_L = 500Ω		
			MIN	TYP	MAX	MIN	MAX	
t_{su} (H) t_{su}(L)	Setup time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.5 1.5			2.0 2.0		ns
t_h (H) t_h (L)	Hold time, high or low Jn, $\overline{K}$n to CPn	Waveform 1	1.0 1.0			1.5 1.5		ns
t_w (H) t_w (L)	CPn pulse width, high or low	Waveform 1	3.0 4.0			3.5 5.0		ns
t_w (L)	$\overline{S}$Dn or $\overline{R}$Dn pulse width, low	Waveform 2	3.5			4.0		ns
t_{rec}	Recovery time $\overline{S}$Dn or $\overline{R}$Dn to CP	Waveform 3	3.0			3.5		ns

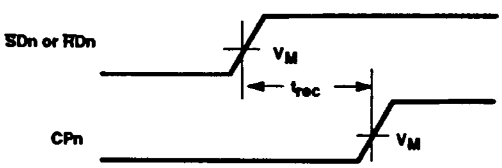
AC WAVEFORMS



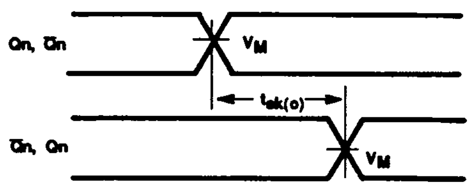
Waveform 1. Propagation delay for data to output, data setup time and hold times, and clock width, and maximum clock frequency



Waveform 2. Propagation delay for set and reset to output, set and reset pulse width



Waveform 3. Recovery time for set or reset to output

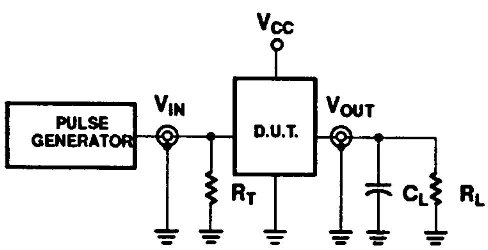


Waveform 4. Output skew

NOTES:

1. For all waveforms, V_M = 1.5V.
2. The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORM



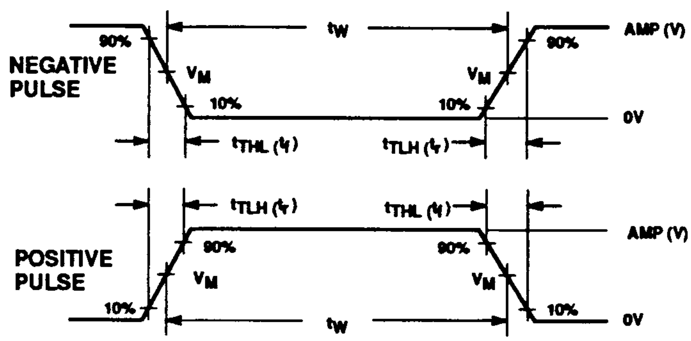
Test circuit for totem-pole outputs

DEFINITIONS:

R_L = Load resistor; see AC electrical characteristics for value.

C_L = Load capacitance includes jig and probe capacitance; see AC electrical characteristics for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



Input pulse definition

family	INPUT PULSE REQUIREMENTS					
	amplitude	V_M	rep. rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1.5V	1MHz	500ns	2.5ns	2.5ns