68HC11 Microcontroller Family Compatible



64K

X68C64 SLIC® E²

8192 x 8 Bit

E² Micro-Peripheral

FEATURES

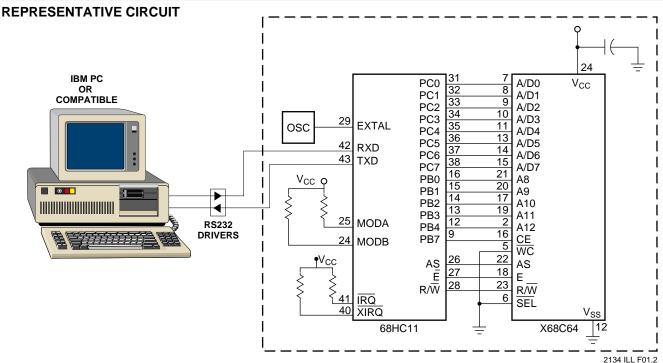
SLIC (SELF LOADING INTEGRATED CODE) FIRMWARE

- Automatically Downloads User's Software into 68HC11 Based Systems
- Features Load, Verify, and Block Protection Capabilities
- Transfers Baud Rate 9600 at 8MHz
- Concurrent Read Write[™]
 - —Dual Plane Architecture
 - —Isolates Read/Write Functions Between Planes
 - Allows Continuous Execution of Code From One Plane While Writing in the Other Plane
- Multiplexed Address/Data Bus
 - —Direct Interface to Popular 68HC11 Family
- Block Protect Register
 - -Individually Set Write Lock Out in 1K Blocks
- Toggle Bit Polling
 - -Early End of Write Detection
- Page Mode Write
 - —Allows up to 32 Bytes to be Written in One Write Cycle

DESCRIPTION

The X68C64 SLIC E^2 is a highly integrated E^2 Microcontroller peripheral which combines the functionality of the X68C64 component with pre-loaded software routines allowing any embedded system using it to upgrade and download software via the serial port. This self-loading integrated code eliminates the need to initially program the firmware into a memory device at the time of initial manufacture. The SLIC E^2 routines also greatly facilitate the loading of subsequent versions of the firmware into the system.

The SLIC E² routines consist of approximately 500 bytes of instructions for the 68HC11 which will initialize the microcontroller and its on-board UART and upload the user's software through the UART. The baud rate for the transfer is 9600 based on a crystal frequency of 8MHz. Data transfer is accomplished using a proprietary format called XCOM. Xicor also has developed a program for IBM PCs and compatibles called XSLIC, which will translate an Intel HEX or Motorola S-record format file into XCOM format and download the program to a X68C64 SLIC E².



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X68C64 SLIC® E²

The X68C64 component is an 8K x 8 E²PROM fabricated with advanced CMOS Textured Poly Floating Gate Technology. The X68C64 features a Multiplexed Address and Data bus allowing direct interface to a variety of popular single-chip microcontrollers operating in expanded multiplexed mode without the need for additional interface circuitry.

The X68C64 is internally configured as two independent 4K x 8 memory arrays. This feature provides the ability to perform nonvolatile memory updates in one array and continue operation out of code stored in the other array; effectively eliminating the need for an auxiliary memory device for code storage.

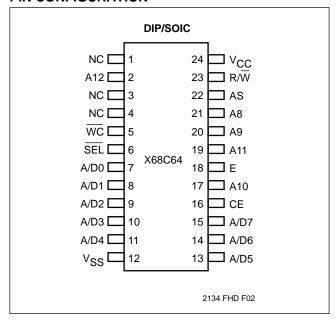
To write to the X68C64 SLIC E², a three-byte command sequence must precede the byte(s) being writ-

ten. This sequence called Software Data Protection prevents the loss of data or program information due to inadvertant write cycles during power-up or power-down. The X68C64 SLIC E² also provides a second generation software data protection scheme called Block Protect.

Block Protect can provide write lockout of the entire device or selected 1K blocks. There are eight 1K x 8 blocks that can be write protected individually in any combination required by the user. Block Protect, in additional to Write Control input, allows the different segments of the memory to have varying degrees of alterability in normal system operation.

For further information on the X68C64 hardware interface, consult the X68C64 Data Sheet.

PIN CONFIGURATION

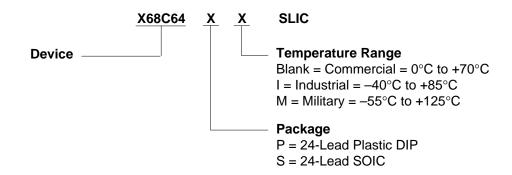


PIN NAMES

Symbol	Description
AS	Address Strobe
A/D ₀ -A/D ₇	Address Inputs/Data I/O
A ₈ -A ₁₂	Address Inputs
E	Enable Input
R/W	Read/Write Input
CE	Chip Enable
WC	Write Control
SEL	Device Select—Connect to V _{SS}
V _{SS}	Ground
Vcc	Supply Voltage

2134 PGM T01

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US. PATENTS

Xicor products are covered by one or more of the following U.S. Patents: 4,263,664; 4,274,012; 4,300,212; 4,314,265; 4,326,134; 4,393,481; 4,404,475; 4,450,402; 4,486,769; 4,488,060; 4,520,461; 4,533,846; 4,599,706; 4,617,652; 4,668,932; 4,752,912; 4,829,482; 4,874,967; 4,883,976; 4,980,859; 5,012,132; 5,003,197; 5,023,694. Foreign patents and additional patents pending.

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