



N-Channel 20-V (D-S) 175°C MOSFET

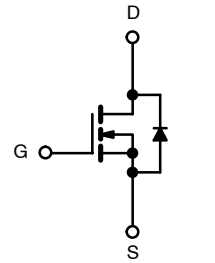
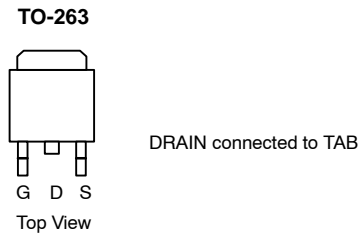
PRODUCT SUMMARY			
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ)
20	0.012 @ $V_{GS} = 10$ V	40 ^a	7.5
	0.026 @ $V_{GS} = 4.5$ V	40 ^a	

FEATURES

- TrenchFET[®] Power MOSFET
- 175°C Junction Temperature
- Optimized for High-Side Synchronous Rectifier
- 100% R_g Tested

APPLICATIONS

- Desktop or Server CPU Core
- Game Station



Ordering Information: SUM40N02-12P
SUM40N02-12P—E3

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)			
Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	20	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 175^\circ\text{C}$)	I_D	$T_C = 25^\circ\text{C}$	40 ^a
		$T_C = 100^\circ\text{C}$	40 ^a
Pulsed Drain Current	I_{DM}	90	A
Maximum Power Dissipation ^b	P_D	$T_C = 25^\circ\text{C}$	83 ^c
		$T_A = 25^\circ\text{C}$ ^d	3.75
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Junction-to-Ambient (PCB Mounted) ^d	R_{thJA}	40	$^\circ\text{C}/\text{W}$
Junction-to-Case	R_{thJC}	1.8	

Notes

- Package limited.
- Duty cycle $\leq 1\%$.
- See SOA curve for voltage derating.
- When mounted on 1" square PCB (FR-4 material).

SUM40N02-12P

Vishay Siliconix



SPECIFICATIONS (T _J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V _{(BR)DSS}	V _{DS} = 0 V, I _D = 250 μA	20			V
Gate-Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.85	2	3	
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 20 V			± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 20 V, V _{GS} = 0 V			1	μA
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 125 °C			50	
		V _{DS} = 20 V, V _{GS} = 0 V, T _J = 175 °C			250	
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≥ 5 V, V _{GS} = 10 V	90			A
Drain-Source On-State Resistance ^a	r _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.0095	0.012	Ω
		V _{GS} = 10 V, I _D = 20 A, T _J = 125 °C			0.0175	
		V _{GS} = 10 V, I _D = 20 A, T _J = 175 °C			0.022	
		V _{GS} = 4.5 V, I _D = 15 A		0.021	0.026	
Forward Transconductance ^a	g _{fs}	V _{DS} = 15 V, I _D = 20 A	10			S
Dynamic^b						
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 10 V, f = 1 MHz		1000		pF
Output Capacitance	C _{oss}			370		
Reverse Transfer Capacitance	C _{rss}			180		
Total Gate Charge ^b	Q _g	V _{DS} = 10 V, V _{GS} = 4.5 V, I _D = 40 A		7.5	12	nC
Gate-Source Charge ^b	Q _{gs}			3.5		
Gate-Drain Charge ^b	Q _{gd}			2.6		
Gate Resistance	R _g		1.5	3.0	5.1	Ω
Turn-On Delay Time ^b	t _{d(on)}	V _{DD} = 10 V, R _L = 0.25 Ω I _D ≅ 40 A, V _{GEN} = 10 V, R _g = 2.5 Ω		11	20	ns
Rise Time ^b	t _r			10	15	
Turn-Off Delay Time ^b	t _{d(off)}			24	35	
Fall Time ^b	t _f			9	15	
Source-Drain Diode Ratings and Characteristics (T_C = 25 °C)^c						
Continuous Current	I _S				40	A
Pulsed Current	I _{SM}				90	
Forward Voltage ^a	V _{SD}	I _F = 40 A, V _{GS} = 0 V		1.1	1.5	V
Reverse Recovery Time	t _{rr}	I _F = 40 A, di/dt = 100 A/μs		20	40	ns
Peak Reverse Recovery Current	I _{RM}			0.7	1.1	A
Reverse Recovery Charge	Q _{rr}			0.007	0.022	μC

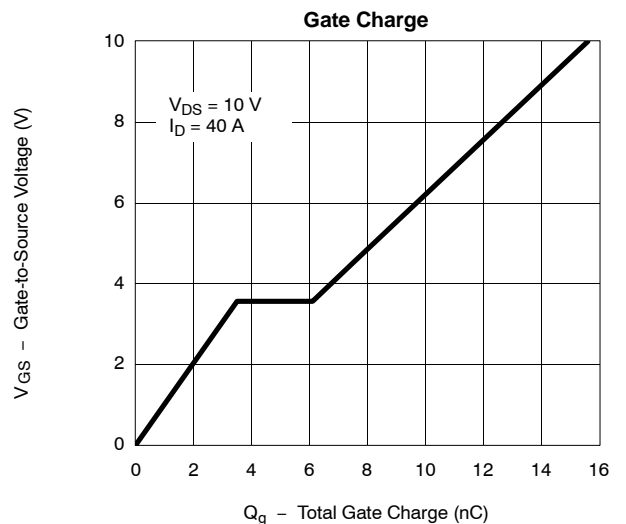
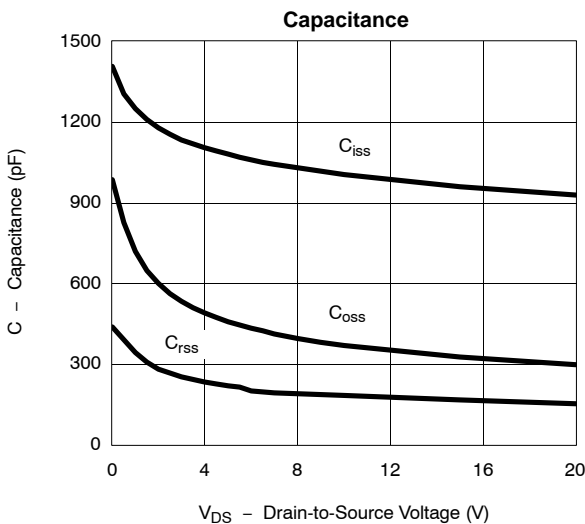
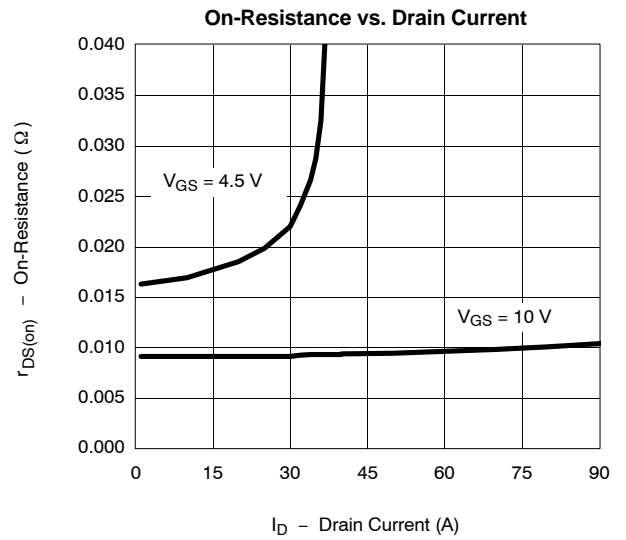
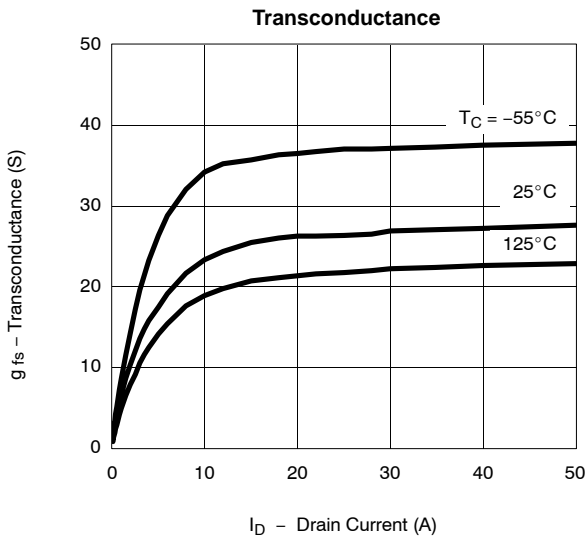
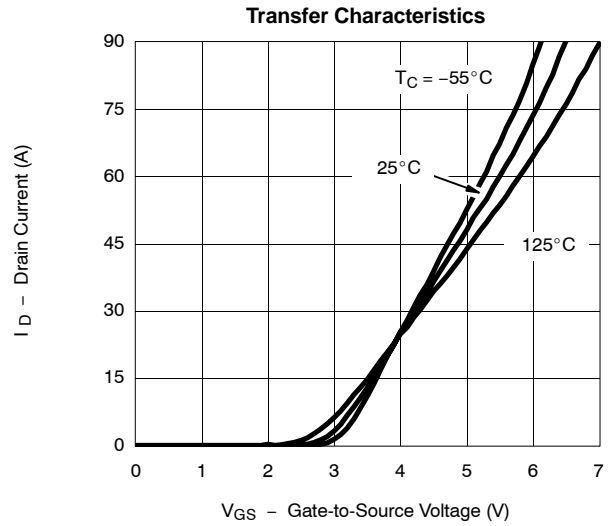
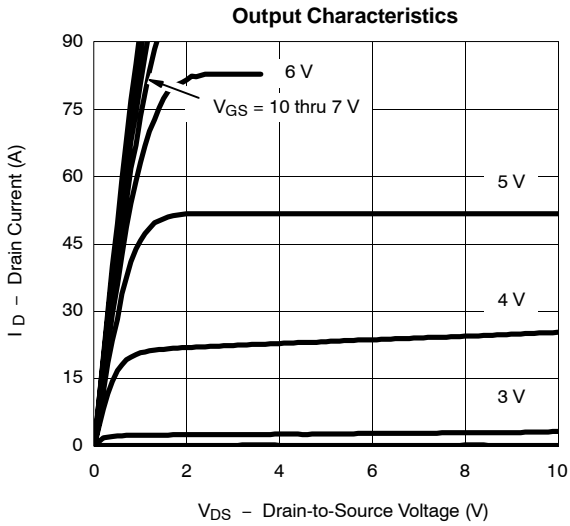
Notes

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- b. Independent of operating temperature.
- c. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

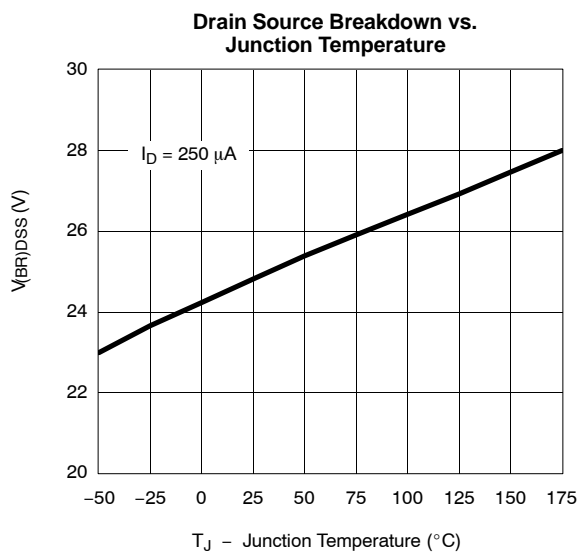
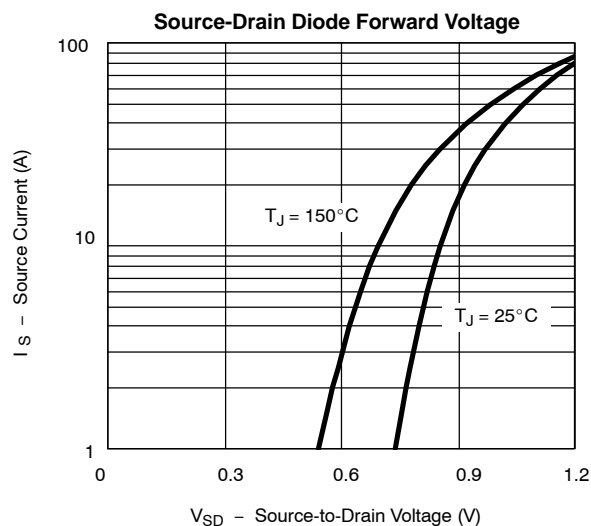
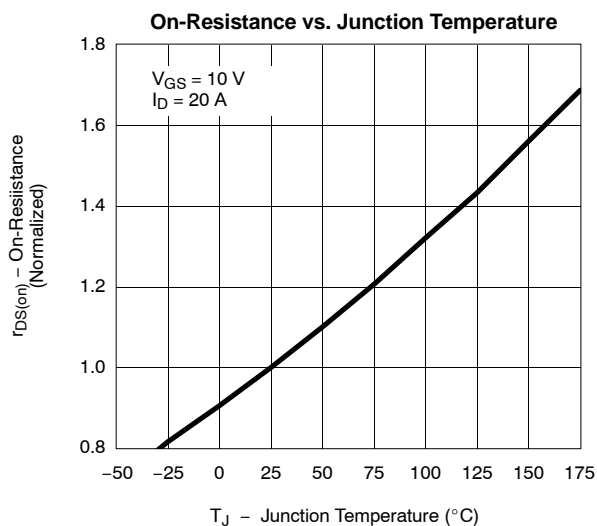


TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)





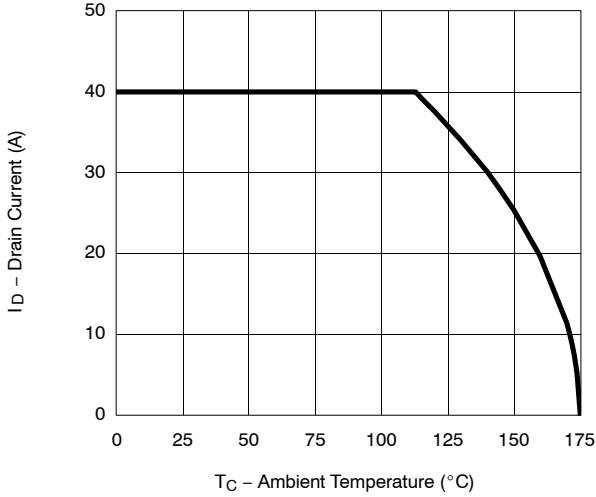
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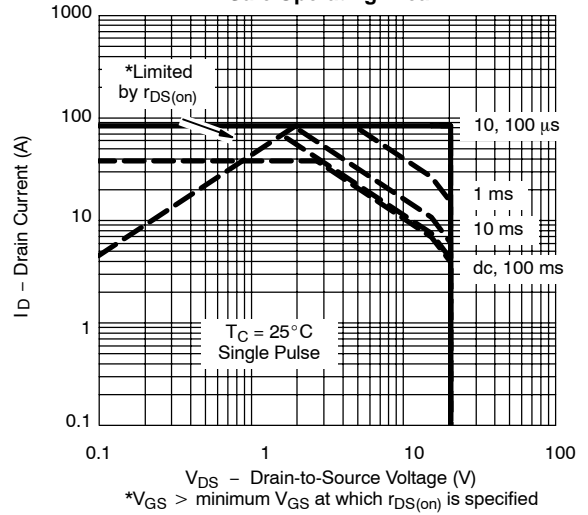


THERMAL RATINGS

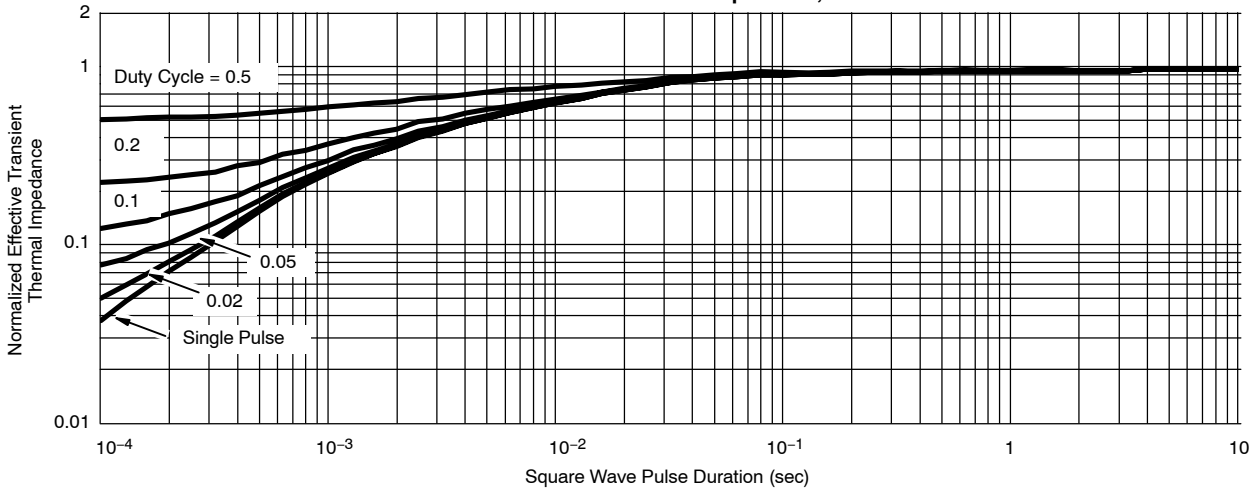
Maximum Avalanche and Drain Current vs. Case Temperature



Safe Operating Area



Normalized Thermal Transient Impedance, Junction-to-Case



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?72111>.