HARDWARE

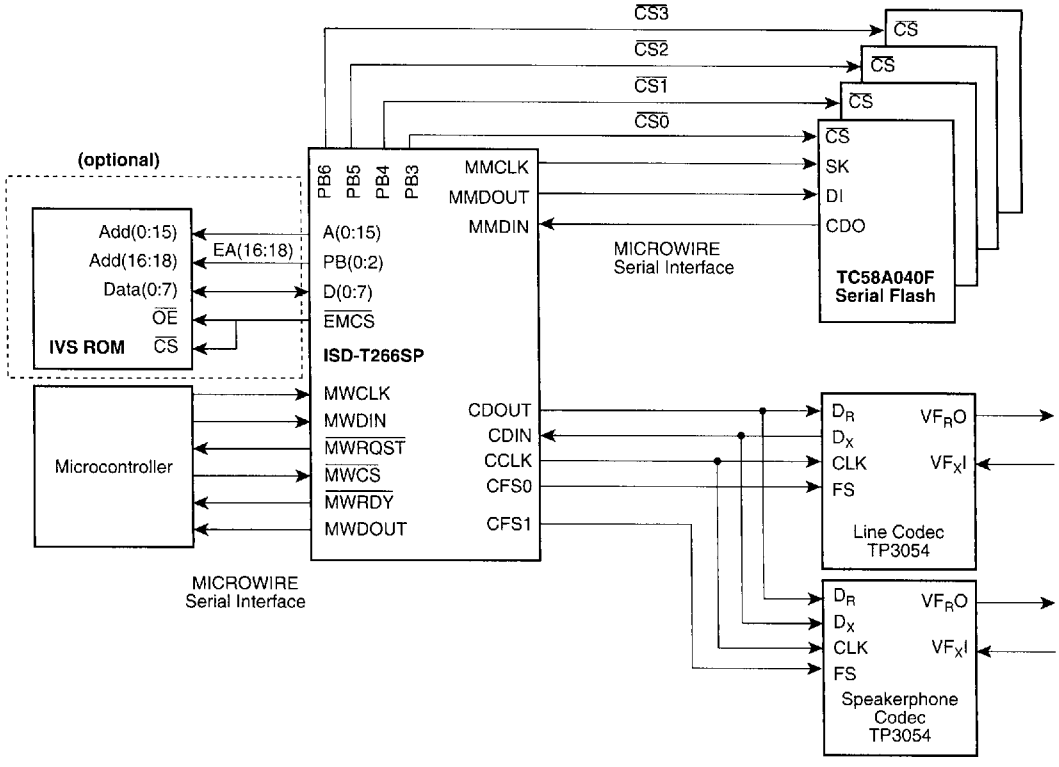


Figure 1-1. Block Diagram

PIN ASSIGNMENT

The following sections detail the pins of the ISD-T266SP processor. Slashes separate the names of signals that share the same pin.

Pin—Signal Assignment

Table 1-1 shows all the pins, and the signals that use them in different configurations. It also shows the type and direction of each signal.

Table 1-1. CompactSPEECH Pin—Signal Assignment

Pin Name	Type	Signal Name	I/O
A(0:15)	TTL	A(0:15)	Output
CCLK	TTL	CCLK	Output
CDIN	TTL	CDIN	Input
CDOUT	TTL	CDOUT	Output
CFS0	TTL	CFS0	Output

Table 1-1. CompactSPEECH Pin—Signal Assignment (Continued)

Pin Name	Type	Signal Name	I/O
CFS1	TTL	CFS1	Output
D(0:7)	TTL	D(0:7)	I/O
$\overline{\text{MWCS}}$	TTL[1]	$\overline{\text{MWCS}}$	Input
$\overline{\text{TST}}$	TTL	$\overline{\text{TST}}$	Input
$\overline{\text{MWRDY}}$	TTL	$\overline{\text{MWRDY}}$	Output
$\overline{\text{MWRQST}}$	TTL	$\overline{\text{MWRQST}}$	Output
MWDOUT	TTL	MWDOUT	Output
PB(0:2)[2]	TTL	EA(16:18)	Output
PB(3:6)[3]	TTL	CS(0:3)	Output
$\overline{\text{EMCS}}$/ENV0	TTL1[4] CMOS[5]	$\overline{\text{EMCS}}$ ENV0	Output Input
MWCLK	TTL	MWCLK	Input
MWDIN	TTL	MWDIN	Input
MMCLK	TTL1[d]	MMCLK	Output
MMDIN	TTL	MMDIN	Input
MMDOUT	TTL1[d]	MMDOUT	Output
$\overline{\text{RESET}}$	Schmitt[a]	$\overline{\text{RESET}}$	Input
V_{CC}	Power	V_{CC}	
V_{SS}	Power	V_{SS}	
X1	XTAL	X1	OSC
X2/CLKIN	XTAL TTL	X2 CLKIN	OSC Input

1. Schmitt trigger input.
2. Virtual address lines for IVS ROM.
3. Chip select lines for Serial Flash devices.
4. TTL1 output signals provide CMOS levels in the steady state, for small loads.
5. Input during reset, CMOS level input.

Pin Assignment in the 68-PLCC Package

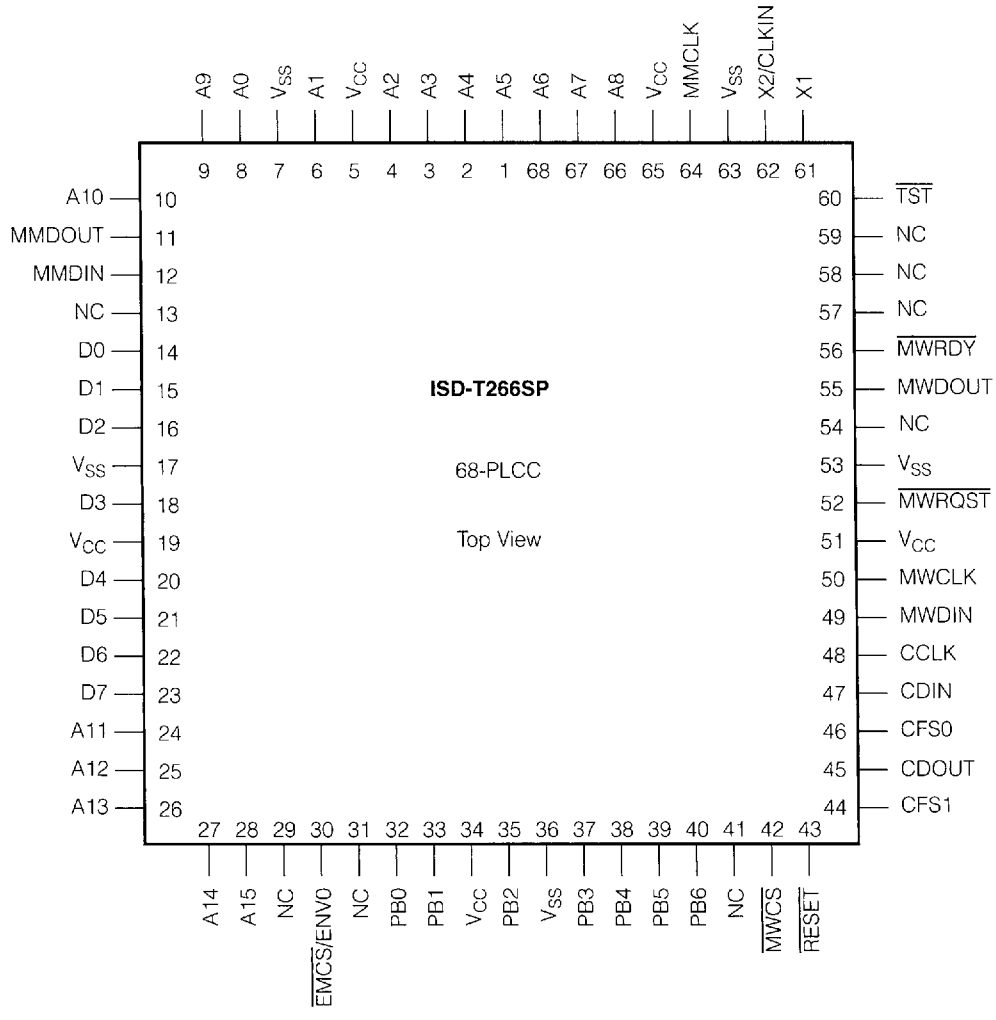


Figure 1-2. 68-PLCC Package Connection Diagram

NOTE: *Pins marked NC should not be connected.*

Pin Assignment in the 100-PQFP Package

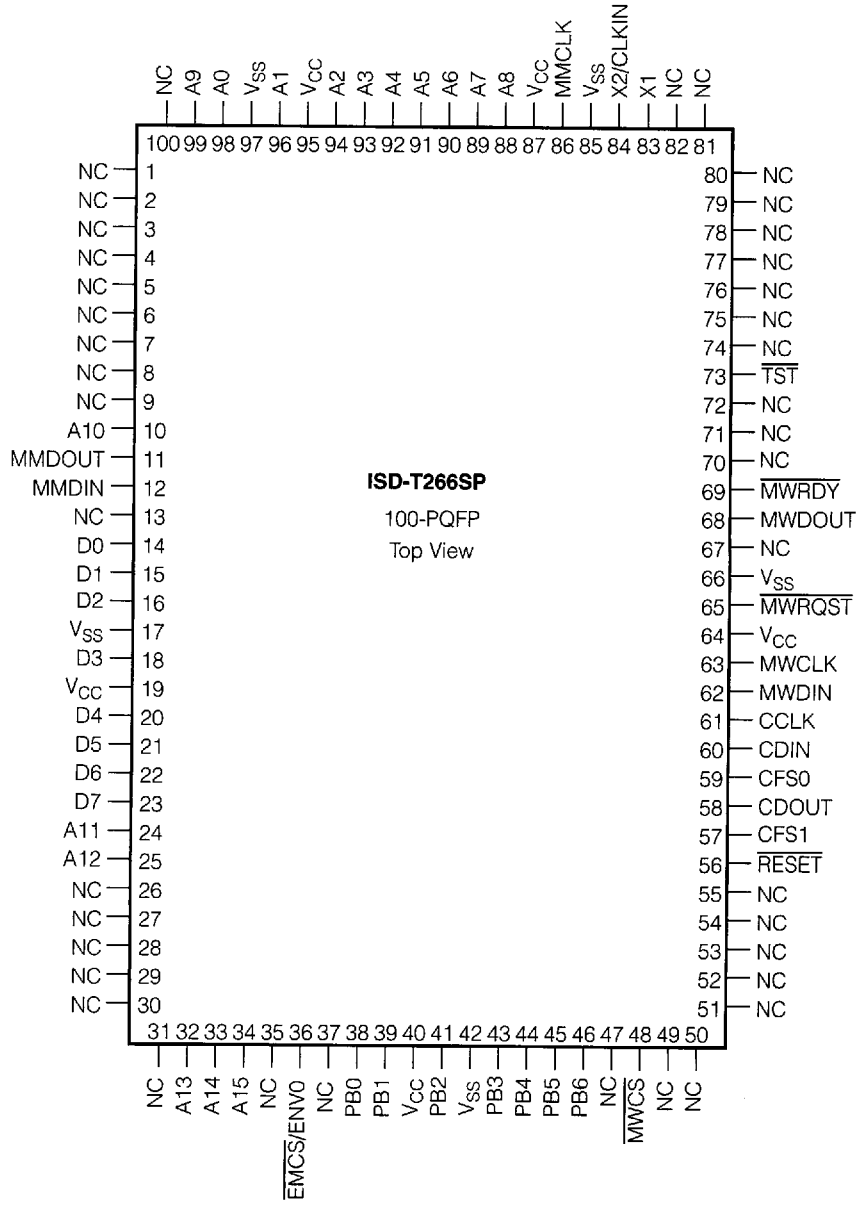


Figure 1-3. 100-PQFP Package Connection Diagram

NOTE: *Pins marked NC should not be connected.*

FUNCTIONAL DESCRIPTION

This section provides details of the functional characteristics of the CompactSPEECH processor. It is divided into the following sections:

- Resetting
- Clocking
- Power-down mode
- Power and grounding
- Memory interface
- Codec interface

Resetting

The $\overline{\text{RESET}}$ pin is used to reset the CompactSPEECH processor.

On application of power, $\overline{\text{RESET}}$ must be held low for at least t_{pwr} after V_{CC} is stable. This ensures that all on-chip voltages are completely stable before operation. Whenever $\overline{\text{RESET}}$ is applied, it must also remain active for not less than t_{RST}. During this period, and for 100 µs after, the $\overline{\text{TST}}$ signal must be high. This can be done with a pull-up resistor on the $\overline{\text{TST}}$ pin.

The value of $\overline{\text{MWRDY}}$ is undefined during the reset period, and for 100 µs after. The microcontroller should either wait before polling the signal for the first time, or the signal should be pulled high during this period.

Upon reset, the ENV0 signal is sampled to determine the operating environment. During reset, the $\overline{\text{EMCS}}$/ENV0 pin is used for the ENV0 input signals. An internal pull-up resistor sets ENV0 to 1.

After reset, the same pin is used for $\overline{\text{EMCS}}$.

System Load on ENV0

For any load on the ENV0 pin, the voltage should not drop below V_{ENVh}.

If the load on the ENV0 pin causes the current to exceed 10 µA, use an external pull-up resistor to keep the pin at 1.

Figure 1-4 shows a recommended circuit for generating a reset signal when the power is turned on.

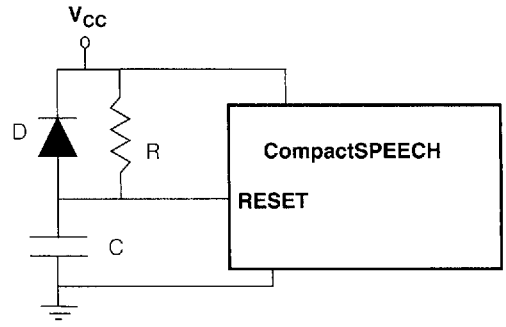


Figure 1-4. Recommended Power-On Reset Circuit

Clocking

The CompactSPEECH processor provides an internal oscillator that interacts with an external clock source through the X1 and X2/CLKIN pins. Either an external single-phase clock signal, or a crystal oscillator, may be used as the clock source.

External Single-phase Clock Signal

If an external single-phase clock source is used, it should be connected to the CLKIN signal as shown in Figure 1-5, and should conform to the voltage-level requirements for CLKIN stated in .

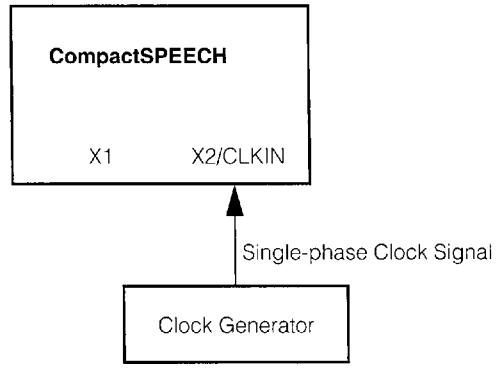


Figure 1-5. External Clock Source

Crystal Oscillator

A crystal oscillator is connected to the on-chip oscillator circuit via the X1 and X2 signals, as shown in Figure 1-6.

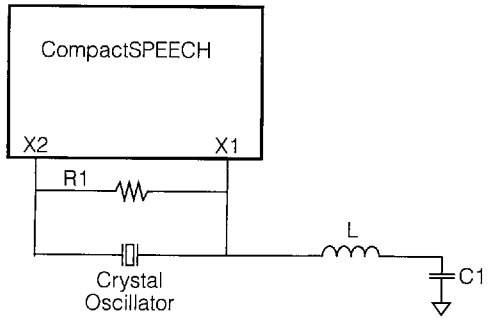


Figure 1-6. Connections for an External Crystal Oscillator

Keep stray capacitance and inductance, in the oscillator circuit, as low as possible. The crystal resonator, and the external components, should be as close to the X1 and X2/CLKIN pins as possible, to keep the trace lengths in the printed circuit to an absolute minimum.

You can use crystal oscillators with maximum load capacitance of 20 pF, although the oscillation frequency may differ from the crystal's specified value.

Table 1-2 lists the components in the crystal oscillator circuit.

Table 1-2. Crystal Oscillator Component List

Component	Parameters	Values	Tolerance
Crystal Oscillator	Resonance Frequency Third Overtone Type Maximum Serial Resistance Maximum Shunt Capacitance Maximum Load Capacitance	40.96 MHz Parallel AT-Cut 50 Ω 7 pF 12 pF	N/A
Resistor R1		10 MΩ	5%
Capacitor C1		1000 pF	20%
Inductor L		3.9 µH	10%

Power-down Mode

Power-down mode is useful during a power failure, when the power source for the CompactSPEECH processor is a backup battery, or in battery powered devices, while the CompactSPEECH processor is idle.

In power-down mode, the clock frequency of the CompactSPEECH processor is reduced, and some of the processor modules are deactivated. As a result, the CompactSPEECH processor consumes much less power than in normal-power mode (less than 1.5 mA). Although the CompactSPEECH processor does not perform all its usual functions in power-down mode, it still keeps stored messages and maintains the time and day.

NOTE *In power-down mode all the chip select signals, CS0 to CS3, are set to 1. To guarantee that there is no current flow from these signals to the Serial Flash devices, the power supply to these devices must not be disconnected.*

The CompactSPEECH processor stores messages, and all memory management information, in flash memory. Thus, there is no need to maintain the power to the processor to preserve stored messages. If the microcontroller's real-time clock (and *not* the CompactSPEECH processor's real-time clock) is used to maintain the time and day, neither the flash nor the CompactSPEECH processor require battery backup during power failure. In this case, when returning to normal mode, the microcontroller should perform the initialization sequence, as described in "Initialization" on page 2–17, and use the SETD command to set the time and day.

To keep power consumption low in power-down mode, the $\overline{\text{RESET}}$, $\overline{\text{MWCS}}$, MWCLK and MWDIN signals should be held above V_{CC} – 0.5V or below V_{SS} + 0.5V.

The PDM (Go To Power-down Mode) command switches the CompactSPEECH processor to power-down mode. (For an explanation of the CompactSPEECH processor commands, see "Command Description" on page 2–22.) It may only be issued when the CompactSPEECH processor is in the **IDLE** state. (For an explanation of the CompactSPEECH processor states, see "The State Machine" on page 2–4.) If it is necessary to switch to power-down mode from any other state, the controller must first issue an S command to switch the CompactSPEECH processor to the **IDLE** state, and then issue the PDM command. Sending any command while in power-down mode resets the CompactSPEECH processor detectors, and returns the CompactSPEECH processor to normal operation mode.

NOTE *Entering or exiting power-down mode can distort the real-time clock by up to 500 µs. Thus, to maintain the accuracy of the real-time clock, enter or exit the power-down mode as infrequently as possible.*

Power and Grounding

The CompactSPEECH processor requires a single 5V power supply, applied to the V_{CC} pins.

The grounding connections are made on the GND pins.

For optimal noise immunity, the power and ground pins should be connected to V_{CC} and the ground planes, respectively, on the printed circuit board. If V_{CC} and the ground planes are not used, single conductors should be run directly from each V_{CC} pin to a power point, and from each GND pin to a ground point. Avoid daisy-chained connections.

Use decoupling capacitors to keep the noise level to a minimum. Attach standard 0.1 µF ceramic capacitors to the V_{CC} and GND pins, as close as possible to the CompactSPEECH processor.

When you build a prototype, using wire-wrap or other methods, solder the capacitors directly to the power pins of the CompactSPEECH processor socket, or as close as possible, with very short leads.

Memory Interface

Serial Flash Interface

The CompactSPEECH processor supports up to four Toshiba's TC58A040F 4-Mbit Serial Flash memory devices for storing messages.

TC58A040F

The TC58A040F is organized as 128 blocks of 128 pages, each containing 32 bytes. A block is the smallest unit that can be erased, and is 4 Kbytes in size.

Not all 128 blocks are available for recording. Up to 10 blocks may contain bad bits, and one block is write-once and holds the locations of these unusable blocks.

For further information about Toshiba's TC58A040F, see the TC58A040F Datasheet.

Message Organization and Recording Time

A CompactSPEECH processor message uses at least one block.

The number of messages that can be stored on one TC58A040F device is 117 to 127 depending on the number of bad blocks.

The maximum recording time depends on four factors:

1. The basic compression rate (5.2 Kbit/s or 7.3 Kbit/s).
2. The amount of silence in the recorded speech.
3. The number of bad blocks.
4. The number of recorded messages. (The basic memory allocation unit for a message is a 4-Kbyte block, which means that half a block on average is wasted per recorded message)

Assuming a single message recorded in all the available memory space of a 4-Mbit device with no bad blocks, the maximum recording time using 5.2 Kbit/s compression is as follows:

Table 1-3. Recording Time on a 4-Mbit Device

Silence	Total Recording Time
0	13 minutes and 9 seconds
10%	14 minutes and 25 seconds
15%	15 minutes and 7 seconds
20%	15 minutes and 47 seconds
25%	16 minutes and 25 seconds

Serial Flash Endurance

The Serial Flash may be erased up to 100,000 times. To reduce the effect of this limitation, the memory manager utilizes the Serial Flash's blocks evenly, i.e., each block is erased more or less the same number of times, to ensure that all blocks have the same lifetime.

Consider the following extensive usage of all the TC58A040F's blocks:

1. Record 15 minutes of messages (until the memory is full).
2. Playback 15 minutes (all the recorded messages).
3. Delete all messages.

Assuming a TC58A040F device is used in this manner 24 times a day, its expected lifetime is:

Flash Lifetime = 100,000 / (24 * 365) = 11.4 years

Thus the TC58A040F device will last for over ten years, even when used for twelve hours of recording per day.

Note, that if an TC58A040F device is used, then, under the same conditions, it will last for more than 20 years.

ROM Interface

IVS vocabularies can be stored in either Serial Flash and/or ROM. The CompactSPEECH processor supports IVS ROM devices through Expansion Memory. Up to 64 Kbytes (64K × 8) of Expansion Memory are supported directly. Nevertheless, the CompactSPEECH processor uses bits of the on-chip port (PB) to further extend the 64 Kbytes address space up to 0.5 Mbytes address space.

ROM is connected to the CompactSPEECH processor using the data bus, D(0:7), the address bus, A(0:15), the extended address signals, EA(16:18), and Expansion Memory Chip Select, $\overline{\text{EMCS}}$, controls. The number of extended address pins to use may vary, depending on the size and configuration of the ROM.

Reading from Expansion Memory

An Expansion Memory read bus-cycle starts at T1, when the data bus is in TRI-STATE, and the address is driven on the address bus. $\overline{EMCS}$ is asserted (cleared to 0) on a T2W1 cycle. This cycle is followed by three T2W cycles and one T2 cycle. The CompactSPEECH processor samples data at the end of the T2 cycle.

The transaction is terminated at T3, when $\overline{EMCS}$ becomes inactive (set to 1). The address remains valid until T3 is complete. A T3H cycle is added after the T3 cycle. The address remains valid until the end of T3H.

Codec Interface

The CompactSPEECH processor provides an on-chip interface to two serial codecs. This interface supports codec operation in long or short-frame formats. The format is selected with the CFG command.

The codec interface uses five signals CDIN, CDOUT, CCLK, CFS0 and CFS1.

The CDIN input pin and the CDOUT, CCLK and CFS0 output pins are connected to the first codec. The second codec is connected to CDIN, CDOUT, CCLK and the CFS1 output pin.

Data is transferred to the codec through the CDOUT pin. Data is read from the codec through the CDIN pin.

Short Frame Protocol

When short frame protocol is configured, eight data bits are exchanged with each codec in each frame, i.e., CFS0 cycle.

Data transfer starts when CFS0 is set to 1 for one CCLK cycle. The data is then transmitted, bit-by-bit, via the CDOUT output pin. Concurrently, the received data is shifted in via the CDIN input pin. Data is shifted one bit in each CCLK cycle.

After the last bit has been shifted, CFS1 is set to 1 for one CCLK cycle. Then, the data from the second codec is shifted out via CDOUT, concurrently with the inward shift of the data received via CDIN.

Figure 1-7 shows how the codec interface signals behave when short frame protocol is configured.

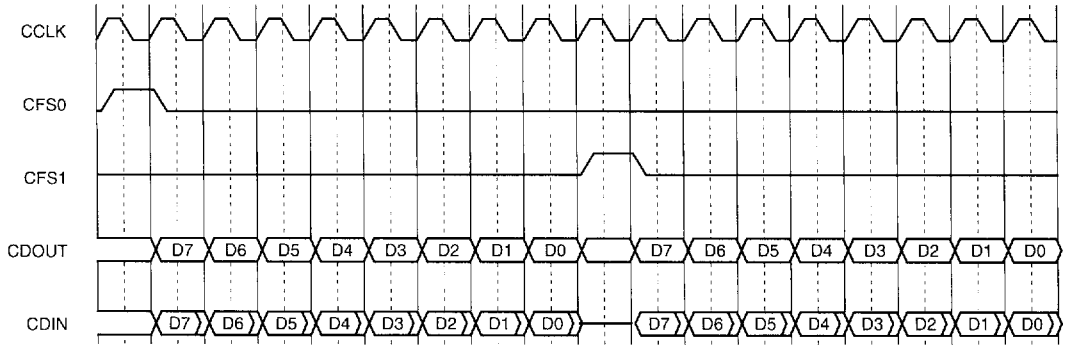


Figure 1-7. Codec Protocol—Short Frame

Long Frame Protocol

When long frame protocol is configured, eight data bits are exchanged with each codec, as for the short frame protocol. However, for the long frame protocol, data transfer starts by setting CFS0 to 1 for eight CCLK cycles.

Simultaneously, the data for the first codec is shifted out bit-by-bit, via the CDOUT output pin, as in short frame protocol. Concurrently, the received data is shifted in through the CDIN input. The data is shifted one bit in each CCLK cycle.

One CCLK cycle after CFS0 has become inactive (0), CFS1 is set to 1, for eight CCLK cycles. Simultaneously, the data for the second codec is shifted out, MSB first, via CDOUT, concurrently with the received data shifted in from CDIN.

Figure 1-8 shows how the codec interface signals behave when long frame protocol is configured.

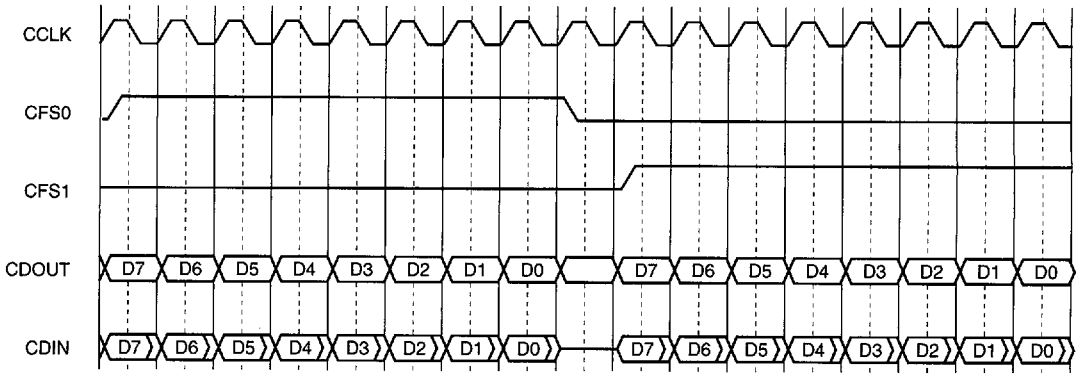


Figure 1-8. Codec Protocol—Long Frame

SPECIFICATIONS

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact ISD for availability and specifications.

Storage temperature	–65°C to +150°C
Temperature under bias	0°C to + 70°C
All input or output voltages, with respect to GND	–0.5V to + 6.5V

NOTE *Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to the conditions specified below.*

Electrical Characteristics

T_A = 0°C to +70°C, V_{CC} = 5V ±10%, GND = 0V

Table 1-4. Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{IH}	TTL Input, Logical 1 Input Voltage		2.0		V_{CC} + 0.5	V
V_{IL}	TTL Input, Logical 0 Input Voltage		–0.5		0.8	V
V_{XH}	CLKIN Input, High Voltage	External Clock	2.0			V
V_{XL}	CLKIN Input, Low Voltage	External Clock			0.8	V

Table 1-4. Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{ENVh}	ENV0 High Level, Input Voltage		3.6			V
V_{Hh}	CMOS Input with Hysteresis, Logical 1 Input Voltage		3.6			V
V_{Hl}	CMOS Input with Hysteresis, Logical 0 Input Voltage				1.1	V
V_{Hys}	Hysteresis Loop Width[1]		0.5			V
V_{OH}	Logical 1 TTL, Output Voltage	I_{OH} = –0.4 mA	2.4			V
V_{OHWC}	MMCLK, MMDOUT and $\overline{EMCS}$ Logical 1, Output Voltage	I_{OH} = –0.4 mA	2.4			V
		I_{OH} = –50 µA[2]	V_{CC} –0.2			V
V_{OL}	Logical 0, TTL Output Voltage	I_{OL} = 4 mA			0.45	V
		I_{OL} = 50 µA [b]			0.2	V
V_{OLWC}	MMCLK, MMDOUT and $\overline{EMCS}$ Logical 0, Output Voltage	I_{OL} = 4 mA			0.45	V
		I_{OL} = 50 µA[2]			0.2	V
I_L	Input Load Current[3]	$0V \le V_{IN} \le V_{CC}$	–5.0		5.0	µA
I_O (Off)	Output Leakage Current (I/O pins in Input Mode) [3]	$0V \le V_{OUT} \le V_{CC}$	–5.0		5.0	µA
I_{CC1}	Active Supply Current	Normal Operation Mode, Running Speech Applications[4]		65.0	80.0	mA
I_{CC2}	Standby supply current	Normal Operation Mode, DSPM Idle[4]		40.0		mA
I_{CC3}	Power-down Mode Supply Current	Power-down Mode[4, 5]			1.5	mA
C_X	X1 and X2 Capacitance[1]			17.0		pF

1. *Guaranteed by design.*
2. *Measured in power-down mode. The total current driven, or sourced, by all the CompactSPEECH processor's output signals is less than 50 µA.*
3. *Maximum 20 µA for all pins together.*
4. *I_{OUT} = 0, T_A = 25°C, V_{CC} = 5V, operating from a 40.96 MHz crystal, and running from internal memory with Expansion Memory disabled.*
5. *All input signals are tied to 1 or 0 (above V_{CC}–0.5V or below V_{SS}+0.5V).*

Switching Characteristics

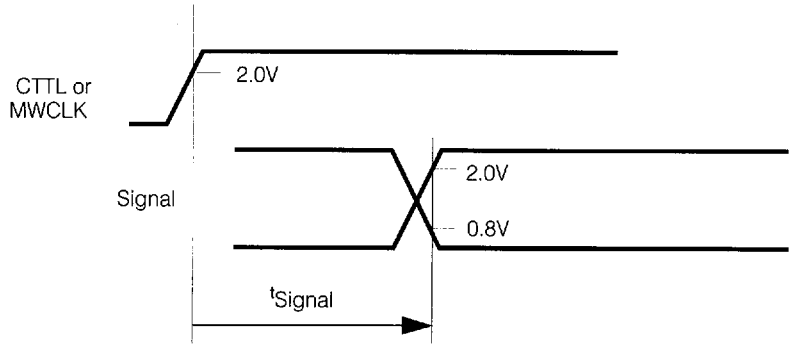
Definitions

All timing specifications in this section refer to 0.8V or 2.0V on the rising or falling edges of the signals, as illustrated in Figures 1-9 through 1-15, unless specifically stated otherwise.

Maximum times assume capacitive loading of 50 pF.

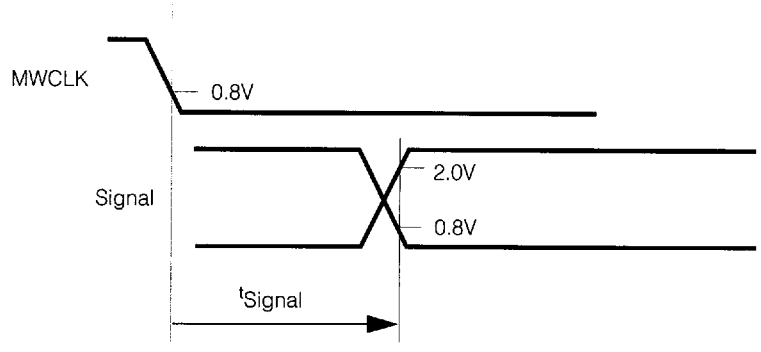
CLKIN crystal frequency is 40.96 MHz.

NOTE *CTTL is an internal signal and is used as a reference to explain the timing of other signals. See Figure 1-23.*



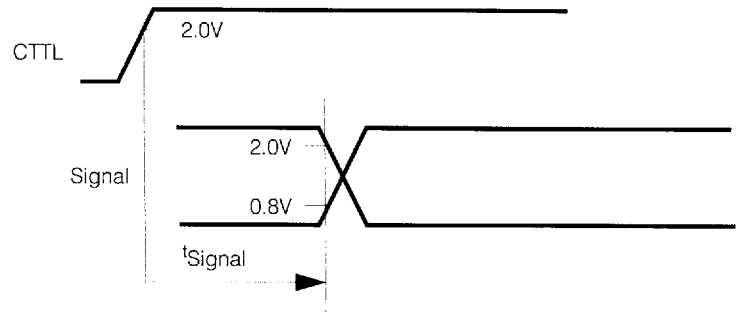
Signal valid, active or inactive time, after a rising edge of CTTL or MWCLK.

Figure 1-9. Synchronous Output Signals (Valid, Active and Inactive)



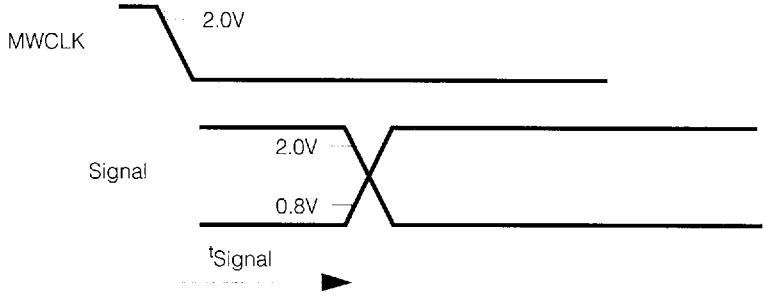
Signal valid time, after a falling edge of MWCLK.

Figure 1-10. Synchronous Output Signals (Valid)



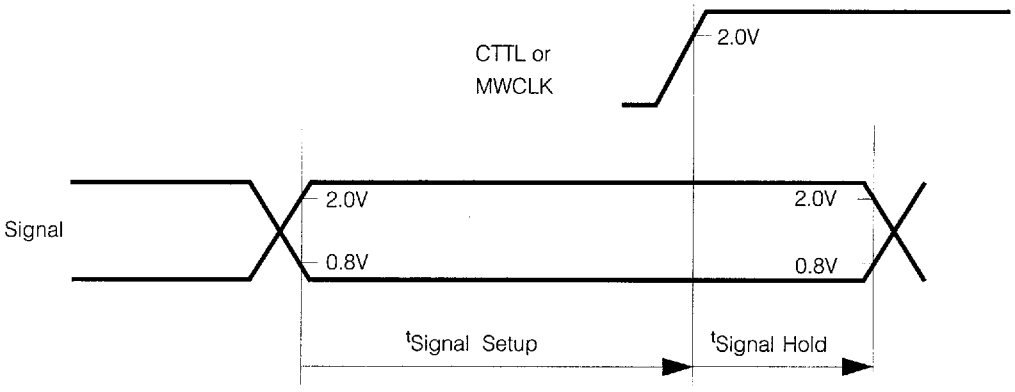
Signal hold time, after a rising edge of CTTL.

Figure 1-11. Synchronous Output Signals (Hold)



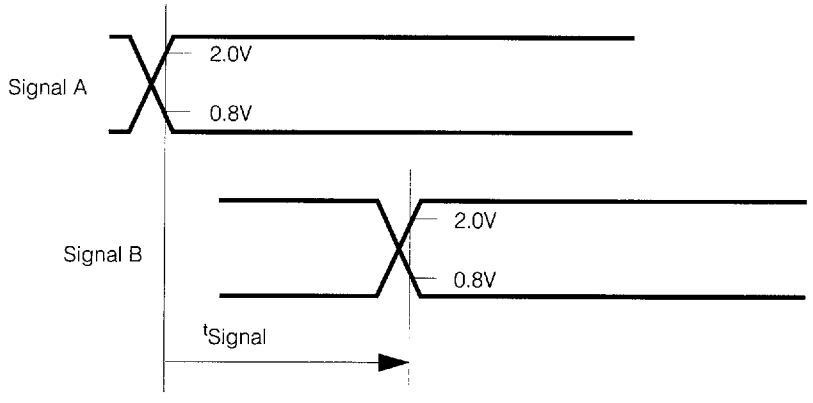
Signal hold time, after a falling edge of MWCLK.

Figure 1-12. Synchronous Output Signals (Hold)



Signal setup time, before a rising edge of CTTL or MWCLK, and signal hold time after a rising edge of CTTL or MWCLK.

Figure 1-13. Synchronous Input Signals



Signal B starts after rising or falling edge of signal A.

Figure 1-14. Asynchronous Signals

The $\overline{\text{RESET}}$ signal has a Schmitt trigger input buffer. Figure 1-15 shows the characteristics of the input buffer.

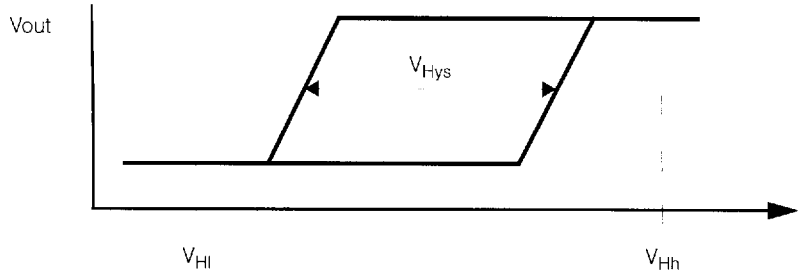


Figure 1-15. Hysteresis Input Characteristics

Synchronous Timing Tables

In this section, R.E. means Rising Edge and F.E. means Falling Edge.

Output Signals

Table 1-5. Output Signals

Symbol	Figure	Description	Reference Conditions	Min (ns)	Max (ns)
t_{Ah}	1-18	Address Hold	After R.E. CTTL	0.0	
t_{Av}	1-18	Address Valid	After R.E. CTTL, T1		12.0
t_{CCLKa}	1-16	CCLK Active	After R.E. CTTL		12.0
t_{CCLKh}	1-16	CCLK Hold	After R.E. CTTL	0.0	
t_{CCLKia}	1-16	CCLK Inactive	After R.E. CTTL		12.0
t_{CDOh}	1-16	CDOUT Hold	After R.E. CTTL	0.0	
t_{CDOv}	1-16	CDOUT Valid	After R.E. CTTL		12.0
t_{CTp}	1-23	CTTL Clock Period[1]	R.E. CTTL to next R.E. CTTL	48.8	50,000
t_{EMCSa}	1-18	$\overline{\text{EMCS}}$ Active	After R.E. CTTL, T2W1		12.0
t_{EMCSh}	1-18	$\overline{\text{EMCS}}$ Hold	After R.E. CTTL	0.0	
t_{EMCSia}	1-18	$\overline{\text{EMCS}}$ Inactive	After R.E. CTTL T3		12.0
t_{FSa}	1-16	CFS0 and CFS1 Active	After R.E. CTTL		25.0
t_{FSh}	1-16	CFS0 and CFS1 Hold	After R.E. CTTL	0.0	
t_{FSia}	1-16	CFS0 and CFS1 Inactive	After R.E. CTTL		25.0
t_{MMCLKa}	1-21	Master MICROWIRE Clock Active	After R.E. CTTL		12.0

Table 1-5. Output Signals

Symbol	Figure	Description	Reference Conditions	Min (ns)	Max (ns)
t_{MMCLKh}	1-21	Master MICROWIRE Clock Hold	After R.E. CTTL	0.0	
$t_{MMCLKia}$	1-21	Master MICROWIRE Clock Inactive	After R.E. CTTL		12.0
t_{MMDOh}	1-21	Master MICROWIRE Data Out Hold	After R.E. CTTL	0.0	
t_{MMDOv}	1-21	Master MICROWIRE Data Out Valid	After R.E. CTTL		12.0
t_{MWDOf}	1-19	MICROWIRE Data Float[2]	After R.E. $\overline{MWCS}$		70.0
t_{MWDOh}	1-19	MICROWIRE Data Out Hold[2]	After F.E. MWCK	0.0	
t_{MWDOnf}	1-19	MICROWIRE Data No Float[2]	After F.E. $\overline{MWCS}$	0.0	70.0
t_{MWDOv}	1-19	MICROWIRE Data Out Valid[2]	After F.E. MWCK		70.0
t_{MWITOp}	1-20	MWDIN to MWDOUT	Propagation Time		70.0
t_{MWRDYa}	1-19	$\overline{MWRDY}$ Active	After R.E. of CTTL	0.0	35.0
$t_{MWRDYia}$	1-19	$\overline{MWRDY}$ Inactive	After F.E. MWCLK	0.0	70.0
t_{PABCh}	1-22	PB and $\overline{MWRQST}$	After R.E. CTTL	0.0	
t_{PABCv}	1-22	PB and $\overline{MWRQST}$	After R.E. CTTL, T2W1		12.0

1. In normal operation mode t_{CTp} must be 48.8 ns; in power-down mode, t_{CTp} must be 50,000 ns.
2. Guaranteed by design, but not fully tested.

Input Signals

Table 1-6. Input Signals

Symbol	Figure	Description	Reference Conditions	Min (ns)
t_{CDIh}	1-16	CDIN Hold	After R.E. CTTL	0.0
t_{CDIs}	1-16	CDIN Setup	Before R.E. CTTL	11 0
t_{DIh}	1-18	Data in Hold (D0:7)	After R.E. CTTL T1, T3 or TI	0.0
t_{DIs}	1-18	Data in Setup (D0:7)	Before R.E. CTTL T1, T3 or TI	15.0
t_{MMDINh}	1-21	Master MICROWIRE Data In Hold	After R.E. CTTL	0.0
t_{MMDINs}	1-21	Master MICROWIRE Data In Setup	Before R.E. CTTL	11.0
t_{MWCKh}	1-19	MICROWIRE Clock High (slave)	At 2.0V (both edges)	100.0

Table 1-6. Input Signals

Symbol	Figure	Description	Reference Conditions	Min (ns)
t_{MWCKl}	1-19	MICROWIRE Clock Low (slave)	At 0.8V (both edges)	100.0
t_{MWCKp}	1-19	MICROWIRE Clock Period (slave)[1]	R.E. MWCLK to next R.E. MWCLK	2.5 µs
t_{MWCLKh}	1-19	MWCLK Hold	After $\overline{MWCS}$ becomes inactive	50.0
t_{MWCLKs}	1-19	MWCLK Setup	Before $\overline{MWCS}$ becomes active	100.0
t_{MWCSh}	1-19	$\overline{MWCS}$ Hold	After F.E. MWCLK	50.0
t_{MWCSs}	1-19	$\overline{MWCS}$ Setup	Before R.E. MWCLK	100.0
t_{MWDIh}	1-19	MWDIN Hold	After R.E. MWCLK	50.0
t_{MWDIs}	1-19	MWDIN Setup	Before R.E. MWCLK	100.0
t_{PWR}	1-25	Power Stable to $\overline{RESET}$ R.E.[2]	After V_{CC} reaches 4.5V	30.0 ms
t_{RSTw}	1-24	$\overline{RESET}$ Pulse Width	At 0.8V (both edges)	10.0 ms
t_{Xh}	1-23	CLKIN High	At 2.0V (both edges)	$t_{X1p}/2 - 5$
t_{Xl}	1-23	CLKIN Low	At 0.8V (both edges)	$t_{X1p}/2 - 5$
t_{Xp}	1-23	CLKIN Clock Period	R.E. CLKIN to next R.E. CLKIN	24.4

1. Guaranteed by design, but not fully tested in power-down mode.
2. Guaranteed by design, but not fully tested.

Timing Diagrams

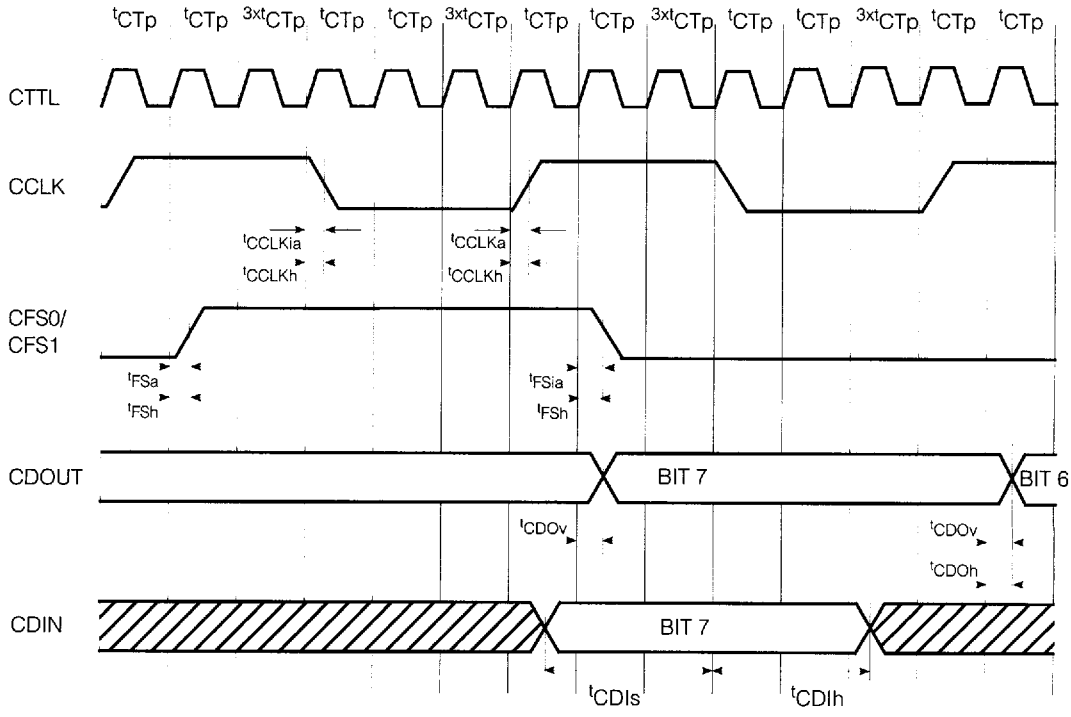


Figure 1-16. Codec Short Frame Timing

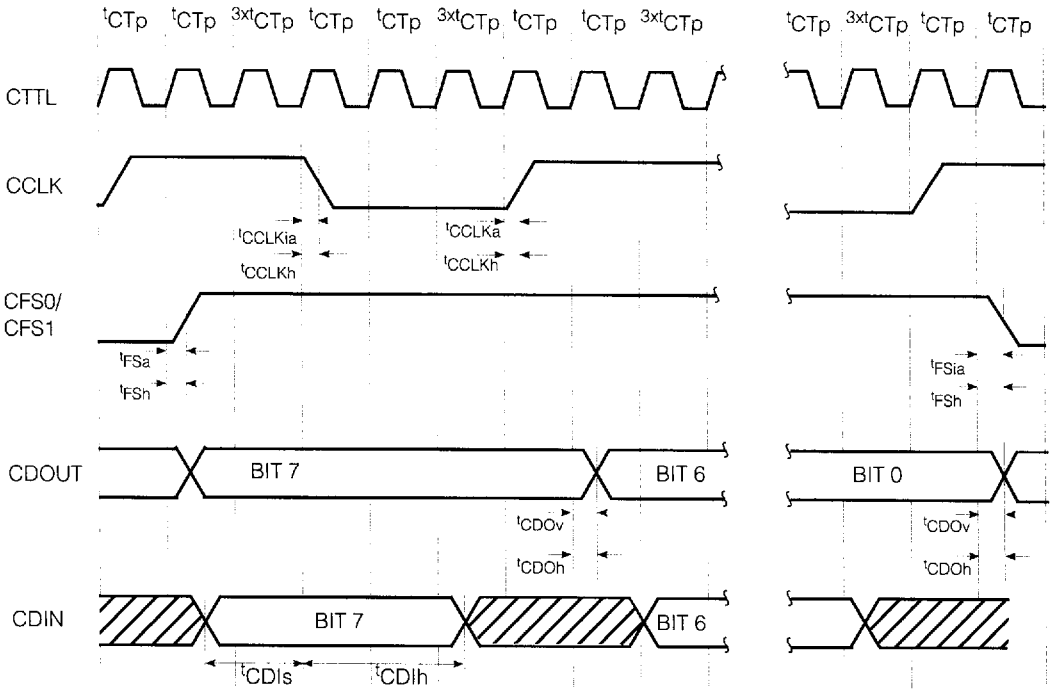
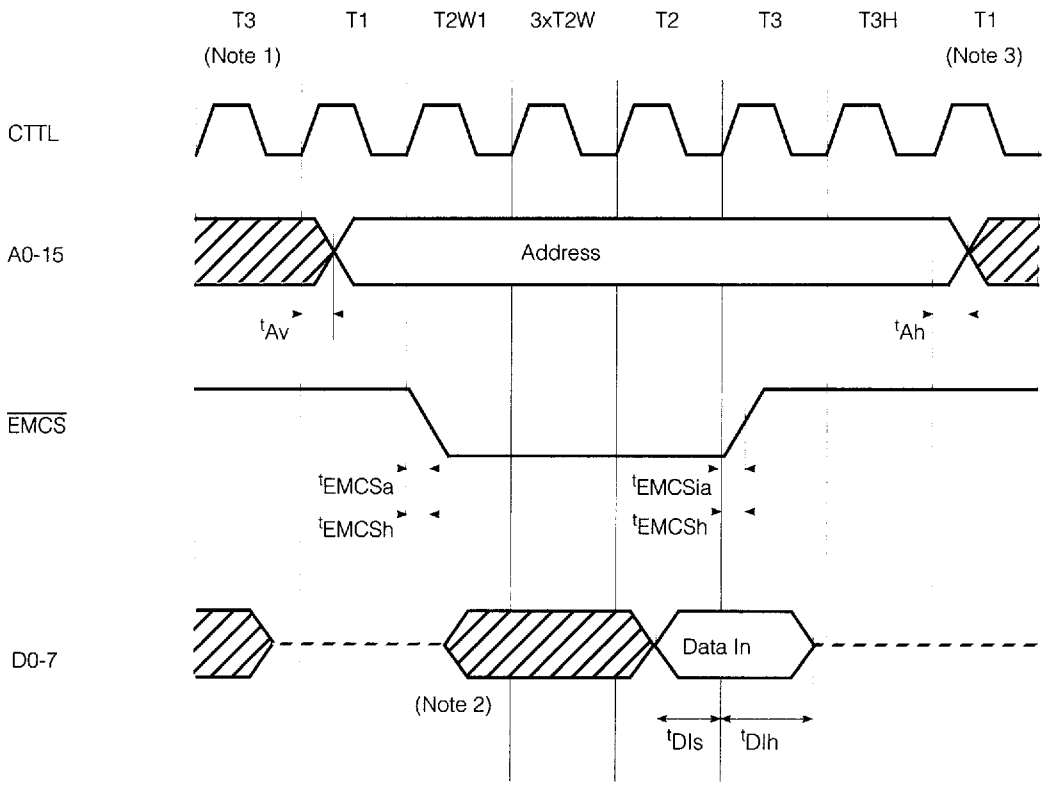


Figure 1-17. Codec Long Frame Timing



NOTES: *1. This cycle may be either TI (Idle), T3 or T3H.*
2. Data can be driven by an external device at T2W1, T2W, T2 and T3.
3. This cycle may be either TI (Idle) or T1.

Figure 1-18. ROM Read Cycle Timing

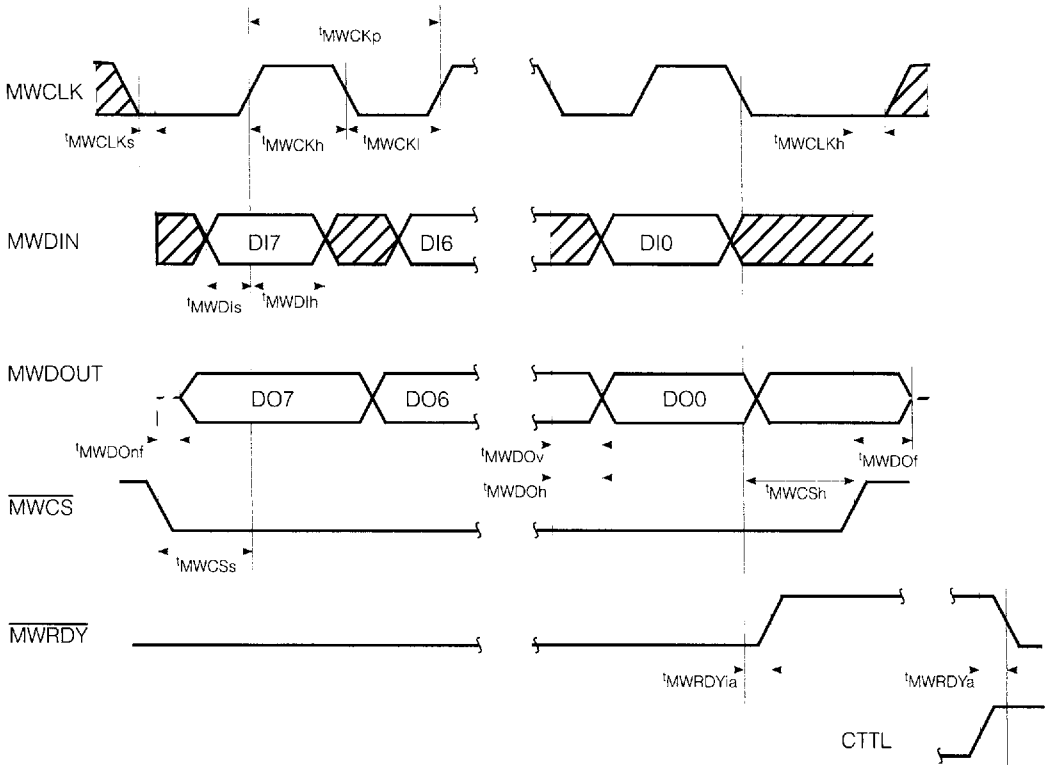


Figure 1-19. MICROWIRE Transaction Timing—Data Transmitted to Output

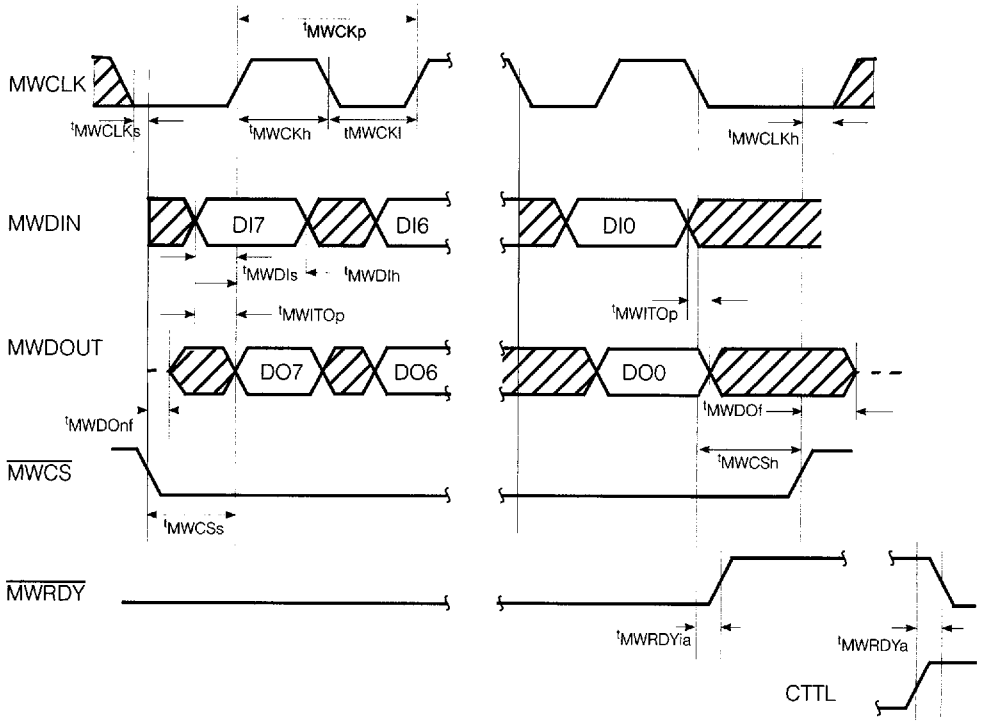


Figure 1-20. MICROWIRE Transaction Timing—Data Echoed to Output

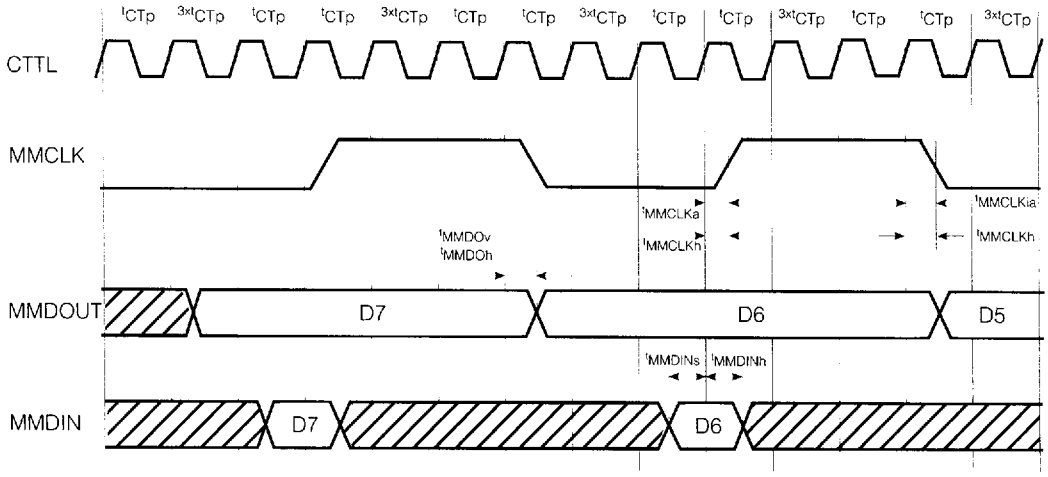
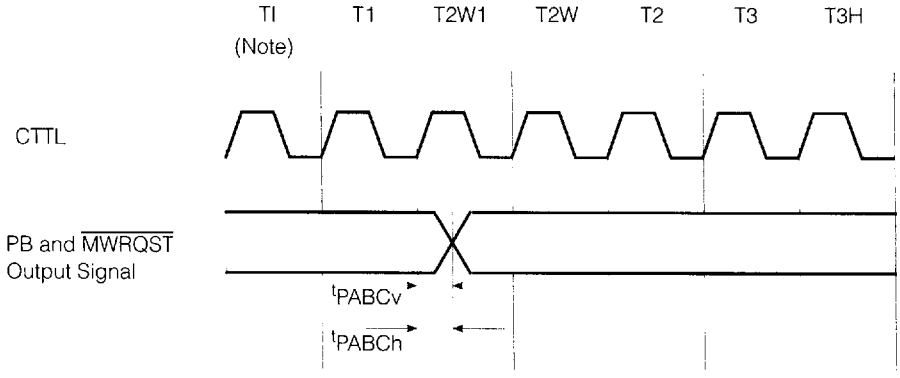


Figure 1-21. Master MICROWIRE Timing



Note: This cycle may be either TI (Idle), T2, T3 or T3H.

Figure 1-22. Output Signal Timing for Port PB and MWRQST

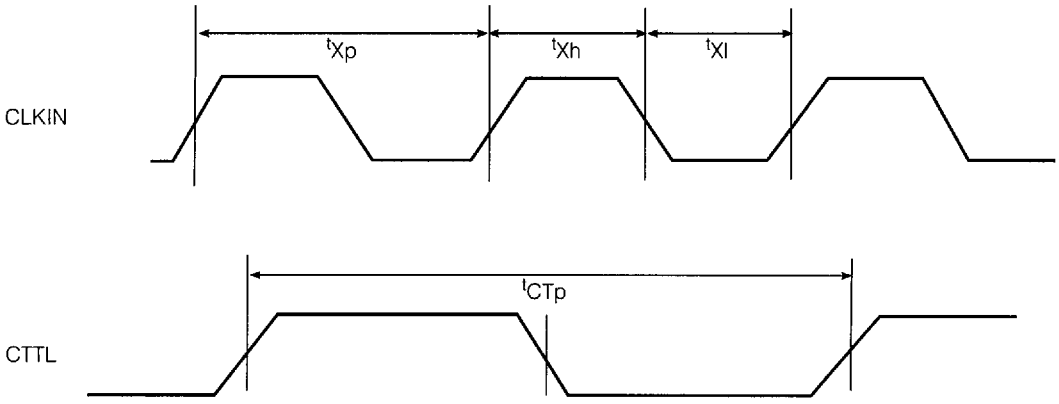


Figure 1-23. CTTL and CLKIN Timing

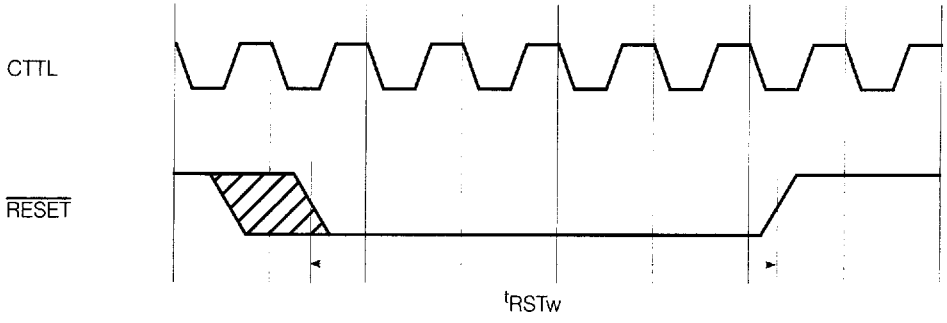


Figure 1-24. Reset Timing When Reset is not at Power-Up

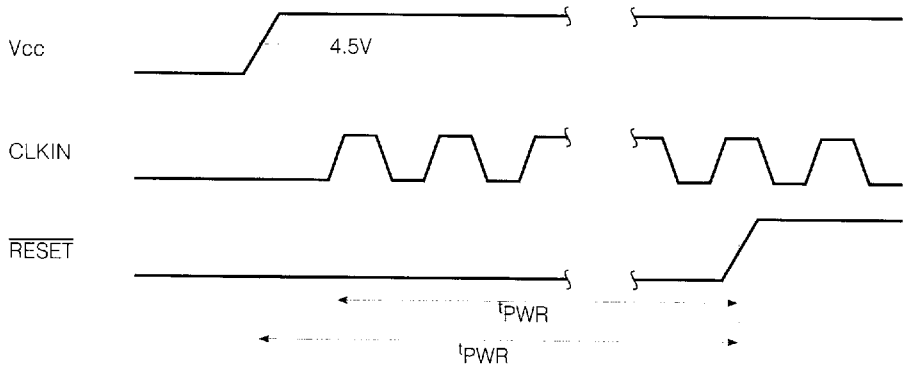
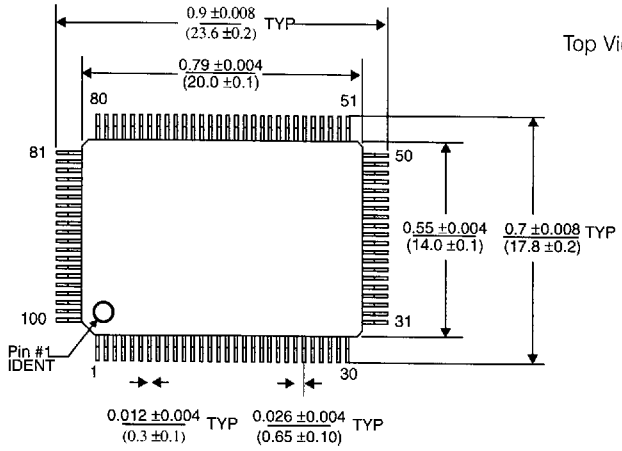
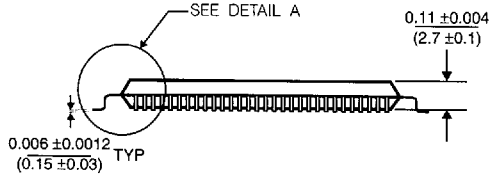
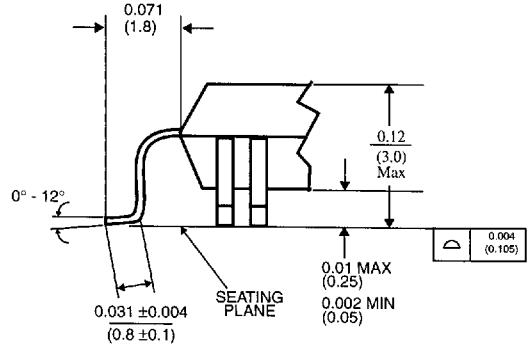


Figure 1-25. Reset Timing When Reset Is at Power-Up

PHYSICAL DIMENSIONS INCHES (MILLIMETERS)



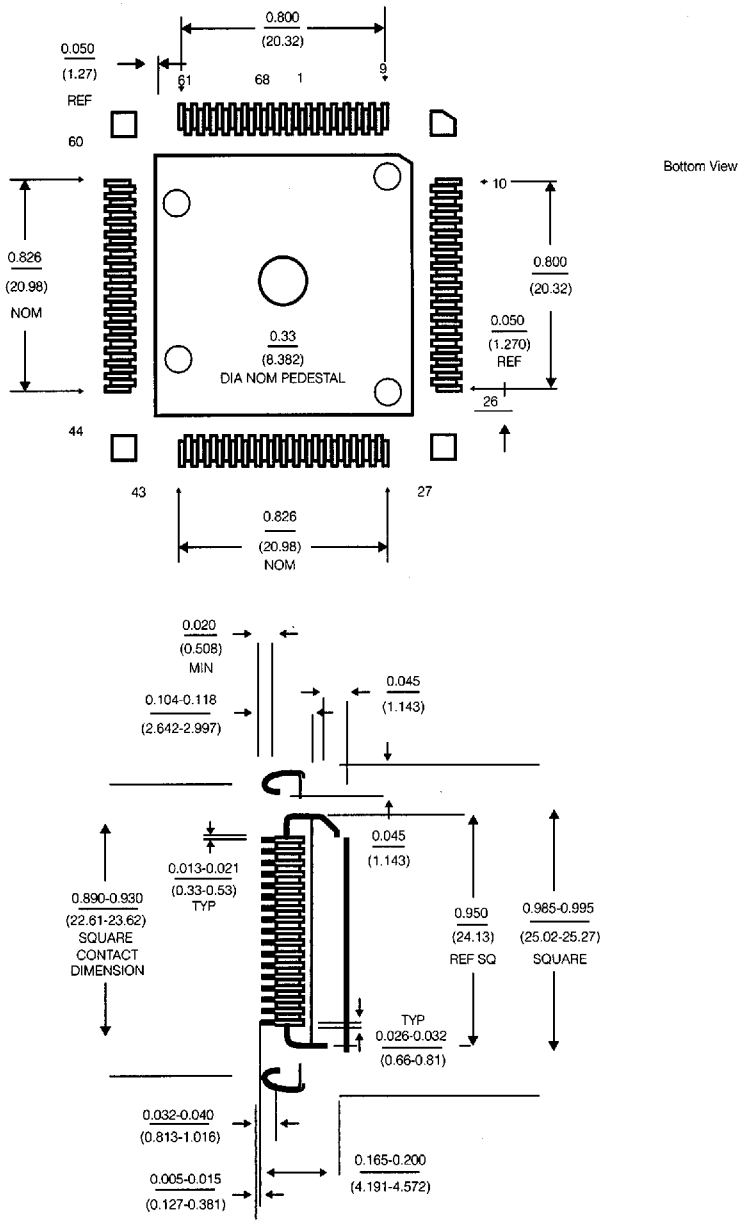




DETAIL A

100-Pin Molded Plastic Quad Flat Package (EIAJ)
Order Number ISD-T266SP/Q

PHYSICAL DIMENSIONS INCHES (MILLIMETERS)



68-Pin Plastic Leaded Chip Carrier (J)
Order Number ISD-T266SP/J