4M x 4

MCM516400B
Fast Page Mode
4096 Cycle Refresh

MCM517400B
Fast Page Mode
2048 Cycle Refresh

Advance Information

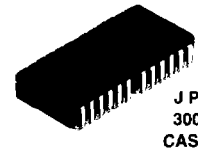
16M CMOS Dynamic RAM Family
Fast Page Mode, x4, 2K and 4K Refresh

The family of 16M dynamic RAMs is fabricated using 0.5µ CMOS high–speed silicon–gate process technology. It includes devices organized as 4,194,304 four–bit words. Advanced circuit design and fine line processing provide high performance, improved reliability, and low cost.

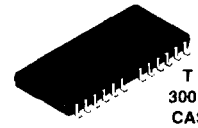
The x4 devices with 4096 cycle refresh (MCM516400B) require 12 address lines (12 rows, 10 columns), while the x4 devices with 2048 cycle refresh (MCM517400B) require only 11 address lines.

These devices are packaged in a standard 300 mil J–lead small outline package (SOJ) and a 300 mil thin–small–outline package (TSOP).

- Three–State Data Output
- Fast Page Mode
- TTL–Compatible Inputs and Outputs
- $\overline{RAS}$–Only Refresh
- $\overline{CAS}$ Before $\overline{RAS}$ Refresh
- Hidden Refresh
- 2048 Cycle Refresh: MCM517400B = 32 ms
- 4096 Cycle Refresh: MCM516400B = 64 ms
- Fast Access Time (t_{RAC}):
  MCM51x400B–50 = 50 ns (Max)
  MCM51x400B–60 = 60 ns (Max)
  MCM51x400B–70 = 70 ns (Max)
- Low Active Power Dissipation:
  MCM516400B–50 = 550 mW (Max)
  MCM516400B–60 = 440 mW (Max)
  MCM516400B–70 = 385 mW (Max)
  MCM517400B–50 = 715 mW (Max)
  MCM517400B–60 = 605 mW (Max)
  MCM517400B–70 = 523 mW (Max)
- Low Standby Power Dissipation:
  All Devices = 11 mW (Max, TTL Levels)
  All Devices = 5.5 mW (Max, CMOS Levels)

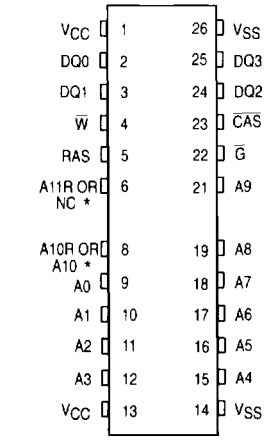


J PACKAGE
300 MIL SOJ
CASE 880A–02



T PACKAGE
300 MIL TSOP II
CASE 892A–02

PIN ASSIGNMENT
300 MIL SOJ
300 MIL TSOP



* 4096 Cycle Refresh or
2048 Cycle Refresh
(R suffix = Row Address)

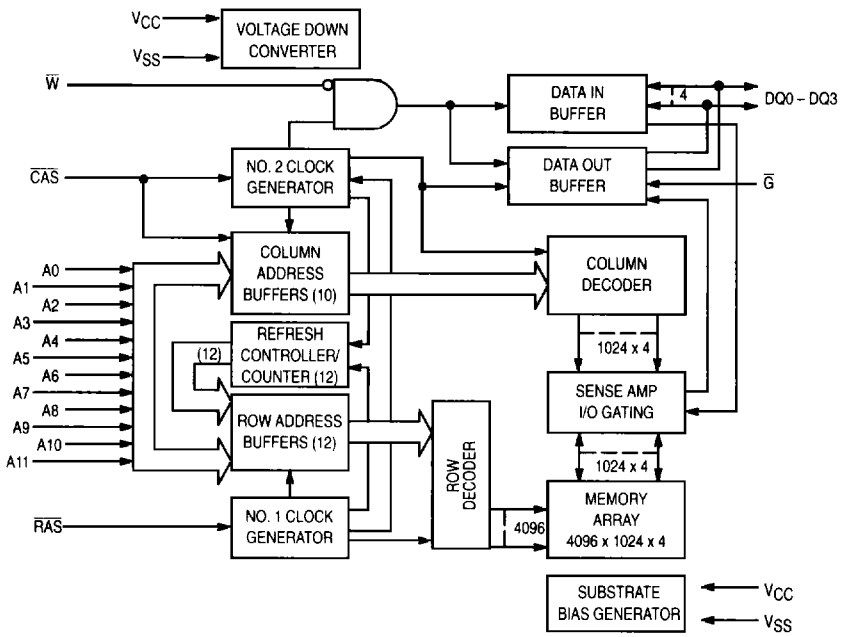
PIN NAMES			
A0 – A11	Address Input	$\overline{CAS}$	Column Address Strobe
DQ0 – DQ3	Data Input/Output	V_{CC}	Power Supply (+ 5 V)
$\overline{G}$	Output Enable	V_{SS}	Ground
$\overline{W}$	Read/Write Enable	NC	No Connection
$\overline{RAS}$	Row Address Strobe		

This document contains information on a new product. Specifications and information herein are subject to change without notice.

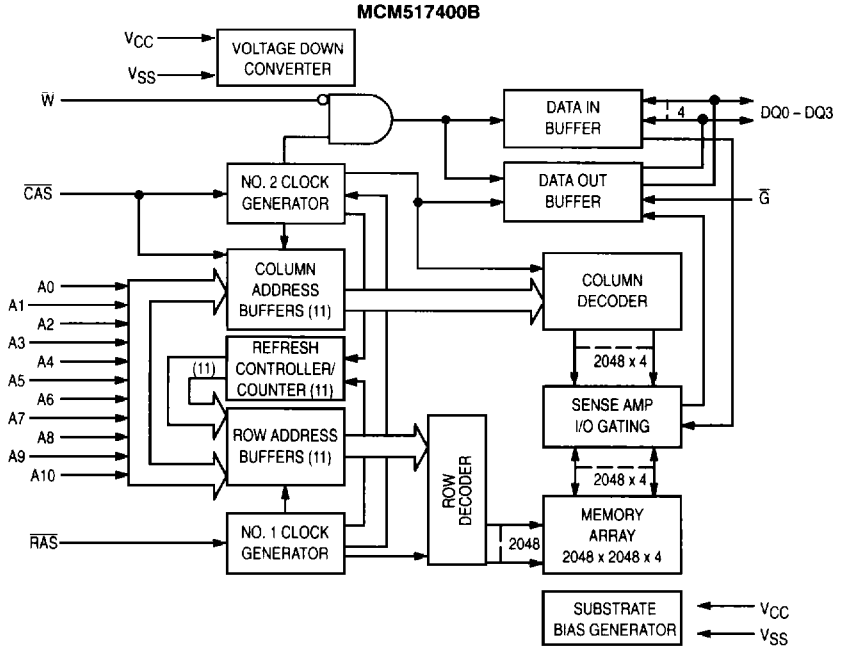
10/95

BLOCK DIAGRAMS

4096 CYCLE REFRESH BLOCK DIAGRAM
MCM516400B



2048 CYCLE REFRESH BLOCK DIAGRAM
MCM517400B



ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	− 0.5 to + 7	V
Voltage Relative to V_{SS} for Any Pin Except V_{CC}	V_{in}, V_{out}	− 0.5 to + 7	V
Data Output Current	I_{out}	50	mA
Power Dissipation	P_D	900	mW
Operating Temperature Range	T_A	0 to + 70	°C
Storage Temperature Range	T_{stg}	− 55 to + 150	°C

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to these high−impedance circuits.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

RECOMMENDED OPERATING CONDITIONS (All voltages referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage (Operating Voltage Range)	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	
Logic High Voltage, All Inputs	V_{IH}	2.4	—	V_{CC} + 0.5 V	V
Logic Low Voltage, All Inputs	V_{IL}	− 0.5*	—	0.8	V

* −2.0 V at pulse width ≤ 20 ns.

DC CHARACTERISTICS AND SUPPLY CURRENTS (See note 1)

Characteristic		Symbol	Min	Max	Unit	Notes
V_{CC} Power Supply Current (Operating)	MCM516400B–50, t_{RC} = 90 ns	I_{CC1}	—	100	mA	2, 3, 4
	MCM516400B–60, t_{RC} = 110 ns		—	80		
	MCM516400B–70, t_{RC} = 130 ns		—	70		
	MCM517400B–50, t_{RC} = 90 ns		—	130		
	MCM517400B–60, t_{RC} = 110 ns		—	110		
	MCM517400B–70, t_{RC} = 130 ns		—	95		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{IH}) Output Open		I_{CC2}	—	2	mA	
V_{CC} Power Supply Current During $\overline{RAS}$–Only Refresh Cycles		I_{CC3}			mA	2, 4
($\overline{CAS}$ = V_{IH}) Output Open	MCM516400B–50, t_{RC} = 90 ns		—	100		
	MCM516400B–60, t_{RC} = 110 ns		—	80		
	MCM516400B–70, t_{RC} = 130 ns		—	70		
	MCM517400B–50, t_{RC} = 90 ns		—	130		
	MCM517400B–60, t_{RC} = 110 ns		—	110		
	MCM517400B–70, t_{RC} = 130 ns		—	95		
V_{CC} Power Supply Current During Fast Page Mode Cycle ($\overline{RAS}$ = V_{IL}),		I_{CC4}			mA	2, 3, 4
($\overline{CAS}$ cycling) Output Open	MCM516400B–50, MCM517400B–50, t_{PC} = 35 ns		—	80		
	MCM516400B–60, MCM517400B–60, t_{PC} = 40 ns		—	70		
	MCM516400B–70, MCM517400B–70, t_{PC} = 45 ns		—	60		
V_{CC} Power Supply Current (Standby) ($\overline{RAS}$ = $\overline{CAS}$ = V_{CC} – 0.5 V)		I_{CC5}	—	1.0	mA	
V_{CC} Power Supply Current During $\overline{CAS}$ or Before $\overline{RAS}$ Refresh Cycle, Output Open		I_{CC6}			mA	2, 4
	MCM516400B–50, t_{RC} = 90 ns		—	100		
	MCM516400B–60, t_{RC} = 110 ns		—	80		
	MCM516400B–70, t_{RC} = 130 ns		—	70		
	MCM517400B–50, t_{RC} = 90 ns		—	130		
	MCM517400B–60, t_{RC} = 110 ns		—	110		
	MCM517400B–70, t_{RC} = 130 ns		—	95		
Input Leakage Current (0 V ≤ V_{in} ≤ 6.0 V, Other Input Pins = 0 V)		$I_{lkg(I)}$	–10	10	µA	
Output Leakage Current (0 V ≤ V_{out} ≤, 5.5 V, Q Floating)		$I_{lkg(O)}$	–10	10	µA	
Output High Voltage (I_{OH} = – 5 mA)		V_{OH}	2.4	—	V	
Output Low Voltage (I_{OL} = 4.2 mA)		V_{OL}	—	0.4	V	

NOTES:
1. All voltages are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4}, and I_{CC6} depend on cycle rate.
3. I_{CC1}, I_{CC4}, depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while $\overline{RAS}$ = V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).

CAPACITANCE (f = 1.0, T_A = 25°, V_{CC} = 5 V, Periodically Sampled Rather Than 100% Tested)

Characteristic		Symbol	Max	Unit
Input Capacitance	A0 – A11, D	C_{in}	5	pF
	$\overline{G}$, $\overline{RAS}$, $\overline{CAS}$, W		7	
I/O Capacitance ($\overline{CAS}$ = V_{IH} to Disable Output)	DQ0 – DQ3, Q	$C_{I/O}$	7	pF

NOTE: Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: C = I Δt/ΔV.

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

ALL DEVICES: READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM51x400B–50		MCM51x400B–60		MCM51x400B–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	90	—	110	—	130	—	ns	
Read–Write Cycle Time MCM516400B MCM517400B	t_{RELREL}	t_{RWC}	 130 135	 — —	 155 155	 — —	 180 180	 — —	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	50	—	60	—	70	ns	8, 13, 14
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	13	—	15	—	20	ns	8, 13
Access Time from Column Address	t_{AVQV}	t_{AA}	—	25	—	30	—	35	ns	8, 14
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	30	—	35	—	40	ns	8
$\overline{CAS}$ to Output in Low–Z	t_{CELQX}	t_{CLZ}	0	—	0	—	0	—	ns	8
Output Buffer and Turn–Off Delay	t_{CEHQZ}	t_{OFF}	0	13	0	15	0	15	ns	9
Transition Time (Rise and Fall)	t_T	t_T	3	50	3	50	3	50	ns	7
$\overline{RAS}$ Precharge Time	t_{REHREL}	t_{RP}	30	—	40	—	50	—	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	50	10 k	60	10 k	70	10 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	13	—	15	—	20	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	50	—	60	—	70	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time	t_{CEHREH}	t_{RHCP}	30	—	35	—	40	—	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	13	10 k	15	10 k	20	10 k	ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RELCEL}	t_{RCD}	17	37	20	45	20	50	ns	13
$\overline{RAS}$ to Column Address Delay Time	t_{RELAV}	t_{RAD}	12	25	15	30	15	35	ns	14
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CEHREL}	t_{CRP}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time	t_{CEHCEL}	t_{CP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{AVREL}	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RELAX}	t_{RAH}	7	—	10	—	10	—	ns	
Column Address Setup Time	t_{AVCEL}	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CELAX}	t_{CAH}	10	—	10	—	15	—	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	25	—	30	—	35	—	ns	
Read Command Setup Time	t_{WHCEL}	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to $\overline{CAS}$	t_{CEHWX}	t_{RCH}	0	—	0	—	0	—	ns	10
Read Command Hold Time Referenced to $\overline{RAS}$	t_{REHWX}	t_{RRH}	0	—	0	—	0	—	ns	10

NOTES: (continued)

1. All voltages are referenced to V_{SS}.
2. I_{CC1}, I_{CC3}, I_{CC4}, I_{CC6} depend on cycle rate.
3. I_{CC1}, I_{CC4} depend on output loading. Specified values are obtained with the output open.
4. Address can be changed once or less while RAS = V_{IL}. In case of I_{CC4}, it can be changed once or less during a fast page mode cycle (t_{PC}).
5. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ only refresh cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of 8 $\overline{CAS}$ before $\overline{RAS}$ refresh cycles instead of 8 $\overline{RAS}$ only refresh cycles are required.
6. AC measurements t_T = 5.0 ns.
7. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.

ALL DEVICES, READ, WRITE, AND READ–WRITE CYCLES (Continued)

Parameter	Symbol		MCM51x400B–50		MCM51x400B–60		MCM51x400B–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Write Command Hold Time Referenced to $\overline{CAS}$	t_{CELWH}	t_{WCH}	10	—	10	—	15	—	ns	
Write Command Pulse Width	t_{WLWH}	t_{WP}	10	—	10	—	15	—	ns	
Write Command to $\overline{RAS}$ Lead Time	t_{WLREH}	t_{RWL}	15	—	15	—	20	—	ns	
Write Command to $\overline{CAS}$ Lead Time	t_{WLCEH}	t_{CWL}	15	—	15	—	20	—	ns	
Data In Setup Time	t_{DVCEL}	t_{DS}	0	—	0	—	0	—	ns	11
Data In Hold Time	t_{CELDX}	t_{DH}	10	—	10	—	15	—	ns	11
Write Command Setup Time	t_{WLCEL}	t_{WCS}	0	—	0	—	0	—	ns	12
$\overline{CAS}$ to Write Delay	t_{CELWL}	t_{CWD}	35	—	40	—	45	—	ns	12
$\overline{RAS}$ to Write Delay	t_{RELWL}	t_{RWD}	73	—	85	—	95	—	ns	12
Column Address to Write Delay	t_{AVWL}	t_{AWD}	48	—	55	—	60	—	ns	12
Refresh Period MCM516400B MCM517400B	t_{RVRV}	t_{RFSH}	— —	64 32	— —	64 32	— —	64 32	ms	
$\overline{CAS}$ Setup Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEL}	t_{CSR}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Hold Time for $\overline{CAS}$ Before $\overline{RAS}$ Refresh	t_{RELCEH}	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{RAS}$ Precharge to $\overline{CAS}$ Active Time	t_{REHCEL}	t_{RPC}	5	—	5	—	5	—	ns	
$\overline{CAS}$ Precharge Time for $\overline{CAS}$ Before $\overline{RAS}$ Counter Time	t_{CEHCEL}	t_{CPT}	20	—	20	—	20	—	ns	
Write Command Setup Time (Test Mode)	t_{WLREL}	t_{WTS}	10	—	10	—	10	—	ns	
Write Command Hold Time (Test Mode)	t_{RELWH}	t_{WTH}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Precharge Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{WHREL}	t_{WRP}	10	—	10	—	10	—	ns	
Write to $\overline{RAS}$ Hold Time ($\overline{CAS}$ Before $\overline{RAS}$ Refresh)	t_{RELWL}	t_{WRH}	10	—	10	—	10	—	ns	

NOTES:

8. Measured with a load equivalent to 2 TTL loads and 100 pF.
9. t_{OFF} (max) and t_{GZ} (max) define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.
10. Either t_{RCH} or t_{RRH} must be satisfied for a read cycle.
11. These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in Read–Modify–Write cycles.
12. t_{WCS}, t_{CWD}, t_{RWD}, t_{AWD} and t_{CPWD} are specified as reference points only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the DQ pins remain high impedance throughout the entire cycle. If $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (for fast page mode cycle only), the cycle is a read–modify–write cycle and the DQ pins will contain the data read from the selected address. If neither of these conditions are met; delayed write or at access time and until $\overline{CAS}$ or OE goes back to V_{IH}, DQ is indeterminate.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only. If t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. Operation within the t_{RAD} (max) limit ensures that t_{RAC} (max) can be met. t_{RAD} (max) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max), then access time is controlled exclusively by t_{AA}.

DEVICE–SPECIFIC AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

4M x 4 CONFIGURATION–SPECIFIC READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

Parameter	Symbol		MCM51x400B–50		MCM51x400B–60		MCM51x400B–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
$\overline{RAS}$ Hold Time Referenced to $\overline{G}$	t_{GLREH}	t_{ROH}	10	—	10	—	10	—	ns	
$\overline{G}$ Access Time	t_{GLQV}	t_{GA}	—	13	—	15	—	15	ns	5
$\overline{G}$ to Data Delay	t_{GLHDX}	t_{GD}	13	—	15	—	15	—	ns	6
Output Buffer Turn–Off Delay Time from $\overline{G}$	t_{GHQZ}	t_{GZ}	0	13	0	15	0	15	ns	
$\overline{G}$ Command Hold Time	t_{WLGL}	t_{GH}	15	—	15	—	15	—	ns	
Output Disable Setup Time	t_{GHCEL}	t_{GDS}	0	—	0	—	0	—	ns	

NOTES:
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 $\overline{RAS}$ cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. Measured with a current load equivalent to 2 TTL (– 200 µA, + 4 mA) loads and 100 pF with the data output trip points set at V_{OH} = 2.0 V and V_{OL} = 0.8 V.
6. t_{OFF} (max) and/or t_{GZ} (max) define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

FAST PAGE MODE READ, WRITE, AND READ–WRITE CYCLES (See Notes 1, 2, 3, and 4)

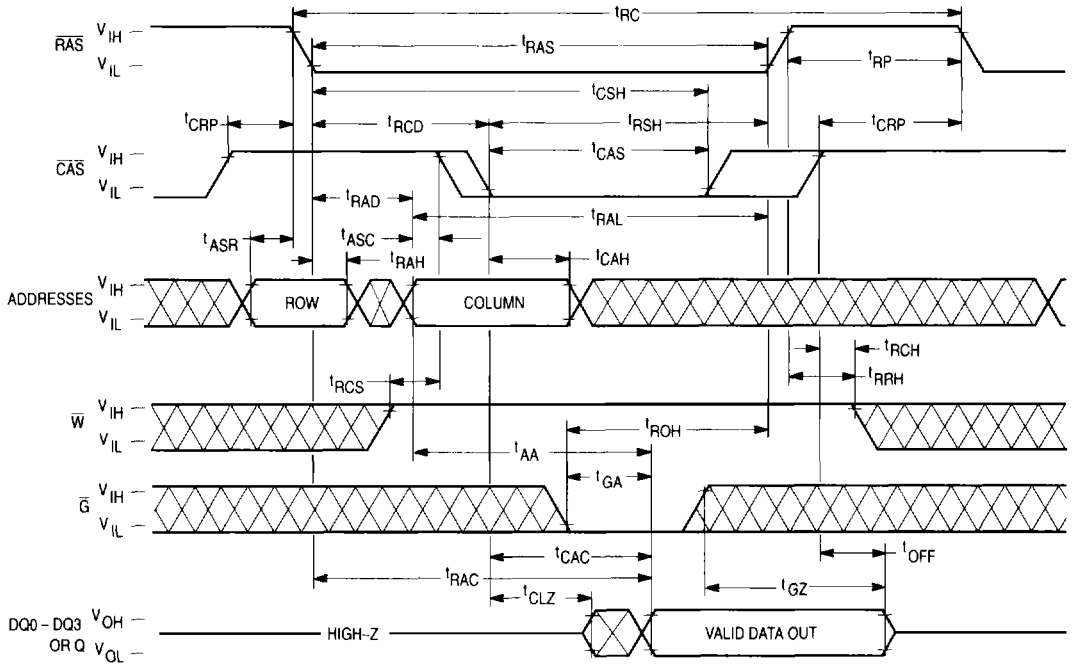
Parameter	Symbol		MCM51x400B–50		MCM51x400B–60		MCM51x400B–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Fast Page Mode Cycle Time	t_{CELCEL}	t_{PC}	35	—	40	—	45	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time (Fast Page Mode)	t_{CEHREH}	t_{RHCP}	30	—	35	—	40	—	ns	
Fast Page Mode Read–Write Cycle Time MCM516400B	t_{CELCEL}	t_{PRWC}	65	—	85	—	95	—	ns	
MCM517400B			80	—	85	—	95	—		
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	50	200 k	60	200 k	70	200 k	ns	
$\overline{CAS}$ Precharge to Write Delay	t_{CEHWL}	t_{CPWD}	53	—	60	—	65	—	ns	5

NOTES:
1. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
2. An initial pause of 200 µs is required after power–up followed by 8 RAS cycles before proper device operation is guaranteed.
3. The transition time specification applies for all input signals. In addition to meeting the transition rate specification, all input signals must transition between V_{IH} and V_{IL} (or between V_{IL} and V_{IH}) in a monotonic manner.
4. AC measurements t_T = 5.0 ns.
5. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD}, and t_{CPWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) through–out the entire cycle; if $t_{CWD} \geq t_{CWD}$ (min), $t_{RWD} \geq t_{RWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min), and $t_{CPWD} \geq t_{CPWD}$ (min) (page mode), the cycle is a read–write cycle and the data out will contain data read from the selected cell. If neither of these sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

3

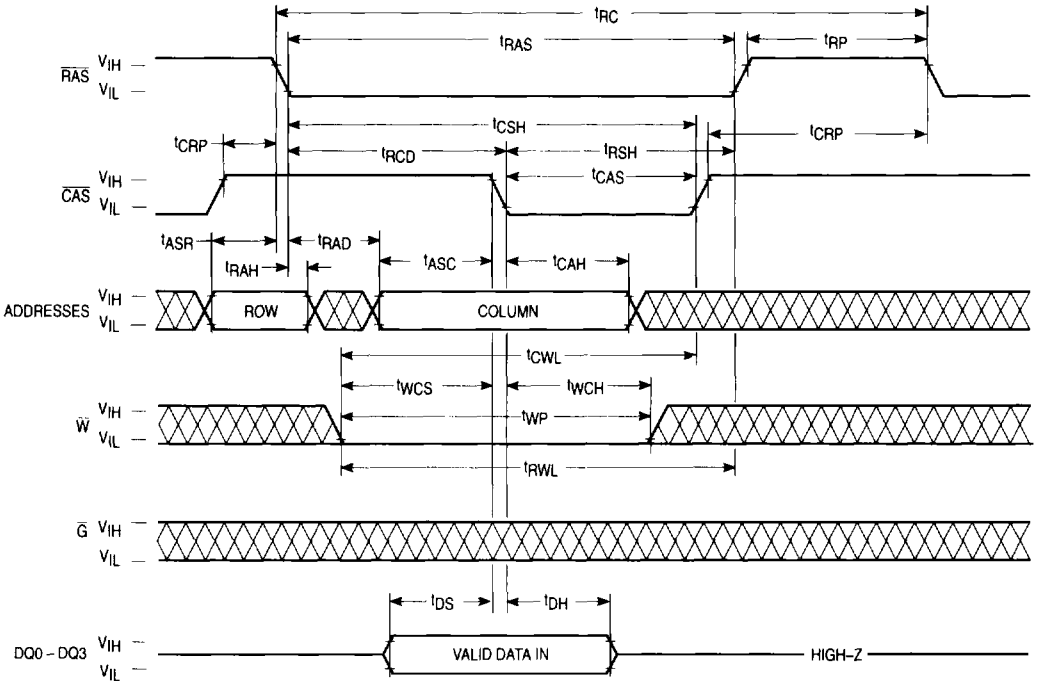
TIMING DIAGRAMS

PAGE MODE READ CYCLE



3

EARLY WRITE CYCLE



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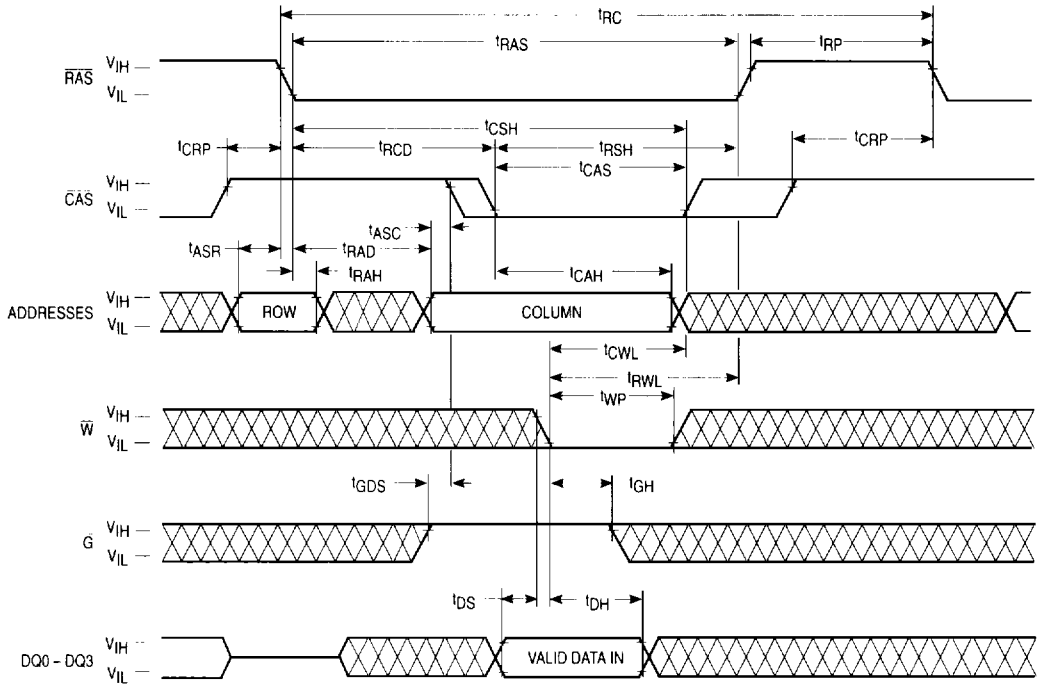
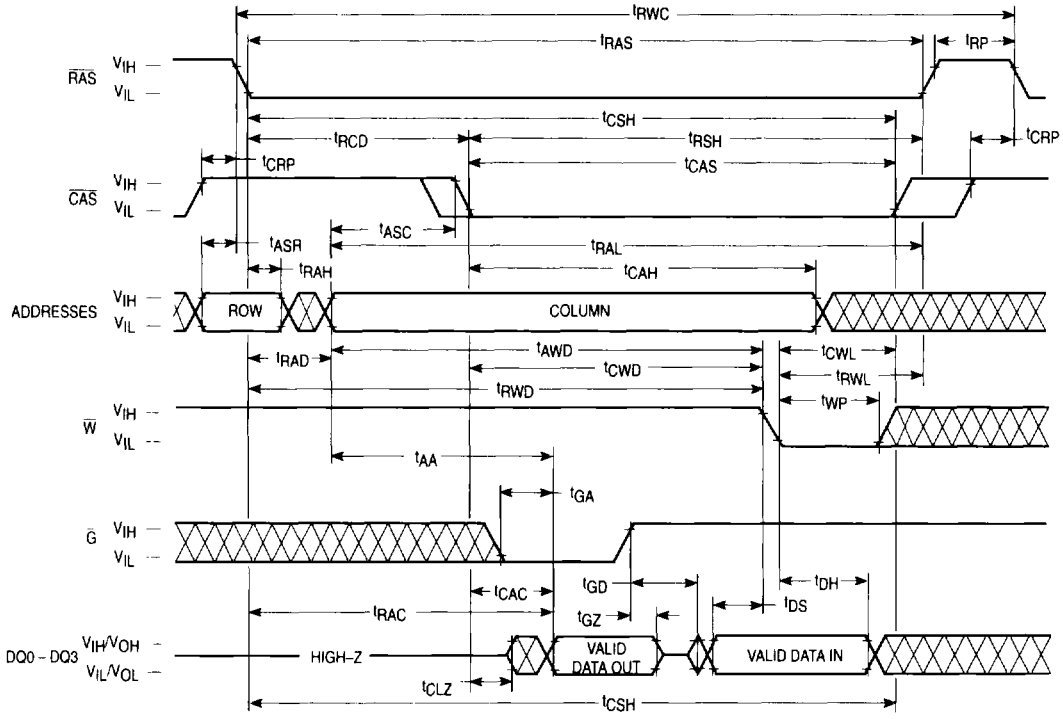
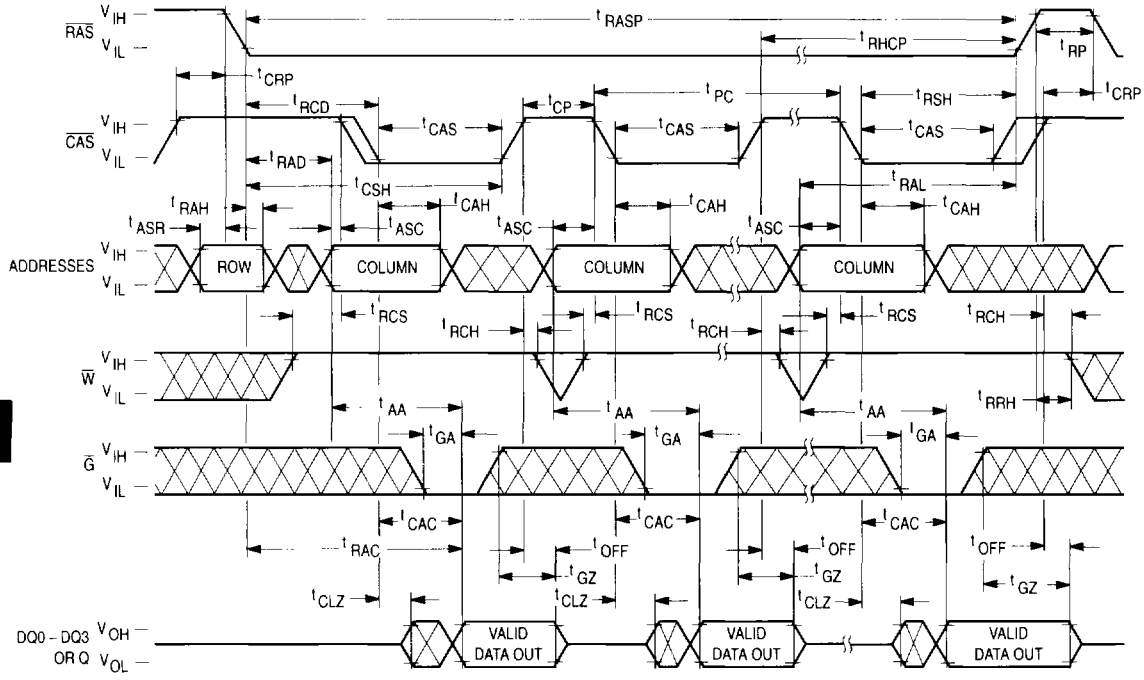
$\overline{G}$ CONTROLLED LATE WRITE CYCLE



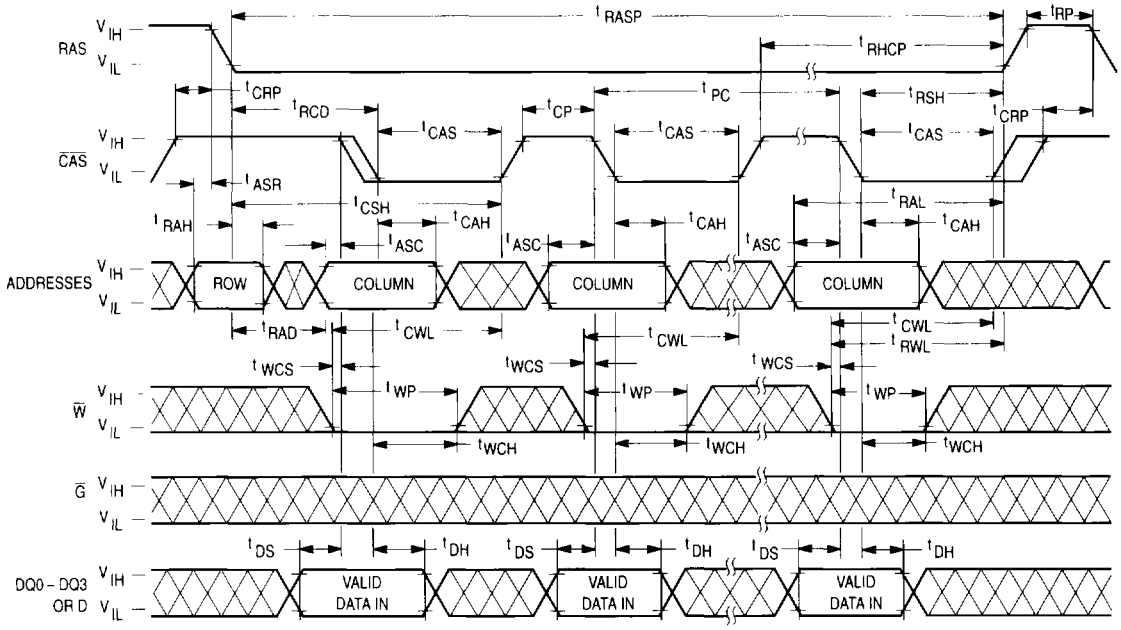
READ – WRITE CYCLE



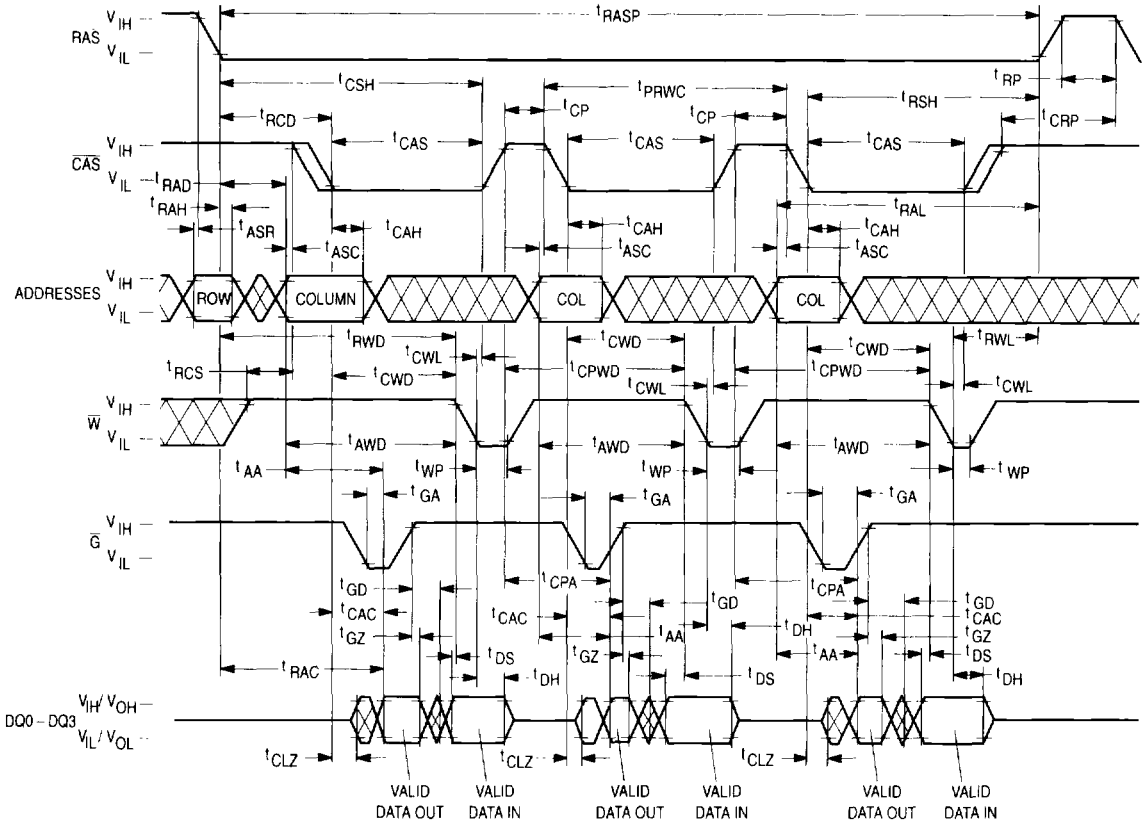
FAST PAGE MODE READ CYCLE



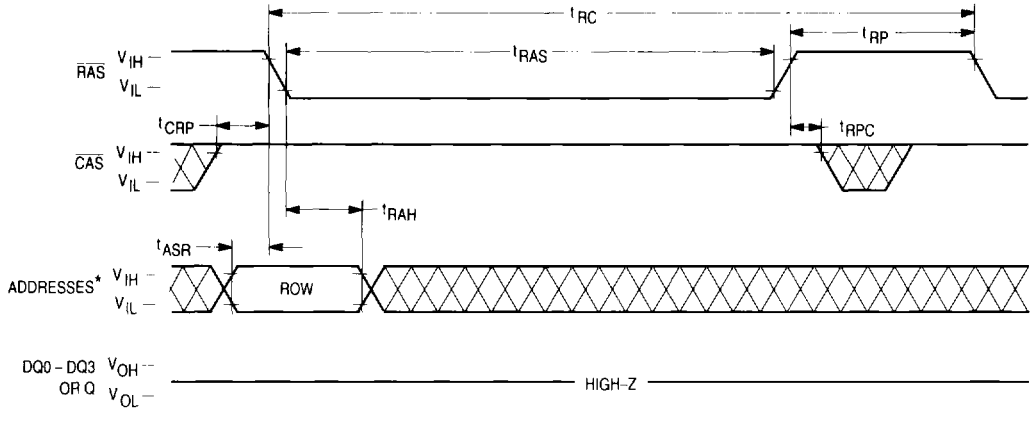
FAST PAGE MODE EARLY WRITE CYCLE



FAST PAGE MODE READ – WRITE CYCLE



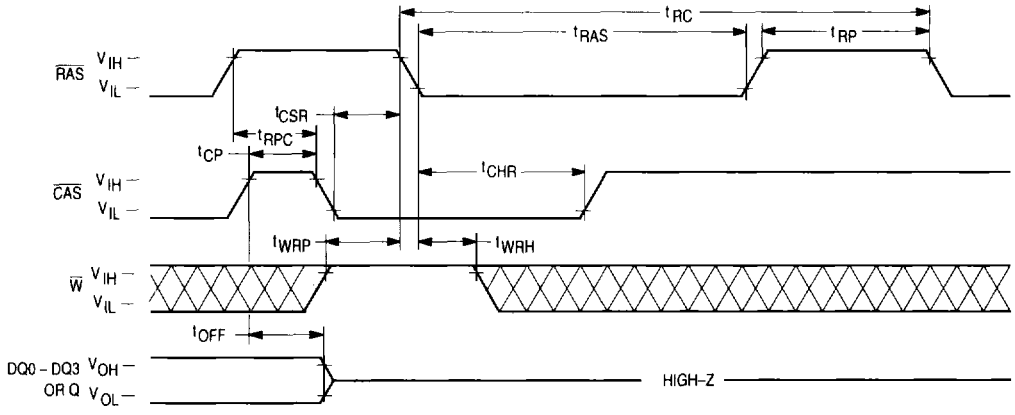
RAS ONLY REFRESH CYCLE
(W and G are Don't Care)



*MCM516400B – A0 – A11; MCM517400B – A0 – A10.

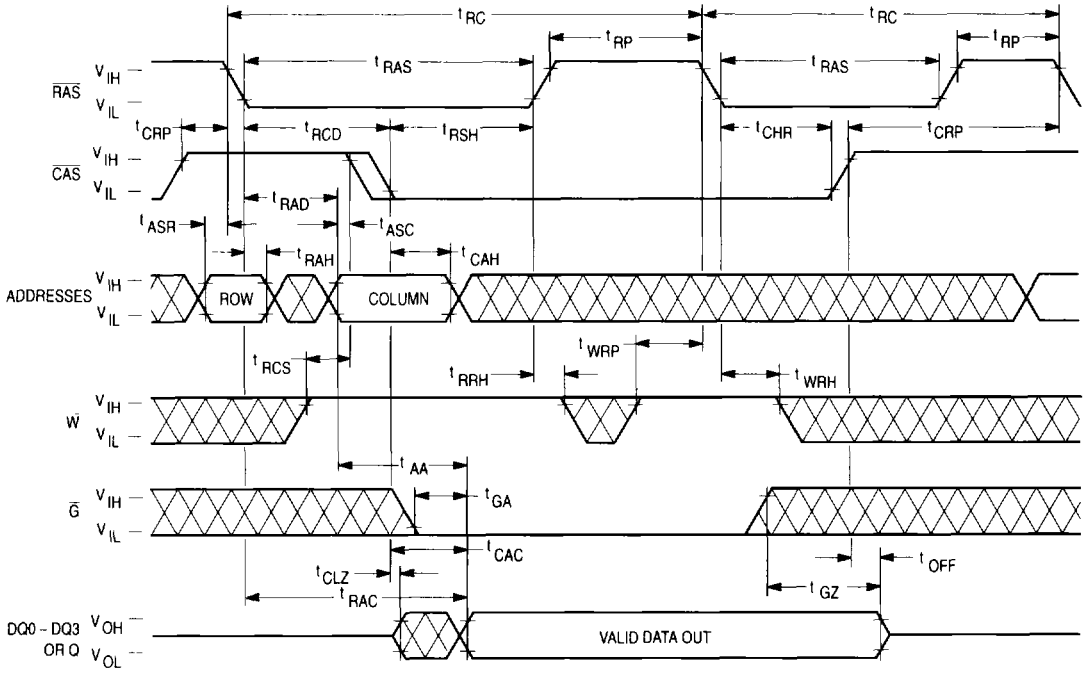
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE

($\overline{G}$ and A0 – A10 or A11 are Don't Care)

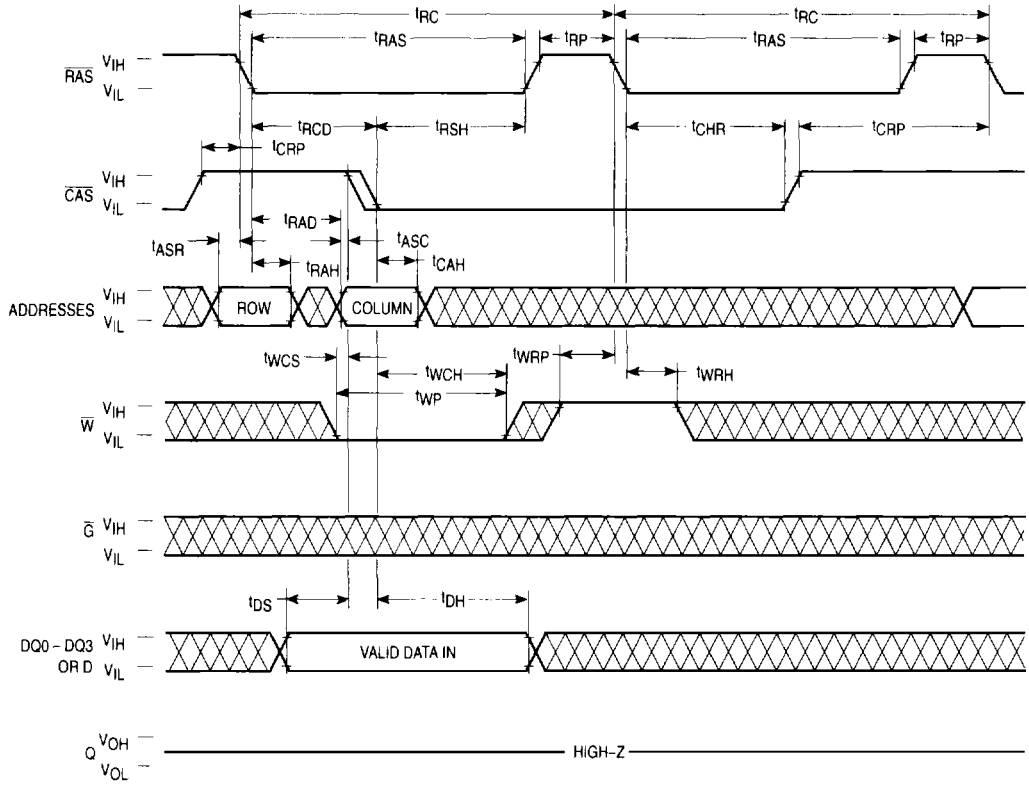


3

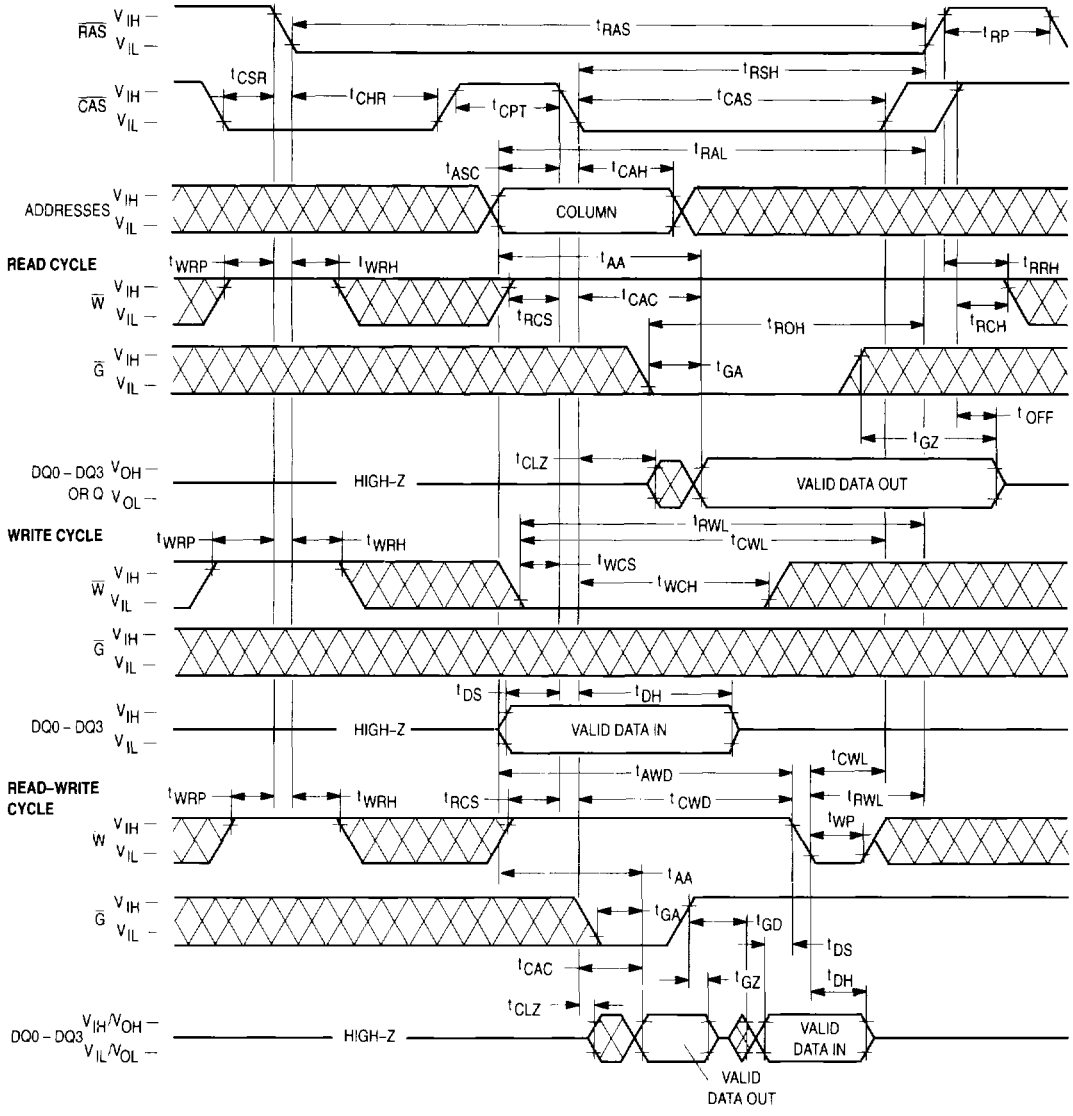
HIDDEN REFRESH CYCLE (READ)



HIDDEN REFRESH CYCLE (EARLY WRITE)



$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE



DEVICE INITIALIZATION

On power–up, an initial pause of 200 microseconds is required for the internal substrate generator to establish the correct bias voltage. This must be followed by a minimum of eight active cycles of the row address strobe (clock) to initialize all dynamic nodes within the RAM. During an extended inactive state (greater than 32 milliseconds or 64 milliseconds, for MCM517400B and MCM516400B, respectively), a wakeup sequence of eight active cycles is necessary to ensure proper operation.

ADDRESSING THE RAM

MCM516400B: The twelve address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate address fields. A total of twenty two address bits, twelve rows and ten columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

MCM517400B: The eleven address pins on the device are time multiplexed at the beginning of a memory cycle by two clocks, row address strobe ($\overline{RAS}$) and column address strobe ($\overline{CAS}$), into two separate 11–bit address fields. A total of twenty two address bits, eleven rows and eleven columns, will decode one of the 4,194,304 four bit word locations in the device. $\overline{RAS}$ active transition is followed by $\overline{CAS}$ active transition (active = V_{IL}, t_{RCD} minimum) for all read or write cycles. The delay between $\overline{RAS}$ and $\overline{CAS}$ active transitions, referred to as the **multiplex window**, gives a system designer flexibility in setting up the external addresses into the RAM.

The external $\overline{CAS}$ signal is ignored until an internal $\overline{RAS}$ signal is available. This "gate" feature on the external $\overline{CAS}$ clock enables the internal $\overline{CAS}$ line as soon as the row address hold time (t_{RAH}) specification is met (and defines t_{RCD} minimum). The multiplex window can be used to absorb skew delays in switching the address bus from row to column addresses and in generating the $\overline{CAS}$ clock.

There are three other variations in addressing the 16M DRAM Family per device: $\overline{RAS}$–only refresh cycle, $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, and page mode. All are discussed in separate sections that follow.

READ CYCLE

The DRAM may be read with four different cycles: "normal" random read cycle, fast page mode read cycle, read–write cycle, and fast page mode read–write cycle. The normal read cycle is outlined here,while the other cycles are discussed in separate sections.

The normal read cycle begins as described in **ADDRESSING THE RAM**, with $\overline{RAS}$ and $\overline{CAS}$ active transitions latching the desired bit location. The write ($\overline{W}$) input level must be high (V_{IH}), t_{RCS} (minimum) before the $\overline{CAS}$ or active transition, to enable read mode.

Both the $\overline{RAS}$ and $\overline{CAS}$ clocks trigger a sequence of events that are controlled by several delayed internal clocks. The internal clocks are linked in such a manner that the read access time of the device is independent of the address multiplex window.

For **MCM516400B and MCM517400B**, both $\overline{CAS}$ and output enable ($\overline{G}$) control read access time: $\overline{CAS}$ must be active before or at t_{RCD} maximum and $\overline{G}$ must be active t_{RAC}–t_{GA} (both minimum) after $\overline{RAS}$ active transition to guarantee valid data out (Q) at t_{RAC}. If the t_{RCD} maximum is exceeded and/or $\overline{G}$ active transition does not occur in time, read access time is determined by either the $\overline{CAS}$ or $\overline{G}$ clock active transition (t_{CAC} or t_{GA}).

WRITE CYCLE

The user can write to the DRAM with any of four cycles: early write, late write, fast page mode early write, and fast page mode read–write. Early and late write modes are discussed here, while fast page mode write operation is covered in a separate section.

A write cycle begins as described in **ADDRESSING THE RAM**. Write mode is enabled by the transition of $\overline{W}$ to active (V_{IL}). Early and late write modes are distinguished by the active transition of $\overline{W}$, with respect to $\overline{CAS}$. Minimum active time t_{RAS} and t_{CAS}, and precharge time t_{RP}, apply to write mode, as in the read mode.

An early write cycle is characterized by $\overline{W}$ active transition at minimum time t_{WCS} before $\overline{CAS}$ active transition. Column address setup and hold times (t_{ASC}, t_{CAH}) and data in (D) setup and hold times (t_{DS}, t_{DH}) are referenced to $\overline{CAS}$ in an early write cycle. $\overline{RAS}$ and $\overline{CAS}$ clocks must stay active for t_{RWL} and t_{CWL}, respectively, after the start of the early write operation to complete the cycle.

A late–write cycle (referred to as $\overline{G}$–controlled write) occurs when $\overline{W}$ active transition is made after $\overline{CAS}$ active transition. $\overline{W}$ active transition could be delayed for almost 10 microseconds after $\overline{CAS}$ active transition, (t_{RCD} + t_{CWD} + t_{RWL} + 2t_T) ≤ t_{RAS}, if other timing minimums (t_{RCD}, t_{RWL}, and t_T) are maintained. D timing parameters are referenced to $\overline{W}$ active transition in a late write cycle. Output buffers are enabled by $\overline{CAS}$ active transition. 4M x 4 outputs are switched off by $\overline{G}$ inactive transition, which is required to write to the device. Q may be indeterminate (see note 12 of AC Operating Conditions table). $\overline{RAS}$ and $\overline{CAS}$ must remain active for t_{RWL} and t_{CWL}, respectively, after $\overline{W}$ active transition to complete the write cycle. $\overline{G}$ (4M x 4) devices must remain inactive for t_{GH} after $\overline{W}$ active transition to complete the write cycle.

READ–WRITE CYCLE

A read–write cycle performs a read and then a write at the same address, during the same cycle. This cycle is basically a late write cycle, as discussed in the **WRITE CYCLE** section, except $\overline{W}$ must remain high for t_{CWD} and/or t_{AWD} minimum, to guarantee valid Q before writing the bit.

PAGE MODE CYCLES

Page mode allows fast successive data operations at all column locations (MCM516400B: 1024 columns; and MCM517400B: 2048 columns) on a selected row of the 16M DRAM family. Read access time in page mode (t_{CAC}) is typically half the regular $\overline{RAS}$ clock access time, t_{RAC}. Page mode operation consists of keeping $\overline{RAS}$ active while toggling $\overline{CAS}$

between V_{IH} and V_{IL}. The row is latched by $\overline{RAS}$ active transition, while each $\overline{CAS}$ active transition allows selection of a new column location on the row.

A page mode cycle is initiated by a normal read, write, or read–write cycle, as described in prior sections. Once the timing requirements for the first cycle are met, $\overline{CAS}$ transitions to inactive for minimum t_{CP}, while $\overline{RAS}$ remains low (V_{IL}). The second $\overline{CAS}$ active transition while $\overline{RAS}$ is low initiates the first page mode cycle (t_{PC} or t_{PRWC}). Either a read, write, or read–write operation can be performed in a page mode cycle, subject to the same conditions as in normal operation (previously described). These operations can be intermixed in consecutive page mode cycles and performed in any order. The maximum number of consecutive page mode cycles is limited by t_{RASP}. Page mode operation is ended when $\overline{RAS}$ transitions to inactive, coincident with or following $\overline{CAS}$ inactive transition.

REFRESH CYCLES

3

The dynamic RAM design is based on capacitor charge storage for each bit in the array. This charge will tend to degrade with time and temperature. Each bit must be periodically **refreshed** (recharged) to maintain the correct bit state. Bits in the MCM516400B require refresh every 64 milliseconds, while refresh time for the MCM517400B is 32 milliseconds.

This is accomplished by cycling through the 4096 and 2048 row addresses in sequence within the specified refresh time. All the bits on a row are refreshed simultaneously when the row is addressed. Distributed refresh implies a row refresh every 15.6 microseconds for the 16M DRAM device family. Burst refresh, a refresh of all rows consecutively, must be performed every 64 milliseconds on the MCM516400B, and 32 milliseconds on the MCM517400B.

A normal read, write, or read–write operation to the RAM will refresh all the bits (4096 or 2048) associated with the particular row decodes. Three other methods of refresh, **$\overline{RAS}$–only refresh, $\overline{CAS}$ before $\overline{RAS}$ refresh,** and **hidden refresh** are available on this device for greater system flexibility.

$\overline{RAS}$–Only Refresh

$\overline{RAS}$–only refresh consists of $\overline{RAS}$ transition to active, latching the row address to be refreshed, while $\overline{CAS}$ remains high (V_{IH}) throughout the cycle. An external counter should be employed to ensure that all rows are refreshed within the specified limit.

$\overline{CAS}$ Before $\overline{RAS}$ Refresh

$\overline{CAS}$ before $\overline{RAS}$ refresh is enabled by bringing $\overline{CAS}$ active before $\overline{RAS}$. This clock order activates an internal refresh counter that generates the row address to be refreshed. External address lines are ignored during the automatic refresh cycle. The output buffer remains at the same state it was in during the previous cycle (hidden refresh). $\overline{W}$ must be inactive for time t_{WRP} before and time t_{WRH} after $\overline{RAS}$ active transition to prevent switching the device into a **test mode cycle**.

Hidden Refresh

Hidden refresh allows refresh cycles to occur while maintaining valid data at the output pin. Holding $\overline{CAS}$ active at the end of a read or write cycle while $\overline{RAS}$ cycles inactive for t_{RP} and back to active starts the hidden refresh. This is essentially the execution of a $\overline{CAS}$ before $\overline{RAS}$ refresh from a cycle in progress (see Figure 1). $\overline{W}$ is subject to the same conditions with respect to $\overline{RAS}$ active transition (to prevent test mode entry) as in $\overline{CAS}$ before $\overline{RAS}$ refresh.

$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST

The internal refresh counter of this device can be tested with a **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test**. This test is performed with a read–write operation. During the test, the internal refresh counter generates the row address, while the external address supplies the column address. The entire array is refreshed after 4096 or 2048 cycles, as indicated by the check data written in each row. See **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test cycle** timing diagram.

The test can be performed after a minimum of eight **$\overline{CAS}$ before $\overline{RAS}$** initialization cycles. Test procedure:

1. Write 0s into all memory cells with normal write mode.
2. Select a column address, read 0 out and write 1 into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read–write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
3. Read the 1s that were written in step two in normal read mode.
4. Using the same starting column address as in step two, read 1 out and write 0 into the cell by performing the **$\overline{CAS}$ before $\overline{RAS}$ refresh counter test, read–write cycle**. Repeat this operation 4096 or 2048 times, depending on device type.
5. Read 0s which were written in step four in normal read mode.
6. Repeat steps one through five using complement data.

TEST MODE

The internal organization of the MCM516400B and MCM517400B allows the device to be tested as if it were a 1M x 16 DRAM. In **Test Mode** operation, column addresses A1 and A0 are ignored. A test mode cycle reads and/or writes data to a bit in each of the sixteen 1M blocks in parallel. During a write cycle, data is written using only DQ0, while during a read cycle, if all 16 bits are equal (all 0s or all 1s), DQ3 will indicate a 1. Otherwise, DQ3 will indicate a 0. DQ0, DQ1, and DQ2 always indicate a 1 during test mode read cycle. See Test Mode block diagram.

$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$ timing puts the device in **Test Mode**, as shown in the test mode timing diagram. A **$\overline{CAS}$ before $\overline{RAS}$** refresh cycle or a **$\overline{RAS}$ only** refresh cycle places the device back in normal mode. Refresh is performed in test mode by using a **$\overline{W}$, $\overline{CAS}$ before $\overline{RAS}$** refresh cycle which uses the internal refresh address counter.

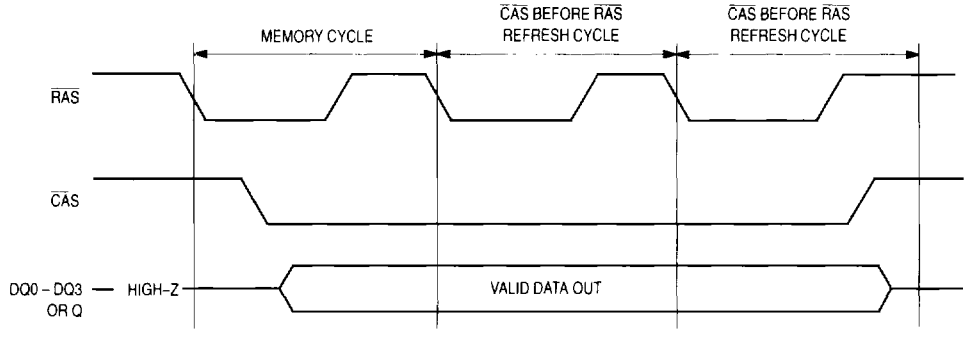


Figure 1. Hidden Refresh Cycle

TEST MODE AC OPERATING CONDITIONS AND CHARACTERISTICS

(V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C, Unless Otherwise Noted)

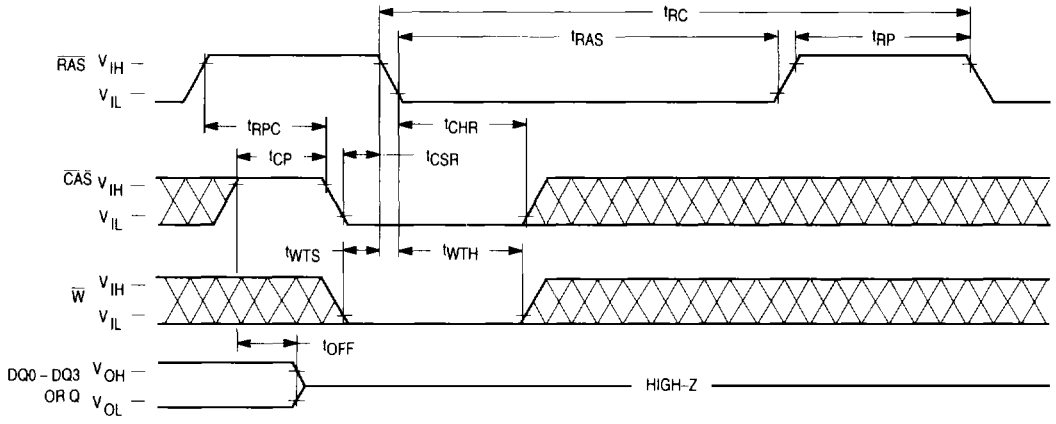
READ, WRITE, AND READ–WRITE CYCLES

Parameter	Symbol		MCM51x400B–50		MCM51x400B–60		MCM51x400B–70		Unit	Notes
	Std	Alt	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RELREL}	t_{RC}	95	—	115	—	135	—	ns	
Fast Page Mode Cycle Time MCM516400B MCM517400B	t_{CELCEL}	t_{PC}	 35 40	 — —	 45 45	 — —	 50 50	—	ns	
Access Time from $\overline{RAS}$	t_{RELQV}	t_{RAC}	—	55	—	65	—	75	ns	
Access Time from $\overline{CAS}$	t_{CELQV}	t_{CAC}	—	18	—	20	—	25	ns	
Access Time from Column Address	t_{AVQV}	t_{AA}	—	30	—	35	—	40	ns	
Access Time from Precharge $\overline{CAS}$	t_{CEHQV}	t_{CPA}	—	35	—	40	—	45	ns	
$\overline{RAS}$ Pulse Width	t_{RELREH}	t_{RAS}	55	10 k	65	10 k	75	10 k	ns	
$\overline{RAS}$ Pulse Width (Fast Page Mode)	t_{RELREH}	t_{RASP}	55	200 k	65	200 k	75	200 k	ns	
$\overline{RAS}$ Hold Time	t_{CELREH}	t_{RSH}	18	—	20	—	25	—	ns	
$\overline{CAS}$ Hold Time	t_{RELCEH}	t_{CSH}	55	—	65	—	75	—	ns	
$\overline{CAS}$ Precharge to $\overline{RAS}$ Hold Time MCM516400B MCM517400B	t_{CEHREH}	t_{RHCP}	 40 35	 — —	 40 40	 — —	 45 45	 — —	ns	
$\overline{CAS}$ Pulse Width	t_{CELCEH}	t_{CAS}	18	10 k	20	10 k	25	10 k	ns	
Column Address to $\overline{RAS}$ Lead Time	t_{AVREH}	t_{RAL}	30	—	35	—	40	—	ns	

TEST MODE TIMING DIAGRAMS

WRITE OR CAS BEFORE RAS REFRESH CYCLE (TEST MODE ENTRY)

(G and A0 – A10 or 11 are Don't Care)



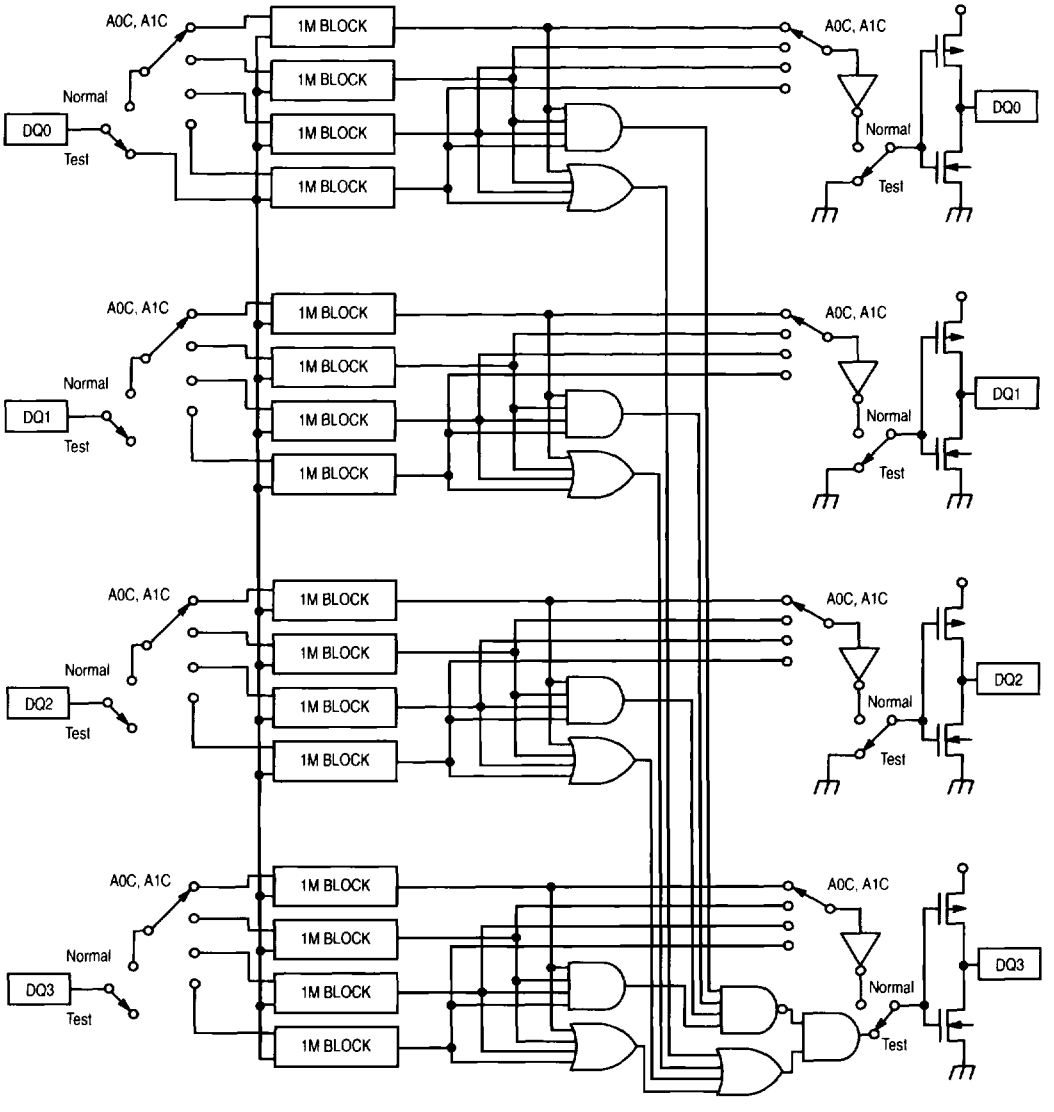
NOTE: Once the device is put into Test Mode with the Test Mode Entry Cycle, any of the standard cycles (Read, Write, Fast Page Mode, etc.) may be used to test the part, providing that the timing parameters are modified as described in the Test Mode AC Operating Conditions and Characteristics table. The timing diagrams previously presented are valid for all cycles performed in Test Mode.

MODE DEPENDENT ON CAS AND W WHEN RAS FALLS

Mode	CAS	W*
Read, Write, RMW, FPM	1	0
CBR Refresh, Test Mode Exit	0	1
Test Mode Entry	0	0

*Logic state when RAS transitions low.

TEST MODE BLOCK DIAGRAM
(MCM516400B, MCM517400B)



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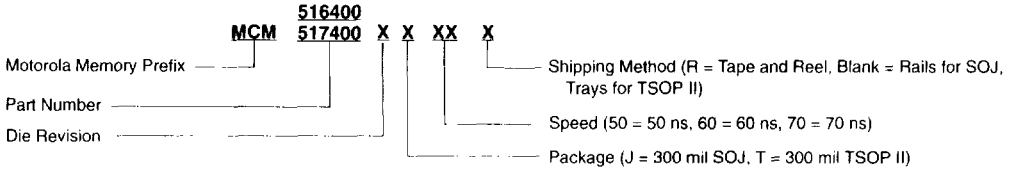
ORDERING INFORMATION
(Order by Full Part Number)



16M DEVICE NUMBERS

MCM516400BJ50	MCM517400BJ50
MCM516400BJ60	MCM517400BJ60
MCM516400BJ70	MCM517400BJ70
MCM516400BT50	MCM517400BT50
MCM516400BT60	MCM517400BT60
MCM516400BT70	MCM517400BT70
MCM516400BJ50R	MCM517400BJ50R
MCM516400BJ60R	MCM517400BJ60R
MCM516400BJ70R	MCM517400BJ70R
MCM516400BT50R	MCM517400BT50R
MCM516400BT60R	MCM517400BT60R
MCM516400BT70R	MCM517400BT70R

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