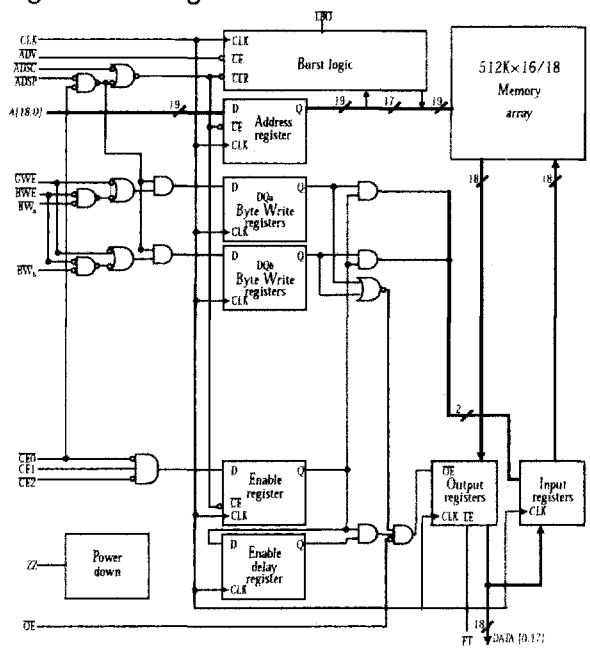
3.3V 512K×16/18 pipeline burst synchronous SRAM

Features

- Organization: 524,288 words × 16 or 18 bits
- Fast clock speeds to 166 MHz in LVTTL/LVCMOS
- Fast clock to data access: 3.5/3.8/4/5 ns
- Fast $\overline{OE}$ access time: 3.5/3.5/3.8/4 ns
- Fully synchronous register-to-register operation
- Single register 'flow-through' mode
- Single cycle de-select
- Pentium® compatible architecture and timing
- Synchronous and asynchronous output enable control
- Multiple packaging options
  - Economical 100-pin TQFP package
  - Chip-scale fBGA package for smallest footprint
- Byte write enables
- Clock enable for operation hold
- Multiple chip enables for easy expansion
- 3.3 core power supply
- 2.5V or 3.3V I/O operation with separate V_{DDQ}
- Automatic power down: 10 mW typical standby power

Logic block diagram



Pin arrangement

For information on the pin arrangement for the TQFP package, refer to the section entitled "Pin arrangement for TQFP (top view)" on page 3.

For information on the pin arrangement for the chip-scale fBGA package, refer to the section entitled "Pin arrangement for chip-scale fBGA (top view)" on page page 3.

Selection guide

	7C3512K18-3.5	7C3512K18-3.8	7C3512K18-4	7C3512K18-5	Units
Minimum cycle time	6	6.7	7.5	10	ns
Maximum pipelined clock frequency	166.7	150	133.3	100	MHz
Maximum pipelined clock access time	3.5	3.8	4	5	ns
Maximum operating current	350	325	300	250	mA
Maximum standby current	60	60	60	60	mA
Maximum CMOS standby current (DC)	5	5	5	5	mA

Functional description

The AS7C3512K18P family is a high performance CMOS 8 Mbit synchronous Static Random Access Memory (SRAM) organized as 524,288 words × 16 or 18 bits and incorporates a two stage register-register pipeline for highest frequency on any given technology. This architecture is suited for ASIC, DSP (TMS320C6X), and PowerPC based systems in computing, datacomm, instrumentation, and telecommunications systems.

Fast cycle times of 6/6.7/7.5/10 ns with clock access times (t_{CD}) of 3.5/3.5/3.8/4 ns enable 167, 150, 133 and 100 MHz bus frequencies. Three chip enable inputs permit easy memory expansion. Burst operation is initiated in one of two ways: the controller address strobe ($\overline{ADSC}$), or the processor address strobe ($\overline{ADSP}$). The burst advance pin ($\overline{ADV}$) allows subsequent internally generated burst addresses.

Read cycles are initiated with $\overline{ADSP}$ (regardless of $\overline{WE}$ and $\overline{ADSC}$) using the new external address clocked into the on-chip address register when $\overline{ADSP}$ is sampled Low, the chip enables are sampled active, and the output buffer is enabled with $\overline{OE}$. In a read operation the data accessed by the current address, registered in the address registers by the positive edge of CLK, are carried to the data-out registers and driven on the output pins on the next positive edge of CLK. $\overline{ADV}$ is ignored on the clock edge that samples $\overline{ADSP}$ asserted, but is sampled on all subsequent clock edges. Address is incremented internally for the next access of the burst when $\overline{WE}$ is sampled High, $\overline{ADV}$ is sampled Low, and both address strobes are High. Burst operation is selectable with the MODE input. With MODE unconnected or driven High, burst operations use a Pentium count sequence. With MODE driven LOW the device uses a linear count sequence, suitable for PowerPC and many other applications.

Write cycles are performed by disabling the output buffers with $\overline{OE}$ and asserting a write command. A global write enable $\overline{GWE}$ writes all 18 bits regardless of the state of individual $\overline{BW[a:b]}$ inputs. Alternately, when $\overline{GWE}$ is High, one or more bytes may be written by asserting $\overline{BWE}$ and the appropriate individual byte $\overline{BW}$ signal(s).

$\overline{BWn}$ is ignored on the clock edge that samples $\overline{ADSP}$ Low, but is sampled on all subsequent clock edges. Output buffers are disabled when $\overline{BWn}$ is sampled LOW (regardless of $\overline{OE}$). Data is clocked into the data input register when $\overline{BWn}$ is sampled Low. Address is incremented internally to the next burst of address if $\overline{BWn}$ and $\overline{ADV}$ are sampled Low.

Read or write cycles may also be initiated with $\overline{ADSC}$ instead of $\overline{ADSP}$. The differences between cycles initiated with $\overline{ADSC}$ and $\overline{ADSP}$ follow.

- $\overline{ADSP}$ must be sampled HIGH when $\overline{ADSC}$ is sampled LOW to initiate a cycle with $\overline{ADSC}$.
- $\overline{WE}$ signals are sampled on the clock edge that samples $\overline{ADSC}$ LOW (and $\overline{ADSP}$ High).
- Master chip select $\overline{CE0}$ blocks $\overline{ADSP}$, but not $\overline{ADSC}$.

The AS7C3512K18P family operates from a 3.3V supply. I/O's use a separate power supply that can operate at 2.5V or 3.3V. This device is available in a 100-pin 14×20 mm TQFP and 119 ball fine-pitch Ball-Grid-Array (fBGA) packaging.

Capacitance [1]

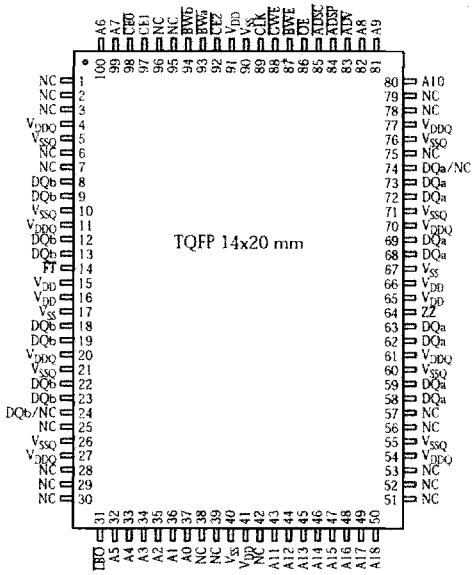
Parameter	Symbol	Signals	Test conditions	Max	Unit
Input capacitance	C_{IN}	Address and control pins	V_{in} = 0V	5	pF
I/O capacitance	$C_{I/O}$	I/O pins	V_{in} = V_{out} = 0V	7	pF

Write enable truth table (per byte)

$\overline{GWE}$	$\overline{BWE}$	$\overline{BWn}$	WRITEn
L	X	X	T
X	L	L	T
H	H	X	F
H	L	H	F [†]

Key: X = Don't Care, L = Low, H = High.
[†] Valid read.

Pin arrangement for TQFP (top view)



Note: Pins 24, 74 are NC for ×16.

Pin arrangement for chip-scale fBGA (top view)

	1	2	3	4	5	6	7
A	Vddq	A	A	$\overline{adsp}$	A	A	Vddq
B	nc	CE1	A	$\overline{adsc}$	A	A	nc
C	nc	A	A	Vdd	A	A	nc
D	DQb	nc	Vss	nc	Vss	DQPb	nc
E	nc	DQb	Vss	$\overline{CE0}$	Vss	nc	DQa
F	Vddq	nc	Vss	$\overline{OE}$	Vss	DQa	Vddq
G	nc	DQb	$\overline{BWb}$	$\overline{ADV}$	Vss	nc	DQa
H	DQb	nc	Vss	$\overline{GWE}$	Vss	DQa	nc
J	Vddq	Vdd	nc	Vdd	nc	Vdd	Vddq
K	nc	DQb	Vss	Clk	Vss	nc	DQa
L	DQb	nc	Vss	nc	$\overline{BWa}$	DQa	nc
M	Vddq	DQb	Vss	$\overline{BWE}$	Vss	nc	Vddq
N	DQb	nc	Vss	A	Vss	nc	nc
P	nc	DQPd	Vss	A	Vss	nc	DQa
R	nc	A	$\overline{LBO}$	Vdd	$\overline{FT}$	A	nc
T	nc	A	A	nc	A	A	ZZ
U	Vddq	nc	nc	nc	nc	nc	Vddq

Note: Pins 2D, 6D are NC for ×16.

Signal descriptions

Signal	I/O	Properties	Description
CLK	I	CLOCK	Clock. All inputs except $\overline{OE}$ are synchronous to this clock.
A0–A18	I	SYNC	Address. Sampled when all chip enables are active and $\overline{ADSC}$ or $\overline{ADSP}$ are asserted.
DQ[a,b]	I/O	SYNC	Data. Driven as output when the chip is enabled and $\overline{OE}$ is active.
$\overline{CE0}$	I	SYNC	Master chip enable. Sampled on clock edges when $\overline{ADSP}$ or $\overline{ADSC}$ is active. When $\overline{CE0}$ is inactive, $\overline{ADSP}$ is blocked. Refer to the SYNCHRONOUS TRUTH TABLE for more information.
CE1, $\overline{CE2}$	I	SYNC	Synchronous chip enables. Active HIGH and active Low, respectively. Sampled on clock edges when $\overline{ADSC}$ is active or when $\overline{CE1}$ and $\overline{ADSP}$ are active.
$\overline{ADSP}$	I	SYNC	Address strobe (processor). Asserted LOW to load a new address or to enter standby mode.
$\overline{ADSC}$	I	SYNC	Address strobe (controller). Asserted LOW to load a new address or to enter standby mode.
$\overline{ADV}$	I	SYNC	Burst advance. Asserted LOW to continue burst read/write.
$\overline{GWE}$	I	SYNC default = HIGH	Global write enable. Asserted LOW to write all 18 bits. When High, $\overline{BWE}$ and $\overline{WE0}$–$\overline{WE3}$ control write enable. *This signal is internally pulled High.*
$\overline{BWE}$	I	SYNC default = LOW	Byte write enable. Asserted LOW with $\overline{GWE}$ = HIGH to enable effect of $\overline{WE0}$–$\overline{WE3}$ inputs. *This signal is internally pulled Low.*
$\overline{BW[a,b]}$	I	SYNC	Write enables. Used to control write of individual bytes when $\overline{GWE}$ = HIGH and $\overline{BWE}$ = Low. If either of $\overline{BW[a:b]}$ is active with $\overline{GWE}$ = HIGH and $\overline{BWE}$ = LOW, the cycle is a write cycle. If both $\overline{BW[a:b]}$ are inactive, the cycle is a read cycle.
$\overline{OE}$	I	ASYNC	Asynchronous output enable. I/O pins are driven when $\overline{OE}$ is active and the chip is synchronously enabled.
$\overline{LBO}$	I	STATIC default = HIGH	Count mode. When driven High, count sequence follows Intel XOR convention. When driven Low, count sequence follows linear convention. *This signal is internally pulled High.*[18]
$\overline{FT}$	I	STATIC	Flow-through mode.When low, enables single register flow-through mode. Connect to V_{DD} if unused or for pipelined operation.
ZZ	I	ASYNC	Sleep. Places device in low power mode; data is retained. Connect to GND if unused.

Absolute maximum ratings

Parameter	Symbol	Min	Max	Unit
Power supply voltage relative to GND	V_{DD}, V_{DDQ}	–0.5	+4.6	V
Input voltage relative to GND (input pins)	V_{IN}	–0.5	+4.6	V
Input voltage relative to GND (I/O pins)	V_{IN}	–0.5	V_{DDQ} + 0.5	V
Power dissipation	P_D	–	1.3	W
DC output current	I_{OUT}	–	30	mA
Storage temperature (plastic)	T_{stg}	–65	+150	°C
Temperature under bias	T_{bias}	–65	+135	°C

Stresses greater than those listed under **Absolute Maximum Ratings** may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions may affect reliability.

Synchronous truth table

$\overline{CE0}$	CE1	$\overline{CE2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	WRITE$_n$[†]	$\overline{OE}$	Address accessed	CLK	Operation
H	X	X	X	L	X	X	X	NA	L to H	Deselect
L	L	X	L	X	X	X	X	NA	L to H	Deselect
L	L	X	H	L	X	X	X	NA	L to H	Deselect
L	X	H	L	X	X	X	X	NA	L to H	Deselect
L	X	H	H	L	X	X	X	NA	L to H	Deselect
L	H	L	L	X	X	F	L	External	L to H	Begin read
L	H	L	L	X	X	F	H	External	L to H	Begin read
L	H	L	H	L	X	F	L	External	L to H	Begin read
L	H	L	H	L	X	F	H	External	L to H	Begin read
X	X	X	H	H	L	F	L	Next	L to H	Cont. read
X	X	X	H	H	L	F	H	Next	L to H	Cont. read
X	X	X	H	H	H	F	L	Current	L to H	Suspend read
X	X	X	H	H	H	F	H	Current	L to H	Suspend read
H	X	X	X	H	L	F	L	Next	L to H	Cont. read
H	X	X	X	H	L	F	H	Next	L to H	Cont. read
H	X	X	X	H	H	F	L	Current	L to H	Suspend read
H	X	X	X	H	H	F	H	Current	L to H	Suspend read
L	H	L	H	L	X	T	X	External	L to H	Begin write
X	X	X	H	H	L	T	X	Next	L to H	Cont. write
H	X	X	X	H	L	T	X	Next	L to H	Cont. write
X	X	X	H	H	H	T	H	Current	L to H	Suspend write
H	X	X	X	H	H	T	H	Current	L to H	Suspend write

Key: X = Don't Care, L = Low, H = High.
[†]See Write enable truth table for more information.

Recommended operating conditions

Parameter		Symbol	Min	Nominal	Max	Unit
Supply voltage		V_{DD}	3.0	3.3	3.6	V
		GND	0.0	0.0	0.0	V
I/O supply voltage		V_{DDQ}	2.375	2.5 or 3.3	3.6	V
		GND_Q	0.0	0.0	0.0	V
Input voltages	Address and control pins	V_{IH}	2.0	–	4.5	V
		V_{IL}	-0.5*	–	0.8	V
	I/O pins	V_{IH}	2.0	–	V_{DDQ} + 0.3	V
		V_{IL}	-0.5*	–	0.8†	V
Ambient operating temperature		T_A	0	–	70	℃

* V_{IL} min = -2.0V for pulse width less than 0.2 x t_{RC}.
† For 2.5V V_{DDQ} operation, V_{IL} = 0.7V max.

DC electrical characteristics over operating range

			-3.5		-3.8		-4		-5		
Parameter	Symbol	Test conditions	Min	Max	Min	Max	Min	Max	Min	Max	Unit
Input leakage current	$\lvert I_{LI} \rvert$	V_{DD} = Max, V_{in} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{OE} \geq V_{IH}$, V_{DD} = Max, V_{out} = GND to V_{DD}	–	2	–	2	–	2	–	2	µA
Operating power supply current	I_{CC}	$\overline{CE}$ = V_{IL}, CE = V_{IH}, $\overline{CE}$ = V_{IL}, f = f_{max}, I_{out} = 0 mA	–	350	–	325	–	300	–	250	mA
Standby power supply current	I_{SB}	Deselected, f = f_{max}	–	60	–	60	–	60	–	60	mA
	I_{SB1}	Deselected, f = 0, all $V_{IN} \leq$ 0.2V or $\geq V_{DD}$ - 0.2V	–	5	–	5	–	5	–	5	mA
Output voltage	V_{OL}	I_{OL} = 8 mA, V_{DDQ} = 3.6V	–	0.4	–	0.4	–	0.4	–	0.4	V
	V_{OH}	I_{OH} = -8 mA, V_{DDQ} = 3.0V	2.4	–	2.4	–	2.4	–	2.4	–	V

Timing characteristics over operating range

		-3.5		-3.8		-4		-5			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Unit	Notes
Clock frequency	F_{MAX}	-	166	-	150	-	133	-	100	MHz	1
Cycle time (pipelined mode)	t_{CYC}	6	-	6.6	-	7.5	-	10	-	ns	
Cycle time (flow-through mode)	t_{CYCF}	7.5	-	10	-	12	-	15	-	ns	
Clock access time (pipelined mode)	t_{CD}	-	3.5	-	3.8	-	4	-	5	ns	
Clock access time (flow-through mode)	t_{CDF}	-	6	-	6.6	-	7.5	-	10	ns	
Output enable Low to data valid	t_{OE}	-	3.5	-	3.5	-	3.8	-	4	ns	
Clock High to output Low Z	t_{LZC}	0	-	0	-	0	-	0	-	ns	8
Data output hold from clock High	t_{OH}	1.5	-	1.5	-	1.5	-	2	-	ns	8
Output enable Low to output Low Z	t_{LZOE}	1	-	1	-	1.5	-	2	-	ns	8
Output enable High to output High Z	t_{HZOE}	-	3	-	3.5	-	4	-	4	ns	8
Clock High to output High Z	t_{HZC}	-	2.5	-	3	-	3.5	-	3.5	ns	8
Clock High to output High Z	t_{HZCN}	-	1.5	-	1.5	-	2	-	2.5	ns	1,9
Clock High pulse width	t_{CH}	2.4	-	2.6	-	2.8	-	3	-	ns	
Clock Low pulse width	t_{CL}	2.4	-	2.6	-	2.8	-	3	-	ns	
Address and Control setup to clock High	t_{AS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Data setup to clock High	t_{DS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Write setup to clock High	t_{WS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Chip select setup to clock High	t_{CSS}	1	-	1.3	-	1.5	-	1.5	-	ns	
Address hold from clock High	t_{AH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Data hold from clock High	t_{DH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Write hold from clock High	t_{WH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Chip select hold from clock High	t_{CSH}	0.5	-	0.5	-	0.5	-	0.5	-	ns	
Output rise time (0 pF load)	t_R	1.5	-	1.5	-	1.5	-	1.5	-	V/ns	1
Output fall time (0 pF load)	t_F	1.5	-	1.5	-	1.5	-	1.5	-	V/ns	1

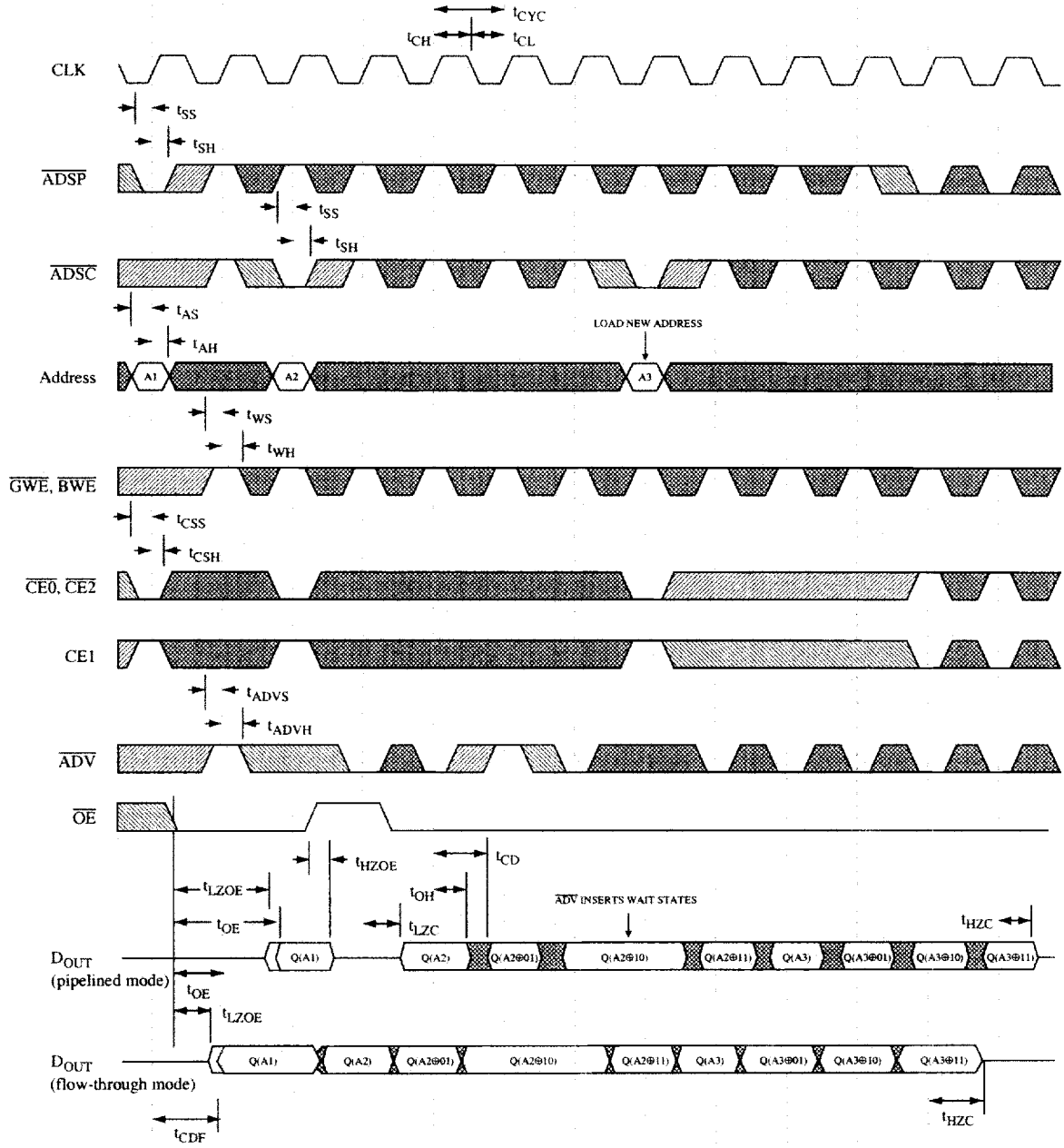
See "Notes" on page 10.

SRAM

Key to switching waveforms

Rising input Falling input Undefined output/don't care

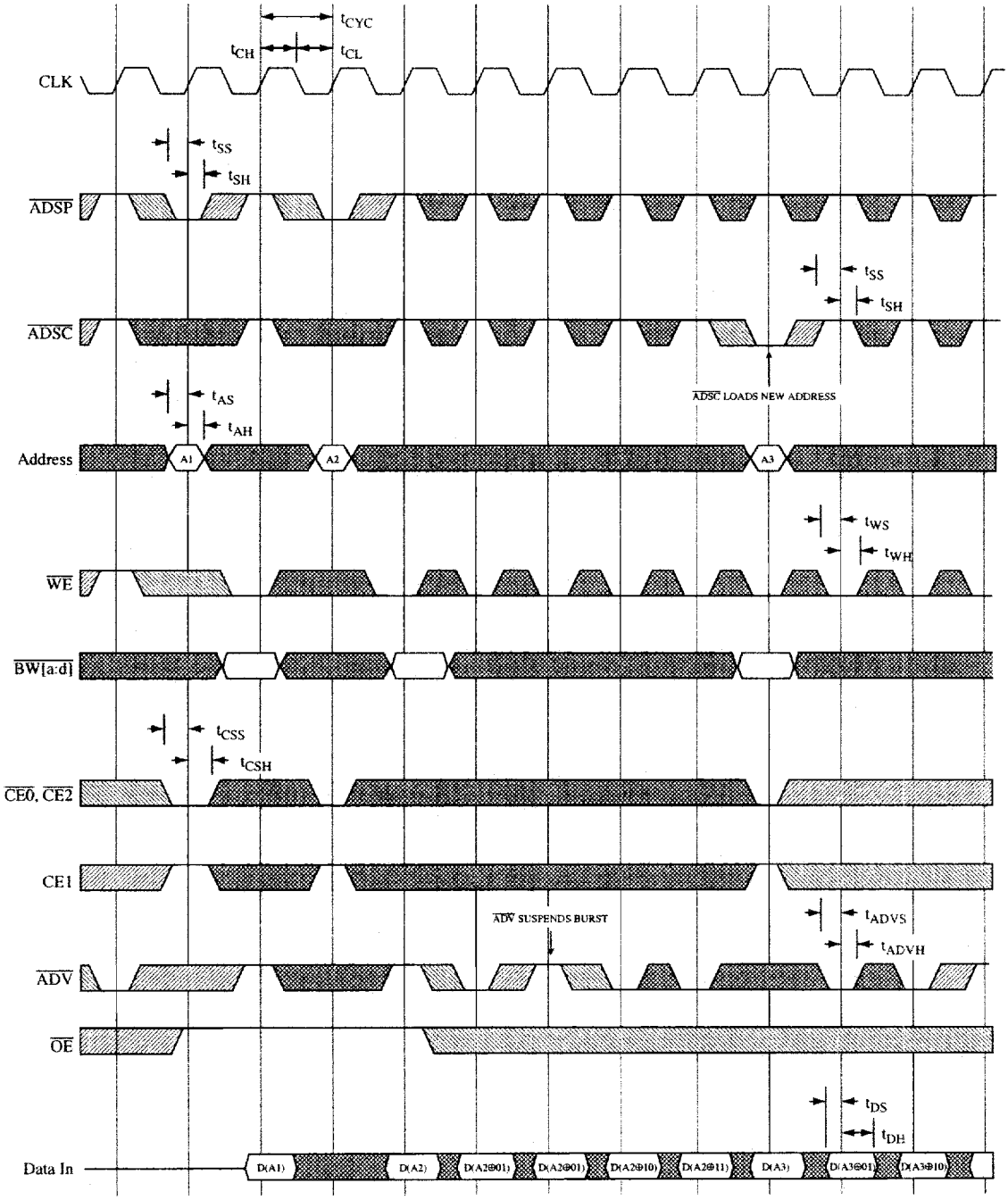
Timing waveform of read cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.
$\overline{WE}$[0:3] is don't care.

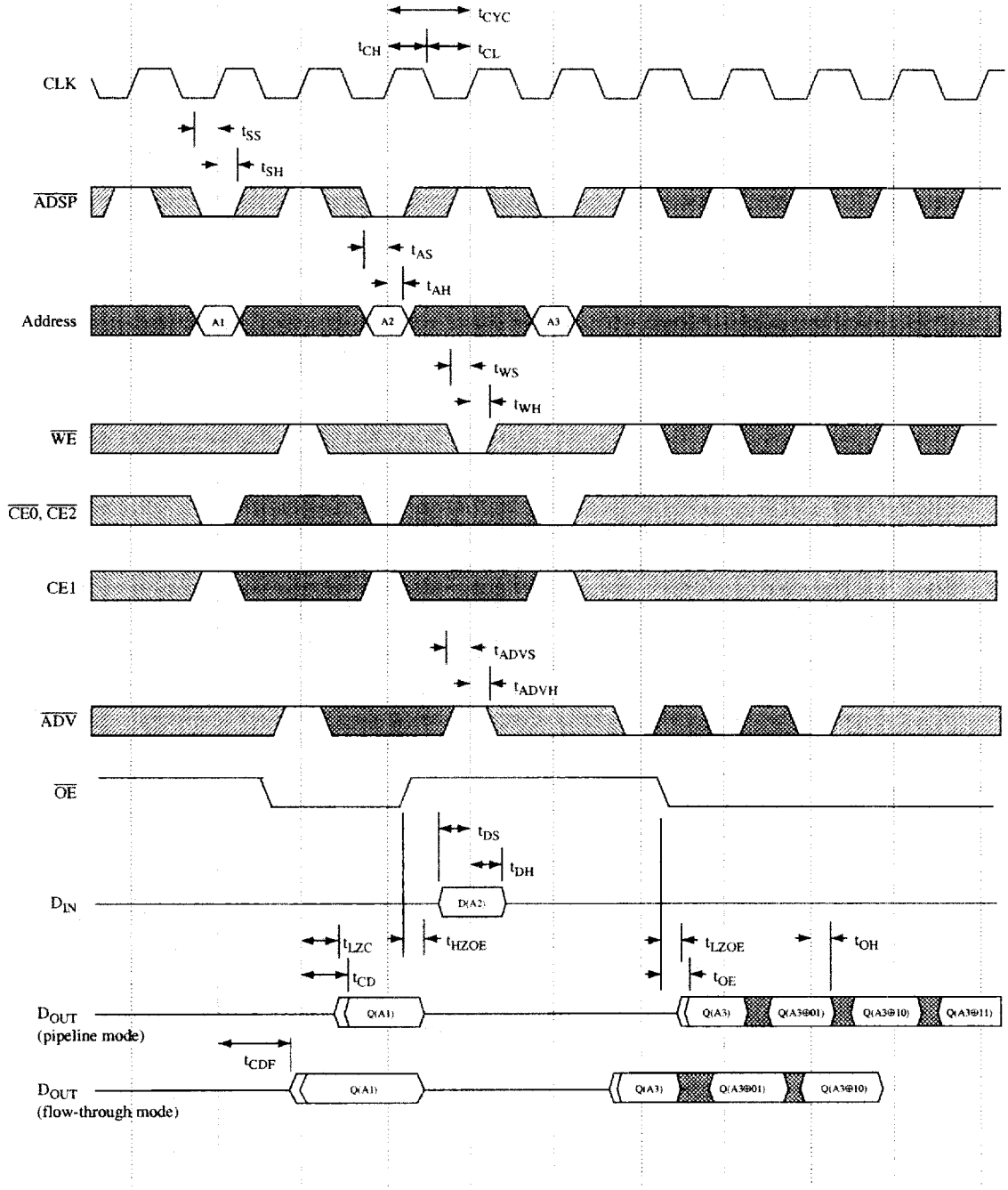
SRAM

Timing waveform of write cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.

Timing waveform of read/write cycle



Note: ⊕ = XOR when MODE = High/No Connect; ⊕ = ADD when MODE = Low.

Notes

1 This parameter is guaranteed but not tested.
2 For test conditions, see AC Test Conditions, Figures A, B, C.
3 This parameter is sampled and not 100% tested.
4 This is a synchronous device. All addresses must meet the specified setup and hold times for all rising edges of CLK. All other synchronous inputs must meet the setup and hold times with stable logic levels for all rising edges of CLK when chip is enabled.
5 Typical values measured at 3.3V, 25 ℃ and 10 ns cycle time.
6 I_{CC} given with no output loading. I_{CC} increases with faster cycle times and greater output loading.
7 Transitions are measured ±500 mV from steady state voltage. Output loading specified with C_L = 5 pF as in Figure C.
8 t_{HZOE} is less than t_{LZOE}; and t_{HZC} is less than t_{LZC} at any given temperature and voltage.
9 t_{HZCN} is a 'no load' parameter to indicate exactly when SRAM outputs have stopped driving.

AC test conditions

- Output Load: see Figure B,
  except for t_{LZC}, t_{LZOE}, t_{HZOE}, t_{HZC} see Figure C.
- Input pulse level: GND to 3V. See Figure A.
- Input rise and fall time (Measured at 0.3V and 2.7V): 2 ns. See Figure A.
- Input and output timing reference levels: 1.5V.

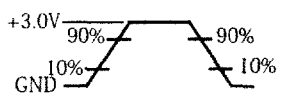


Figure A: Input waveform

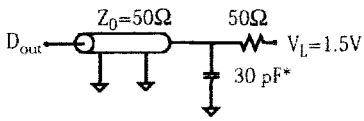


Figure B: Output load (A)

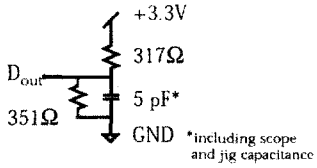


Figure C: Output load(B)

AS7C3512K18P and AS7C3512K16P ordering information

Package	Width	166 MHz	150 MHz	133 MHz	100 MHz
TQFP	×16	AS7C3512K16P-3.5TQC	AS7C3512K16P-3.8TQC	AS7C3512K16P-4TQC	AS7C3512K16P-5TQC
TQFP	×18	AS7C3512K18P-3.5TQC	AS7C3512K18P-3.8TQC	AS7C3512K18P-4TQC	AS7C3512K18P-5TQC
fBGA	×16	AS7C3512K16P-3.5BC	AS7C3512K16P-3.8BC	AS7C3512K16P-4BC	AS7C3512K16P-5BC
fBGA	×18	AS7C3512K18P-3.5BC	AS7C3512K18P-3.8BC	AS7C3512K18P-4BC	AS7C3512K18P-5BC

AS7C3512K18P and AS7C3512K16P part numbering system

AS7C	3	512K18	Z	-XX	XX	C
SRAM prefix	Operating voltage	Part number, organization	Timing Z=ZBT timing P=PBSRAM	Access time (ns)	Package: TQ = TQFP B = fBGA	Commercial temperature, 0 ℃ to 70 ℃

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Pentium is a trademark of Intel Corporation.