Zero Power CMOS Hard Array Logic ZHAL™ 20A Series

Features/Benefits

- **Zero standby power**
- **25-ns maximum propagation delay**
- **HC and HCT compatible**
- **Space saving PLCC available**
- **Low power alternative for Small and Medium 20-pin PAL® devices, including 16L8/16R8/16R6/16R4**

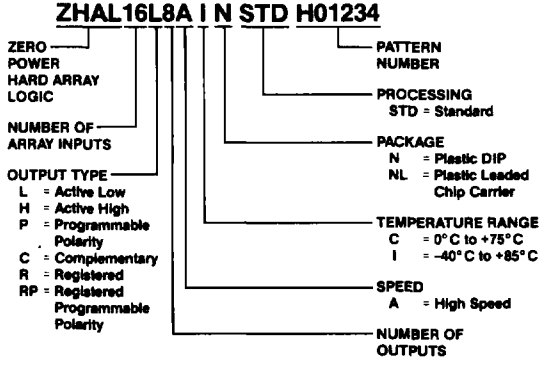
Description

The Zero Power Hard Array Logic (ZHAL) devices are ideal in low-power applications that require high-speed operation. These attributes are achieved through the use of Monolithic Memories' advanced high-speed CMOS process. Now system designers have the option of using a ZHAL device that matches fast PAL device speeds, but with the added advantage of zero standby power. These features are ideal for power-critical areas such as portable digital equipment or lap-top computers.

This family of ZHAL devices utilizes a unique architecture that is designed for a high degree of flexibility in implementing most patterns of the listed 20-pin PAL/HAL® devices. Prototyping can be done using standard PAL devices before converting to ZHAL circuits for production. ZHAL devices are fabricated by Monolithic Memories with custom metallization masks defined by a user-supplied HAL Design Specification.

Ordering Information

PART NUMBER	PACKAGE	ARRAY	OUTPUTS	
			COMB	REG
ZHAL10H8A	N, NL	10	8	—
ZHAL12H6A		12	6	—
ZHAL14H4A		14	4	—
ZHAL16H2A		16	2	—
ZHAL16C1A		16	2	—
ZHAL10L8A		10	8	—
ZHAL12L6A		12	6	—
ZHAL14L4A		14	4	—
ZHAL16L2A		16	2	—
ZHAL16L8A	N, NL	16	8	—
ZHAL16R8A		16	—	8
ZHAL16R6A		16	2	6
ZHAL16R4A		16	4	4
ZHAL16P8A	N, NL	16	8	—
ZHAL16RP8A		16	—	8
ZHAL16RP6A		16	2	6
ZHAL16RP4A		16	4	4



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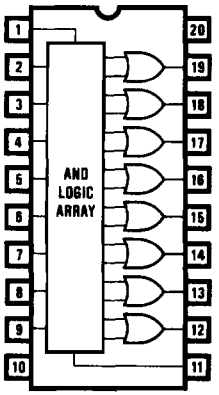

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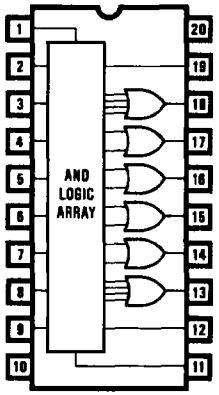

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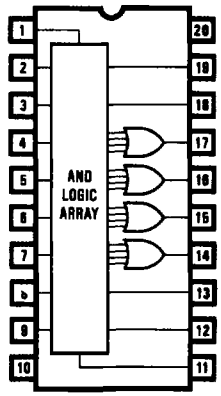

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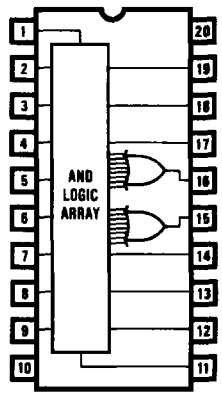

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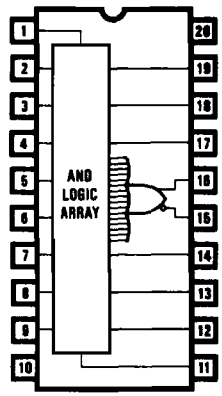

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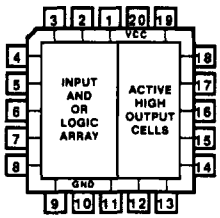

Plastic Chip Carrier

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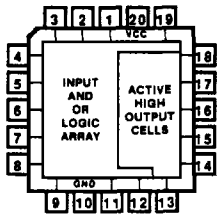

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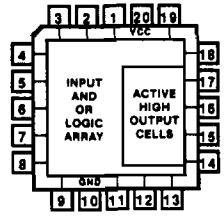

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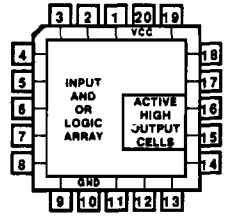

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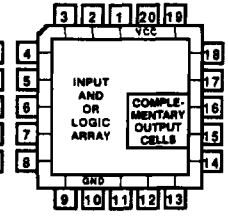

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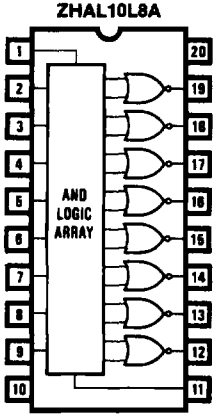

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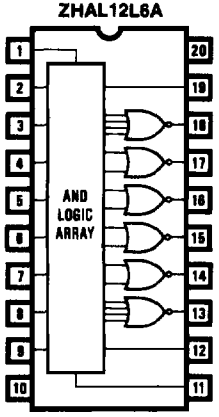

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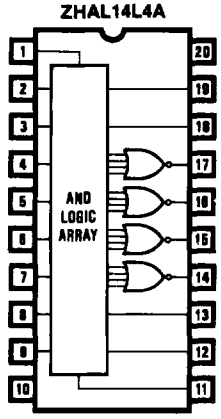

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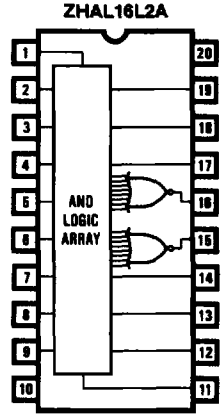

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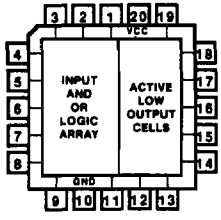

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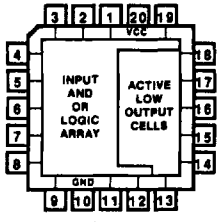

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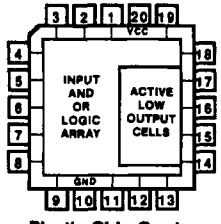

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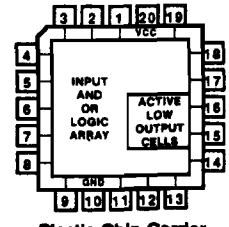

Plastic Chip Carrier

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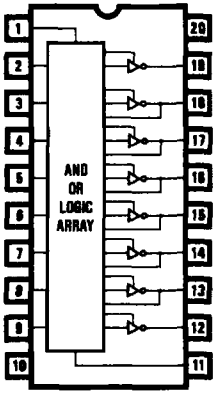

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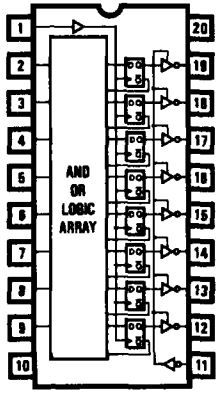

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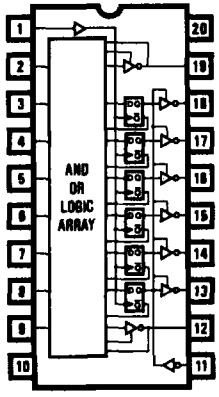

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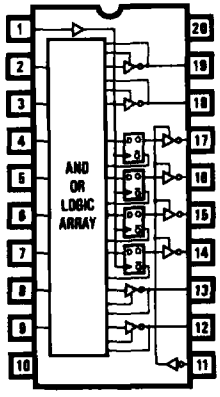

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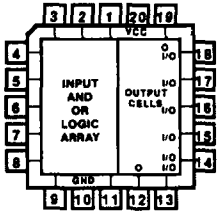

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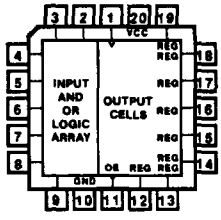

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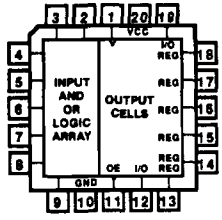

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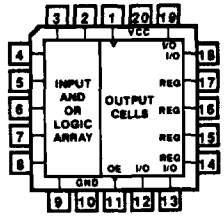

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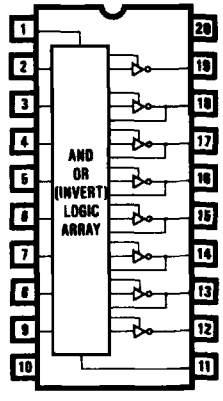

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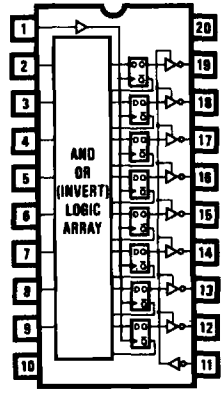

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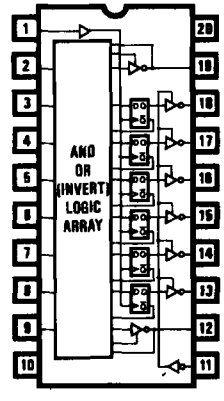

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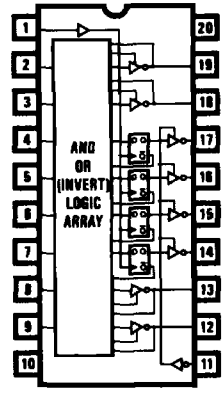

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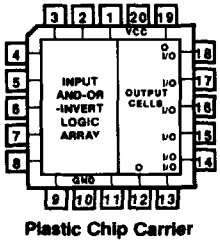

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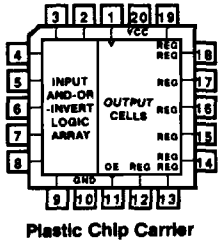

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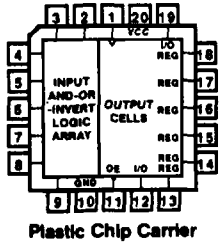

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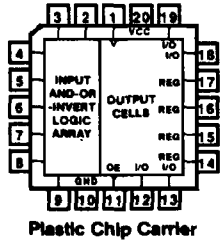


Plastic Chip Carrier

Operating Conditions

SYMBOL	PARAMETER		INDUSTRIAL MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
t_w	Width of clock	16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A	15	10		15	10		ns
t_{su}	Setup time from input or feedback to clock		20	13		20	13		ns
t_h	Hold time		0	-10		0	-10		ns
T_A	Operating free-air temperature		-40	25	85	0	25	75	°C

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IL}[1]	Low-level input voltage				0		0.8	V
V_{IH}[1]	High-level input voltage				2		V_{CC}	V
I_{IL}	Low-level input current		V_{CC} = MAX	V_I = GND			-1	μA
I_{IH}	High-level input current	Pin 8[2]	V_{CC} = MAX	V_I = V_{CC}		1	10	μA
		All other pins					1	μA
V_{OL}	Low-level output voltage		V_{CC} = MIN	I_{OL} = 8 mA		0.1	0.4	V
			V_{CC} = 5 V	I_{OL} = 1 μA			0.05	
V_{OH}	High-level output voltage		V_{CC} = MIN	I_{OH} = -6 mA	3.76[3]	4.1		V
			V_{CC} = 5 V	I_{OH} = -1 μA	4.95			
I_{OZL}[3]	Off-state output current		V_{CC} = MAX	V_O = GND		0	-10	μA
I_{OZH}[3]				V_O = V_{CC}		0	10	μA
I_{CC}	Standby supply current[4]		I_O = 0 mA, V_I = GND or V_{CC}			0	100	μA
	Operating supply current		f = 1 MHz, I_O = 0 mA, V_I = GND or V_{CC}			2	5[5]	mA

Switching Characteristics Over Operating Conditions

SYMBOL	PARAMETER		TEST CONDITIONS (See Test Load)	INDUSTRIAL MIN	TYP	MAX	COMMERCIAL MIN	TYP	MAX	UNIT
t_{PD}	Input or feedback to output 10H8A, 12H6A, 14H4A, 16H2A, 16C1A, 10L8A, 12L6A, 14L4A 16L2A, 16L8A, 16R6A, 16R4A, 16P8A, 16RP6A, 16RP8A		R_L = 1 KΩ C_L = 50 pF		15	25		15	25	ns
t_{CLK}	Clock to output or feedback 16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A				10	15		10	15	ns
t_{PZX}	Input to output enable	16L8A, 16R4A, 16R6A, 16P8A, 16RP4A, 16RP6A			12	25		12	25	ns
t_{PXZ}[6]	Input to output disable				14	25		14	25	ns
t_{PXZ}[6] t_{PZX}	Pin 11 to output disable/enable	16R4A, 16R6A, 16R8A, 16RP4A, 16RP6A, 16RP8A			12	15		12	15	ns
f_{MAX}	Maximum frequency			28.5	40		28.5	40		MHz

Notes. Apply to electrical and switching characteristics.

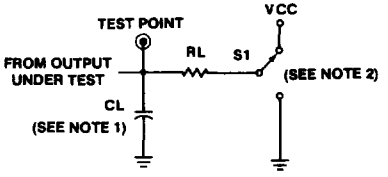
1. These are absolute voltages with respect to the ground pin on the device and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
2. Pin 8 (PRELOAD pin). Applies to all devices whether registered or non-registered.
3. JEDEC standard no. 7 for high-speed CMOS devices.
4. Disable output pins = V_{CC} or GND.
5. Add 3 mA per additional 1.0 MHz of operation over 1 MHz.
6. C_L = 5 pF.

5

Absolute Maximum Ratings

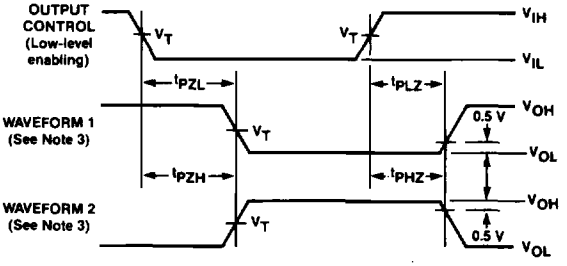
Supply voltage, V_{CC} ..... -0.5 V to 7 V
DC input voltage, V_I ..... -0.5 V to V_{CC} +0.5 V
DC output voltage, V_O ..... -0.5 V to V_{CC} +0.5 V
DC output source/sink current per output pin, I_O ..... ±35 mA
DC V_{CC} or ground current, I_{CC} or I_{GND} ..... ±100 mA
Input diode current, I_{IK}:
V_I<0 ..... -20 mA
V_I>V_{CC} ..... +20 mA
Output diode current, I_{OK}:
V_O<0 ..... -20 mA
V_O>V_{CC} ..... +20 mA
Storage temperature ..... -65°C to 150°C

Switching Test Load

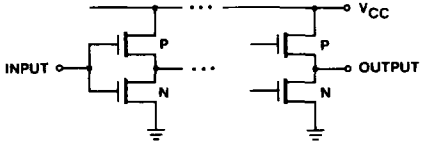


Notes 1. CL includes probe and jig capacitance.
2. When measuring t_{PLZ} and t_{PZL}, S1 is tied to V_{CC}.
When measuring t_{PHZ} and t_{PZH}, S1 is tied to ground.
t_{PZX} is measured with C_L = 50 pF. t_{PXZ} is measured with C_L = 5 pF.
When measuring propagation delay times of 3-state outputs, S1 is open, i.e., not connected to V_{CC} or ground.
3. Waveform 1 is for an output with internal conditions such that the output is Low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is High except when disabled by the output control.

Enable/Disable Delay



Schematic of Inputs and Outputs



Output Register PRELOAD†

The PRELOAD function allows the register to be loaded from data placed on the output pins. This feature aids functional testing of state sequencer designs by allowing direct setting of output states for improved test coverage. The procedure for PRELOAD is as follows:

1. Raise V_{CC} to 4.5 V.
2. Disable output registers by setting pin 11 to V_{IH}. Set pin 1 to 0 V.
3. Apply V_{IL}/V_{IH} to all registered output pins.
4. Pulse pin 8 to V_p (12 V), then back to 0 V.
5. Remove V_{IL}/V_{IH} from all registered output pins.
6. Lower pin 11 to V_{IL} to enable the output registers.
7. Verify for V_{OL}/V_{OH} at all registered output pins.

† Note. Only applies to parts with output registers.
Typical t_{sup} = 50 ns
t_{wp} = 100 ns
t_{hp} = 50 ns
I_{IH} = 30 μA (Pin 8)