# ANALOG DEVICES

# 28 V, 200 W Pulsed DC/DC Converter with Integral EMI Filter

## ADDC02808PB

## FEATURES
28 V dc Input, 8 V dc @ 25 A, 200 W Pulse Output
Integral EMI Filter
Ultrafast Transient Response
Minimal Output Voltage Deviation
Low Weight: 80 Grams
NAVMAT Derated
Many Protection and System Features

## APPLICATIONS
Distributed Power Architecture for Driving T/R Modules
Motor and Actuator Drivers

## FUNCTIONAL BLOCK DIAGRAM
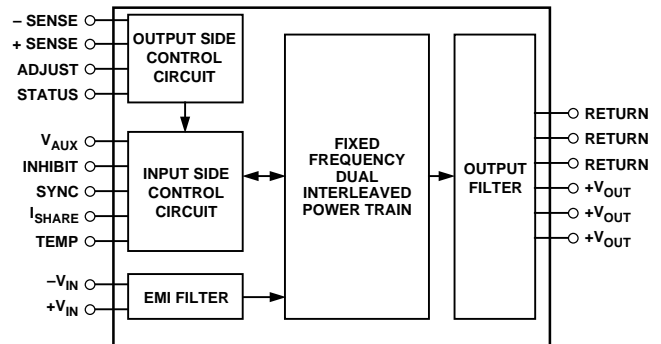


## GENERAL DESCRIPTION

The ADDC02808PB hybrid military dc/dc converter is compensated specifically for pulse applications where fast transient response and minimum output voltage deviation are required. It is also designed to deliver very high, pulsed output power. The unit is designed for high reliability and high performance applications where saving space and/or weight are critical.

The ADDC02808PB has been characterized over a wide variety of load conditions. Its transient response has been set to insure output stability over a broad range of load capacitance. For applications that require factory modified compensation optimized for a specific load, or for applications that require a different output voltage than 8 V dc, contact the factory.

The ADDC02808PB is available in a hermetically sealed, molybdenum based hybrid package and is easily heatsink mountable. For MIL-STD-883 devices, contact the factory for availability.

## PRODUCT HIGHLIGHTS

1. 120 W/cubic inch pulsed power density with an integral EMI filter

2. Ultrafast transient response time with minimum output voltage deviation

3. Light weight: 80 grams

4. Operational and survivable over a wide range of input conditions: 16 V–50 V dc; survives low line, high line

5. High reliability; NAVMAT derated

6. Protection features include:
   Output Overvoltage Protection
   Output Short Circuit Current Protection
   Thermal Monitor/Shutdown
   Input Overvoltage Shutdown
   Input Transient Protection

7. System level features include:
   Current Sharing for Parallel Operation
   Logic Level Disable
   Output Status Signal
   Synchronization for Multiple Units
   Input Referenced Auxiliary Voltage Supply

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# ADDC02808PB–SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS ($T_C$ = +25°C, $V_{IN}$ = 28 V dc ±0.5 V dc, unless otherwise noted; full temperature range is −55°C to +90°C; all temperatures are case and $T_C$ is the temperature measured at the center of the package bottom.)

| Parameter | Case Temp | Test Level | Conditions | ADDC02808PB Min | Typ | Max | Units |
|---|---|---|---|---|---|---|---|
| **INPUT CHARACTERISTICS** | | | | | | | |
| Steady State Operating Input Voltage Range[1] | Full | VI | $I_O$ = 1.25 A to 25 A Pulsed | 18 | 28 | 40 | V |
| Abnormal Operating Input Voltage Range (Per MIL-STD-704D)[1] | Full | VI | $I_O$ = 1.25 A to 25 A Pulsed | 16 | | 50 | V |
| Input Overvoltage Shutdown | +25°C | I | | 50 | 52.5 | 55 | V |
| No Load Input Current | +25°C | VI | | | 45 | 100 | mA |
| Disabled Input Current | +25°C | VI | | | 1 | 5 | mA |
| **OUTPUT CHARACTERISTICS[2, 3]** | | | | | | | |
| Output Voltage ($V_O$) | +25°C | I | $I_O$ = 1.25 A to 25 A, $V_{IN}$ = 18 V to 40 V dc | 7.92 | 8.00 | 8.08 | V |
| | Full | VI | $I_O$ = 1.25 A to 25 A, $V_{IN}$ = 18 V to 40 V dc | 7.84 | | 8.16 | V |
| | Full | VI | $I_O$ = 1.25 A to 20 A, $V_{IN}$ = 16 V to 50 V dc | 7.84 | | 8.16 | V |
| Line Regulation | +25°C | VI | $I_O$ = 25 A Pulsed, $V_{IN}$ = 18 V to 40 V dc | | 1 | 5 | mV |
| Load Regulation | +25°C | VI | $V_{IN}$ = 28 V dc, $I_O$ = 1.25 A to 25 A Pulsed | | 2.5 | 10 | mV |
| Output Ripple/Noise[4] | +25°C | I | $I_O$ = 25 A, 5 kHz – 2 MHz BW | | 40 | 60 | mV p-p |
| Output Current ($I_O$)[5] | Full | VI | $V_{IN}$ = 18 V to 40 V dc, Pulsed | 1.25 | | 25 | A |
| Output Overvoltage Protection | +25°C | V | $I_O$ = 25 A, Open Remote Sense Connection | | 120 | | % $V_O$ nom |
| Output Current Limit | +25°C | V | $V_O$ = 90% $V_{OUT}$ Nom | | 130 | | % $I_O$ max |
| Output Short Circuit Current | +25°C | I | 45 m$\Omega$ ≤ $R_{SHORT}$ Circuit ≤ 60 m$\Omega$ | | | 40 | A |
| **ISOLATION CHARACTERISTICS** | | | | | | | |
| Isolation Resistance | +25°C | I | Input to Output or Any Pin to Case at 500 V dc | 100 | | | M$\Omega$ |
| **DYNAMIC CHARACTERISTICS[4]** | | | | | | | |
| Step Changes In Load (min to max) | +25°C | I | (Reference Section Entitled "Transient Response") | | | | |
| Step Changes In Load (max to min) | | | (Reference Section Entitled "Response at End of Pulse") | | | | |
| Soft Start Turn-On Time | +25°C | I | $I_O$ = 25 A, From Inhibit High to Status High | | | 10 | ms |
| **THERMAL CHARACTERISTICS** | | | | | | | |
| Efficiency | +25°C | I | $I_O$ = 12.5 A | 79 | 80 | | % |
| | Full | VI | $I_O$ = 12.5 A | 78 | | | % |
| | +25°C | I | $I_O$ = 25 A | 75 | 76 | | % |
| | Full | VI | $I_O$ = 25 A | 72.5 | | | % |
| Hottest Junction Temperature[5] | +90°C | V | $I_O$ = 25 A | | | 110 | °C |
| **CONTROL CHARACTERISTICS** | | | | | | | |
| Clock Frequency | Full | VI | $I_O$ = 2 A | 0.85 | | 0.99 | MHz |
| ADJUST (Pin 3) V ADJ | +25°C | I | | 3.1 | 3.2 | 3.3 | V |
| STATUS (Pin 4) | | | | | | | |
| $V_{OH}$ | +25°C | I | $I_{OH}$ = 400 μA | 2.4 | 4.0 | | V |
| $V_{OL}$ | +25°C | I | $I_{OL}$ = 1 mA | | 0.15 | 0.7 | V |
| $V_{AUX}$ (Pin 5) | | | | | | | |
| $V_O$ (nom) | +25°C | I | $I_{AUX}$ = 5 mA, Load Current = 12.5 A | 14.9 | 15.15 | 15.4 | V |
| INHIBIT (Pin 6) | | | | | | | |
| $V_{IL}$ | +25°C | I | | | | 0.5 | V |
| $I_{IL}$ | +25°C | I | $V_{IL}$ = 0.5 V | | | 1.2 | mA |
| $V_I$ (Open Circuit) | +25°C | I | | | | 15 | V |
| SYNC (Pin 7)[6] | | | | | | | |
| $V_{IH}$ | +25°C | I | | 4.0 | | | V |
| $I_{IH}$ | +25°C | I | $V_{IH}$ = 7.0 V | | | 150 | μA |
| $I_{SHARE}$ (Pin 8) | +25°C | I | $I_O$ = 20 A | 2.45 | 2.55 | 2.65 | V |
| TEMP (Pin 9) | +25°C | V | | | 3.90 | | V |

NOTES

[1] 50 V dc upper limit rated for transient condition of up to 50 ms. 16 V dc lower limit rated for continuous operation during emergency condition. Steady state and abnormal input voltage range require source impedance sufficient to insure input stability at low line. See sections entitled System Instability Considerations and Input Voltage Range.

[2] Measured at the remote sense points.

[3] Unit regulates output voltage to zero load; tests performed at low continuous load and 200 W pulsed load.

[4] $C_{LOAD}$ = 1,000 μF. Output ripple/noise measured at converter output; may be smaller at external load capacitance. Unit is stable for $C_{LOAD}$ ranging from 500 μF to 4,000 μF.

[5] Refer to section entitled "Pulse Output Power vs. Pulse Length" for more information.

[6] Unit has internal pull-down; refer to section entitled Pin 7 (SYNC).

Specifications subject to change without notice.

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## ABSOLUTE MAXIMUM RATINGS*

INHIBIT . . . . . . . . . . . . . . . . . . . . . . . . 50 V dc, –0.5 V dc
SYNC . . . . . . . . . . . . . . . . . . . . . . . . . 8.0 V dc, –0.5 V dc
$I_{SHARE}$ . . . . . . . . . . . . . . . . . . . . . . . . 6 V dc, –0.5 V dc
TEMP . . . . . . . . . . . . . . . . . . . . . . . . 12 V dc, –0.3 V dc
Common-Mode Voltage, Input to Output . . . . . . . . 500 V dc
Lead Soldering Temp (10 sec) . . . . . . . . . . . . . . . . . . +300°C
Storage Temperature . . . . . . . . . . . . . . . . . . –65°C to +150°C
Maximum Junction Temperature . . . . . . . . . . . . . . . . +150°C
Maximum Case Operating Temperature . . . . . . . . . . +125°C

*Absolute maximum ratings are limiting values, to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied. Exposure of absolute maximum rating conditions for extended periods of time may affect device reliability.

## ORDERING GUIDE

| Device | Operating Temperature Range (Case) | Description |
|---|---|---|
| ADDC02808PBKV | –40°C to +85°C | Hermetic Package |
| ADDC02808PBTV | –55°C to +90°C | Hermetic Package |
| ADDC02808PBTV/883B* | –55°C to +125°C | Hermetic Package |

*Contact factory.

## EXPLANATION OF TEST LEVELS

**Test Level**

I – 100% production tested.

II – 100% production tested at +25°C, and sample tested at specified temperatures.

III – Sample tested only.

IV – Parameter is guaranteed by design and characterization testing.

V – Parameter is a typical value only.

VI – All devices are 100% production tested at +25°C. 100% production tested at temperature extremes for military temperature devices; guaranteed by design and characterization testing for industrial devices.

## PIN DESCRIPTIONS

| Pin No. | Name | Function |
|---|---|---|
| 1 | –SENSE | Feedback loop connection for remote sensing output voltage. Must always be connected to output return for proper operation. |
| 2 | +SENSE | Feedback loop connection for remote sensing output voltage. Must always be connected to $+V_{OUT}$ for proper operation. |
| 3 | ADJUST | Adjusts output voltage setpoint. |
| 4 | STATUS | Indicates output voltage is within ±5% of nominal. Active high referenced to –SENSE (Pin 1). |
| 5 | $V_{AUX}$ | Low level dc auxiliary voltage supply referenced to input return (Pin 10). |
| 6 | INHIBIT | Power Supply Inhibit. Active low and referenced to input return (Pin 10). |
| 7 | SYNC | Clock synchronization input for multiple units; referenced to input return (Pin 10). |
| 8 | $I_{SHARE}$ | Current share pin which allows paralleled units to share current typically within ±5% at full load; referenced to input return (Pin 10). |
| 9 | TEMP | Case temperature indicator and temperature shutdown override; referenced to input return (Pin 10). |
| 10 | $-V_{IN}$ | Input Return. |
| 11 | $+V_{IN}$ | +28 V Nominal Input Bus. |
| 12 | $+V_{OUT}$ | +8 V dc Output. |
| 13 | $+V_{OUT}$ | +8 V dc Output. |
| 14 | $+V_{OUT}$ | +8 V dc Output. |
| 15 | RETURN | Output Return. |
| 16 | RETURN | Output Return. |
| 17 | RETURN | Output Return. |

## PIN CONFIGURATION
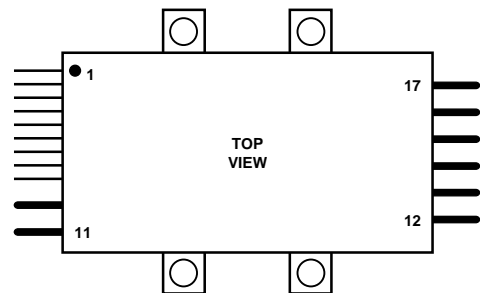
# ADDC02808PB–Typical Performance Curves
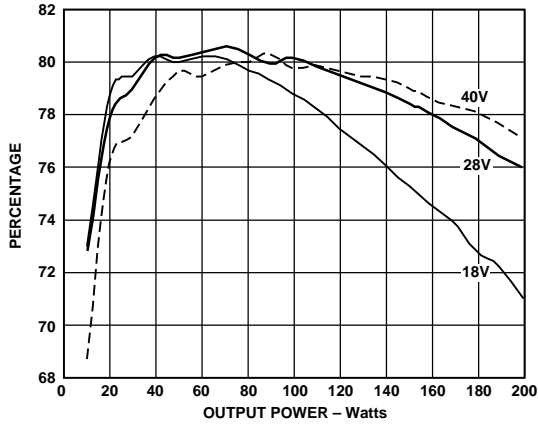


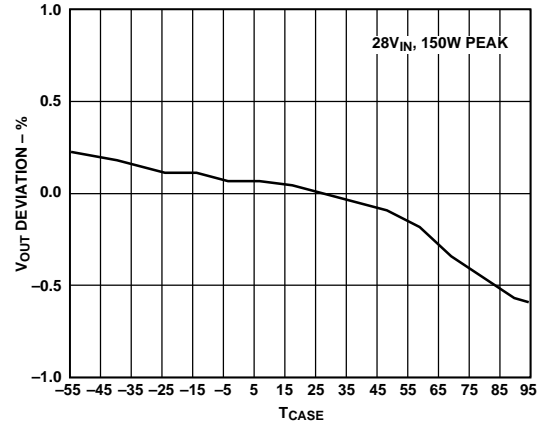Figure 1. Efficiency vs. Line and Load at +25°C (Load Pulse Width of 50 ms)
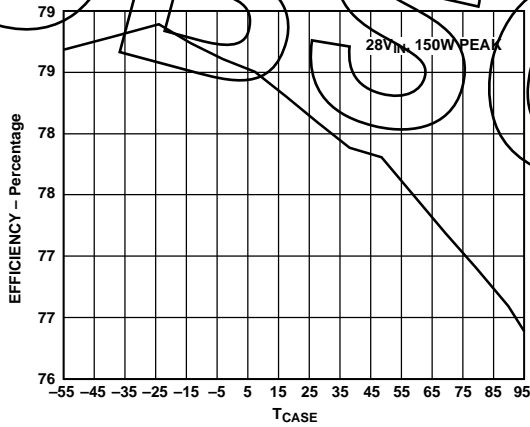


Figure 2. Efficiency vs. Case Temperature (°C) (at Nominal V_IN, 75% Max Load, Load Pulse Width of 50 ms)



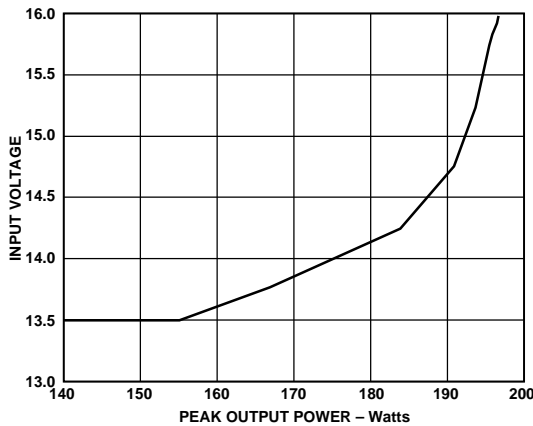Figure 3. Low Line Dropout vs. Load at 90°C Case Temperature (Load Pulse Width of 50 ms)



Figure 4. Output Voltage vs. Case Temperature (°C)



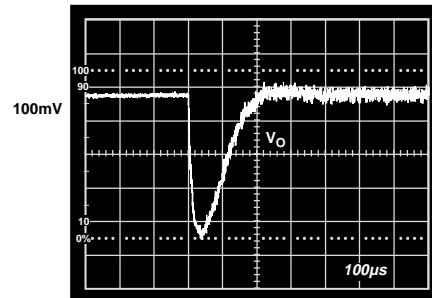Figure 5. Output Voltage Transient During Turn-On with 0.1 A Load Displaying Soft Start When Supply Is Enabled



Figure 6. Output Voltage Transient Response to a 1 A to 25 A Step Change in Load, di/dt = 12 A/μs, with 1,000 μF Load Capacitance ($R_{ESR}$ = 10 mΩ)
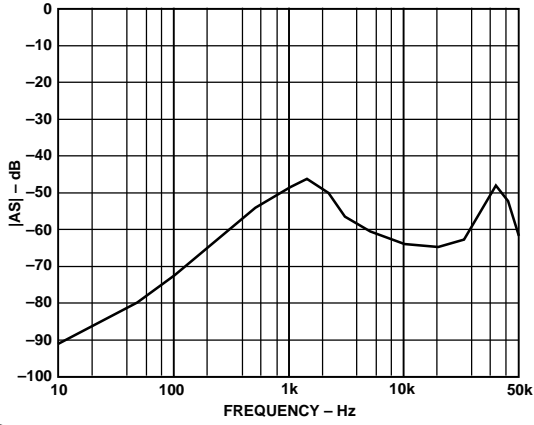
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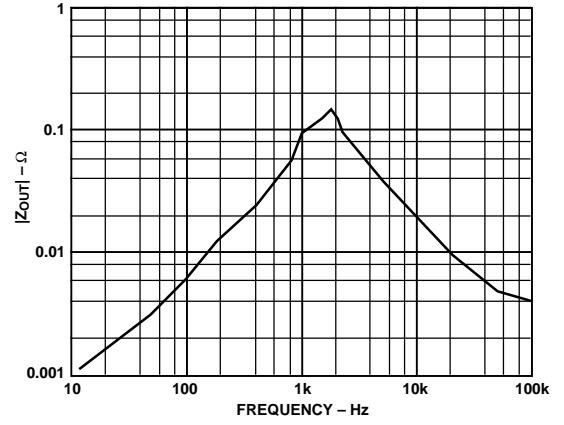Figure 7. Audio Susceptibility (Magnitude of $V_{OUT}/V_{IN}$)



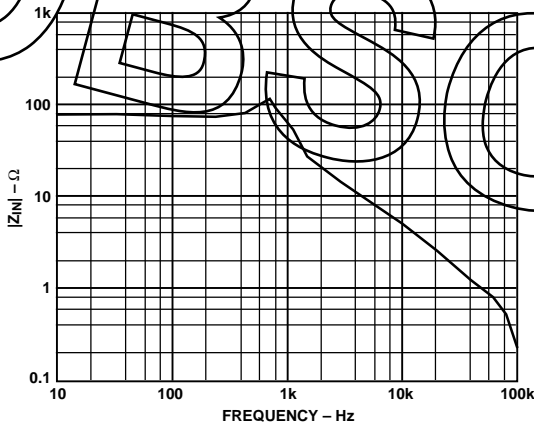Figure 9. Incremental Output Impedance (Magnitude)
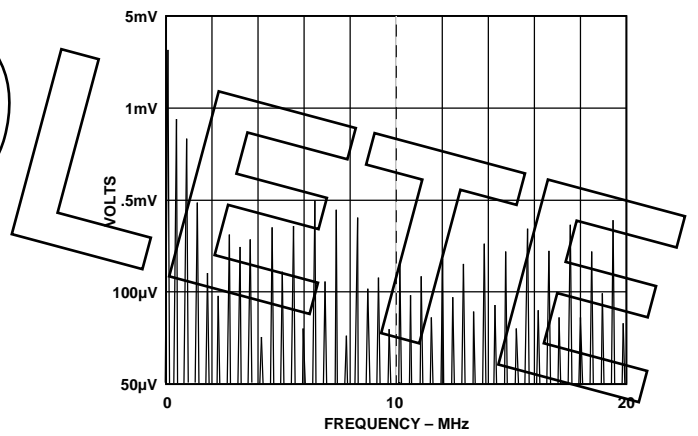


Figure 8. Incremental Input Impedance (Magnitude)



Figure 10. Output Frequency Spectrum
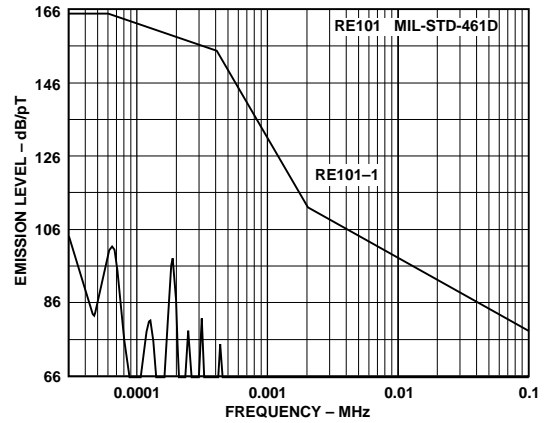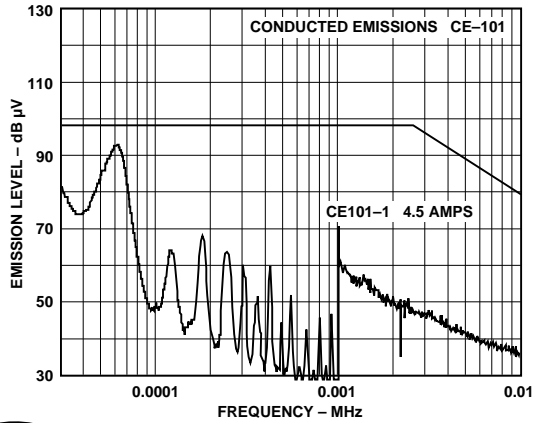
Figure 11. Conducted Emissions, MIL-STD-461D, CE101, +28 V Hot Line 100 W Load



Figure 13. Radiated Emissions, MIL-STD-461D, RE101, 100 W Load



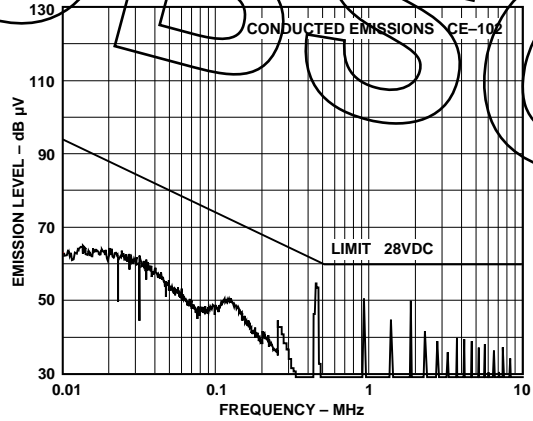Figure 12. Conducted Emissions, MIL-STD-461D, CE102, +28 V Hot Line 100 W Load


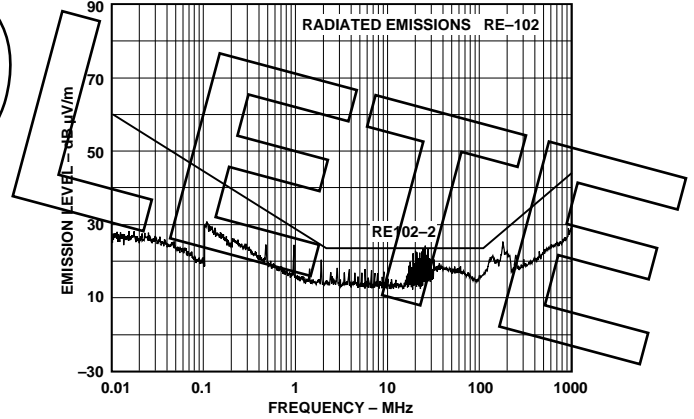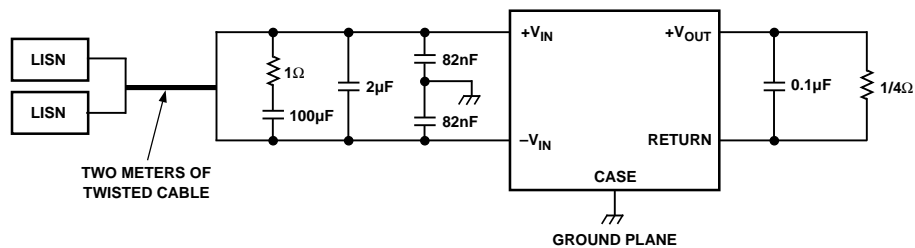
Figure 14. Radiated Emissions, MIL-STD-461D, RE102, Vertical Polarity, 100 W Load



NOTE: 100µF CAPACITOR AND 1Ω RESISTOR PROVIDE STABILIZATION FOR 100µH DIFFERENTIAL SOURCE INDUCTANCE INTRODUCED BY THE LISNs. REFER TO SECTION ON EMI CONSIDERATIONS FOR MORE INFORMATION.

Figure 15. Schematic of Test Setup for EMI Measurements

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## BASIC OPERATION

The ADDC02808PB converter uses a flyback topology with dual interleaved power trains operating 180° out of phase. Each power train switches at a fixed frequency of 500 kHz, resulting in a 1 MHz fixed switching frequency as seen at the input and output of the converter. In a flyback topology, energy is stored in the inductor during one half portion of the switching cycle and is then transferred to the output filter during the next half portion. With two interleaved power trains, energy is transferred to the output filter during both halves of the switching cycle, resulting in smaller filters to meet the required ripple.

A five pole differential input EMI filter, along with a common-mode EMI capacitor and careful attention to layout parasitics, is designed to meet all applicable requirements in MIL-STD-461D when installed in a typical system setup. Due to the higher output level in this product compared to the 100 W continuous output products, input stability is more of a concern. As a result, the two inductors in the internal input EMI filter have smaller values of inductance to mitigate input stability concerns. The effectiveness of the internal input EMI filter is, therefore, slightly diminished compared to these other products. A more detailed discussion of CE102 and other EMI issues is included in the section entitled "EMI Considerations."

The maximum available peak power out is 200 W and is based on a combination of maximum junction temperatures, maximum pulse width, and maximum duty cycle. Refer to section entitled, "Pulsed Output Power vs. Pulse Length," for peak power derating curves for varying conditions.

The unit is compensated for ultrafast transient response with minimum output voltage deviation. The compensation has been optimized and output stability insured for an external load capacitance in the range of 500 μF, 20 mΩ ESR to 4,000 μF, 2.5 mΩ ESR. Peak performance and output stability are dependent on minimizing parasitic inductance and resistance in the connection from the converter to the load.

The converter uses current mode control and employs a high performance opto-isolator in its feedback path to maintain isolation between input and output. The control circuit is designed to give a nearly constant output current as the output voltage drops from $V_O$ nom to $V_{SC}$ during a short circuit condition. It does not let the current fold back below the maximum rated output current. The output overvoltage protection circuitry, which is independent from the normal feedback loop, protects the load against a break in the remote sense leads. Remote sense connections, which can be made at the load, can adjust for voltage drops of as much as 0.25 V dc between the converter and the load, thereby maintaining an accurate voltage level at the load.

An input overvoltage protection feature shuts down the converter when the input voltage exceeds (nominally) 52.5 V dc.

An internal temperature sensor shuts down the unit and prevents it from becoming too hot if the heat removal system fails. The temperature sensed is the case temperature and is factory set to trip at a nominal case temperature of 110°C to 115°C. The shut down temperature setting can be raised externally or disabled by the user.

Each unit has an INHIBIT pin that can be used to turn off the converter. This feature can be used to sequence the turn-on of multiple converters and to reduce input power draw during extended time in a no load condition.

A SYNC pin, referenced to the input return line (Pin 10), is available to synchronize multiple units to one switching frequency. This feature is particularly useful in eliminating beat frequencies which may cause increased output ripple on paralleled units. A current share pin ($I_{SHARE}$) is available which permits paralleled units to share current typically within 5% at full load.

A low level dc auxiliary voltage supply referenced to the input return line is provided for miscellaneous system use.

## PULSED OUTPUT POWER VS. PULSE LENGTH

The maximum specified pulsed output power in the standard configuration of the ADDC02808PB is 200 W. This limit is based on issues of working down to the minimum input voltage, of providing a reasonable short circuit current limit, and so on. However, this power level assumes that the junction temperatures of the converter's power semiconductor devices have not exceeded 110°C. For short pulse lengths and low duty cycles, this condition will be met. Otherwise, the pulsed output power will have to be reduced to keep the junction temperatures below 110°C if NAVMAT guidelines are to be followed.

Figures 16 and 17 show the tradeoff that must be made between the highest allowable pulsed output power and the pulse length. Notice that for each curve, as the pulse length is made longer, the pulsed power that causes a 110°C junction temperature to be reached is lower. The curves are provided for two baseplate temperatures (25°C and 90°C) and three average output powers. The duty cycle that corresponds to any point on a curve can be calculated by dividing the average power by the pulsed power for that point. The curves represent typical upper limits; operation anywhere below the curves is acceptable and will result in cooler junctions.

The ADDC02808PB is designed to deliver a continuous 100 watts to its output while keeping its hottest junction temperature below 110°C with a baseplate temperature of 90°C.
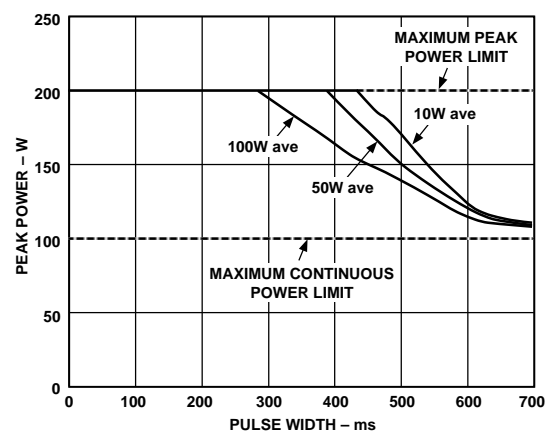


Figure 16. Largest On-State Power vs. Pulse Width that Maintains $T_{JMAX} \leq 110°C$ at 25°C Baseplate
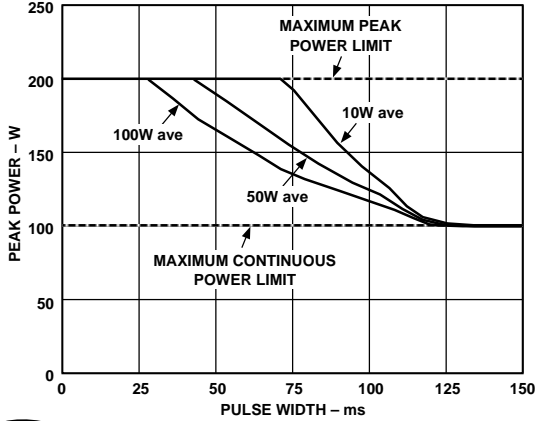
Figure 17. Largest On-State Power vs. Pulse Width that Maintains $T_{JMAX} \leq 110^\circ C$ at $90^\circ C$ Baseplate

## TRANSIENT RESPONSE

The standard ADDC02808PB is designed to deliver large changes, or pulses, in load current with minimum output voltage deviation and an ultrafast return to the nominal output voltage. The compensation of the feedback loop is optimized, and output stability is insured, for a broad range of external load capacitance extending from 500 µF ($R_{ESR}$ = 20 mΩ) to 4,000 µF ($R_{ESR}$ = 2.5 mΩ). The variables that impact pulse performance (the maximum output voltage deviation and the settling time) are:

1. Size of step change in the output current.
2. Amount of external load capacitance.
3. Internal compensation of the feedback loop (factory set).
4. Connection from converter output to load.

Extensive modeling of the converter with ADI proprietary software permits analysis and prediction of the impact each of these parameters has on the pulse response. The analyses in this data sheet are based on the load capacitance being comprised of 100 µF, 100 mΩ tantalum load capacitors such as the CSR21 style. Figure 18 is the prediction of the standard converter's response to a 24 A step change in load current (from 1 A to 25 A) with a load capacitance of 1,000 µF ($R_{ESR}$ = 10 mΩ). This is very close to the measured pulse response under the same conditions shown in Figure 6.
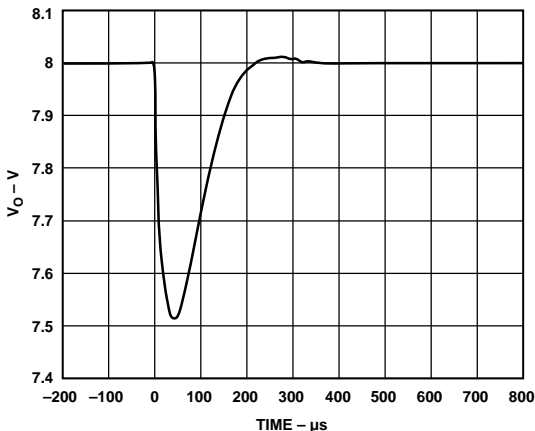


Figure 18. Predicted Response to 24 A Step Change in Load Current, di/dt = 12 A/µs, for $C_{LOAD}$ = 1,000 µF and $R_{ESR}$ = 10 mΩ
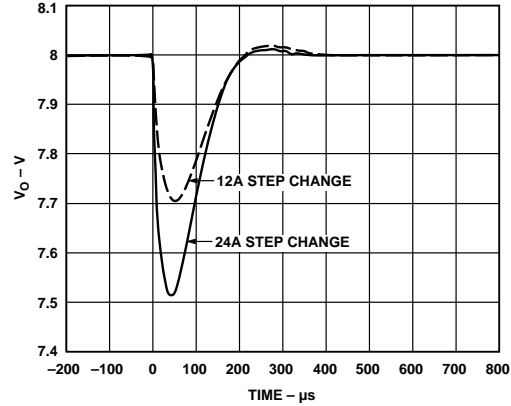


Figure 19. Predicted Response to 12 A and 24 A Step Change in Load Current, di/dt = 12 A/µs, for $C_{LOAD}$ = 1000 µF and $R_{ESR}$ = 10 mΩ

### Step Change

If the step change is less than 24 A, the pulse response will improve. For instance, with a 12 A step change, Figure 19 shows a comparison of the response for a 24 A step change and a 12 A step change in load.

### Load Capacitance

Varying the external load capacitance and associated $R_{ESR}$ between the range of $C_{LOAD}$ = 500 µF ($R_{ESR}$ = 20 mΩ) and $C_{LOAD}$ = 4,000 µF ($R_{ESR}$ = 2.5 mΩ) results in the predicted waveforms shown in Figures 20, 21, and 22. As can be seen, the larger the capacitor, the smaller the deviation, but the longer the settling time. Table I lists the maximum output voltage deviations and settling times for the four combinations of $C_{LOAD}$ and $R_{ESR}$ mentioned above. Note that these are based on the standard compensation for the feedback loop.

**Table I. Output Response to a 24 A (1 A–25 A) Step in Load Current (Standard Compensation)**

| $C_{LOAD}$ | $R_{ESR}$ | Typical Deviation | Settling Time (Within 1%) | See Figure |
|---|---|---|---|---|
| 500 µF | 20 mΩ | –7% | 150 µs | 20 |
| 1,000 µF | 10 mΩ | –6% | 175 µs | 18 |
| 2,000 µF | 5 mΩ | –5% | 200 µs | 21 |
| 4,000 µF | 2.5 mΩ | –4% | 250 µs | 22 |
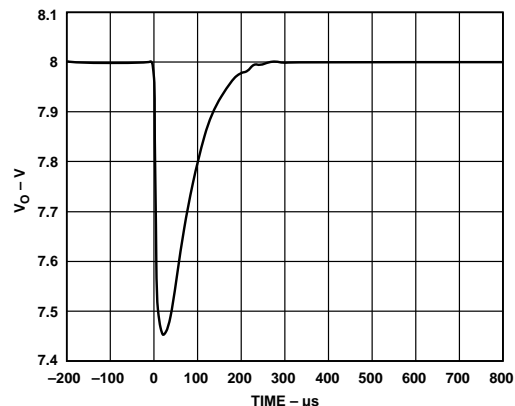


Figure 20. Predicted Response for 24 A Step Load Change in Load Current, di/dt = 12 A/µs, for $C_{LOAD}$ = 500 µF and $R_{ESR}$ = 20 mΩ
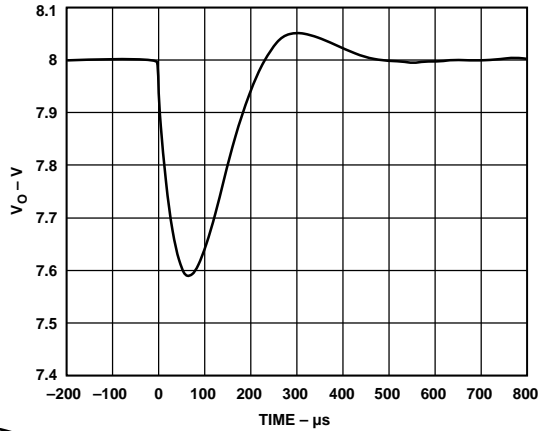
Figure 21. Predicted Response for 24 A Step Load Change in Load Current, di/dt = 12 A/µs, for $C_{LOAD}$ = 2,000 µF and $R_{ESR}$ = 5 mΩ
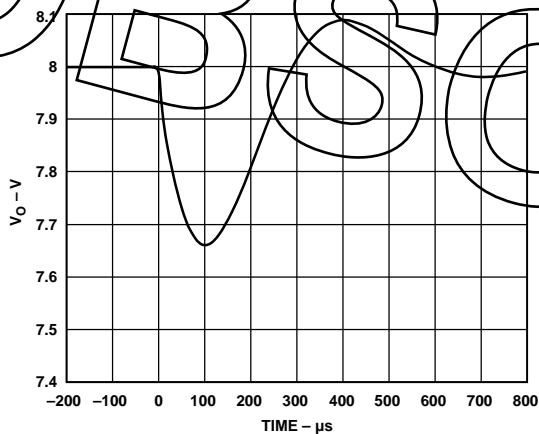


Figure 22. Predicted Response for 24 A Step Load Change in Load Current, di/dt = 12 A/µs, for $C_{LOAD}$ = 4,000 µF and $R_{ESR}$ = 2.5 mΩ

**Factory Set Internal Compensation**

If the user knows the external load capacitance and $R_{ESR}$ to be used in the application and if the application requires better pulse response than is summarized in Table I, then the internal feedback compensation can be modified at the factory to improve the transient response. In these instances, the compensation is optimized for a particular $C_{LOAD}$ at the expense of performing well over a broader range of $C_{LOAD}$. The predicted maximum output voltage deviation and settling times for factory-modified feedback compensation are shown in Figures 23, 24, and 25, and summarized in Table II, for three combinations of $C_{LOAD}$ and $R_{ESR}$. As can be seen, optimizing the compensation for a given load capacitance gives the best transient response in terms of both voltage deviation and settling time.

**Table II. Output Response to a 24 A (1 A-25 A) Step in Load Current (Compensation Optimized)**

| $C_{LOAD}$ | $R_{ESR}$ | Typical Deviation | Settling Time (Within 1%) | See Figure |
|---|---|---|---|---|
| 1,000 µF | 10 mΩ | –4% | 125 µs | 23 |
| 2,000 µF | 5 mΩ | –2.5% | 100 µs | 24 |
| 4,000 µF | 2.5 mΩ | –1% | 0 µs | 25 |

**Connection to Load**

Pulse performance is dependent on minimizing the parasitic impedances in the connection between the converter output and the load and external capacitors. Low inductance and low resistance connections should be used. Multilayer connections should be avoided to minimize stray capacitance. The converter should be placed as close to the load and external capacitors as possible.



Figure 23. Predicted Response for 24 A Step Load Change, di/dt = 12 A/µs, with Factory Set Internal Compensation Optimized for $C_{LOAD}$ = 1,000 µF and $R_{ESR}$ = 10 mΩ



Figure 24. Predicted Response for 24 A Step Load Change, di/dt = 12 A/µs, with Factory Set Internal Compensation Optimized for $C_{LOAD}$ = 2,000 µF and $R_{ESR}$ = 5 mΩ

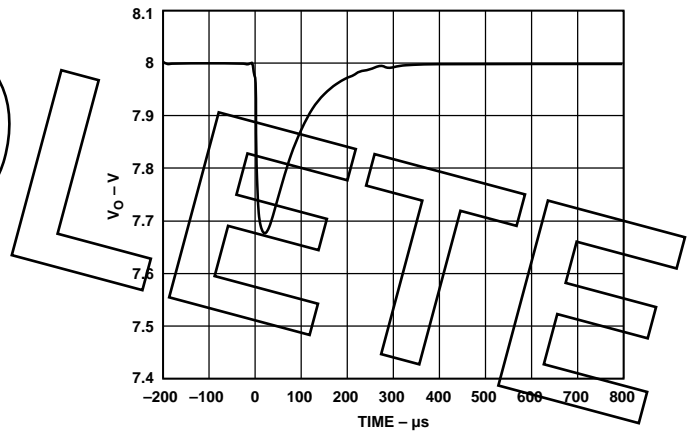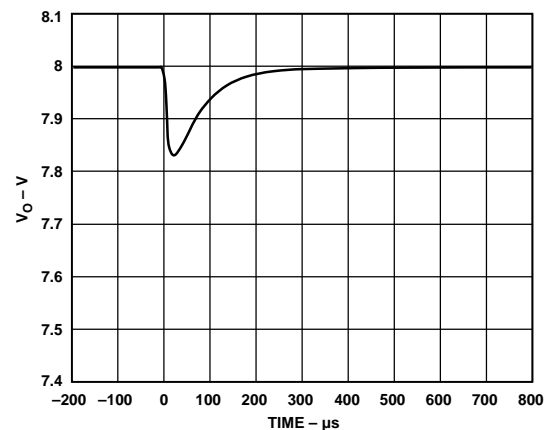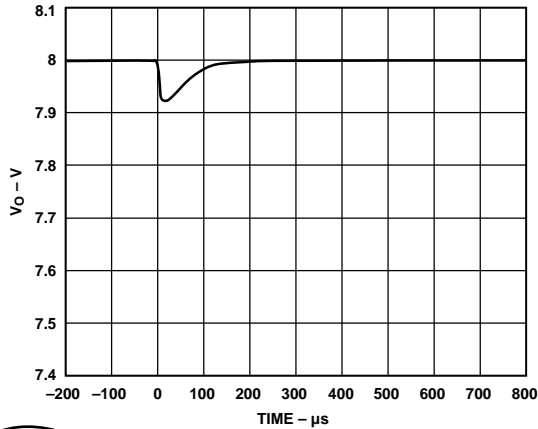*Figure 25. Predicted Response for 24 A Step Load Change, di/dt = 12 A/μs, with Factory Set Internal Compensation Optimized for $C_{LOAD}$ = 4,000 μF and $R_{ESR}$ = 2.5 mΩ*

## RESPONSE AT END OF PULSE

The previous section describes how the ADDC02808PB converter responds to the positive step change in load current that occurs at the beginning of a power pulse. This section will discuss the converter's response at the end of the power pulse when the load current is abruptly returned to a small value.

Figures 26-29 show the converter's measured output voltage as the load current is stepped from 25 A down to 4 A, 2 A, 1 A, and 0.1 A, respectively. The load capacitance is 1,000 μF with
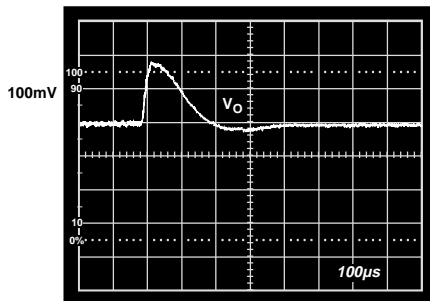


*Figure 26. Output Voltage Transient Response to a 25 A to 4 A Step Change in Load, di/dt/ = 12 A/μs, with 1,000 μF Load Capacitance ($R_{ESR}$ = 10 mΩ)*
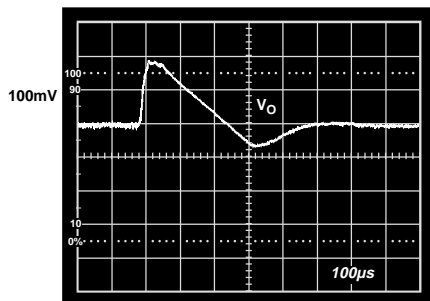


*Figure 27. Output Voltage Transient Response to a 25 A to 2 A Step Change in Load, di/dt/ = 12 A/μs, with 1,000 μF Load Capacitance ($R_{ESR}$ = 10 mΩ)*

$R_{ESR}$ = 10 mΩ. The di/dt is 12 A/μs. As can be seen, the peak deviations for these curves are close to each other and comparable to the negative deviation shown in Figure 6 for a similarly sized positive step change in load current.
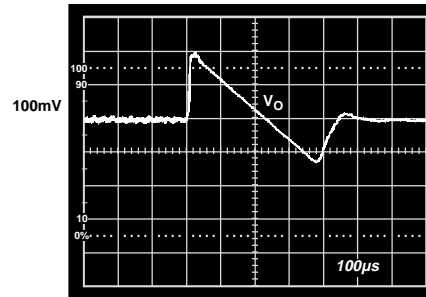


*Figure 28. Output Voltage Transient Response to a 25 A to 1 A Step Change in Load, di/dt/ = 12 A/μs, with 1,000 μF Load Capacitance ($R_{ESR}$ = 10 mΩ)*
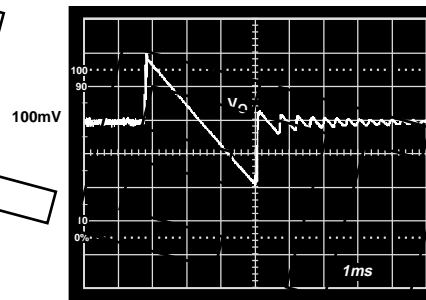


*Figure 29. Output Voltage Transient Response to a 25 A to 0.1 A Step Change in Load, di/dt/ = 12 A/μs, with 1,000 μF Load Capacitance ($R_{ESR}$ = 10 mΩ)*

What is different about these curves is the settling time. Once the converter's output voltage rises above nominal, the converter cannot help to discharge the load capacitor. It can only reduce its output current to zero; it cannot draw a negative current. As such, the time it takes to bring the output voltage back down to its nominal value depends on the load current during the low load portion of the cycle. The rate at which the output voltage falls to its nominal value is the load current divided by the load capacitance (including the 150 μF capacitance that is inside the converter). The smaller the load current, the longer it takes to get the output voltage back to its nominal value.

During the time that the output voltage is too high, the integrator in the converter's feedback circuitry is continuing to ramp out of range. As the output voltage then falls below its nominal value, it must have an undershoot error to bring the integrator back into range. As can be seen from these figures, the lower the load current, the longer the output voltage remains too high, and the longer and the greater the output voltage undershoot is.

Even when the load current steps down to 0.1 A, the maximum deviation of the output voltage is only about 400 mV, or 5%. However, it is important to realize that if the next power pulse occurs before this transient is over, then the output voltage will

not have the response depicted in the last section. This is because the feedback integrator will not have had time to return to its normal state, and so the converter's ability to respond to a positive step change in load current will be reduced. The maximum negative going deviation in the output voltage under this circumstance will then be greater than is shown in the figures of that section.

Should this situation arise, one approach would be to step the load current down to an intermediate value (e.g., 4 A) at the end of the power pulse, and then let this current decay to a smaller value (e.g., 0.1 A) with a time constant in the 100 μs to 200 μs range. This should permit a rapid return to a steady state condition at the end of the power pulse without requiring a large average load current during the low power portion of the cycle.

## PIN CONNECTIONS
### Pins 1 and 2 (±SENSE)
Pins 1 and 2 must always be connected for proper operation, although failure to make these connections will not be catastrophic to the converter under normal operating conditions. Pin 1 must always be connected to the output return and Pin 2 must always be connected to +V$_{OUT}$. These connections can be made at any one of the output pins of the converter, or remotely at the load. A remote connection at the load can adjust for voltage drops of as much as 0.25 V dc between the converter and the load.

Long remote sense leads can affect converter stability, although this condition is rare. The impedance of the long power leads between the converter and the remote sense point could affect the converter's unity gain crossover frequency and phase margin. Consult factory if long remote sense leads are to be used.

### Pin 3 (ADJUST)
An adjustment pin is provided so that the user can change the nominal output voltage during the prototype stage. Since very low temperature coefficient resistors are used to set the output voltage and maintain tight regulation over temperature, using standard external resistors to adjust the output voltage will loosen output regulation over temperature. Furthermore, since the status trip point is not changed when the output voltage is adjusted using external resistors, the status line will no longer trip at the standard levels of the newly adjusted output voltage. If necessary, modified standard units can be ordered with the necessary changes made inside the package at the factory. The ADJUST function is sensitive to noise, and care should be taken in the routing of connections.

To make the output voltage higher, place a resistor from ADJUST (Pin 3) to –SENSE (Pin 1). To make the output voltage lower, place a resistor from ADJUST (Pin 3) to +SENSE (Pin 2). Figures 30 and 31 show resistor values for a ±5% change in output voltage.

With regard to the range that the output voltage can be adjusted by the user, there are two concerns. As the output voltage is raised it may become difficult to maintain regulation at full power and low input voltage. As the output voltage is lowered, it may become difficult to maintain regulation at minimum power and high input line.
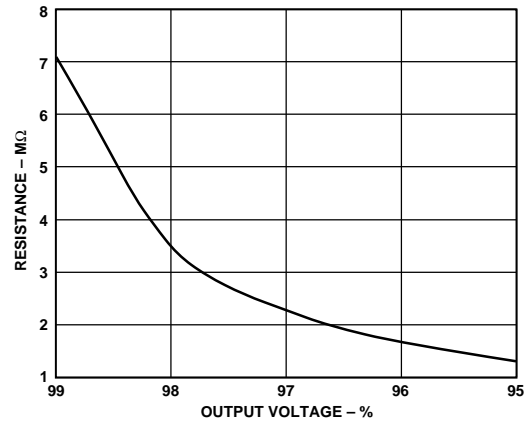

Figure 30. External Resistor Value for Reducing Output Voltage
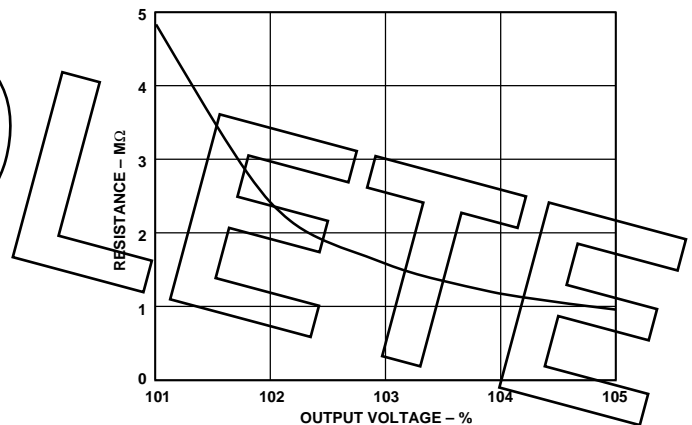

Figure 31. External Resistor for Increasing Output Voltage

### Pin 4 (STATUS)
Pin 4 is active high referenced to –SENSE (Pin 1), indicating that the output voltage is typically within ±5%. The pin is both pulled up and down by internal circuitry. Figures 32 and 33 show the typical source and sink capabilities of the status output. Refer to the paragraphs describing Pin 3 (ADJUST) for effect on status trip point.
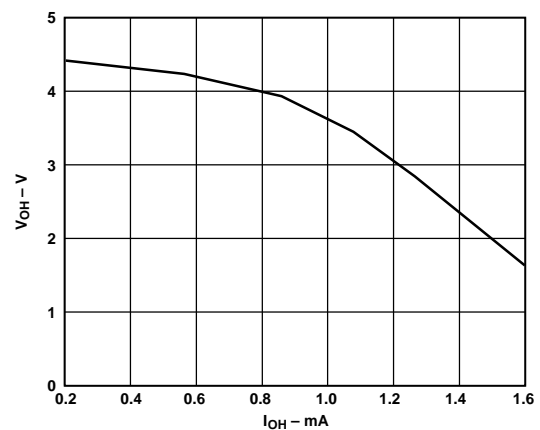

Figure 32. Source Capability of Status Output

# ADDC02808PB
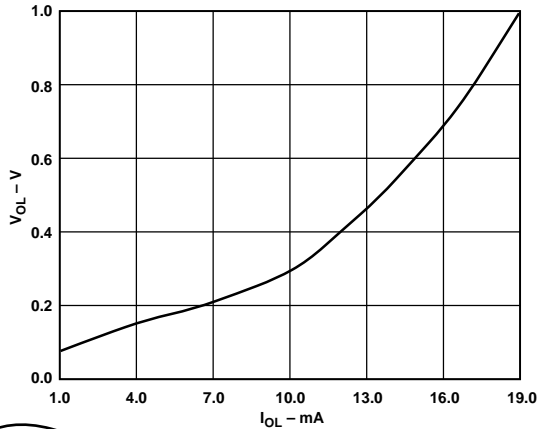


Figure 33. Sink Capability of Status Output

**Pin 5 ($V_{AUX}$)**
Pin 5 is referenced to the input return and provides a semi-regulated 14 V to 16 V dc voltage supply for miscellaneous system use. The maximum permissible current draw is 5 mA and the voltage varies with the output load of the converter shown in Figure 34.
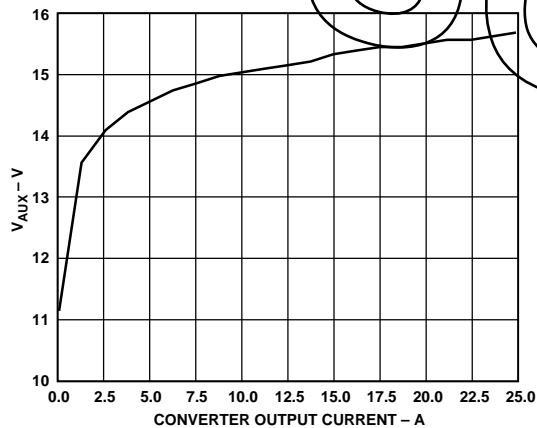


Figure 34.

**Pin 6 (INHIBIT)**
Pin 6 is active low and is referenced to the input return of the converter. Connecting it to the input return will turn the converter off. For normal operation, the inhibit pin is internally pulled up to 12 V. Use of an open collector circuit is recommended.
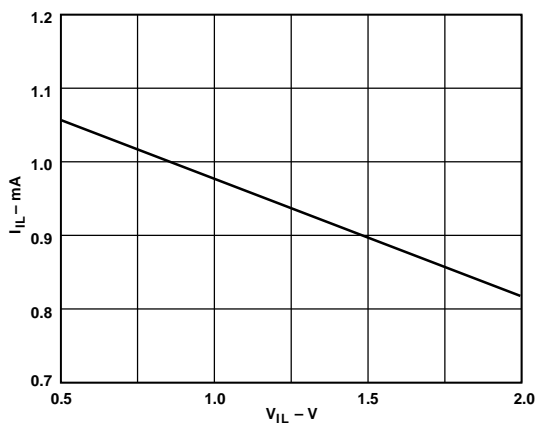


Figure 35. Input Characteristics of Pin 6 When Pulled Low

When Pin 6 is disconnected from input return, the converter will restart in the soft-start mode. Pin 6 must be kept low for at least 2 milli- seconds to initiate a full soft start. Shorter off times will result in a partial soft start. Figure 35 shows the input characteristics of Pin 6.

**Pin 7 (SYNC)**
Pin 7 can be used for connecting multiple converters to a master clock. This master clock can be either an externally user-supplied clock or it can be a converter that has been modified and designated as a master unit. Consult factory for availability of these devices. Capacitive coupling of the clock signal will insure that if the master clock stops working the individual units will continue to operate at their own internal clock frequency, thereby eliminating a potential single point failure. Capacitive coupling will also permit a wider duty cycle to be used. Consult factory for more information. The SYNC pin has an internal pull-down so it is not necessary to sink any current when driving the pin low.

For user-supplied master clocks with no external circuitry, the following specifications must be met:

a. Frequency: 1.00 MHz min
b. Duty cycle: 7% min, 14% max
c. High state voltage high level: 4 V min to 7 V max
d. Low state voltage low level: 0 V min to 3.0 V max

Users should note that the SYNC pin is referenced to the input return of the converter. If the user-supplied master clock is generated on the output side of the converter, the signal should be isolated.

Users should be careful about the frequency selected for the external master clock. Higher switching frequencies will reduce efficiency and may reduce the amount of output power available at minimum input line. Consult factory for modified standard switching frequency to accommodate system clock characteristics.

**Pin 8 ($I_{SHARE}$)**
Pin 8 allows paralleled converters to share the total load current, typically within ±5% at full load. To use the current share feature, connect all current share pins to each other and connect the SENSE pins on each of the converters. The current sharing function is sensitive to the differential voltage between the input return pins of paralleled converters. The current sharing function is also sensitive to noise, and care should be taken in the routing of connections. Refer to Figure 45 for typical application circuits using paralleled converters.

**Pin 9 (TEMP)**
Pin 9 can be used to indicate case temperature or to raise or disable the temperature at which thermal shutdown occurs. Typically, 3.90 V corresponds to +25°C, with a +13.1 mV/°C change for every 1°C rise. The sensor IC (connected from Pin 9 to the input return (Pin 10)) has a 13.1 kΩ impedance.

The thermal shutdown feature has been set to shut down the converter when the case temperature is nominally 110°C to 115°C. To raise the temperature at which shutdown occurs, connect a resistor with the value shown in Figure 36 from Pin 9 to the input return (Pin 10). To completely disable the temperature shutdown feature, connect a 50 kΩ resistor from Pin 9 to the input return (Pin 10).
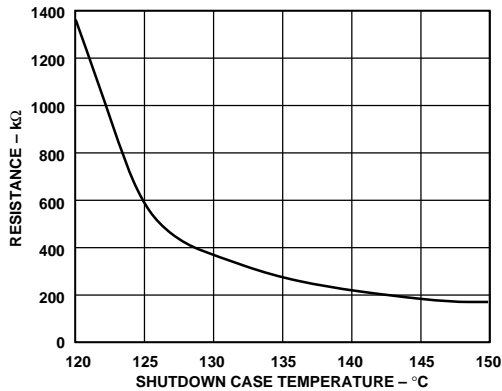
Figure 36. External Resistor Value for Raising Temperature Shutdown Point

## INPUT VOLTAGE RANGE

The steady state operating input voltage range for the converter is defined as 18 V to 40 V. The abnormal operating input voltage range is defined as 16 V to 50 V. In accordance with MIL-STD-704D, the converter can operate up to 50 V dc input for transient conditions as long as 50 milliseconds, and it can operate down to 16 V dc input for continuous operation during emergency conditions. Figure 3 (typical low line dropout vs. load) shows that the converter can work continuously down to and below 16 V dc under reduced load conditions.

The ADDC02808PB can be modified to survive, but not work through, the upper limit input voltages defined in MIL-STD-704A (aircraft) and MIL-STD-1275A (military vehicles). MIL-STD-704A defines an 80 V surge that lasts for 1 second before it falls below 50 V, while MIL-STD-1275A defines a 100 V surge that lasts for 200 milliseconds before it falls below 50 V. In both cases, the ADDC02808PB can be modified to operate to specification up to the 50 V input voltage limit and to shut down and protect itself during the time the input voltage exceeds 50 V. When the input voltage falls below 50 V as the surge ends, the converter will automatically initiate a soft start. In order to survive these higher input voltage surges, the modified converter will no longer have input transient protection, however, as described below.

Contact the factory for information on units surviving high input voltage surges.

**Input Voltage Transient Protection:** The converter has a transient voltage suppressor connected across its input leads to protect the unit against high voltage pulses (both positive and negative) of short duration. With the power supply connected in the typical system setup shown in Figure 15, a transient voltage pulse is created across the converter in the following manner. A 20 µF capacitor is first charged to 400 V. It is then connected directly across the converter's end of the two meter power lead cable through a 2 Ω on-state resistance MOSFET. The duration of this connection is 10 µs. The pulse is repeated every second for 30 minutes. This test is repeated with the connection of the 20 µF capacitor reversed to create a negative pulse on the supply leads. (If continuous reverse voltage protection is required, a diode can be added externally in series at the expense of lower efficiency for the power system.)

The converter responds to this input transient voltage test by shutting down due to its input overvoltage protection feature.

Once the pulse is over, the converter initiates a soft-start, which is completed before the next pulse. No degradation of converter performance occurs.

## THERMAL CHARACTERISTICS

**Junction and Case Temperatures:** It is important for the user to know how hot the hottest semiconductor junctions within the converter get and to understand the relationship between junction, case, and ambient temperatures. The hottest semiconductors in the 100 W product line of Analog Devices' high density power supplies are the switching MOSFETs and the output rectifiers. There is an area inside the main power transformers that is hotter than these semiconductors, but it is within NAVMAT guidelines and well below the Curie temperature of the ferrite. (The Curie temperature is the point at which the ferrite begins to lose its magnetic properties.)

Since NAVMAT guidelines require that the maximum junction temperature be 110°C, the power supply manufacturer must specify the temperature rise above the case for the hottest semiconductors so the user can determine what case temperature is required to meet NAVMAT guidelines. The thermal characteristics section of the specification table states the hottest junction temperature for maximum output power at a specified case temperature. The unit can operate to higher case temperatures than 90°C, but 90°C is the maximum temperature that permits NAVMAT guidelines to be met.

**Case and Ambient Temperatures:** It is the user's responsibility to properly heat sink the power supply in order to maintain the appropriate case temperature and, in turn, the maximum junction temperature. Maintaining the appropriate case temperature is a function of the ambient temperature and the mechanical heat removal system. The static relationship of these variables is established by the following formula:

$$T_C = T_A + (P_D \times R_{\theta_{CA}})$$

where

$T_C$ = case temperature measured at the center of the package bottom,

$T_A$ = ambient temperature of the air available for cooling,

$P_D$ = the power, in watts, dissipated in the power supply,

$R_{\theta_{CA}}$ = the thermal resistance from the center of the package to free air, or case to ambient.

The power dissipated in the power supply, $P_D$, can be calculated from the efficiency, $\eta$, given in the data sheets and the actual output power, $P_O$, in the user's application by the following formula:

$$P_D = P_O \left( \frac{1}{\eta} - 1 \right)$$

For example, at 80 W of output power and 80% efficiency, the power dissipated in the power supply is 20 W. If under these conditions, the user wants to maintain NAVMAT deratings (i.e., a case temperature of approximately 90°C) with an ambient temperature of 75°C, the required thermal resistance, case to ambient, can be calculated as

$$90 = 75 + (20 \times R_{\theta_{CA}}) \quad \text{or} \quad R_{\theta_{CA}} = 0.75°C/W$$

This thermal resistance, case to ambient, will determine what kind of heat sink and whether convection cooling or forced air cooling is required to meet the constraints of the system.

# ADDC02808PB

**SYSTEM INSTABILITY CONSIDERATIONS**
In a distributed power supply architecture, a power source provides power to many "point-of-load" (POL) converters. At low frequencies, the POL converters appear incrementally as *negative* resistance loads. This negative resistance could cause system instability problems.

**Incremental Negative Resistance:** A POL converter is designed to hold its output voltage constant no matter how its input voltage varies. Given a constant load current, the power drawn from the input bus is therefore also a constant. If the input voltage increases by some factor, the input current must decrease by the same factor to keep the power level constant. In incremental terms, a positive incremental change in the input voltage results in a negative incremental change in the input current. The POL converter therefore looks, incrementally, as a negative resistor.

The value of this negative resistor at a particular operating point, $V_{IN}$, $I_{IN}$, is:

$$R_N = \frac{V_{IN}}{I_{IN}}$$

Note that this resistance is a function of the operating point. At full load and low input line, the resistance is its smallest, while at light load and high input line, it is its largest.

**Potential System Instability:** The preceding analysis assumes dc voltages and currents. For ac waveforms the incremental input model for the POL converter must also include the effects of its input filter and control loop dynamics. When the POL converter is connected to a power source, modeled as a voltage source, $V_S$, in series with an inductor, $L_S$, and some positive resistor, $R_S$, the network of Figure 37 results.
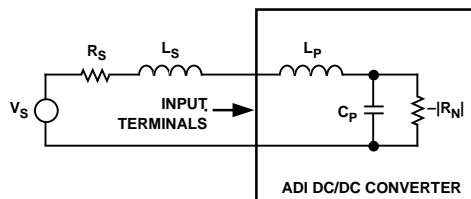


*Figure 37. Model of Power Source and POL Converter Connection*

The network shown in Figure 37 is second order and has the following characteristic equation:

$$s^2(L_S + L_P)C + s\left(\frac{(L_S + L_P)}{-|R_N|} + R_S C_P\right) + 1 = 0$$

For the power delivery to be efficient, it is required that $R_S \ll R_N$. For the system to be stable, however, the following relationship must hold:

$$C_P|R_N| > \frac{(L_S + L_P)}{R_S} \quad \text{or} \quad R_S > \frac{(L_S + L_P)}{C_P|R_N|}$$

Notice from this result that if $(L_S + L_P)$ is too large, or if $R_S$ is too small, the system might be unstable. This condition would first be observed at low input line and full load since the absolute value of $R_N$ is smallest at this operating condition.

If an instability results and it cannot be corrected by changing $L_S$ or $R_S$, such as during the MIL-STD-461D tests due to the LISN requirement, one possible solution is to place a capacitor across the input of the POL converter. Another possibility is to place a small resistor in series with this extra capacitor.

The analysis so far has assumed the source of power was a voltage source (e.g., a battery) with some source impedance. In some cases, this source may be the output of a front-end (FE) converter. Although each FE converter is different, a model for a typical one would have an LC output filter driven by a voltage source whose value was determined by the feedback loop. The LC filter usually has a high Q, so the compensation of the feedback loop is chosen to help dampen any oscillations that result from load transients. In effect, the feedback loop adds "positive resistance" to the LC network.

When the POL converter is connected to the output of this FE converter, the POL's "negative resistance" counteracts the effects of the FE's "positive resistance" offered by the feedback loop. Depending on the specific details, this might simply mean that the FE converter's transient response is slightly more oscillatory, or it may cause the entire system to be unstable.

For the ADDC02808PB, $L_P$ is approximately 0.5 μH and $C_P$ is approximately 4 μF. Figure 8 shows a more accurate depiction of the input impedance of the converter as a function of frequency. The negative resistance is, itself, a very good incremental model for the power state of the converter for frequencies into the several kHz range (see Figure 8).

**NAVMAT DERATING**
NAVMAT is a Navy power supply reliability manual that is frequently cited by specifiers of power supplies. A key section of NAVMAT P4855-1A discusses guidelines for derating designs and their components. The two key derating criteria are voltage derating and power derating. Voltage derating is done to reduce the possibility of electrical breakdown, whereas power derating is done to maintain the component material below a specified maximum temperature. While power deratings are typically stated in terms of current limits (e.g., derate to x% of maximum rating), NAVMAT also specifies a maximum junction temperature of the semiconductor devices in a power supply. The NAVMAT component deratings applicable to the ADDC02808PB are as follows:

*Resistors*
80% voltage derating
50% power derating

*Capacitors*
50% voltage and ripple voltage derating
70% ripple current derating

*Transformers and Inductors*
60% continuous voltage and current derating
90% surge voltage and current derating
20°C less than rated core temperature
30°C below insulation rating for hot spot temperature
25% insulation breakdown voltage derating
40°C maximum temperature rise

*Transistors*
50% power derating
60% forward current (continuous) derating
75% voltage and transient peak voltage derating
110°C maximum junction temperature

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*Diodes (Switching, General Purpose, Rectifiers)*
70% current (surge and continuous) derating
65% peak inverse voltage derating
110°C maximum junction temperature

*Diodes (Zeners)*
70% surge current derating
60% continuous current derating
50% power derating
110°C maximum junction temperature

*Microcircuits (Linears)*
70% continuous current derating
75% signal voltage derating
110°C maximum junction temperature

The ADDC02808PB can meet all the derating criteria listed above. However, there are a few areas of the NAVMAT deratings where meeting the guidelines unduly sacrifices performance of the circuit. Therefore, the standard unit makes the following exceptions.

**Common-Mode EMI Filter Capacitors:** The standard supply uses 500 V capacitors to filter common-mode EMI. NAVMAT guidelines would require 1000 V capacitors to meet the 50% voltage derating (500 V dc input to output isolation), resulting in less common-mode capacitance for the same space. In typical electrical power supply systems, where the load ground is eventually connected to the source ground, common-mode voltages never get near the 500 V dc rating of the standard supply. Therefore, a lower voltage rating capacitor (500 V) was chosen to fit more capacitance in the same space in order to better meet the conducted emissions requirement of MIL-STD-461D (CE102). For those applications which require 250 V or less of isolation from input to output, the present designs would meet NAVMAT guidelines.

**Switching Transistors:** 100 V MOSFETs are used in the standard unit to switch the primary side of the transformers. Their nominal off-state voltage meets the NAVMAT derating guidelines. When the MOSFETs are turned off, however, momentary spikes occur that reach 100 V. The present generation of MOSFETs are rated for repetitive avalanche, a condition that was not considered by the NAVMAT deratings. In the worst case condition, the energy dissipated during avalanche is 1% of the device's rated repetitive avalanche energy. To meet the NAVMAT derating, 200 V MOSFETs could be used. The 100 V MOSFETs are used instead for their lower on-state resistance, resulting in higher efficiency for the power supply.

**NAVMAT Junction Temperatures:** The two types of power deratings (current and temperature) can be independent of one another. For instance, a switching diode can meet its derating of 70% of its maximum current, but its junction temperature can be higher than 110°C if the case temperature of the converter, which is not controlled by the manufacturer, is allowed to go higher. Since some users may choose to operate the power supply at a case temperature higher than 90°C, it then becomes important to know the temperature rise of the hottest semiconductors. This is covered in the specification table in the section entitled "Thermal Characteristics".

## EMI CONSIDERATIONS

Figures 11 through 14 show the results of EMI measurements conducted in accordance with MIL-STD-461D/462D for the ADDC02805SA dc/dc converter (28 $V_{IN}$, 5 $V_{OUT}$, 100 W) using the test setup shown in Figure 15. The EMI performance of the ADDC02808PB dc/dc converter will be different for several reasons. The purpose of this section is to describe the various MIL-STD-461D baseline tests and the ADDC02805SA converter's corresponding performance and then explain how the EMI performance of the ADDC02808PB will differ from this baseline.

**28 $V_{IN}$, 100 W Out, Baseline Performance:** The ADDC02805SA has an integral differential- and common-mode EMI filter that is designed to meet all applicable requirements in MIL-STD-461D when the power converter is installed in a typical system setup (described below). The converter also contains transient protection circuitry that permits the unit to survive short, high voltage transients across its input power leads.

Electromagnetic interference (EMI) is governed by MIL-STD-461D, which establishes design requirements, and MIL-STD-462D, which defines test methods. EMI requirements are categorized as follows (xxx designates a three digit number):

- CExxx: conducted emissions (EMI produced internal to the power supply which is conducted externally through its input power leads)
- CSxxx: conducted susceptibility (EMI produced external to the power supply which is conducted internally through the input power leads and may interfere with the supply's operation)
- RExxx: radiated emissions (EMI produced internal to the power supply which is radiated into the surrounding space)
- RSxxx: radiated susceptibility (EMI produced external to the power supply which radiates into or through the power supply and may interfere with its proper operation)

It should be noted that there are several areas of ambiguity with respect to CE102 measurements that may concern the systems engineer. One area of ambiguity in this measurement is the nature of the load. If it is constant, then the ripple voltage on the converter's input leads is due only to the operation of the converter. If, on the other hand, the load is changing over time, this variation causes an additional input current and voltage ripple to be drawn at the same frequency. If the frequency is high enough, the converter's filter will help attenuate this second source of ripple, but if it is below approximately 100 kHz, it will not. The system may then not meet the CE102 requirement, even though the converter is not the source of the EMI. If this is the case, additional capacitance may be needed across the load or across the input to the converter.

Another ambiguity in the CE102 measurement concerns common-mode voltage. If the load is left unconnected from the ground plane (even though the case is grounded), the common-mode ripple voltages will be smaller than if the load is grounded. The test specifications do not state which procedure should be used. However, in neither case (load grounded or floating) will the typical EMI test setup described below be exactly representative of the final system configuration EMI test. For the following reasons, the same is true if separately packaged EMI filters are used.

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In almost all systems the output ground of the converter is ultimately connected to the input ground of the system. The parasitic capacitances and inductances in this connection will affect the common-mode voltage and the CE102 measurement. In addition, the inductive impedance of this ground connection can cause resonances, thereby affecting the performance of the common-mode filter in the power supply.

In response to these ambiguities, the Analog Devices' converter has been tested for CE102 under a constant load and with the output ground floating. While these measurements are a good indication of how the converter will operate in the final system configuration, the user should confirm CE102 testing in the final system configuration.

**CE101:** This test measures emissions on the input leads in the frequency range between 30 Hz and 10 kHz. The intent of this requirement is to ensure that the dc/dc converter does not corrupt the power quality (allowable voltage distortion) on the power busses present on the platform. There are several CE101 limit curves in MIL-STD-461D. The most stringent one applicable for the converter is the one for submarine applications. Figure 14 shows that the converter easily meets this requirement (the return line measurement is similar). The components at 60 Hz and its harmonics are a result of ripple in the output of the power source used to supply the converter.

**CE102:** This test measures emissions in the frequency range between 10 kHz and 10 MHz. The measurements are made on both of the input leads of the converter which are connected to the power source through LISNs. The intent of this requirement in the lower frequency portion of the requirement is to ensure that the dc/dc converter does not corrupt the power quality (allowable voltage distortion) on the power busses present on the platform. At higher frequencies, the intent is to serve as a separate control from RE102 on potential radiation from power leads which may couple into sensitive electronic equipment.

Figure 12 shows the CE102 limit and the measurement taken from the +$V_{IN}$ line. While the measurement taken from the input return line is slightly different, both comfortably meet the MIL-STD-461D, CE102 limit.

**CS101:** This test measures the ability of the converter to reject low frequency differential signals, 30 Hz to 50 kHz, injected on the dc inputs. The measurement is taken on the output power leads. The intent is to ensure that equipment performance is not degraded from ripple voltages associated with allowable distortion of power source voltage waveforms. Figure 7 shows a typical audio susceptibility graph. Note that according to the MIL-STD-461D test requirements, the injected signal between 30 Hz and 5 kHz has an amplitude of 2 V rms and from 5 kHz to 50 kHz the amplitude decreases inversely with frequency to 0.2 V rms. The curve of the injected signal should be multiplied by the audio susceptibility curve to determine the output ripple at any frequency. When this is done, the worst case output ripple at the frequency of the input ripple occurs at 5 kHz, at which point there is typically a 25 mV peak-to-peak output ripple.

It should be noted that MIL-STD-704 has a more relaxed requirement for rejection of low frequency differential signals injected on the dc inputs than MIL-STD-461D. MIL-STD-704 calls for a lower amplitude ripple to be injected on the input in a narrower frequency band, 10 Hz to 20 kHz.

**CS114:** This test measures the ability of the converter to operate correctly during and after being subjected to currents injected into bulk cables in the 10 kHz to 400 MHz range. Its purpose is to simulate currents that would be developed in these cables due to electromagnetic fields generated by antenna transmissions. The converter is designed to meet the requirements of this test when the current is injected on the input power leads cable. Consult factory for more information.

**CS115:** This test measures the ability of the converter to operate correctly during and after being subjected to 30 ns long pulses of current injected into bulk cables. Its purpose is to simulate transients caused by lightning or electromagnetic pulses. The converter is designed to meet this requirement when applied to its input power leads cable. Consult factory for more information.

**CS116:** This test measures the ability of the converter to operate correctly during and after being subjected to damped sinusoid transients in the 10 kHz to 100 MHz range. Its purpose is to simulate current and voltage waveforms that would occur when natural resonances in the system are excited. The converter is designed to meet this requirement when applied to its input power leads cable. Consult factory for more information.

**RE101:** This requirement limits the strength of the magnetic field created by the converter in order to avoid interference with sensitive equipment located nearby. The measurement is made from 30 Hz to 100 kHz. The most stringent requirement is for the Navy. Figure 13 shows the test results when the pickup coil is held 7 cm above the converter. As can be seen, the converter easily meets this requirement.

**RE102:** This requirements limits the strength of the electric field emissions from the power converter to protect sensitive receivers from interference. The measurement is made from 10 kHz to 18 GHz with the antenna oriented in the vertical plane. For the 30 MHz and above range the standard calls for the measurement to be made with the antenna oriented in the horizontal plane, as well.

In a typical power converter system setup, the radiated emissions can come from two sources: 1) the input power leads as they extend over the two meter distance between the LISNs and the converter, as required for this test, and 2) the converter output leads and load. The latter is likely to create significant emissions if left uncovered since minimal EMI filtering is provided at the converter's output. It is typical, however, that the power supply and its load would be contained in a conductive enclosure in applications where this test is applicable. A metal screen enclosure was therefore used to cover the converter and its load for this test.

Figure 14 shows test results for the vertical measurement and compares them against the most stringent RE102 requirement; the horizontal measurement (30 MHz and above) was similar. As can be seen, the emissions just meet the standard in the 18 MHz–28 MHz range. This component of the emissions is due to common-mode currents flowing through the input power leads. As mentioned in the section on CE102 above, the level of common-mode current that flows is dependent on how the load is connected. This measurement is therefore a good indication of how well the converter will perform in the final configuration, but the user should confirm RE102 testing in the final system.

**RS101:** This requirement is specialized and is intended to check for sensitivity to low frequency magnetic fields in the 30 Hz to 50 kHz range. The converter is designed to meet this requirement. Consult factory for more information.

**RS103:** This test calls for correct operation during and after the unit under test is subjected to radiated electric fields in the 10 kHz to 40 GHz range. The intent is to simulate electromagnetic fields generated by antenna transmissions. The converter is designed to meet this requirement. Consult factory for more information.

**Circuit Setup for EMI Test**
Figure 15 shows a schematic of the test setup used for the EMI measurements discussed above. The output of the converter is connected to a resistive load designed to draw full power. There is a 0.1 μF capacitor placed across this resistor that typifies bypass capacitance normally used in this application. At the input of the converter there are two differential capacitors (the larger one having a series resistance) and two small common-mode capacitors connected to case ground. The case itself was connected to the metal ground plane in the test chamber. For the RE102 test, a metal screen box was used to cover both the converter and its load (but not the two meters of input power lead cables). This box was also electrically connected to the metal ground plane.

With regard to the components added to the input power lines, the 100 μF capacitor with its 1 Ω series resistance is required to achieve system stability when the unit is powered through the LISNs, as the MIL-STD-461D standard requires. These LISNs have a series inductance of 50 μH at low frequencies, giving a total differential inductance of 100 μH. As explained earlier in the System Instability section, such a large series source inductance will cause an instability as it interacts with the converter's negative incremental input resistance unless some corrective action is taken. The 100 μF capacitor and 1 Ω resistor provide the stabilization required.

It should be noted that the values of these stabilization components are appropriate for a single converter load. If the system makes use of several converters, the values of the components will need to be changed slightly, but not such that they are repeated for every converter. It should also be noted that most system applications will not have a source inductance as large as the 100 μH built into the LISNs. For those systems, a much smaller input capacitor could be used.

The 2 μF differential-mode capacitor and the two 82 nF common-mode capacitors were added to achieve the results shown in the EMI measurement figures described above.

**ADDC02808PB EMI Performance**
The EMI performance of the ADDC02808PB power converter will be different from the ADDC02805SA baseline previously discussed for several reasons:

1. Its maximum power is 200 W, or twice that of the ADDC02805SA converter.

2. Its differential input filter inductors are smaller in value by a factor of two compared to those in the ADDC02805SA converter to accommodate input stability at the higher power level.

3. A repetitively pulsed load will cause large input currents at the fundamental frequency (and harmonics) of the pulse waveform.

The result of Items 1 and 2 is that the ADDC02808PB converter will have higher conducted and radiated emissions in the 1/2 MHz to 10 MHz range. The emissions in this range are dominated by differential currents. These currents are proportional to power, so we would expect a factor of two increase in emissions due to the 200 W operating level. It does not matter that the average power of this pulsed unit is 100 W or lower. MIL-STD-462D calls for measurements to be made with peak detectors that will determine the emissions during the 200 W pulse, and not average them in any way with the lower power part of the cycle.

In addition, the differential EMI filter in the ADDC02808PB converter is less effective at attenuating the ripple currents than is the filter in the ADDC02805SA converter due to smaller value inductors. Figure 38 shows the transfer functions of these two filters in the frequency range of interest.

Combining the factor of two and the reduced filter attenuation, Figure 39 shows the ratio, in dB, by which the emissions of Figures 12 and 14 should be increased to estimate the emissions of the ADDC02808PB converter in this frequency range. From this curve the 1/2 MHz component should increase by 25 dB, and the 1 MHz and higher components should increase by 22 dB.

For both conducted and radiated tests, this increase would require some additional differential filtering to meet the most stringent MIL-STD-461D levels shown in the figures. This could be done, for example, by increasing the 2 μF ceramic (low parasitic inductance) capacitor placed across the input of the converter in Figure 15 to 30 μF or, a small 0.5 μH, 16 A inductor could be placed in series between the top of the 2 μF capacitor and the +V$_{IN}$ pin. Figures 40 and 41 show the ratios,
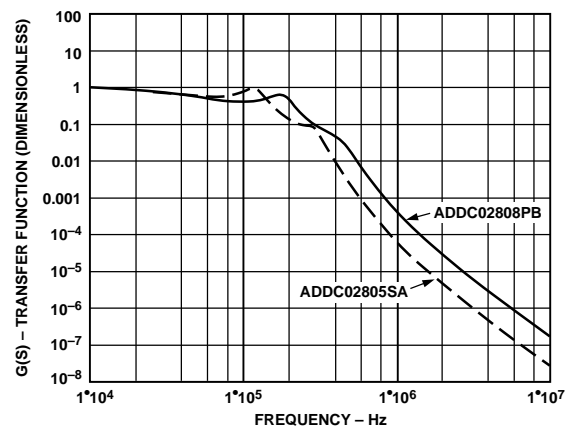


Figure 38. Comparison of Transfer Functions for the Input EMI Filters in ADDC02805SA and ADDC02808PB
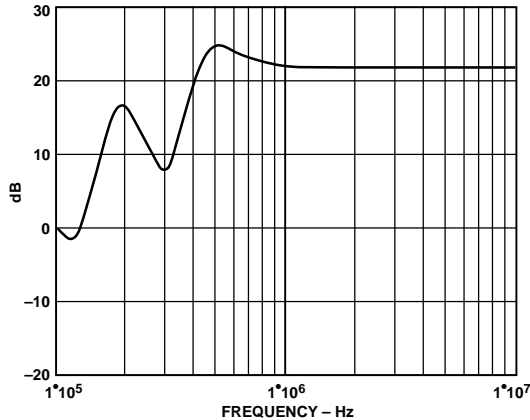
Figure 39.  Change in ADDC02808PB Differential Emissions vs. ADDC02805SA Emissions with the Same Test Setup

in dB, by which the differential emissions would change if either of these approaches were followed.  Notice that the inductor solution provides substantial attenuation in the 1 MHz and higher frequency range, while the larger capacitor solution has a more uniform effect.  These proposed solutions are suggestions; they have not been tested.
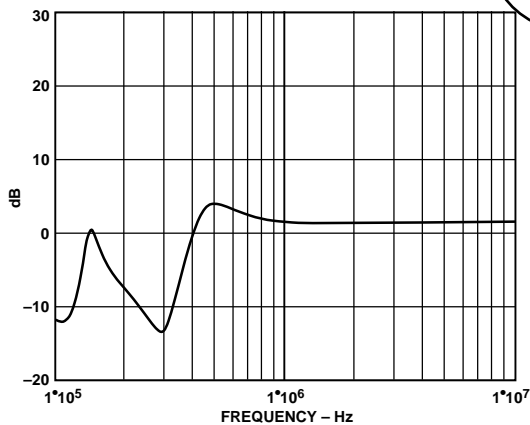


Figure 40.  Change in ADDC02808PB Differential Emissions vs. the ADDC02805SA Emissions with External 30 µF Capacitor
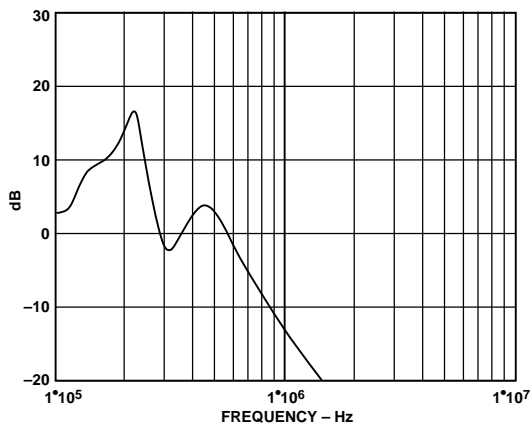


Figure 41.  Change in ADDC02808PB Differential Emissions vs. the ADDC02805SA Emissions with External 0.5 µH, 16 A Inductor

The peak in the radiated emissions in the 20 MHz–30 MHz range of Figure 14 is dominated by common-mode noise.  This common-mode noise emission is changed only slightly between the ADDC02808PB and the ADDC02805SA converters since it does not depend on the power level or the differential input filter.  The turns ratio on the transformer has been changed, so we expect the common-mode emissions might be 2–4 times larger. This increase could be countered by increasing the 82 nF common-mode capacitors of Figure 15 correspondingly. Again, this solution is a suggestion; it has not been tested.

Finally, the pulsed nature of the load means there will be a substantial ripple in the input current at the fundamental pulse rate and its harmonics. This ripple can be calculated once the power is known as a function of time by dividing by the input voltage.  For instance, if the load switches between zero and 200 W (260 W at the input) at 1 kHz with a duty ratio of 50%, the current drawn by the converter will have a 9.3 A on, 0 A off, 50% duty ratio input current waveform (260 W/28 V = 9.3 A). This waveform has an average of 4.65 A and a square wave of plus and minus 4.65 A around this average. This square wave of current has a fundamental component as well as odd harmonics (3rd, 5th, 7th, . . .). The peak of the fundamental component is $(4/\pi)$ 4.65.  The rms value of this component is .707 times the peak, or 4.2 A.

With the test setup in Figure 15, given the impedances of the LISNs and the 100 µF capacitor with its 1 Ω series resistance, a 3.6 V rms waveform would result from this fundamental component of the input current.  The MIL-STD-461D limit shown in Figure 11 calls for approximately 100 mV at the 1 kHz frequency.  If this limit is to be met, substantial filtering at the lower frequencies will have to be added to the system.

## RELIABILITY CONSIDERATIONS
MTBF (Mean Time Between Failure) is a commonly used reliability concept that applies to repairable items in which failed elements are replaced upon failure.  The expression for MTBF is

$$MTBF = T/r$$

where

$T$ = total operating time
$r$ = number of failures

In lieu of actual field data, MTBF can be predicted per MIL-HDBK-217.

**MTBF, Failure Rate, and Probability of Failure:**  A proper understanding of MTBF begins with its relationship to lambda $(\lambda)$, which is the failure rate. If a constant failure rate is assumed, then MTBF = $1/\lambda$, or $\lambda$ = 1/MTBF.  If a power supply has an MTBF of 1,000,000 hours, this does not mean it will last 1,000,000 hours before it fails.  Instead, the MTBF describes the failure rate.  For 1,000,000 hours MTBF, the failure rate during any hour is 1/1,000,000, or 0.0001%.  Thus, a power supply with an MTBF of 500,000 hours would have twice the failure rate (0.0002%) of one with 1,000,000 hours.

What users should be interested in is the probability of a power supply not failing prior to some time t.  Given the assumption of a constant failure rate, this probability is defined as

$$R(t) = e^{-\lambda t}$$

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where $R(t)$ is the probability of a device not failing prior to some time t.

If we substitute $\lambda = 1/MTBF$ in the above formula, then the expression becomes

$$R(t) = e^{\frac{-t}{MTBF}}$$

This formula is the correct way to interpret the meaning of MTBF.

If we assume t = MTBF = 1,000,000 hours, then the probability that a power supply will not fail prior to 1,000,000 hours of use is $e^{-1}$, or 36.8%. This is quite different from saying the power supply will last 1,000,000 hours before it fails. The probability that the power supply will not fail prior to 50,000 hours of use is $e^{-.05}$, or 95%. For t = 10,000 hours, the probability of no failure is $e^{-.01}$, or 99%.

**Temperature and Environmental Factors:** Although the calculation of MTBF per MIL-HDBK-217 is a detailed process, there are two key variables that give the manufacturer significant leeway in predicting an MTBF rating. These two variables are temperature and environmental factor. Therefore, for users to properly compare MTBF numbers from two different manufacturers, the environmental factor and the temperature must be identical. Contact the factory for MTBF calculations for specific environmental factors and temperatures.

## MECHANICAL CONSIDERATIONS

When mounting the converter into the next higher level assembly, it is important to insure good thermal contact is made between the converter and the external heat sink. Poor thermal connection can result in the converter shutting off, due to the temperature shutdown feature (Pin 9), or reduced reliability for the converter due to higher than anticipated junction and case temperatures. For these reasons the mounting tab locations were selected to insure good thermal contact is made near the hot spots of the converter which are shown in the shaded areas of Figure 42.
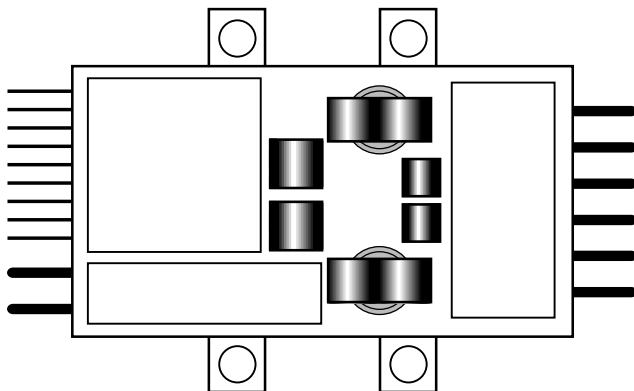


Figure 42. Hot Spots (Shaded Areas) of DC/DC Converter

The pins of the converter are typically connected to the next higher level assembly by bending them at right angles, either down or up, and cutting them shorter for insertion in printed

circuit board through holes. In order to maintain the hermetic integrity of the seals around the pins, a fixture should be used for bending the pins without stressing the pin-to-sidewall seals. It is recommended that the minimum distance between the package edge and the inside of the pin be 100 mils (2.54 mm) for the 40 mil (1.02 mm) diameter pins; 120 mils (3.05 mm) from the package edge to the center of the pin as shown in Figure 43.
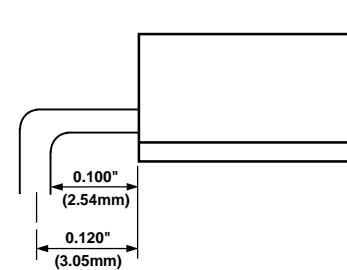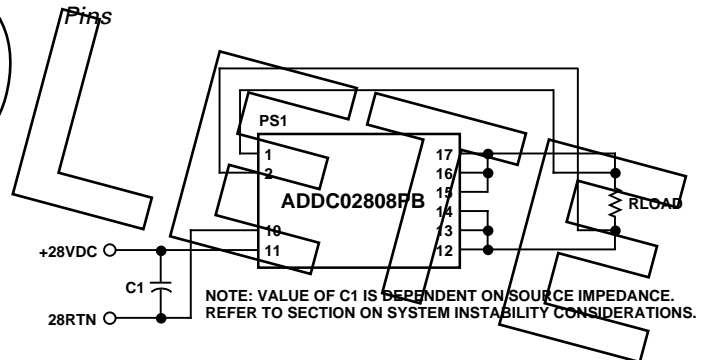


Figure 43. Minimum Bend Radius of 40 Mil (1.02 mm) Pins



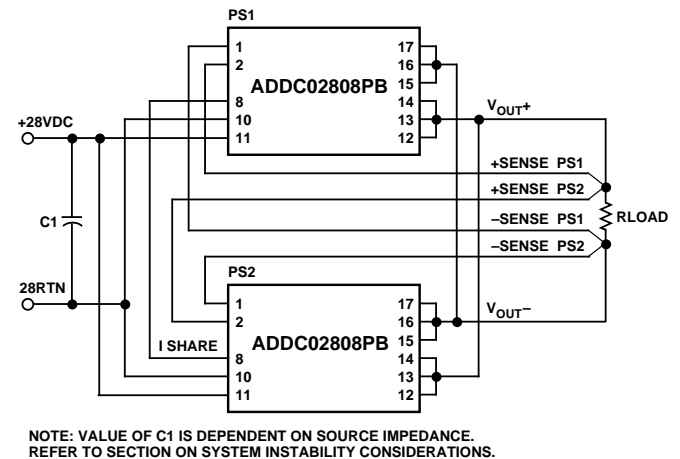Figure 44. Typical Power Connections and External Parts for Converter
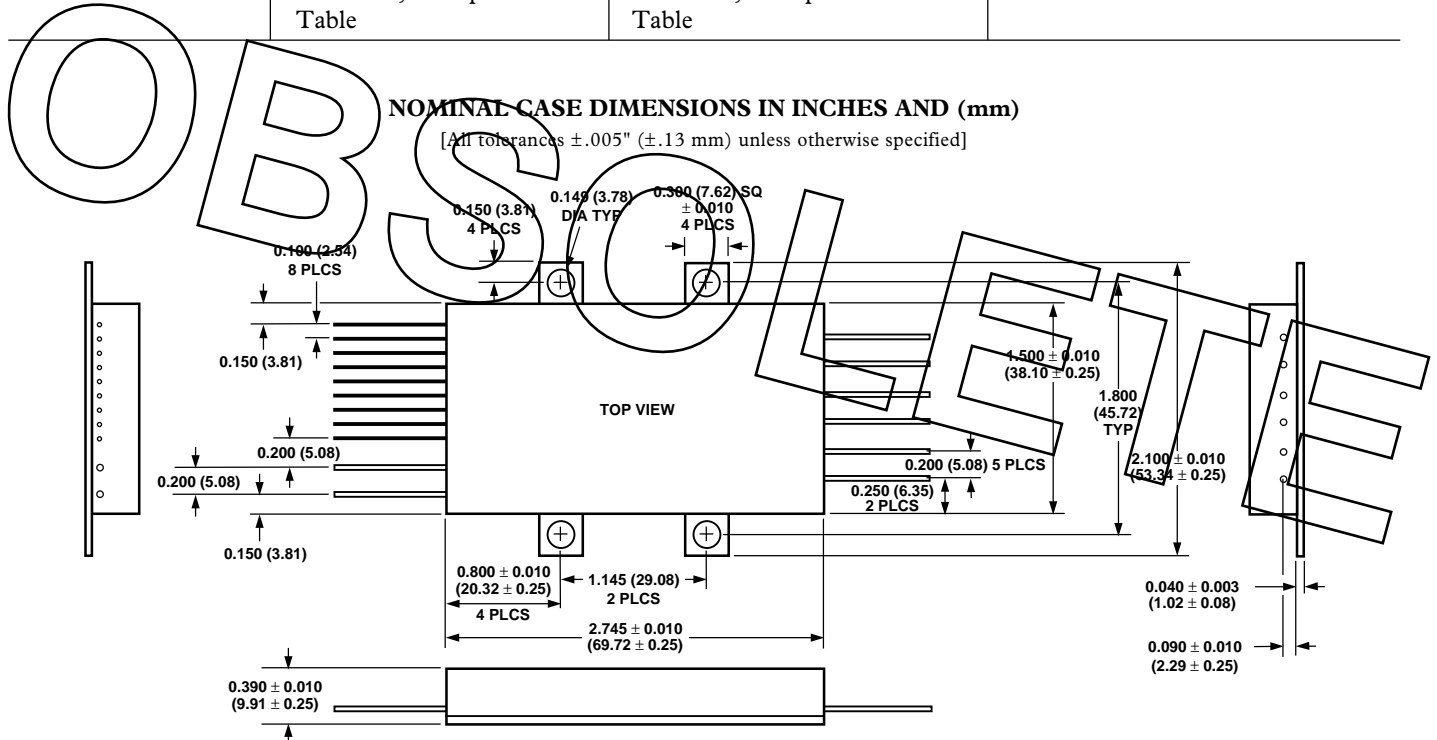


Figure 45. Typical Connections for Paralleling Two Converters

# ADDC02808PB

**Screening Levels for ADDC02808PB**

| Screening Steps | Industrial (KV) | Ruggedized Industrial (TV) | MIL-STD-883B/SMD (TV/883B) |
|---|---|---|---|
| Pre-Cap Visual | 100% | MIL-STD-883, TM2017 | |
| Temp Cycle | N/A | N/A | |
| Constant Acceleration | N/A | N/A | |
| Fine Leak | Guaranteed to Meet MIL-STD-883, TM1014 | Guaranteed to Meet MIL-STD-883, TM1014 | Compliant to MIL-PRF-38534 |
| Gross Leak | Guaranteed to Meet MIL-STD-883, TM1014 | Guaranteed to Meet MIL-STD-883, TM1014 | |
| Burn-In | N/A | MIL-STD-883, TM1015, 96 Hrs at +115°C Case | |
| Final Electrical Test | At +25°C, Per Specification Table | At +25°C, Per Specification Table | |

**NOMINAL CASE DIMENSIONS IN INCHES AND (mm)**

[All tolerances ±.005" (±.13 mm) unless otherwise specified]



NOTES

1. The final product weight is 85 grams maximum.

2. The package base material is made of molybdenum and is nominally 40 mils (1.02 mm) thick. The "runout" is less than 2 mils per inch (0.02 mm per cm).

3. The high current pins (10–17) are 40 mil (1.02 mm) diameter; are 99.8% copper; and are plated with gold over nickel.

4. The signal carrying pins (1–9) are 18 mil (0.46 mm) diameter; are Kovar; and are plated with gold over nickel.

5. All pins are a minimum length of 0.740 inches (18.80 mm) when the product is shipped. The pins are typically bent up or down and cut shorter for proper connection into the user's system.

6. All pin-to-sidewall spacings are guaranteed for a minimum of 500 V dc breakdown at standard air pressure.

7. The case outline was originally designed using the inch-pound units of measurement. In the event of conflict between the metric and inch-pound units, the inch-pound shall take precedence.

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