HYE18P64160AF-9.6
HYE18P64160AF-12.5
HYE18P64160AF-15

Synchronous Burst CellularRAM™ (1.5G)
CellularRAM

Memory Products

Infineon
technologies

N e v e r   s t o p   t h i n k i n g .

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Revision History:	2005-5	V1.5

Previous Version:	1.4 (Target data sheet)
Page	Subjects (major changes since last revision)
23	DPD Duration time adjusted
30, **31**	Row boundary crossing is not supported in all cases
19, **37**, **41**	CRE timing clarified in asynchronous control register access

Previous Version:	1.3 (Target data sheet)
All	Min. Duration of DPD mode is set to 1ms
14, **19**, **20**, **37**, **45**	$\overline{UB}, \overline{LB}$ low required for register read (FCR)
19, **20**, **45**	Clarified WAIT behavior in synchronous register access
18	BCR.bit6 has no effect.
34	DIDR.bit15 reads out the information of page size. If no use, please ignore the bit.
56	Adjusted the values of Operating Currents

Previous Version:	1.2 (Target data sheet)
Page	Subjects (major changes since last revision)
All	Adjusted CLK frequency target Vs. latency code in fixed latency mode

Previous Version:	1.1 (Target data sheet)
All	V_{DD}, min = 1.7V (contact factory for the part of 1.65V min)
All	Wireless operating temperature goes down to - 30°C
All	Variable lat=2 reaches 66MHz max for 12.5 part
10, 11	J5 and J6 ball : "NC" to "RFU"
33, 56	Density and Design Version fields are added to DIDR.
Asynchronous	Value change in t_{OHZ}, t_{WP}, t_{DS}. t_{AX} removed from the spec. (per spec alignment)
Synchronous	Value change in t_{CWT}, t_{CSS}, $t_{CKH/L}$, t_{SP}, t_T, t_{KOH} per spec alignment
Synchronous	t_{KADV} is added to specify timing requirement between last data-in to new burst_init.

Previous Version:	1.02 (Target data sheet)
All	t_{CSL} max is 4μs (changed from 8μs)
24, 25	Change default strength to Half from Full drive
52	Added overshoot, Undershoot allowance for input pins
53	AC test load introduces resistive load of 50 Ohm
55, 56	S/W Register entry mode supports DPD

Previous Version:	1.01 (Target data sheet)
Synchronous	Corrected timing error in synchronous mode (incl. NOR Flash) to show UB/LB low time at burst_init. (Figure 26, 27, 29, 32-35)

Previous Version:	1.0 (Target data sheet)
33	In chapter 2.6, DIDR mapping is finalized - Manufacturer's ID and Generation fields only
51	Abs. max rating for V_{IN} from 2.5V to 2.8V (following QRP)
56-57	Added DIDR mapping (Figure 41)
34	FIG.19 indicates wrong tOE notation. Shout it be tOLZ.
37, 40	Type error : t_{CSL} max is 8μs, not 10μs
47	t_{CSL} added to the table
Synchronous	$\overline{ADV}$ low hold time from CLK is needed. t_{AVH} is removed from synchronous timing
21-22	DPD exit is triggered by $\overline{CS}$ going low
45-46	$\overline{ADV}$ low hold time from $\overline{CS}$ low-going (t_{CVP}) is added to ensure valid address input
Synchronous	t_{HD} is 2ns for all speed grade

Previous Version:	0.9 (Target data sheet)
all	CellularRAM1.5G compatible datasheet

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64M Synchronous Burst CellularRAM^{TM} (1.5G)
CellularRAM

1 Overview

1.1 Features

- High density (1T1C-cell) Synchronous 64Mbit Pseudo-Static RAM
- Designed for cell phone applications - low power, high density, refresh-free operation (CellularRAM)
- CellularRAM1.5G of more features, maintaining functional-compatibility to 1st-generation CellularRAM
- Organization 4M × 16
- High bandwidth:
  - **104 MHz** synchronous burst read/write, **20 ns** page read (16-word), **70 ns** random access
- 1.8 V single power supply (V_{DD} for core and V_{DDQ} for I/O)
- Low power optimized design
  - I_{ACTIVE} = 25 mA @70 ns random cycle (with output disabled)
  - I_{SB} = 140 µA, data retention mode
  - I_{DPD} = < 10 µA (typ), non-data retention mode
- Low power features
  - Partial Array Self-Refresh (PASR)
  - Deep Power Down Mode (DPD)
  - Temparature Compensated Self-Refresh (TCSR) by the control of On-chip Temperature Sensor (OCTS)
- User configurable interface supporting three different access protocols (values from 9.6 part)
  - asynchronous SRAM protocol, 70 ns random access cycle time, 20 ns page mode (read only) cycle time
  - NOR-Flash burst protocol, 70 ns write cycle time, 104 MHz burst mode read cycle
  - Full synchronous interface protocol, 70 ns random cycle time, 104 MHz burst mode read/write cycle
- User settings for NOR-Flash burst or in synchronous mode
  - fixed burst length of 4/8/16/32 words or continuous burst mode
  - latency mode (variable or fixed) and various latency codes at desired CLK frequency
  - wrap mode function available for both read and write burst
  - WAIT signal polarity and timing configurable
  - Driver strength of full, 1/2, or 1/4
- Write burst operates at fixed latency regardless of latency mode
- 2 sets of programmable registers (RCR & BCR) accessed (set or fetch) by CRE-pin control or S/W entry mode
- 1 set of read-only register for device ID accessed via fetch register command
- Byte read/write control by $\overline{UB}/\overline{LB}$
- Wireless operating temperature range from -30 °C to +85 °C
- PG-VFBGA-54 chip-scale package - Green Product (9 × 6 ball grid)
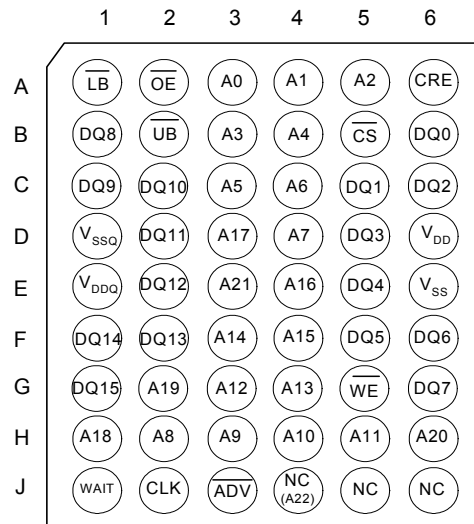
Top-side view (ball down)
J4 is NC for 64Mb and A22 for 128Mb

Table 1 Product Selection & Marking

HYE18P64160AF		-9.6	-12.5	-15
Maximum Input CLK frequency (MHz)	Lat = 2	66	66	40
	Lat = 3	104	80	66
Min. Random Cycle time (t_{RC})		70 ns	70 ns	85 ns
Ordering Information		contact factory		contact factory

HY	**E**	**18**	**P**	**64**	**16**	**0**	**A**	**F**
Infineon Memory Product	Wireless temperature range -30 °C to +85 °C	1.8V Supply	CellularRAM Product Family	64M 128: 128M	x16	Synch Burst	Product Version	Green Package W: KGD (Wafer Form)

1.2 General Description

The Synchronous Burst CellularRAM™ (1.5G) (CellularRAM) is designed to better serve the growing memory density and bandwidth demand in 2.5G and 3G cellular phone application. Its high density 1T1C-cell concept, the multi-protocol interface capabilities, its highly optimized low power design and its refresh-free operation make the CellularRAM the perfect fit for advanced baseband applications.

Configured in synchronous burst mode, a peak bandwidth of > 200 Mbyte/s is achieved at the max. clock rate of 104 MHz. The burst length can be programmed and set to either fixed burst lengths of 4, 8, 16- or 32-words[1] or set to continuous mode. The 16-word burst mode is specially designed for cached processor designs to speed up cache re-fill operations. The addition of fixed latency mode to 1st-generation CellularRAM expands the support into legacy application where NOR-type burst flash has been adopted.

In NOR-Flash interface, burst read accesses are synchronous whereas write accesses are of asynchronous nature. This is to retain compatibility to today's NOR-Flash protocols and thus to make sure that existing baseband designs do get instantly a performance gain in read direction by deploying the NOR-Flash burst protocol. The different access protocols that are supported by the CellularRAM are illustrated in **Figure 1**. Data byte control ($\overline{UB}$, $\overline{LB}$) is featured in all modes and provides dedicated lower and upper byte access.
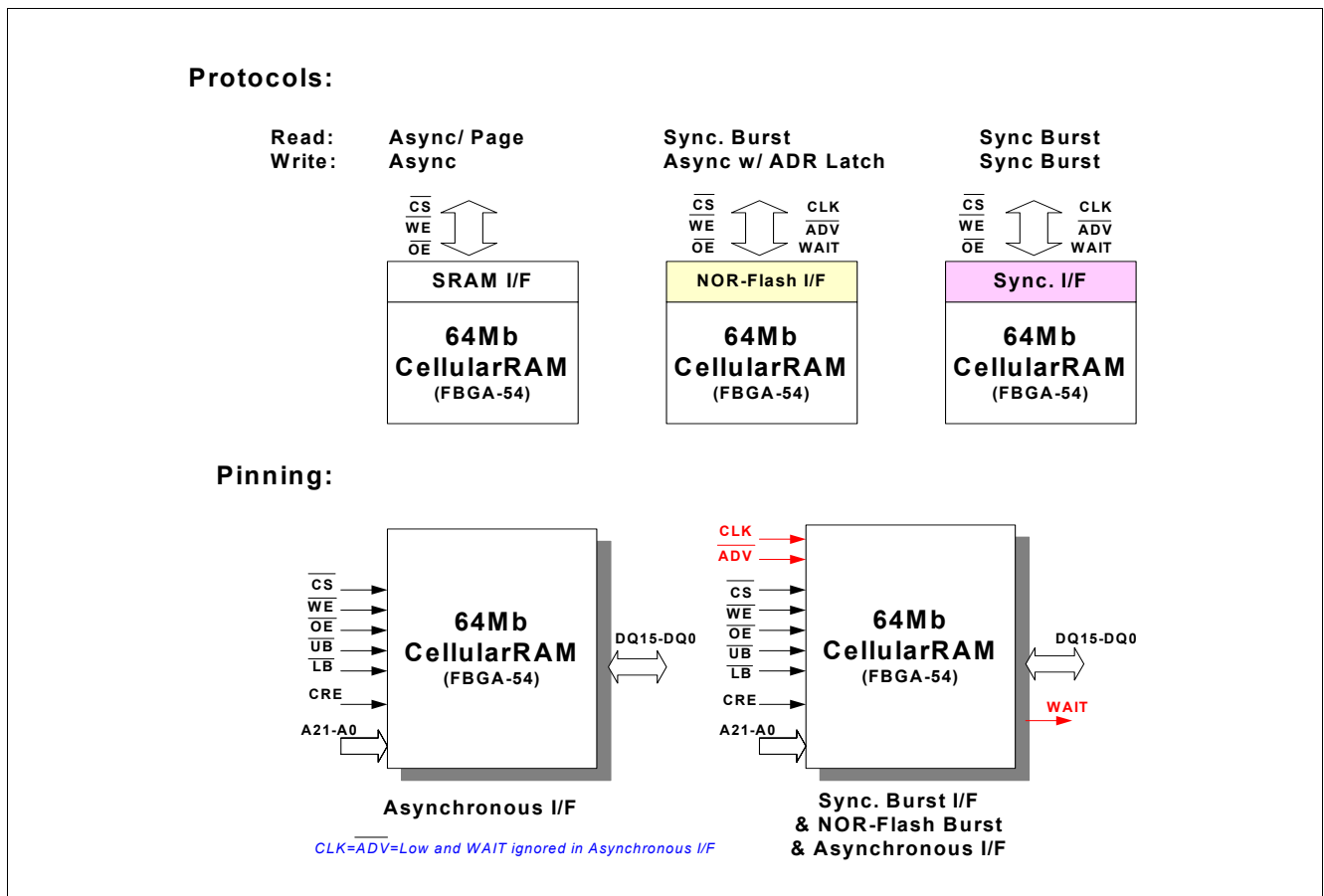
Figure 1   CellularRAM - Interface Configuration Options

The CellularRAM can be operated from a single 1.8 V power supply feeding the core and the output drivers. The chip is fabricated in Infineon Technologies advanced low power 0.11 μm process technology and comes in a PG-VFBGA-54 package.

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1)   1 word is equal 16 bits

1.3 HYE18P64160AF-9.6/12.5/15 Ball Configuration
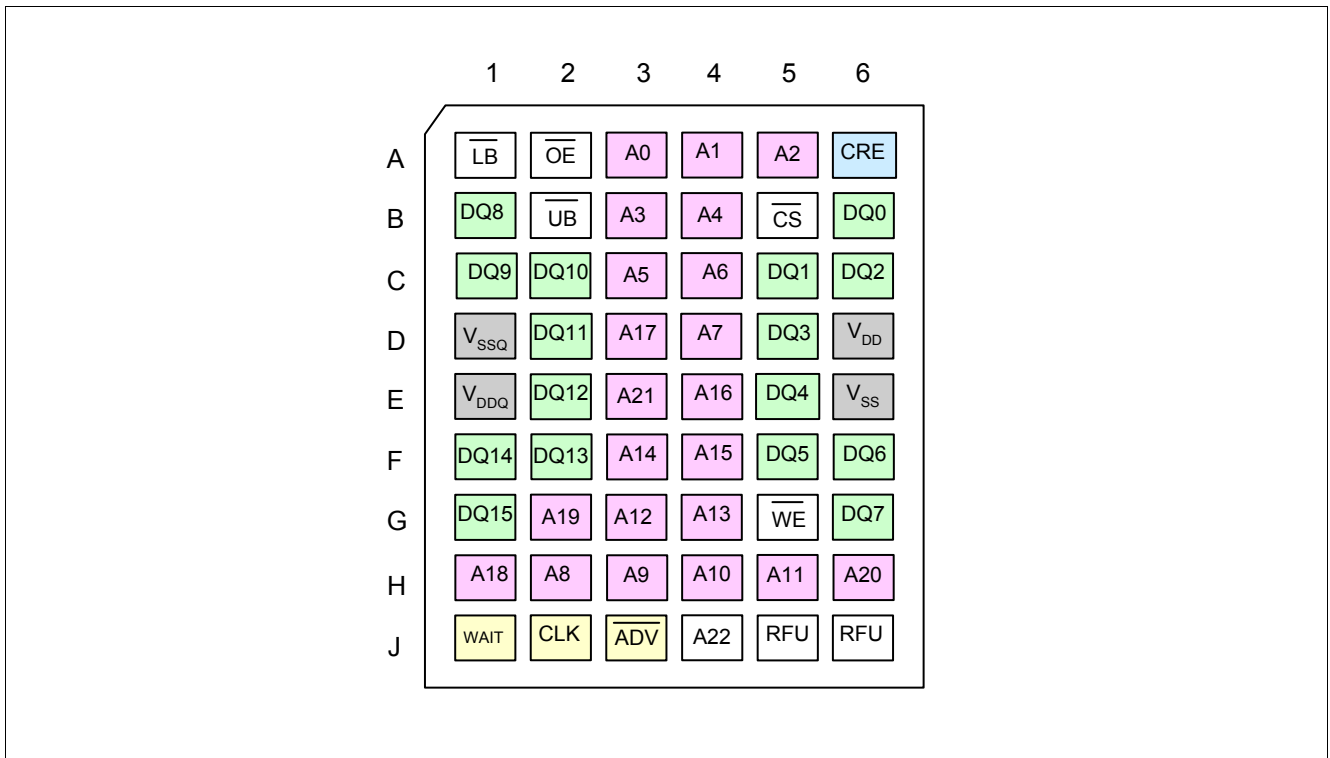
Figure 2 Standard Ballout - HYE18P64160AF-9.6/12.5/15

Note: **Figure 2** shows top view

Note: A22, ball J4, is not used for 64Mb CellularRAM

1.4 HYE18P64160AF-9.6/12.5/15 Ball Definition and Description

Table 2 Ball Description - HYE18P64160AF-9.6/12.5/15

Ball	Type	Detailed Function
CLK	Input	**Clock Signal** In synchronous burst mode, address and command inputs and data are referenced to the positive (rising) edge of CLK. In asynchronous SRAM-type mode and write accesses in NOR-Flash operation mode, the CLK signal must be tied down to low.
CRE	Input	**Control Register Enable** CRE set to high enables the access to the control register map. By applying the Set Control Register (SCR) command (see **Table 3**) the address bus is loaded into the selected control register, while Fetch Control Register (FCR) reads the contents of it onto DQ pins.
$\overline{ADV}$	Input	**Address Valid** $\overline{ADV}$ signals in NOR-Flash and full synchronous mode that a valid address is present on the address bus. In NOR-Flash read mode and full synchronous mode the address is latched on the programmed clock edge while $\overline{ADV}$ is held low. In NOR-Flash write mode $\overline{ADV}$ can be used to latch the address, but can be held low as well. In asynchronous SRAM-type mode $\overline{ADV}$ needs to be active, it may be tied to low.
$\overline{CS}$	Input	**Chip Select** $\overline{CS}$ enables the command decoder when low and disables it when high. When the command decoder is disabled new commands are ignored, addresses are don't care and outputs are forced to high-Z. Internal operations, however, continue. For the details, please refer to the command tables in **Chapter 1.6**.
$\overline{OE}$	Input	**Output Enable** $\overline{OE}$ controls DQ output driver. $\overline{OE}$ low drives DQ, $\overline{OE}$ high sets DQ to high-Z.
$\overline{WE}$	Input	**Write Enable** $\overline{WE}$ set to low while $\overline{CS}$ is low initiates a write command.
$\overline{UB}$, $\overline{LB}$	Input	**Upper/Lower Byte Enable** $\overline{UB}$ enables the upper byte DQ15-8 (resp. $\overline{LB}$ DQ7 … 0) during read/write operations. $\overline{UB}$ ($\overline{LB}$) deassertion prevents the upper (lower) byte from being driven during read or being written.
WAIT	Output 3-state	**Wait State Signal** In synchronous mode, WAIT signal indicates the host system when the output data is valid during read and when the input data should be asserted during write operation, though monitoring of WAIT is not mandatory for write burst, since a write burst operates at fixed latency always. In asynchronous mode, the signal has to be ignored.
A <21:0>	Input	**Address Inputs** During a Control Register Set operation by CRE access, the address inputs define the register settings.
DQ <15:0>	I/O	**Data Input/Output** The DQ signals $\overline{0}$ to $\overline{15}$ form the 16-bit data bus.
$1 \times V_{DD}$ $1 \times V_{SS}$	Power Supply	**Power Supply, Core** Power and Ground for the internal logic.
$1 \times V_{DDQ}$ $1 \times V_{SSQ}$	Power Supply	**Power Supply, I/O Buffer** Isolated Power and Ground for the output buffers to provide improved noise immunity.
$3 \times$ RFU	–	**Reserved for Future Use (RFU)** Please do not connect. J5 and J6 are reserved for future use. J4 will be A22 at 128Mb CellularRAM. See ballout in **Figure 2** on **Page 11**.

1.5 Functional Block Diagram
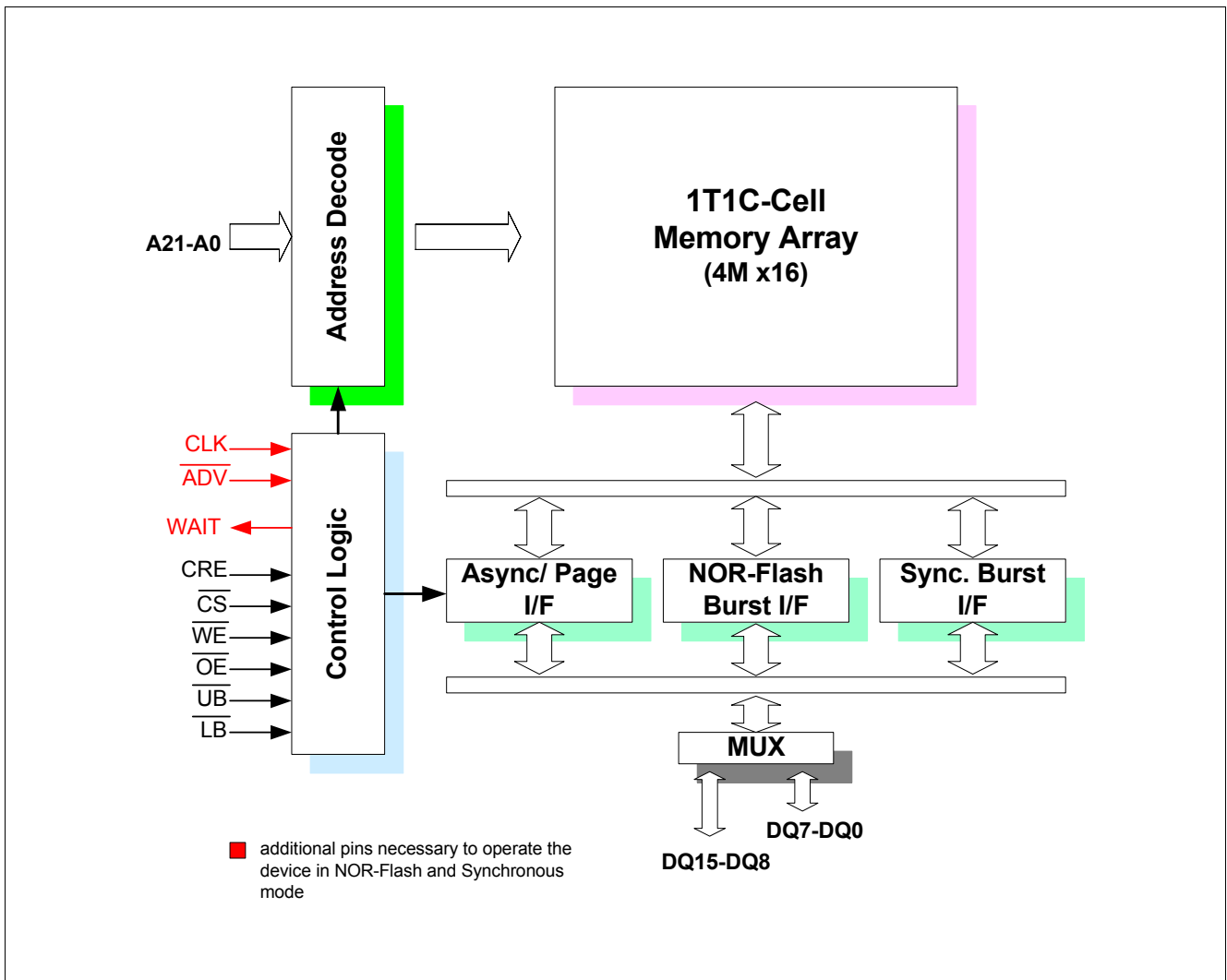
Figure 3   Functional Block Diagram

1.6 Commands

The supported command set depends on the selected operation mode. By default the CellularRAM device is reset to the asynchronous SRAM-type mode after power-up. To put the device in a different operation mode the Bus Configuration Register (BCR) must be programmed first accordingly. The valid control input states and sequences are listed below in asynchronous commands (while CLK is held low) or synchronous commands. Other control signal combinations are not supported.

1.6.1 Asynchronous Commands

In the SRAM-type operation mode, all commands are of asynchronous nature. Write operation in NOR-Flash mode is done asynchronously as well. **Table 3** lists the asynchronous commands and CLK has to be held low for entire asynchronous mode operation.

Table 3 Asynchronous Command Table[1]

Operation Mode	Power Mode	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{OE}$	$\overline{UB}/\overline{LB}$	CRE	A19	A18	Amax - A0	DQ15:0
READ	Active	L	L	H	L	L[2]	L	V	V	ADR	DOUT
WRITE	Active	L	L	L	X[3]	L[2]	L	V	V	ADR	DIN
Set Control REGISTER (SCR)	Active	L	L	L	X[3]	X	H	L H	L L	RCR DIN BCR DIN	X
Fetch Control REGISTER (FCR)	Active	L	L	H	L	L	H	L H X	L L H	X	RCR bits BCR bits Device ID
NO OPERATION	Standby~Active[4]	L	X	H	H	X	L	X	X	X	High-Z
DESELECT	Standby	H	X	X	X	X	X	X	X	X	High-Z
DPD[5]	DPD	H	X	X	X	X	X	X	X	X	High-Z

1) CLK has to be held low for entire asynchronous operation. Amax is A21 for 64Mb.

2) **Table 3** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0).

3) During a write access invoked by $\overline{WE}$ set to low the $\overline{OE}$ signal is ignored.

4) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. Toggling address results in active power mode. Also, NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

5) After entry, $\overline{CS}$ has to be held high to maintain DPD. $\overline{CS}$ low-going starts wake-up out of DPD and automatically reset DPD control bit (RCR Bit 4) to be diabled whether it is SCR command or not. All the other contents of control registers should be maintained during DPD in the same state when it was before this mode.

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 4 Description of Asynchronous Commands

Mode	Description
READ	The READ command is used to perform an asynchronous read cycle. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is output.
WRITE	The WRITE command is used to perform an asynchronous write cycle. The data is latched on the rising edge of either $\overline{CS}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, whichever comes first. The signals, $\overline{UB}$ and $\overline{LB}$, define whether only the lower, the upper or the whole 16-bit word is latched into the CellularRAM.

Table 4   Description of Asynchronous Commands (cont'd)

Mode	Description
SET CONTROL REGISTER	The control registers are loaded via the address inputs A19, A15 - A0 performing an asynchronous write access. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state.
FETCH CONTROL REGISTER	The content of selected control register is loaded via DQ15-DQ0 by performing this command. Please refer to the control register description for details. The FCR command can only be issued when the CellularRAM is in idle state.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS}$ = 0). Operations already in progress are not affected. Power consumption of this command mode varies by address change and initiating condition.
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 μA. Wake-up from DPD also requires 150 μs to get ready for normal operation. The use of DPD mode for duration of no longer than 1ms is not allowed.

1.6.2   Synchronous Commands

In NOR-Flash-type mode read commands are performed in a synchronous burst, whereas both read and write in synchronous mode.

All synchronous commands are defined by the states of the control signals $\overline{CS}$, $\overline{ADV}$, and $\overline{WE}$ ($\overline{UB}$, $\overline{LB}$ and $\overline{OE}$ controls output at read asynchronously and $\overline{UB}$, $\overline{LB}$ masks input data during write in synchronous way) at the positive (rising) edge of the clock signal, CLK. To enable the synchronous commands, the device has to be programmed in the Bus Configuration Register (BCR) first accordingly.

Table 5 lists the truth table for the supported synchronous commands.

Table 5   Synchronous Command Table[1]

Operation Mode	Power Mode	CLK	$\overline{CS}$	$\overline{ADV}$	$\overline{WE}$	$\overline{UB}/$ $\overline{LB}$	CRE	A19	A18	Amax - A0	DQ15:0
BURST INIT READ	Active	L->H	L	L	H	L	L	V	V	ADR	X
BURST READ	Active	L->H	L	H	X	L[2]	X	X	X	X	DOUT[3]
BURST INIT WRITE	Active	L->H	L	L	L	X	L	V	V	ADR	X
BURST WRITE	Active	L->H	L	H	X	L[2]	X	X	X	X	DIN
SET CONTROL REGISTER	Active	L->H	L	L	L	X	H	L H	L L	RCR DIN BCR DIN	X
FETCH CONTROL REGISTER	Active	L->H	L	L	H	L	H	L H X	L L H	X	RCR bits BCR bits Device ID
NO OPERATION	Standby~Active[4]	L->H	L	H	H	X	L	X	X	X	High-Z[5]
DESELECT	Standby	L->H	H	X	X	X	X	X	X	X	High-Z
DPD[6]	DPD	L	H	X	X	X	X	X	X	X	High-Z

1) Synchronous commands are sampled at rising edge of CLK except DPD. Amax is A21 for 64Mb.

2) **Table 5** reflects the behaviour if $\overline{UB}$ and $\overline{LB}$ are asserted to low. If only either of the signals, $\overline{UB}$ or $\overline{LB}$, is asserted to low only the corresponding data byte will be output or written ($\overline{UB}$ enables DQ15 - DQ8, $\overline{LB}$ enables DQ7 - DQ0). If both signals are disabled the device is put in deselect mode.

3) Output driver controlled by the asynchronous $\overline{OE}$ control signal

4) Stand-by power mode applies only to the case when $\overline{CS}$ goes low from DESELECT while no address change occurs. NO OPERATION from any active power mode by keeping $\overline{CS}$ low consumes the power higher than stand-by mode.

5) The asynchronous $\overline{OE}$ control signal has to be asserted to 'H'.

6) After entry, $\overline{CS}$ has to be held high to maintain DPD. $\overline{CS}$ low-going starts wake-up out of DPD and automatically reset DPD control bit (RCR Bit 4) to be diabled whether it is SCR command or not. All the other contents of control registers should be maintained during DPD in the same state when it was before this mode.

Note: 'L' represents a low voltage level, 'H' a high voltage level, 'X' represents "Don't Care", 'V' represents "Valid".

Table 6   Description of Synchronous Commands

Mode	Description
BURST INIT	The BURST INIT command is used to initiate a synchronous burst access and to latch the burst start address. The burst length is determined by the setting in the Bus Configuration Register.
BURST READ	The BURST READ command is used to perform a synchronous burst read access. The first data is output after the number of clock cycles as defined by the programmed latency mode.
BURST WRITE	The BURST WRITE command is used to perform a synchronous burst write access. The point of time when the first data is written is indicated by the WAIT signal. It varies with the selected clock frequency and the occurrence of a refresh cycle.
SET CONTROL REGISTER	The control registers are loaded via the address inputs A19, A15 - A0 performing a single word burst. Please refer to the control register description for details. The SCR command can only be issued when the CellularRAM is in idle state and no bursts are in progress.
FETCH CONTROL REGISTER	The content of selected control register is loaded on DQ15 - DQ0 by performing this command like a single read burst. Please refer to the control register description for details. The FCR command can only be issued when the CellularRAM is in idle state and no bursts are in progress.
NO OPERATION	The NOP command is used to perform a no operation to the CellularRAM, which is selected ($\overline{CS}$ = 0). Operations already in progress are not affected.
DESELECT	The DESELECT function prevents new commands from being executed by the CellularRAM. The CellularRAM is effectively deselected. I/O signals are put to high impedance state.
DPD	DPD stops all refresh-related activities and entire on-chip circuit operation. Current consumption drops below 25 μA. Wake-up from DPD also requires 150 μs to get ready for normal operation. The use of DPD mode for duration of no longer than 1ms is not allowed.

2 Functional Description

2.1 Power-Up and Initialization

The power-up and initialization sequence guarantees that the device is preconditioned to the user's specific needs. Like conventional DRAMs, the CellularRAM must be powered up and initialized in a predefined manner. V_{DD} and V_{DDQ} must be applied at the same time to the specified voltage while the input signals are held in "DESELECT" state ($\overline{CS}$ = High).

After power on, an initial pause of 150 μs is required prior to the control register access or normal operation. Failure to follow these steps may lead to unpredictable start-up modes.

Please note the default operation mode after power up is the asynchronous SRAM I/F mode (see **Chapter 2.4**).
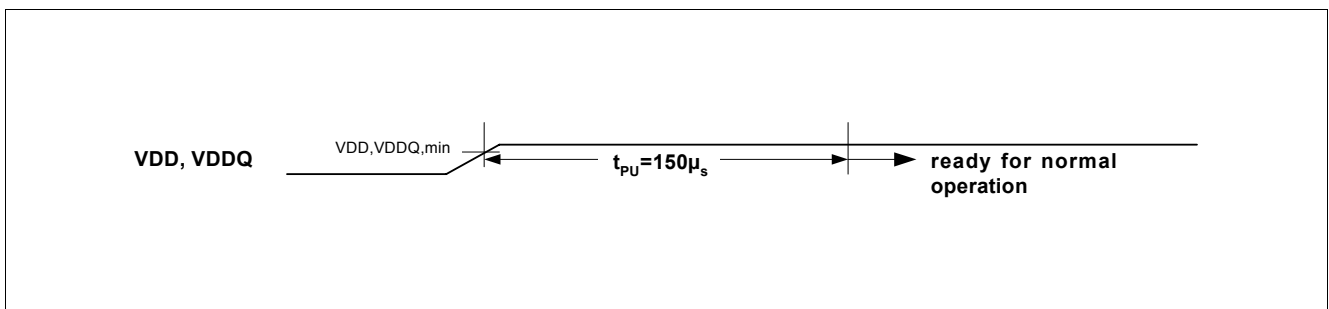
Figure 4   Power Up Sequence

2.2 Access To The Control Register Map

[Disclaimer]

Amax for 64Mbit CellularRAM is A21. A22 for 128Mbit density. A22 shown in timing diagrams has to be ignored for 64Mb CellularRAM.

Write access to the control register map is enabled by applying the SCR command asserting the CRE-pin to high. In combination with CRE set to high, Pin A19 designates the operation to one of either control registers. Pin A19 set to low selects the Refresh Control Register (RCR), Pin A19 set to high addresses the Bus Configuration Register (BCR), while A18 is applied low.

Write and read access to the control registers is also available at S/W entry method. For details, please refer to **"Appendix : S/W Register Entry Mode ("4-cycle method")" on Page 58**.
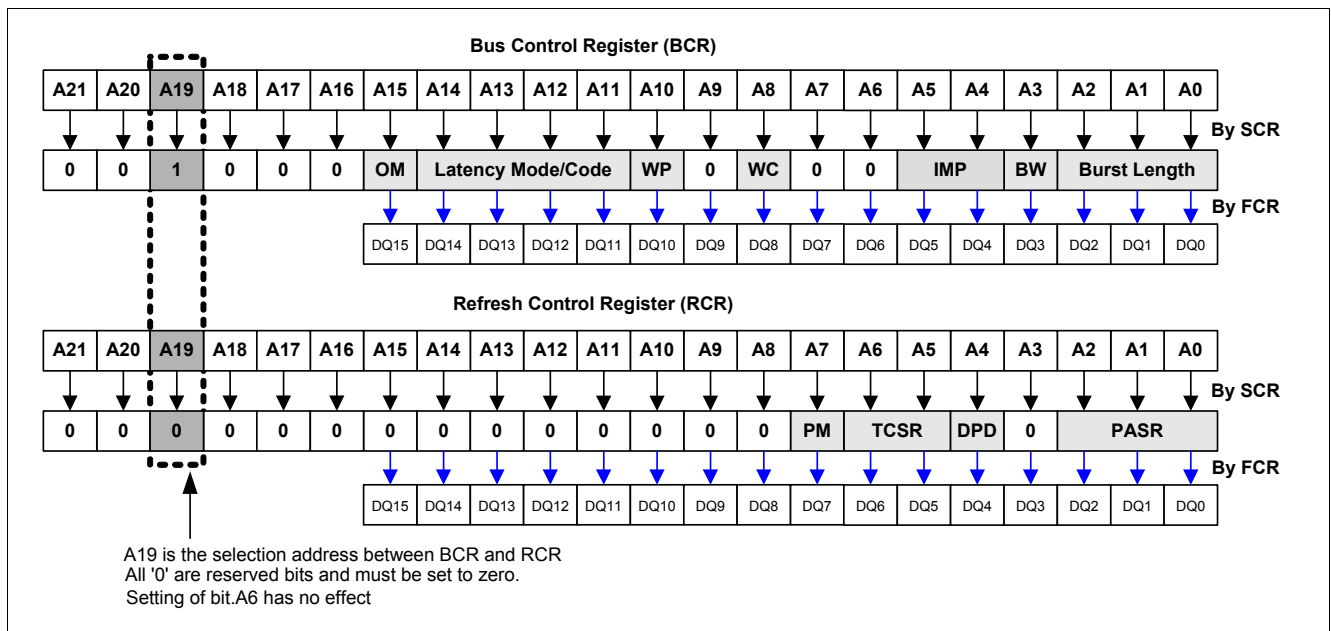
The two Control Registers (Write and Read access)
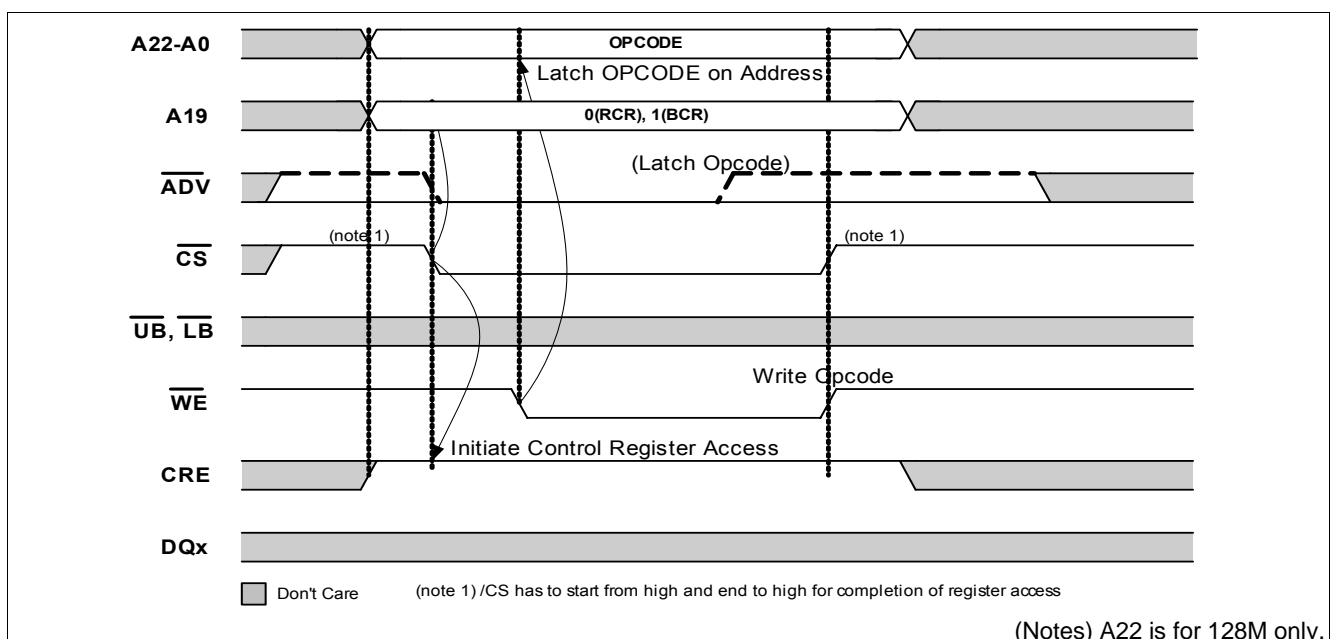
Figure 5   Control Register Write (SCR) in Asynchronous command

Figure 5 shows SCR command in asynchronous way. CRE is asserted high and the op-code is loaded to the selected register via address bus. A19 selects either BCR (=1) or RCR (=0) while A18 is supplied low. $\overline{ADV}$ may be held low for entire operation, but $\overline{CS}$ has to start from high, goes low, then back to high to complete the cycle.
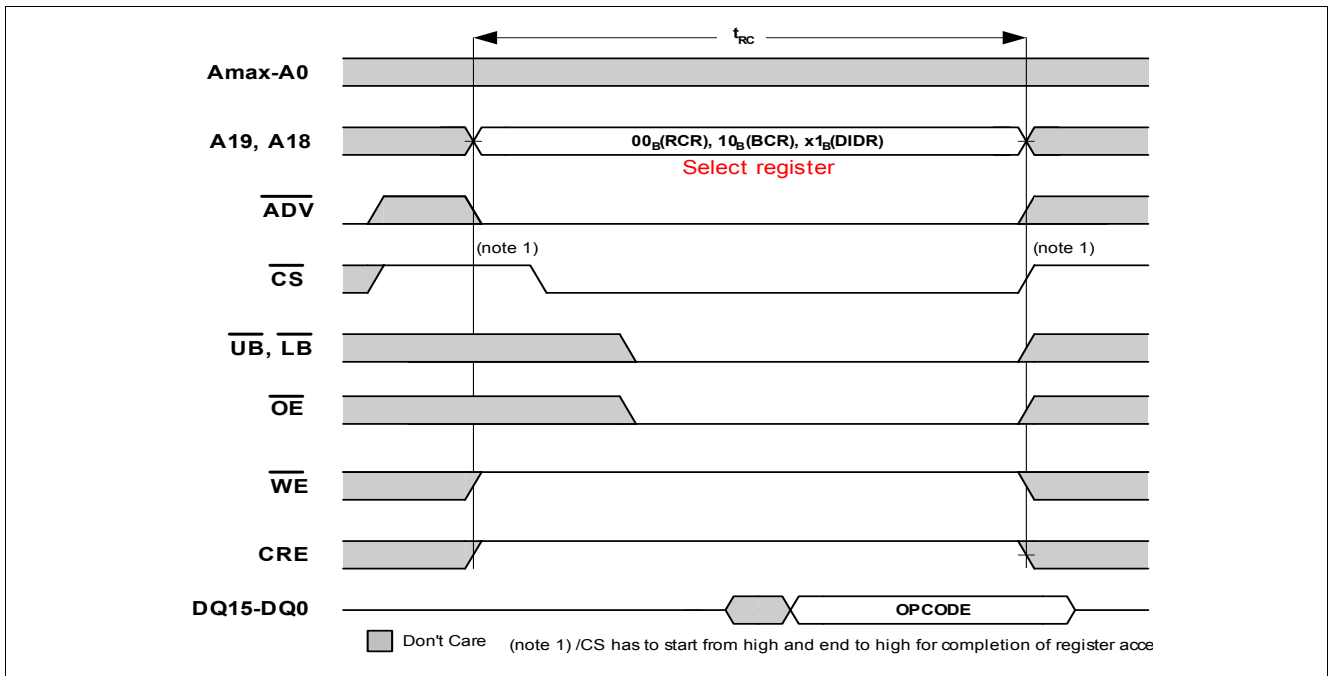
Figure 6   Control Register Read (FCR) in Asynchronous command

FCR command is introduced to this CellularRAM design so that the programmed content of the selected register can be checked. The timing diagram in **Figure 6** is identical to asynchronous read operation except CRE state.
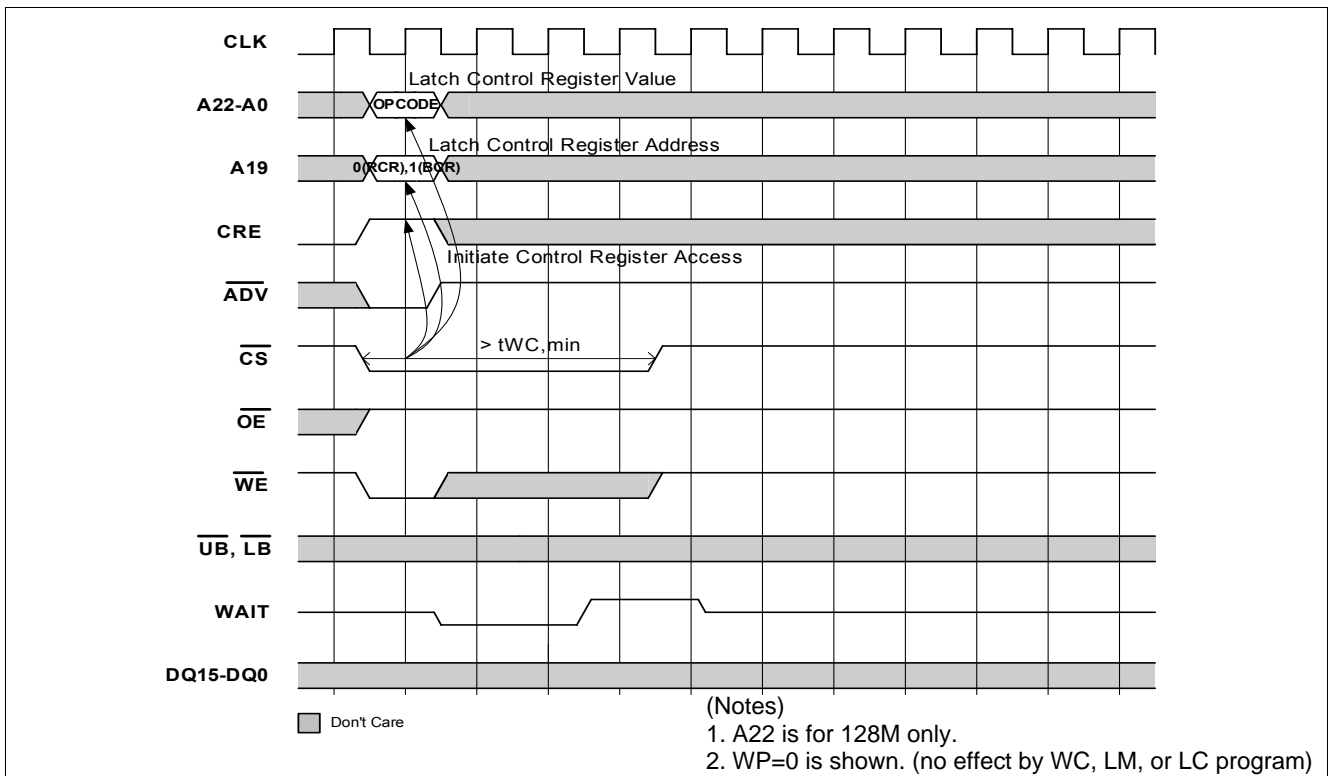
Figure 7   Control Register Write (SCR) in Synchronous Mode

SCR can be performed in synchronous way. CRE sampled high at rising edge of CLK initiates and completes the operation. Please note than WAIT goes deasserted after synchronous SCR command is decoded and $\overline{CS}$ has to go high to complete the cycle before issuing new command.
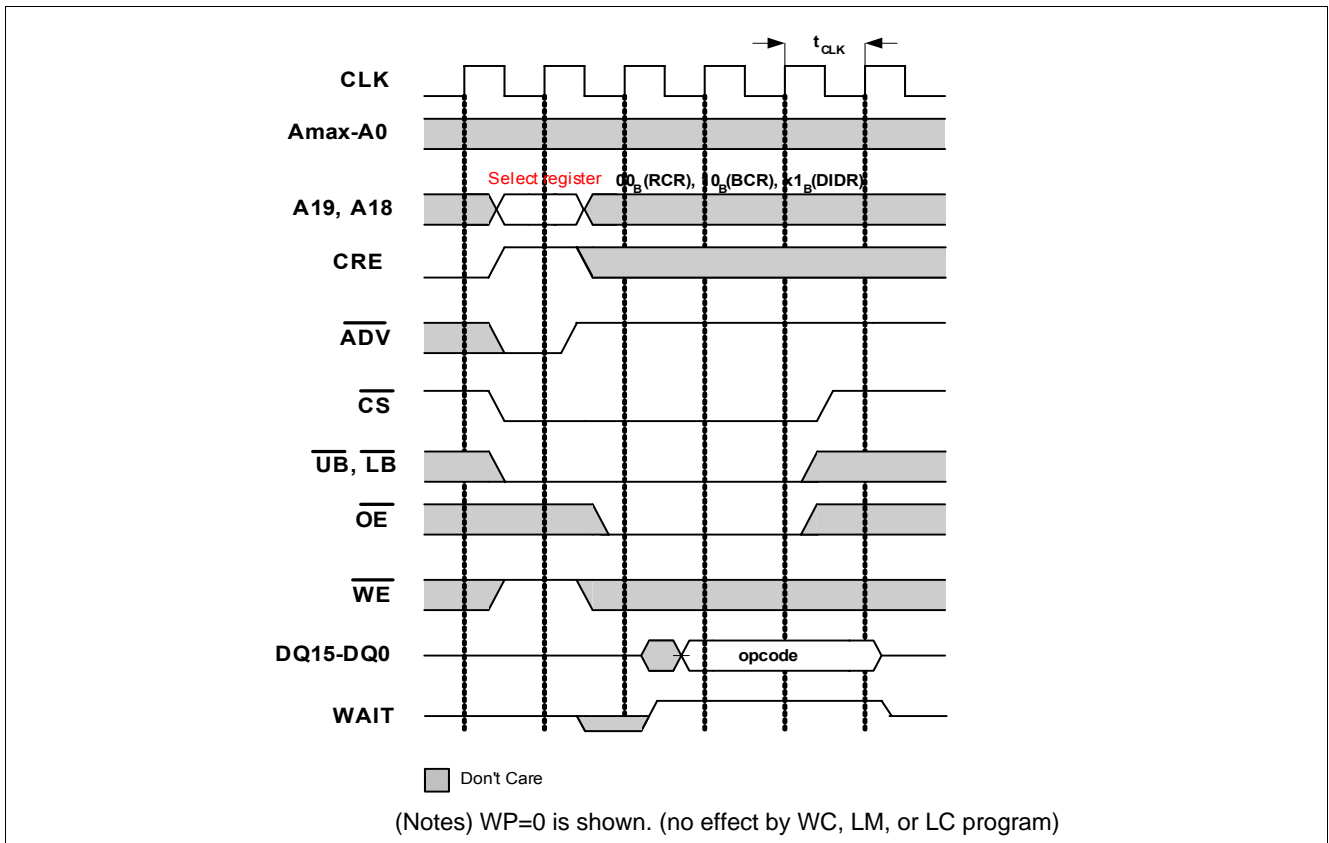
Figure 8   Control Register Read (FCR) in Synchronous Mode

FCR in synchronous command is identical to a read burst of single-bit, but high CRE enables read access from the register, not from the memory array. Please note than WAIT goes deasserted after synchronous SCR command is decoded and $\overline{OE}$ becomes low.

2.3 Refresh Control Register

The Refresh Control Register (RCR) allows to save stand-by power additionally by making use of the Partial-Array Self Refresh (PASR) and Deep Power Down (DPD) features. The Refresh Control Register is programmed via the Control Register Set command (with CRE = 1 and A19 = 0) and retains the stored information until it is reprogrammed or the device loses power. The field for the Temperature-Compensated Self Refresh (TCSR) is not in use since OCTS controls and adjusts refresh rate according to die temperature. Any setting of this field has no effect.

Please note that the RCR contents can only be set or changed when the CellularRAM is in idle state.

RCR
Refresh Control Register $\qquad$ **(CRE, A19 = 10$_B$)**

Amax-A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	**RS**						**0**						**PM**	**(TCSR)**		**DPD**	**0**		**PASR**	

Field	Bits	Type[1)	Description
RS	19	-	**Register Select** 0 set to 0 to select this RCR (= 1 to select BCR).
PM	7	wr	**Page Mode Enable/Disable** In asynchronous operation mode the user has the option to toggle A0 - A3 in a random way at higher rate (20 ns vs. 70 ns) to lower access times of subsequent reads with 16-word boundary. In synchronous mode this option has no effect. The max. page length is 16 words. Please note that as soon as page mode is enabled the $\overline{CS}$ low time restriction applies. This means that the $\overline{CS}$ signal must not be kept low longer than t_{CSL} = 4 µs. Please refer to **Figure 22**. 0 page mode disabled (default) 1 page mode enabled
(TCSR)	[6:5]	NA	**Temperature Compensated Self Refresh (Not in use)** The 2-bit wide TCSR field is not in use. On-chip temperature sensor (OCTS) adjusts the refresh period according to the actual temperature of die. Since DRAM technology requires higher refresh rates at higher temperature this enables the device to lower power consumption in case of low or medium temperatures. All are reserved. Setting has no effect.
DPD	4	wr	**Deep Power Down Enable/Disable** The DPD control bit puts the CellularRAM device in an extreme low power mode cutting current consumption to less than 25 µA. Stored memory data is not retained in this mode. The settings of both control registers RCR and BCR are maintained during DPD. Please note that the use of DPD mode for duration of no longer than 1ms is strictly prohibited. 0 DPD enabled 1 DPD disabled (default)

Field	Bits	Type[1]	Description
PASR	[2:0]	wr	**Partial Array Self Refresh** The 3-bit PASR field is used to specify the active memory array. The active memory array will be kept periodically refreshed whereas the disabled parts will be excluded from refresh and previously stored data will get lost. The normal operation still can be executed in disabled array, but stored data is not guaranteed. This way the customer can dynamically adapt the memory capacity to one's need without paying a power penalty. Please refer to **Figure 9**. 000 entire memory array (default) 001 lower 1/2 of the memory array (32 Mb) 010 lower 1/4 of the memory array (16 Mb) 011 lower 1/8 of the memory array (8 Mb) 100 zero 101 upper 1/2 of the memory array (32 Mb) 110 upper 1/4 of the memory array (16 Mb) 111 upper 1/8 of the memory array (8 Mb)
Res	max-20, [18:8], 3	w	**Reserved** must be set to '0'

1) wr: write-read access

2.3.1 Partial Array Self Refresh (PASR)

By applying PASR the user can dynamically customize the memory capacity to one's actual needs in normal operation mode and standby mode. With the activation of PASR there is no longer a power penalty paid for the larger CellularRAM memory capacity in case only e.g. 16 Mbits are used by the host system.

Bit2 down to bit0 specify the active memory array and its location (starting from bottom or top memory location). The memory array outside the selected range is powered down immediately after the mode register has been programmed. Advice for the proper register setting including the address ranges is given in **Figure 9**.
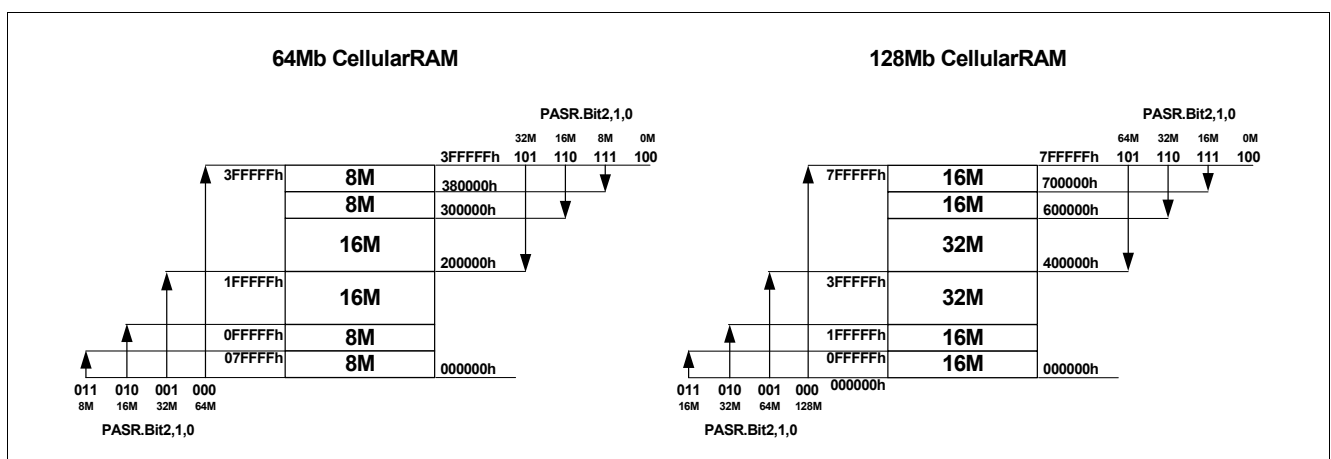
Figure 9   PASR Programming Scheme

PASR is effective in normal operation and standby mode as soon as it has been configured by register programming. Default setting is the entire memory array.

Figure 10 shows an exemplary PASR configuration where it is assumed that the application uses max. 16 Mbit out of 64 Mbit.
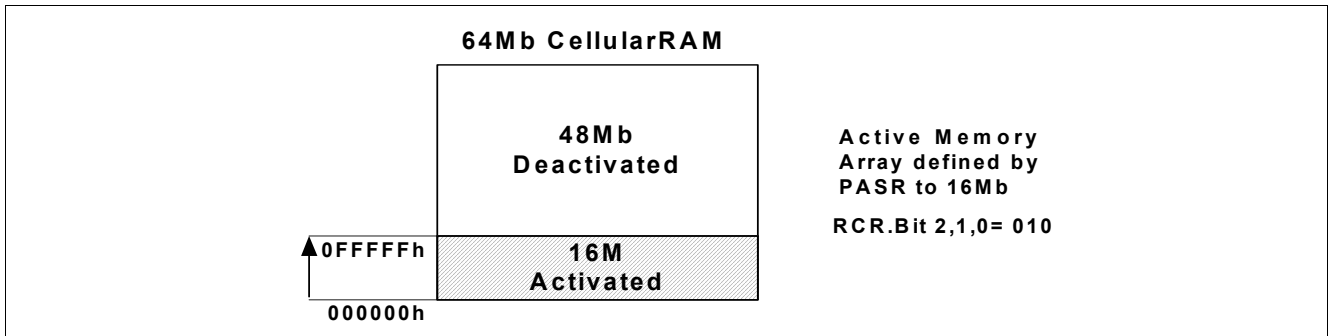
Figure 10   PASR Configuration Example

2.3.2   Deep Power Down Mode

To put the device in deep power down mode, the DPD control bit must be asserted to low and $\overline{CS}$ has to be pulled up and maintained high. Once set into this extreme low power mode current consumption is cut down to less than 25 µA until $\overline{CS}$ goes low automatically resetting the DPD control bit to be disabled.

All internal voltage generators inside the CellularRAM are switched off and the internal self-refresh is stopped. This means that all stored memory information will be lost by entering DPD. Only the register values of BCR and RCR are kept valid during DPD.

A guard time of at least 150 µs has to be met where no commands beside a NOP must be applied to re-enter again standby or idle mode.

Figure 11 helps to overview how DPD mode is entered, maintained, then exited. DPD mode starts from the time when $\overline{CS}$ is high and the DPD control bits is programmed to low (enabled). Then DPD exit is simply initiated by seeing $\overline{CS}$ low resulting in automatic reset of the DPD control bit. The time when DPD mode is maintained should exceed **150µs** for proper operation of the CellularRAM.
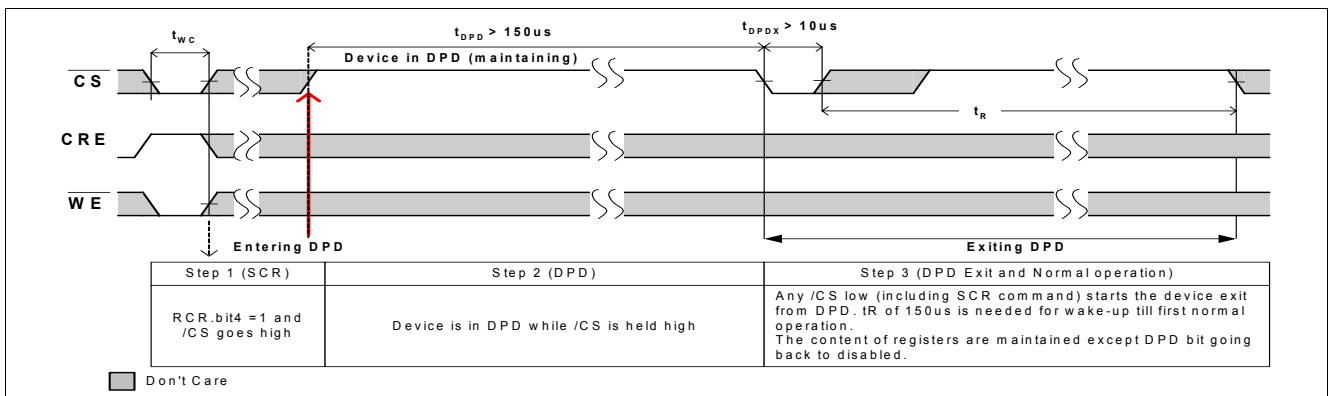
Figure 11   DPD Entry and Exit

Table 7 compares several methods available to suppress the power consumption down to deep level. Since wake-up time is required for DPD, it is recommended to use PASR of zero range for relatively short duration in the mode. To chop completely off the residual power consumption, disconneting the power supply from the device must be better.

Table 7   Timing Parameters for DPD Operation

Parameter	Symbol	9.6, 12.5, 15		Unit	Note
		Min.	Max.		
Duration of DPD operation	t_{DPD}	150	–	µs	–
DPD Exit Time	t_{DPDX}	10	–	µs	–
DPD Recovery Time	t_R	150	–	µs	–

2.3.3 Temperature Compensated Self Refresh (TCSR)

The setting of this register has no effect any longer due to the use of OCTS. Actual die temperature is measured and refresh rate is adjusted accordingly by OCTS.

2.3.4 Power Saving Potential in Standby When Applying PASR, TCSR or DPD

Table 8 demonstrates the currents in standby mode when PASR, TCSR or DPD is applied. TCSR is for reference only, since it reflects the reading of OCTS instead of external programming of the register.

The values in **Table 8** is not tested for all samples in every cases. For reference use only.

Table 8   Standby Currents When Applying PASR, TCSR or DPD

Operation Mode	Power Mode	PASR	RCR Control	Wake-Up Phase	Active Array	Standby [μA]			
						85°	70°	45°	15°
NO OPERATION/ DESELECT	STANDBY	TCSR	No (OCTS)	–	–				
		PASR	Bit2-0	–	Full	140	120	100	80
					1/2	110	100	90	75
					1/4	95	90	85	73
					1/8	90	85	80	73
					0	80	80	75	70
DPD	DEEP POWER DOWN	DPD	Bit4	~150 μs	0	25.0		10.0	

2.3.5 Page Mode Enable/Disable

In asynchronous operation mode, the user has the option to enable page mode to toggle A0 - A3 in random way at higher cycle rate (20 ns vs. 70 ns) to lower access times of subsequent reads within 16-word boundary. Write operation is not supported in the manner of page mode access. In synchronous mode, this option has no effect. The max. page length is 16 words, so which A0 - A3 is regarded as page-mode address. If the access needs to cross the boundary of 16-word (any difference in A21 - A4), then it should start over new random access cycle by toggling $\overline{CS}$.

Please note that as soon as page mode is enabled the $\overline{CS}$ low time restriction applies. This means that $\overline{CS}$ signal must not be kept low longer than t_{CSL} = 4 μs. Please refer to **Figure 22**.

Refresh Control Register (RCR)

Control Register Select

A19	control reg
0	RCR
1	BCR

A22, A21, A20, A18....A8: reserved, must be set to '0'.

Page Mode Bit

A7	page mode
0	disabled (def.)
1	enabled

Temperature-Compensated Self-Refresh (no effect)

A6	A5	max. case temp.
1	1	+85°C (def.)
0	0	+70°C
0	1	+45°C
1	0	+15°C

The reading from OCTS will override this register setting.

Deep Power Down Mode

A4	power down
0	enabled
1	disabled (def.)

Partial Array Self Refresh

A2	A1	A0	refreshed memory area
0	0	0	entire memory array (def.)
0	0	1	lower **1/2** of memory array
0	1	0	lower **1/4** of memory array
0	1	1	lower **1/8** of memory array
1	0	0	zero
1	0	1	upper **1/2** of memory array
1	1	0	upper **1/4** of memory array
1	1	1	upper **1/8** of memory array

(Notes) A22 is for 128M only

2.4 Bus Control Register

The Bus Control Register (BCR) specifies the interface configurations. For the various configuration options please refer to the register description below. The Bus Control Register is programmed via the Control Register Set command (with CRE = 1 and A19 = 1) and retains the stored information until it is reprogrammed or the device loses power. Most of BCR fields are assigned to configure the CellularRAM in a proper way to operate in burst mode and there are some additions to 1st-generation CellularRAM such as fixed latency mode, 32-word burst, etc.

Please note that the BCR contents can only be set or changed when the CellularRAM is in idle state.

Note: Bit 9 and bit 7 must be set to "0" for proper operation and setting of bit 6 has no effect.

BCR
Bus Control Register $\qquad$ **(CRE, A19 = 11$_B$)**

Amax-A20	A19	A18-A16	A15	A14	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
0	1	0	OM	Latency Mode/Code				WP	0	WC	0	X	IMP		BW	Burst Length		

Field	Bits	Type[1]	Description
RS	19	-	**Register Select** 1 set to 1 to select this BCR (= 0 to select RCR).
OP-MODE (OM)	15	wr	**Operation Mode** The CellularRAM supports three different interface access protocols, • the SRAM-type protocol with asynchronous read and write accesses • the NOR-FLASH-type protocol with synchronous read and asynchronous write accesses • the FULL SYNCHRONOUS mode with synchronous read and synchronous write accesses Operating the device in synchronous mode maximizes bandwidth. The NOR-Flash type mode is the recommended mode for legacy baseband systems which are not able to run the synchronous write protocol. The OPMODE bit defines whether the device is operating in synchronous (fully or partially) mode or asynchronous mode. 0 NOR-FLASH-type mode read: synchronous burst mode write: asynchronous access mode 0 FULL SYNCHRONOUS mode read: synchronous burst mode write: synchronous burst mode The mode of write operation, NOR-FLASH or FULL SYNCHRONOUS, is adaptively detected, which means asynchronous write operation in NOR-FLASH mode can be performed while CLK is stopped at low. If a rising clock edge occurs within $\overline{ADV}$ valid, FULL SYNCHRONOUS write is detected. Please refer to **Figure 30** on **Page 47** for asynchronous write and to **Figure 33** on **Page 50** for synchronous write. 1 SRAM-type mode (default) read: asynchronous access mode write: asynchronous access mode

Field	Bits	Type[1)	Description
LM, LC	[14], [13:11]	wr	**Latency Mode / Code** The latency is the number of CLK cycles from the burst_init command (the address valid strobe signal, $\overline{ADV}$ sampled at positive edge of CLK) to either the CLK being able to sample 1st valid data output (read burst) or to write 1st valid data input to the memory (write). 1st-generation CellularRAM only offers "variable latency mode" which may assert more wait cycles than programmed in the register (LC: latency code) when the burst operaiton collides with on-going refresh. Due to variable number of wait states possible at this mode, the monitoring WAIT signal is mandatory to use. The CellularRAM now adds the support on "fixed latency mode" for the legacy system which does not monitor WAIT signal. The choice of the mode is done by bit. 14. The latency code defines the number of the latency and configured in bit. 13-11. Bit.14=0 (default, variable latency mode), Bit13-11 is; 010 Variable latency 2, max 66MHz CLK 011 Variable latency 3 (default), max 104MHz CLK Bit.14=1 (fixed latency mode), Bit13-11 is; 010 Fixed latency 2, max 33MHz CLK 011 Fixed latency 3, max 52MHz CLK 100 Fixed latency 4, max 66MHz CLK 101 Fixed latency 5, max 75MHz CLK 110 Fixed latency 6, max 104MHz CLK *Note: All others reserved.*
WP	10	wr	**WAIT Polarity** The WAIT polarity control bit allows the user to define the polarity of the WAIT output signal. The WAIT output line is used during a synchronous read burst to signal when the output data is invalid (WAIT is active). 0 active low 1 active high (default)
WC	8	wr	**WAIT Configuration** The WAIT signal configuration control bit specifies whether the WAIT signal is asserted at the same time of the delay or whether it is asserted one clock cycle in advance to the data output or input. 0 WAIT is asserted during the delay 1 WAIT is asserted one data cycle before the delay (default)
IMP	[5:4]	wr	**Output Impedance** For adaptation to different system characteristics the output impedance can be configured. 00 Full drive strength of 25~30 Ω impedance 01 Half drive strength of 50 Ω impedance (default) 10 Quarter drive strength of 100 Ω impedance
BW	3	wr	**Burst Wrap** The burst wrap control bit defines whether there is a wrap around within a burst access or not. In case of fixed 8-word burst length, this means that after $\overline{word7}$, $\overline{word0}$ is going to be output in wrap mode. In case of continuous burst mode the internal address counter will wrap from the last address, $3FFFFF_H$ to 000000_H regardless of the setting. Please note this setting is applied to both read and write burst. 0 wrap 1 no wrap (default)

Field	Bits	Type[1]	Description
BL	[2:0]	wr	**Burst Length** Via the burst length field the user can select between fixed burst lengths of 4, 8, 16, 32, or any arbitrary burst length until it reaches the end of row by choosing the continuous mode option. In continuous mode the burst length is controlled by the active low period of the control lines $\overline{CS}$. Please note this setting is applied to both read and write burst. 001 4-word burst 010 8-word burst 011 16-word burst 100 32-word burst 111 continuous (default) *Note: All others reserved.*
Res	21, 20, [18:16], 14, 9, 7, 6, 4	-	**Reserved** must be set to '0' except Bit.6 which has no effect by setting.

1)   wr: write-read access

Bus Control Register (BCR)
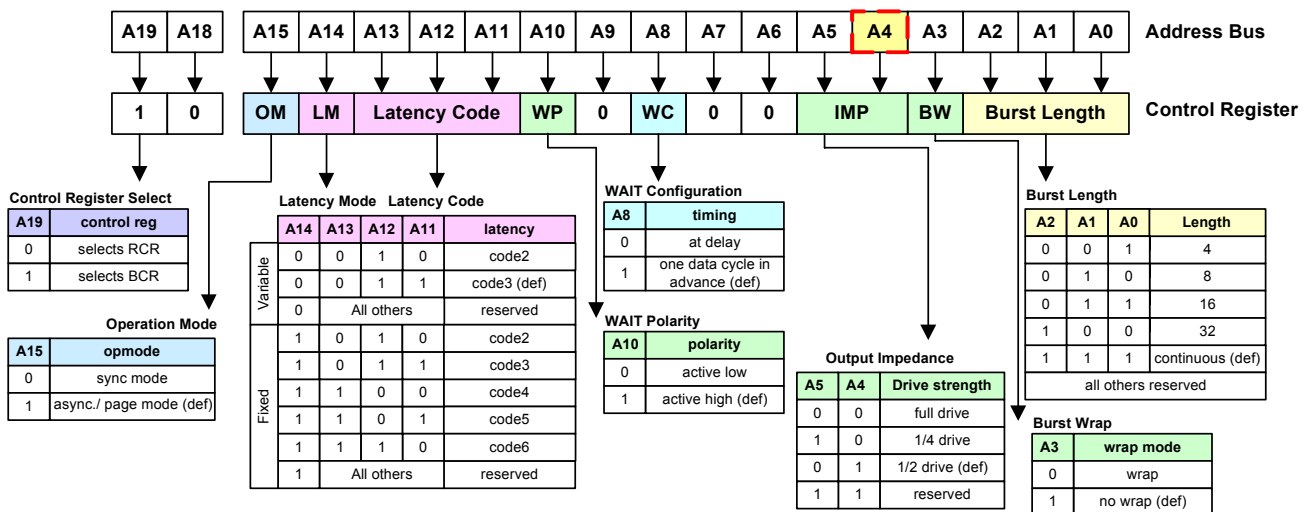
2.4.1   Latency Mode / Code

The latency code defines the number of clock cycles which pass before the first output data is valid within a read burst access (counting from the clock edge where $\overline{ADV}$ was detected low) or the first data input becomes valid within a write burst access. The invalid state on DQ pins is indicated by asserting WAIT signal active, so that the latency equals to the number of wait states.

2.4.1.1   Variable latency mode

2 latency modes are supported in this design - Variable or Fixed. In variable latency mode, compatible to first-generation CellularRAM, the latency code programmed in BCR represents only the minimum latency of the CellularRAM, since the latency may be extended (means more wait states) if the burst collides with on-going self refresh operation. The wrap-off burst or continuous burst may continue across the row boundary (each row has

256-word size, coupled to every address of FF$_H$). Since boundary crossing is not supported in CellularRAM 1.5G, the controller has to manage such a case by either terminating the ongoing burst at the end of row or issuing new burst command to continue with designated address location. Refer to **"End-of-Row Condition" on Page 30** for more details.

The programmed latency code is only based on the case of new burst_init command from all precharged memory (usually $\overline{CS}$ toggling from high to low) when no refresh operation is performed. Variable latency mode is capable of offering higher CLK frequency at the given latency code. For example, latency code of 3 in variable latency can operate the CellularRAM at max 104MHz CLK, but the same code in fixed latency only upto 52MHz.

This unpredictable nature of latency code makes the monitoring of WAIT signal mandatory, since only WAIT signal can inform when the valid data is present.
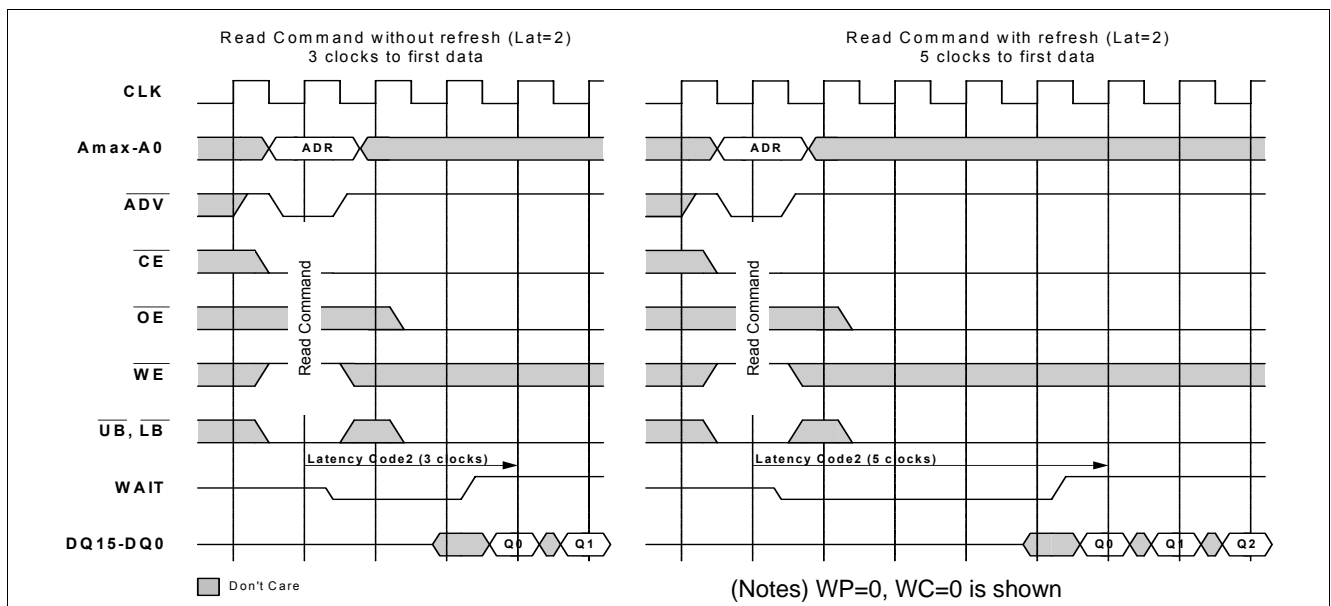
Figure 12   Variable Latency Mode - Functional Diagram (Lat=2, Variable, WC=0 shown)

2.4.1.2   Fixed latency mode

In the contrast to variable latency mode, the fixed latency mode guarantees that the initial latency of any burst operation always equals to the code programmed in BCR whether on-going refresh is in place or not. The latency code is derived from the longest path of the delay which includes refresh operation and initial burst access. Therefore, the fixed latency limits CLK frequency lower than the same latency of variable latency mode (52MHz Vs. 104MHz at latency code = 3). The row boundary crossing is **not permitted**. The number of inserted wait cycles, which is the latency code, increases along with the input clock frequency. Please refer to **Table 9** for the proper setting.

Table 9   Latency Mode / Code Configuration

Latency Mode	Latency Code	Max. Input Clock Frequency [MHz]		
		-9.6	**-12.5**	**-15**
Variable (Bit.14=0) (default)	2	66	66	40
	3	104	80	66
	all others	reserved	reserved	reserved

Table 9   Latency Mode / Code Configuration (cont'd)

Latency Mode	Latency Code	Max. Input Clock Frequency [MHz]		
		-9.6	-12.5	-15
Fixed (Bit.14=1)	2	33	33	20
	3	52	52	33
	4	66	66	40
	5	75	75	52
	6	104	80	66
	all others	reserved	reserved	reserved
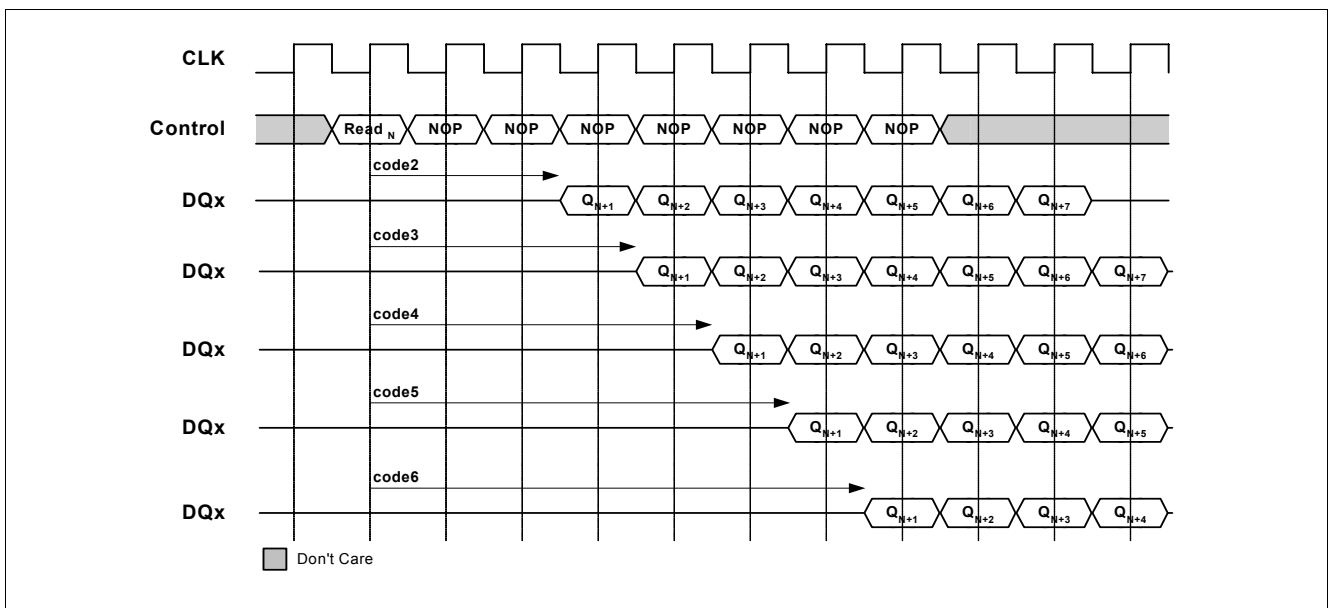
Figure 13   Latency Code - Functional Diagram

2.4.1.3   Burst Write always produces fixed latency

The monitoring of WAIT for a write burst may become blocking point to the system upgrading CLK frequency. Unlike WAIT is used to indicate valid data output on DQ pins from the CellularRAM can be sampled at the controller during a read burst, the controller has to drive next data input onto DQ pins in time once WAIT is de-asserted.

To address this concern, the CellularRAM in this design offers fixed latency always for a write burst though latency mode bit is configured in variable latency (BCR.bit14=0). The fixed latency behavior of a write burst while read burst in variable latency mode applies to burst_init situation. The controller has to observe maximum t_{CSL} (= 4 μs) in case a write burst continues over long bursts. As discussed in **"Burst Interrupt operation" on Page 30**, burst interrupt operation while $\overline{CS}$ being held low is another case which can not schedule refresh operation properly, so that t_{CSL} (= 4 μs) limitation also applies.

On the other hand, if BCR.bit14 is set to "1", the CellularRAM operates in fixed latency mode. The latency for a write burst, of course, is fixed at burst_init command. Burst interrupt operation while $\overline{CS}$ being held low is the case which can not schedule refresh operation properly, so that t_{CSL} (= 4 μs) limitation applies.

2.4.1.4 Burst Interrupt operation

When any burst is complete or needs to be terminated to start new burst, bringing $\overline{CS}$ high and back low in next clock cycle is usual and recommended. Burst interrupt is referred to the case when the on-going burst is terminated by newly issued burst_init command without toggling $\overline{CS}$. In case of doing this, special care has to be taken to avoid any malfunction of CellularRAM.

In any case, the burst interrupt is prohibited until burst_init command completes the first valid data cycle (first data output or first data input cycle) as shown in **Figure 14**. At new burst_init command, DQ pins go into high-Z if on-going burst is a read. In case of write burst being interrupted, the data input is masked, not updated to the memory location.
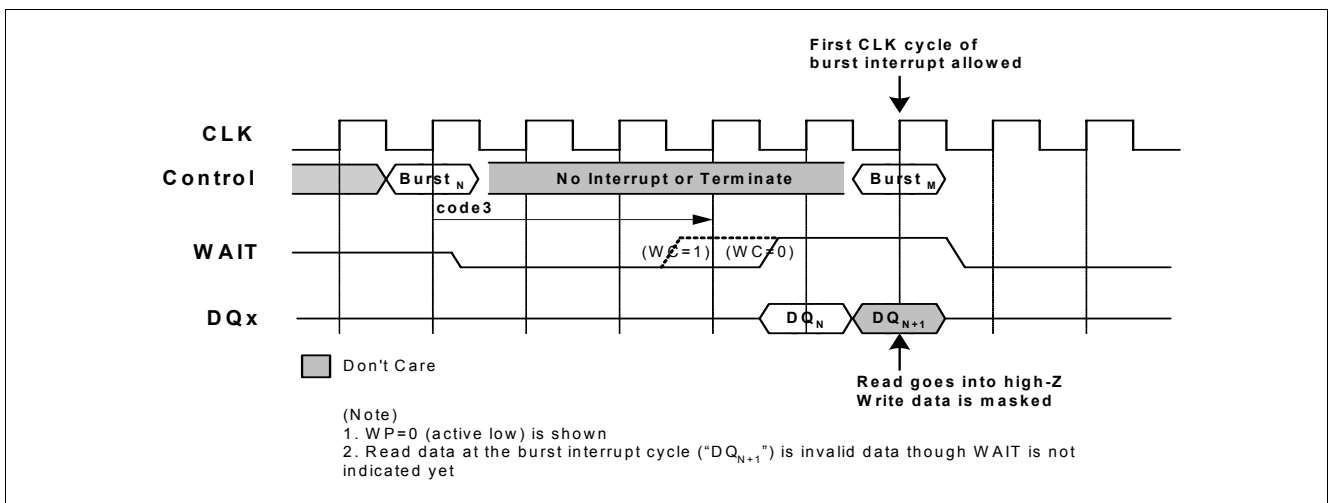
Figure 14   Burst Interrupt after Burst_init command

(1) In variable latency mode;

Read burst works at variable latency, but write burst has to meet fixed latency requirement. Unlike normal burst_init situation from precharged memory, burst interrupt by a write burst does not schedule refresh operation.

- On-going read or write burst can be interrupted by a read burst. Refresh is taken in place if needed, but additional wait cycles are added to the latency for a read burst.
- On-going read or write burst can be interrupted by a write burst. Refresh is never scheduled in this case. $\overline{CS}$ low time being engaged with the interrupt by write burst should not exceed maximum t_{CSL} (= 4 µs).

(2) In fixed latency mode;

The fixed latency mode is designed to completely guarantee the refresh operation at burst_init situation from the precharged memory (from $\overline{CS}$ high). However, any burst interrupt while $\overline{CS}$ is held low can not guarantee proper refresh operation in fixed latency mode.

Maximum t_{CSL} (= 4 µs) limit should be observed for any burst operation whether it is interrupted or not.

2.4.1.5 End-of-Row Condition

The CellularRAM in this design has the row size of 256-word, so that boundary between adjacent rows (= end of row) takes place at every address of FF_H (FF_H, $1FF_H$, $2FF_H$, ..). If the burst operation continues over the boundary when it is in continous burst mode or wrap-off burst advances, the controller should take care of it when the ongoing burst reaches the end of row. It may do terminate ongoing burst or issue new burst_init command of next row or random location different from next address. WAIT pin indicates when the ongoing burst meets the end of row condition.

Note: If the controller can do nothing with the ongoing burst at the end of row, the row boundary crossing operation will occur so that WAIT goes de-asserted back with valid next data after a few clock cycles. Monitoring WAIT

is mandatory in this case, since the CellularRAM from different vendors may have not identical behavior as to row boundary crossing. Please contact factory for advice.

The end of row condition can be detected by tracking the address of ongoing burst, of course. Since the row size may be different over the vendors, it is available to read out the row size through accessing device ID register (DIDR). Please refer to **"Device ID Register (DIDR)" on Page 34** for details.

Figure 15 depicts WAIT timing and recommended operation when the burst advances to the end of row.
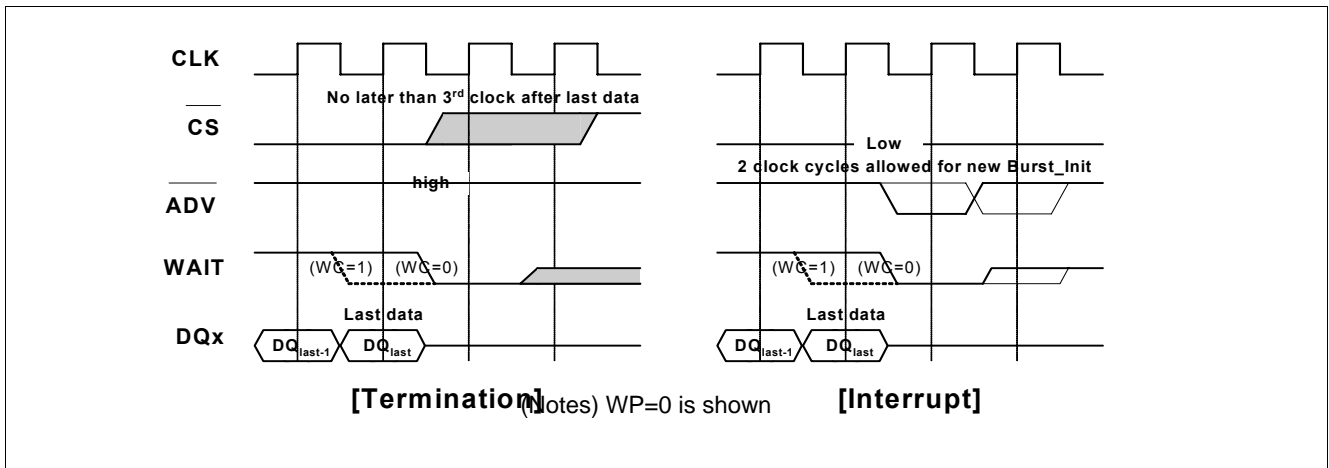
Figure 15   WAIT Timing and Recommended Operation at the End of Row

2.4.2 Read Burst Configurations/Sequences

The numbers of words that are accessed during a burst is defined by the burst length field which is programmed in the Bus Control Register. The user can either program fixed burst lengths of 4-, 8-, 16-, or 32-words or operate the device in continuous mode operation. The burst start address is latched by $\overline{ADV}$ set to low at burst_init command time. An internal address counter then increments automatically the address with respect to the programmed burst length.

Continuous burst operation offers arbitrary length of burst until it reaches the end of row. In other words, unlike with fixed burst lengths, a continuous burst goes on until it is actively terminated by bringing $\overline{CS}$ to high.

The wrap mode option specifies whether the burst address overflows and restarts at address $\overline{0}$ (A4 - A0) or keeps incrementing. For the several possible burst sequences please refer to **Table 10**.

Table 10   Burst Sequences

Burst Length	Starting Address (A4 A3 A2 A1 A0)	Sequential Burst Addressing Scheme (decimal)	
		Wrap On	**Wrap Off** [1]
4	xxx00 xxx01 xxx10 xxx11	0 1 2 3 1 2 3 0 2 3 0 1 3 0 1 2	0 1 2 3 1 2 3 4 2 3 4 5 3 4 5 6
8	xx000 xx001 xx010 … … xx101 xx110 xx111	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 0 2 3 4 5 6 7 0 1 … … 5 6 7 0 1 2 3 4 6 7 0 1 2 3 4 5 7 0 1 2 3 4 5 6	0 1 2 3 4 5 6 7 1 2 3 4 5 6 7 8 2 3 4 5 6 7 8 9 … … 5 6 7 8 9 10 11 12 6 7 8 9 10 11 12 13 7 8 9 10 11 12 13 14
16	x0000 x0001 x0010 … … x1101 x1110 x1111	0 1 2 … 13 14 15 1 2 3 … 14 15 0 2 3 4 … 15 0 1 … … 13 14 15 … 10 11 12 14 15 0 … 11 12 13 15 0 1 … 12 13 14	0 1 2 … 13 14 15 1 2 3 … 14 15 16 2 3 4 … 15 16 17 … … 13 14 15 … 26 27 28 14 15 16 … 27 28 29 15 16 17 … 28 29 30
32	00000 00001 00010 … … 11101 11110 11111	0 1 2 … 29 30 31 1 2 3 … 30 31 0 2 3 4 … 31 0 1 … … 29 30 31 … 26 27 28 30 31 0 … 27 28 29 31 0 1 … 29 30 31	0 1 2 … 29 30 31 1 2 3 … 30 31 32 2 3 4 … 31 32 33 … … 29 30 31… 58 59 60 30 31 32… 59 60 61 31 32 33… 60 61 62
Continuous [1]	n	Cn, Cn+1, Cn+2, … Cmax [2] (default, write burst)	

1) Wrap-off burst goes up to the end of row.

2) Cmax = end of row

2.4.3 WAIT Signal in Synchronous Burst Mode

The WAIT signal is used in synchronous burst read mode to indicate to the host system when the output data is invalid. Periods of invalid output data within a burst access might be caused either by first access delays, or by self-refresh cycles.

To match with the Flash interfaces of different microprocessor types the polarity and the timing of the WAIT signal can be configured. The polarity can be programmed to either active low or active high logic. The timing of the WAIT signal can be adjusted as well. Depending on the BCR setting the WAIT signal will be either asserted at the same time the data becomes invalid or it will be set active already one clock period in advance.

In asynchronous read mode including page mode, the WAIT signal is not used but always stays asserted as BCR. bit 10 is specified. In this case, system should ignore WAIT state, since it does not reflect any valid information of data output status.
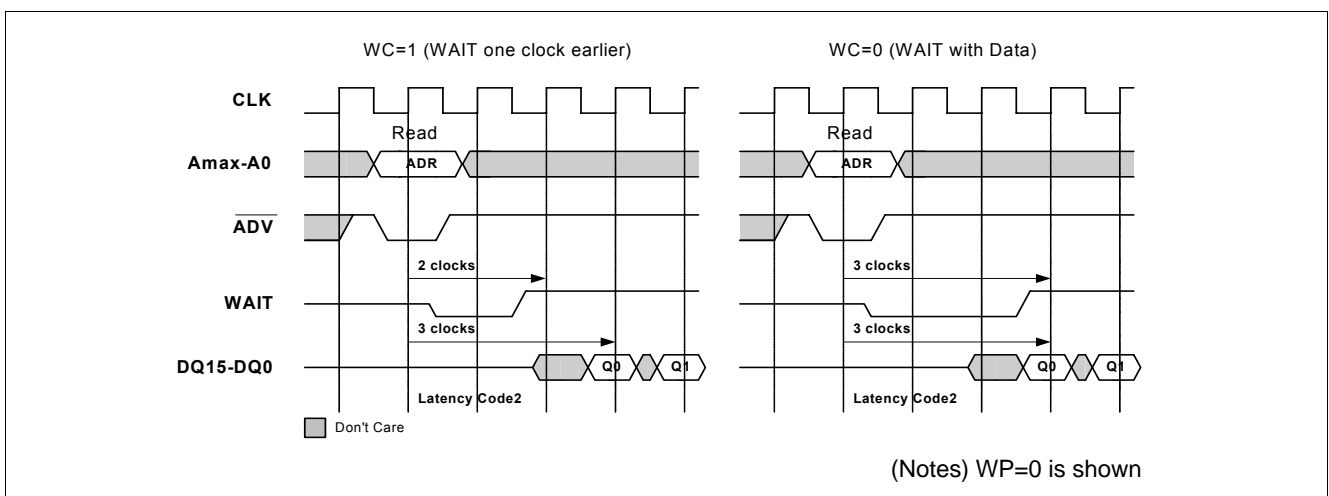
Figure 16   WAIT Function by configuration (WC) - Lat=2, WP=0

2.4.4 Output Impedance

According to the setting of BCR.bit 4 and bit5, the output drive strength can be adjusted to full, one-half, or one-quarter strength. The choice must depend on loading condition of DQ bus and speed requirement of the system. Reduced-drive strength on very heavily loaded bus will slow down the speed too much, while full drive strength on the bus of relatively light loading will result in unacceptable noise. Please refer to **Table 11** for general guidance of proper selection of output drive strength.

Table 11   Output Impedance

BCR.bit <5:4>	Drive Strength	Impedance Typ. (Ohm) [1]	Use Recommendation
00_B	Full	25~30	C_L = 30pF or heavier
01_B (default)	1/2	50~60	C_L = 15pF to 30pF AC test load for spec parameters
10_B	1/4	100~120	C_L = 15pF or lighter

1) The value is for reference only. Not all samples tested. Refer to IBIS model for accurate I-V characteristics.

2.5 Self-Refresh

The CellularRAM relieves the host system from triggering and commanding refresh-operations like it is the case with conventional DRAMs by performing automatic self-refresh. Self-refresh operations are autonomously scheduled and performed by the CellularRAM device.

2.6 Device ID Register (DIDR)
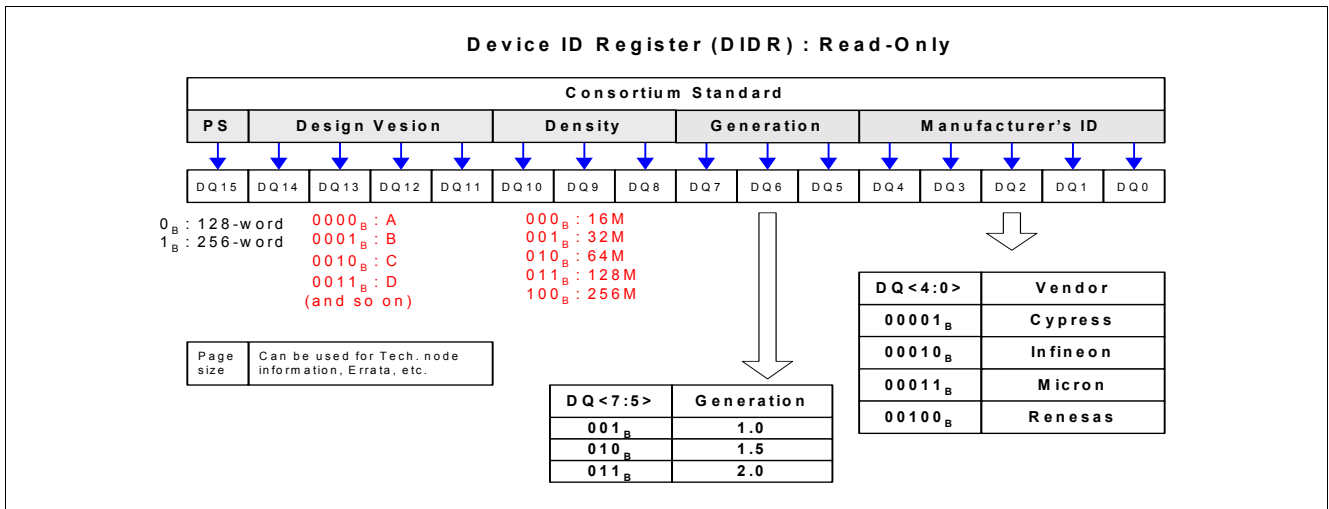
Figure 17 Device ID Register (DIDR) Mapping

Device ID register offers the way the user can check manufacturer's ID (5-bit), spec-compliance generation of CellularRAM (3-bit), density (3-bit), design version (4-bit), and page size (1-bit) information.

This is read-only register, so that SCR command has no effect to the content of DIDR. A18 input has to be applied HIGH to select DIDR at FCR command timing when CRE-controlled is used(**Figure 6** and **Figure 8**).

DIDR
Device ID Register (CRE, A18 = 11$_B$)

A18		bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
1		**PS**	**Design Version**				**Density**			**Generation**			**Manufacturer's ID**				

		Page size	**Design Version**	**Density**	**Spec_Gen**	**Manufacturer's ID**	
		1_B : 256-w	0000_B : A 0001_B : B and so on	010_B : 64M	010_B : 1.5	00010_B : Infineon	

(Read-only register)

For bit 15 of page size, please ignore the readout in case that the information is not needed.

2.7 Consideration on Address Skew

It is understood that the skew among multiple address lines is unavoidable. However, the amount of it has to be well controlled for proper device operation.
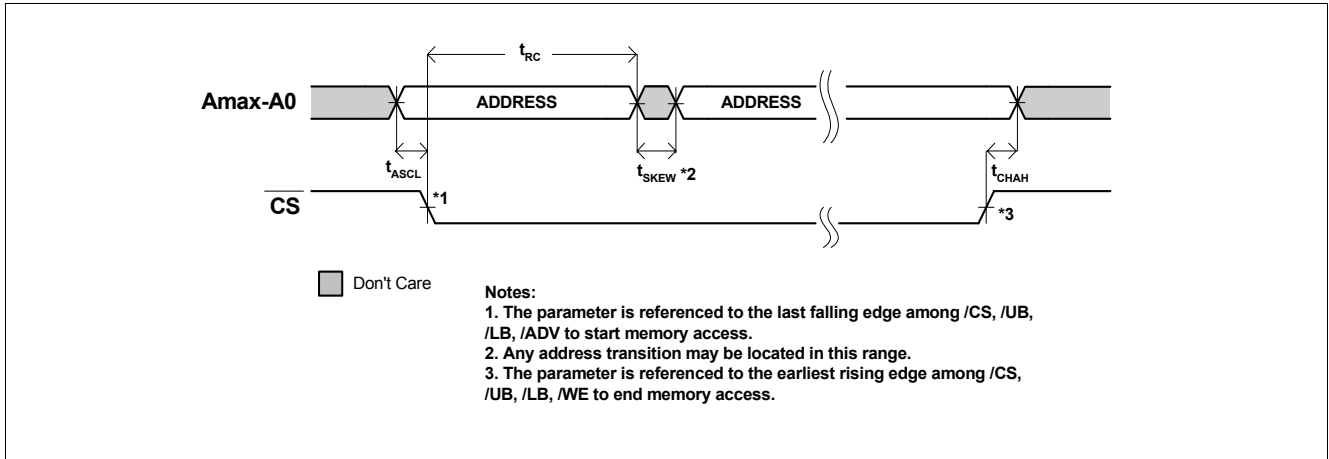
Figure 18   Timing Diagram of Address Skew

As depicted in **Figure 18**, 3 parameters have to be met to avoid any malfunction of the device. Any valid address input when all active control signals - $\overline{CS}$, $\overline{UB}$, $\overline{LB}$, and $\overline{ADV}$ become low has to meet $t_{RC.}$

Table 12   Timing Parameters - Address Skew

Parameter	Symbol	9.6, 12.5		15		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	70	–	85	–	ns	–
Address skew window	t_{SKEW}	–	10	–	10	ns	–
Address set-up to the last active control signal low	t_{ASCL}	-10	–	-10	–	ns	–
Address hold from the first active control signal high	t_{CHAH}	0	–	0	–	ns	1, 2

Note: 1. In case of $\overline{ADV}$ latching the address, this parameter is not applied.

Note: 2. In page read mode, 0ns is required for this parameter in case that inter-page address, A4 and higher change.

2.8 SRAM-Type Mode

[Disclaimer]

Amax for 64Mbit CellularRAM is A21. A22 is for 128Mbit density. WAIT signal is shown in the selected timing diagrams for the case of WP=0 (active low) though it is not default state.

In SRAM-type mode, the CellularRAM applies asynchronous SRAM protocol to perform read and write accesses.

2.8.1 Asynchronous Read

After power-up the CellularRAM operates per default in asynchronous SRAM-type mode. The synchronous clock line, CLK has to be held low, while address latch signal, $\overline{\text{ADV}}$ can be held low for entire read and write operation in this mode or toggled to latch valid address input (refer to **"Asynchronous Write with Address Latch (ADV) Control" on Page 47** for detailed timing diagram and parameters as to toggling $\overline{\text{ADV}}$). **WAIT is asserted as BCR. Bit 10 is programmed during $\overline{\text{CS}}$ low time, so that the controller should ignore WAIT during asynchronous mode operation**. (not shown in all timing diagrams)

Reading from the device in asynchronous mode is accomplished by asserting the Chip Select ($\overline{\text{CS}}$) and Output Enable ($\overline{\text{OE}}$) signals to low while forcing Write Enable ($\overline{\text{WE}}$) to high. If the Upper Byte ($\overline{\text{UB}}$) control line is set active low then the upper word of the addressed data is driven on the output lines, DQ15 to DQ8. If the Lower Byte ($\overline{\text{LB}}$) control line is set active low then the lower word of the addressed data is driven on the output lines, DQ7 to DQ0.

The access time is determined by the triggering input - slowest one in low-going transition - in combination with access timing parameters among valid address (t_{AA}), $\overline{\text{CS}}$(t_{CO}), $\overline{\text{OE}}$(t_{OE}), $\overline{\text{UB}}$ or $\overline{\text{LB}}$(t_{BA}), or $\overline{\text{ADV}}$(t_{AADV}).
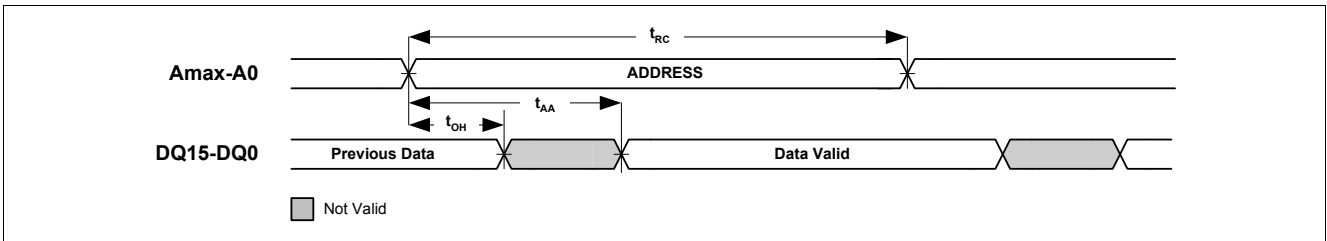
Figure 19   Asynchronous Read - Address Controlled ($\overline{\text{CS}} = \overline{\text{OE}} = V_{IL}$, $\overline{\text{WE}} = V_{IH}$, $\overline{\text{UB}}$ and/or $\overline{\text{LB}} = V_{IL}$, CRE = $V_{IL,}$ $\overline{\text{ADV}} = V_{IL}$)
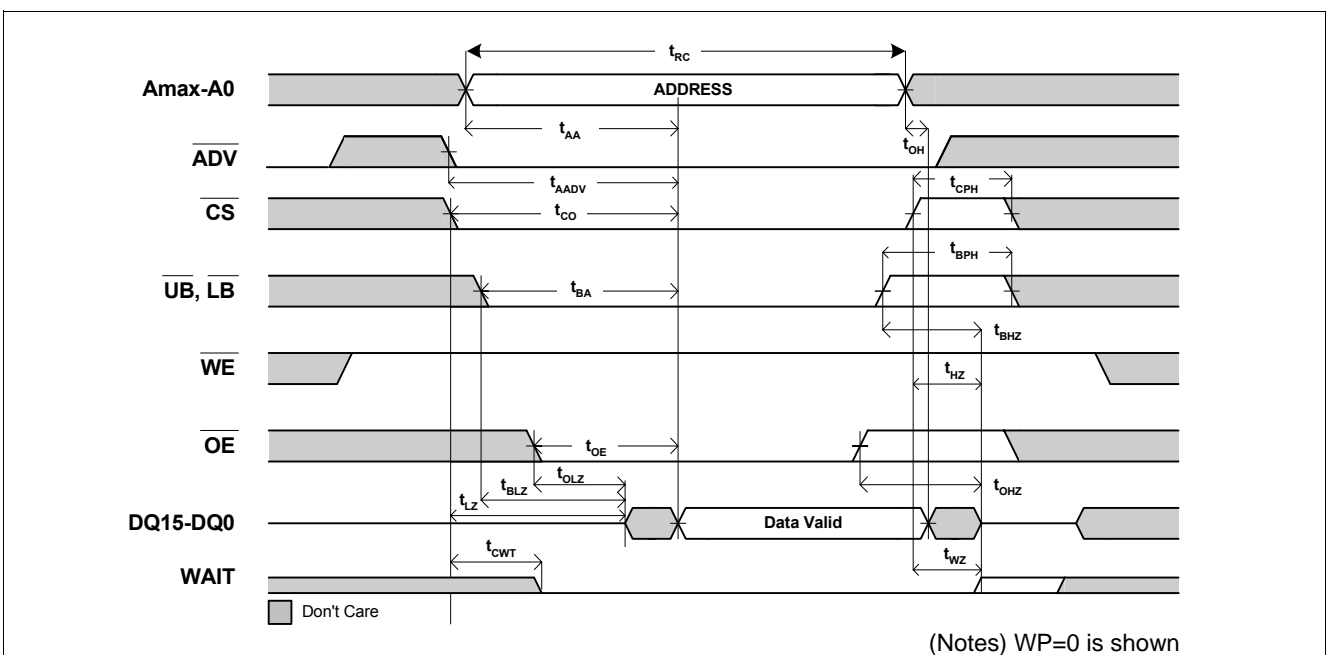
Figure 20   Asynchronous Read ($\overline{\text{WE}} = V_{IH}$, CRE = V_{IL})
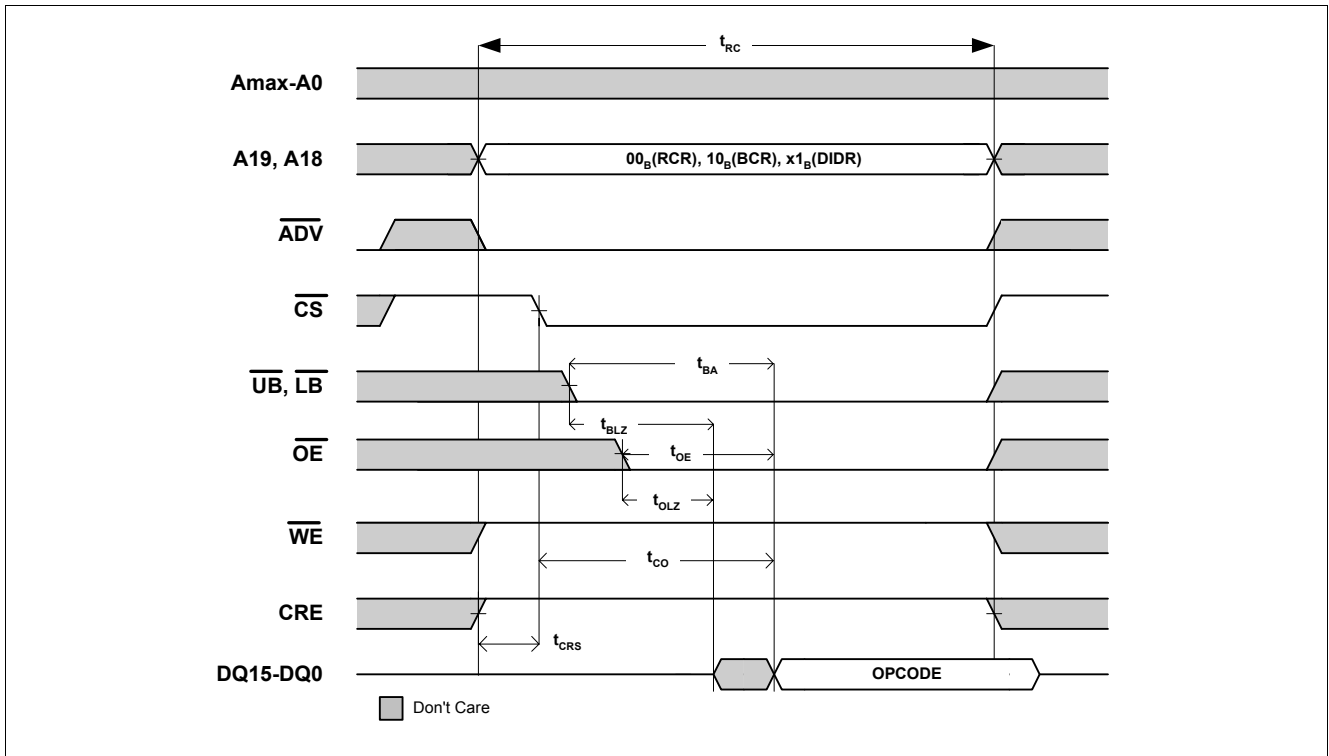
Figure 21   Asynchronous Control Register Read

2.8.2 Page Mode

If activated by RCR.Bit7 page mode allows to toggle the four lower address bits (A3 to A0) to perform subsequent random read accesses (max. 16-words by A3 - A0) at much faster speed than 1st read access. Page mode operation supports only read access in CellularRAM. As soon as page mode is activated, $\overline{CS}$ low time restriction (t_{CSL}) applies. It is recommended to bring $\overline{CS}$ high and back low to access different page. Therefore the usage of page mode is only recommended in systems which can respect this limitation. $\overline{ADV}$ has to be held low for entire page operation.

WAIT is always asserted as BCR. Bit 10 is programmed as to $\overline{CS}$ low time, so that the controller should ignore WAIT during asynchronous mode operation. (not shown in the timing diagrams)
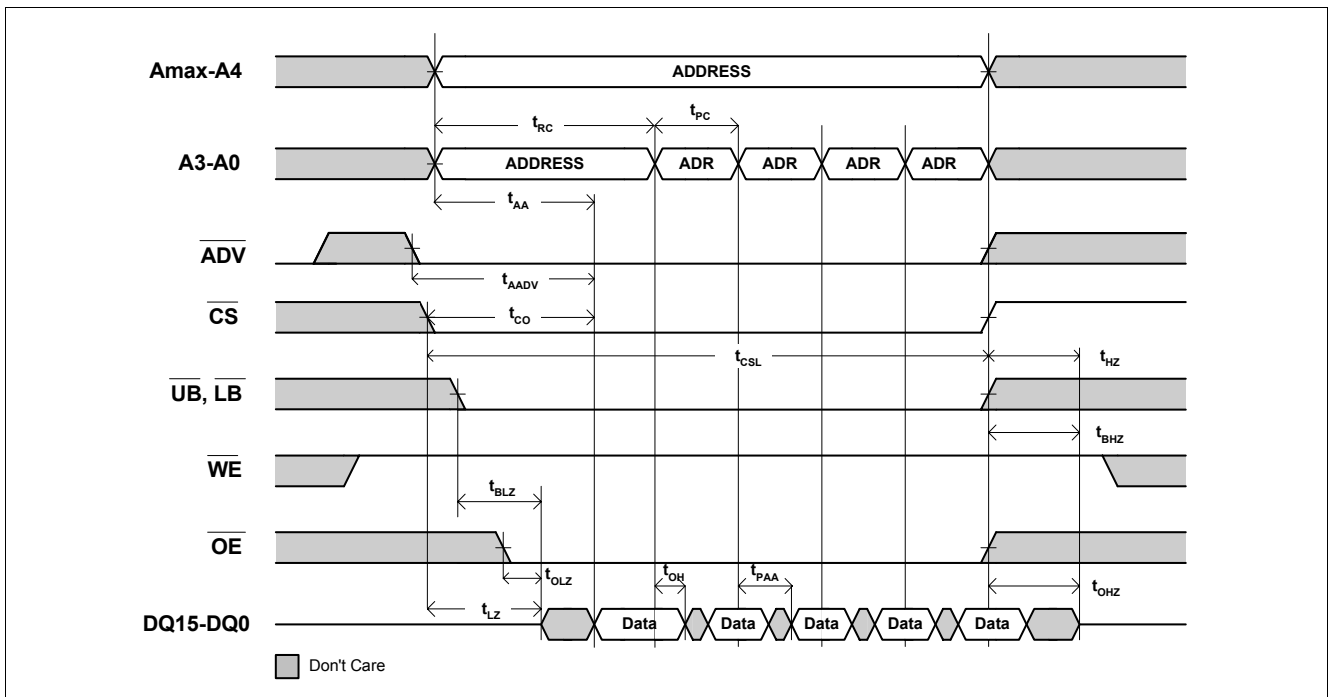
Figure 22   Asynchronous Page Read Mode (CRE = V_{IL}, $\overline{ADV} = V_{IL}$)

Table 13   Timing Parameters - Asynchronous Read

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	70	–	85	–	ns	–
Address access time	t_{AA}	–	70	–	85	ns	–
$\overline{ADV}$ access time	t_{AADV}	–	70	–	85	ns	–
Page address cycle time	t_{PC}	20	–	25	–	ns	–
Page address access time	t_{PAA}	–	20	–	25	ns	–
Output hold from address change	t_{OH}	5	–	6	–	ns	–
Chip select access time	t_{CO}	–	70	–	85	ns	–
$\overline{UB}$, $\overline{LB}$ access time	t_{BA}	–	70	–	85	ns	–
$\overline{OE}$ to valid output data	t_{OE}	–	20	–	25	ns	–
Chip select pulse width low time	t_{CSL}	–	4	–	4	µs	–
Chip select to output active	t_{LZ}	6	–	6	–	ns	–
Chip select disable to high-Z output	t_{HZ}	–	8	–	8	ns	–
$\overline{UB}$, $\overline{LB}$ enable to output active	t_{BLZ}	6	–	6	–	ns	–
$\overline{UB}$, $\overline{LB}$ disable to high-Z output	t_{BHZ}	–	8	–	8	ns	–
Output enable to output active	t_{OLZ}	3	–	3	–	ns	–
Output disable to high-Z output	t_{OHZ}	–	8	–	8	ns	–
$\overline{CS}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–
CRE setup time to Chip Select low	t_{CRS}	0	–	0	–	ns	–
$\overline{CS}$ low to WAIT valid	t_{CWT}	1	7.5	1	7.5	ns	–
$\overline{CS}$ high to WAIT high-Z	t_{WZ}	0	8	0	8	ns	–

Note: The AC parameter is measured with default drive strength, 1/2.

2.8.3 Asynchronous Write

[Disclaimer]

Amax for 64Mbit CellularRAM is A21. A22 is for 128Mbit density. WAIT signal is shown in the selected timing diagrams for the case of WP=0 (active low) though it is not default state.

Writing to the device in asynchronous SRAM mode is accomplished by asserting the Chip Select ($\overline{CS}$) and Write Enable ($\overline{WE}$) signals to low. $\overline{ADV}$ can be used to latch the address (refer to **"Asynchronous Write with Address Latch (ADV) Control" on Page 47** for detailed timing diagram and parameters as to toggling $\overline{ADV}$) or simply held low for entire write operation. If the Upper Byte ($\overline{UB}$) control line is set active low then the upper word (DQ15 to DQ8) of the data bus is written to the specified memory location. If the Lower Byte ($\overline{LB}$) control line is set active low then the lower word (DQ7 to DQ0) of the data bus is written to the specified memory location. Write operation takes place when either one or both $\overline{UB}$ and $\overline{LB}$ is asserted low. The data is latched by the rising edge of either $\overline{CS}$, $\overline{WE}$, or $\overline{UB}/\overline{LB}$ whichever signal comes first.

WAIT is always asserted as BCR. Bit 10 is programmed as to $\overline{CS}$ low time, so that the controller should ignore WAIT during asynchronous mode operation. (not shown in all timing diagrams)
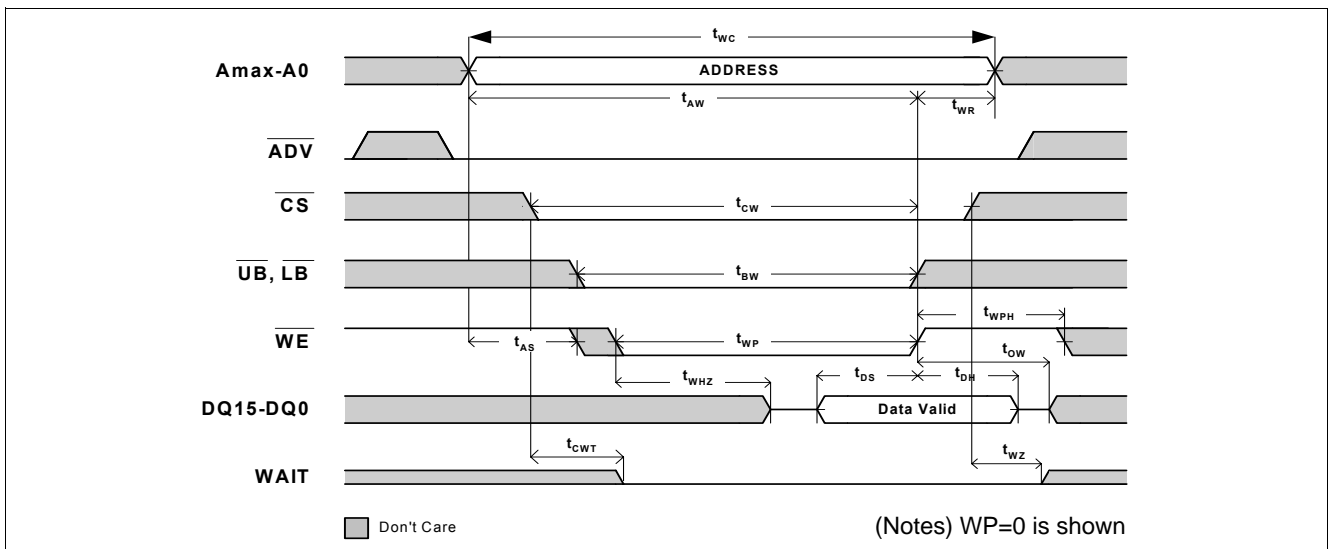
Figure 23   Asynchronous Write - $\overline{WE}$ Controlled ($\overline{OE} = V_{IH}$ or V_{IL}, CRE $= V_{IL}$)
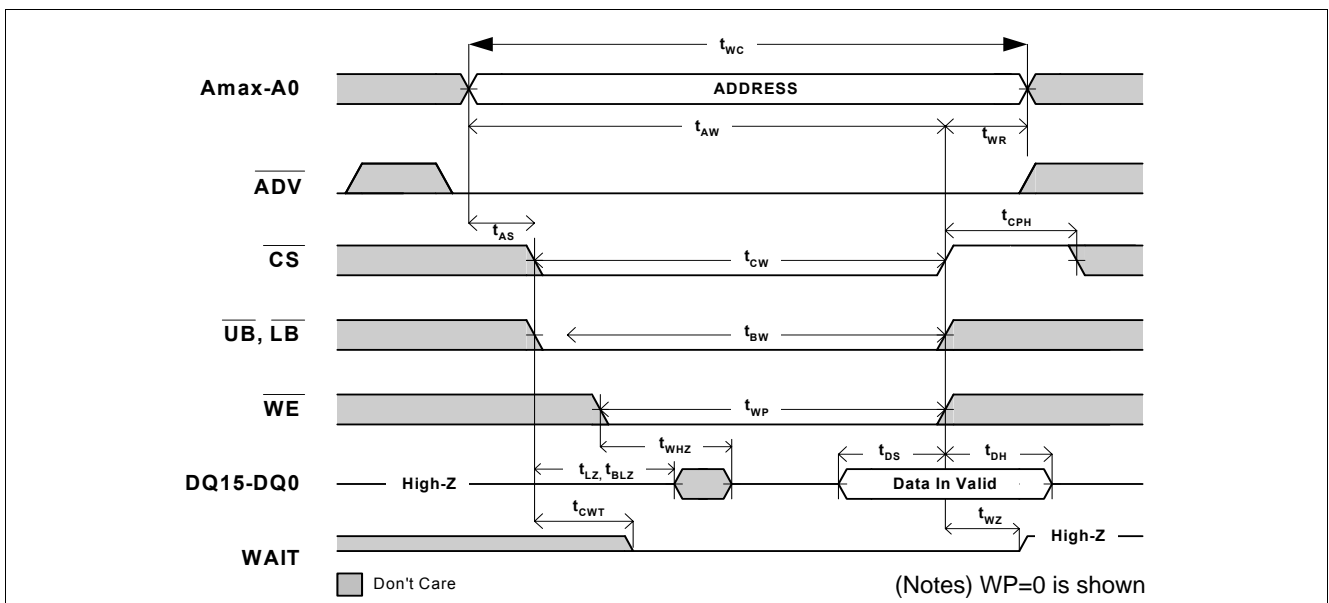
Figure 24   Asynchronous Write - $\overline{CS}$ Controlled ($\overline{OE} = V_{IH}$ or V_{IL}, CRE $= V_{IL}$)
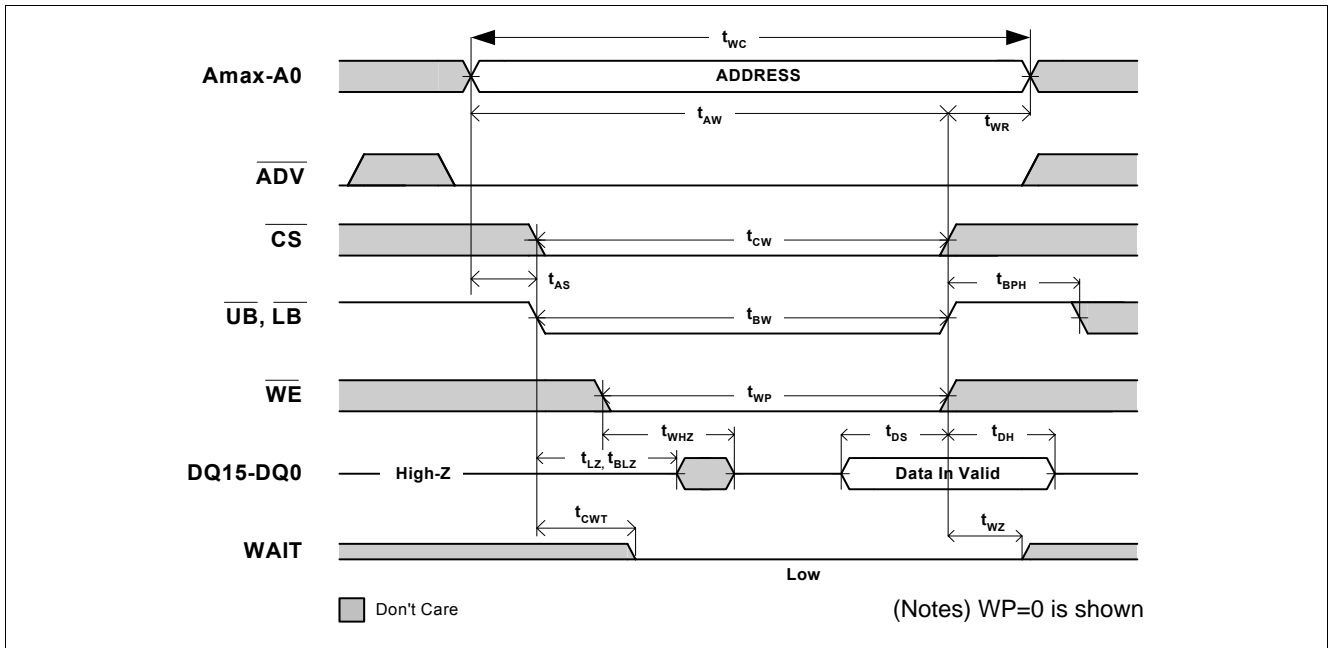
Figure 25   Asynchronous Write - $\overline{UB}$, $\overline{LB}$ Controlled ($\overline{OE}$ = V_{IH} or V_{IL}, CRE = V_{IL})

The programming of control register in SRAM-type mode is performed in the similar manner as asynchronous write except CRE being held high during the operation. Note that CRE has to meet set-up (t_{CRES}) and hold time (t_{CREH}) of valid state (= High) in reference to $\overline{WE}$ falling and rising edge, respectively. $\overline{ADV}$ may be kept low for entire operation. $\overline{CS}$ should toggle at the end of the operation to get ready for following access.
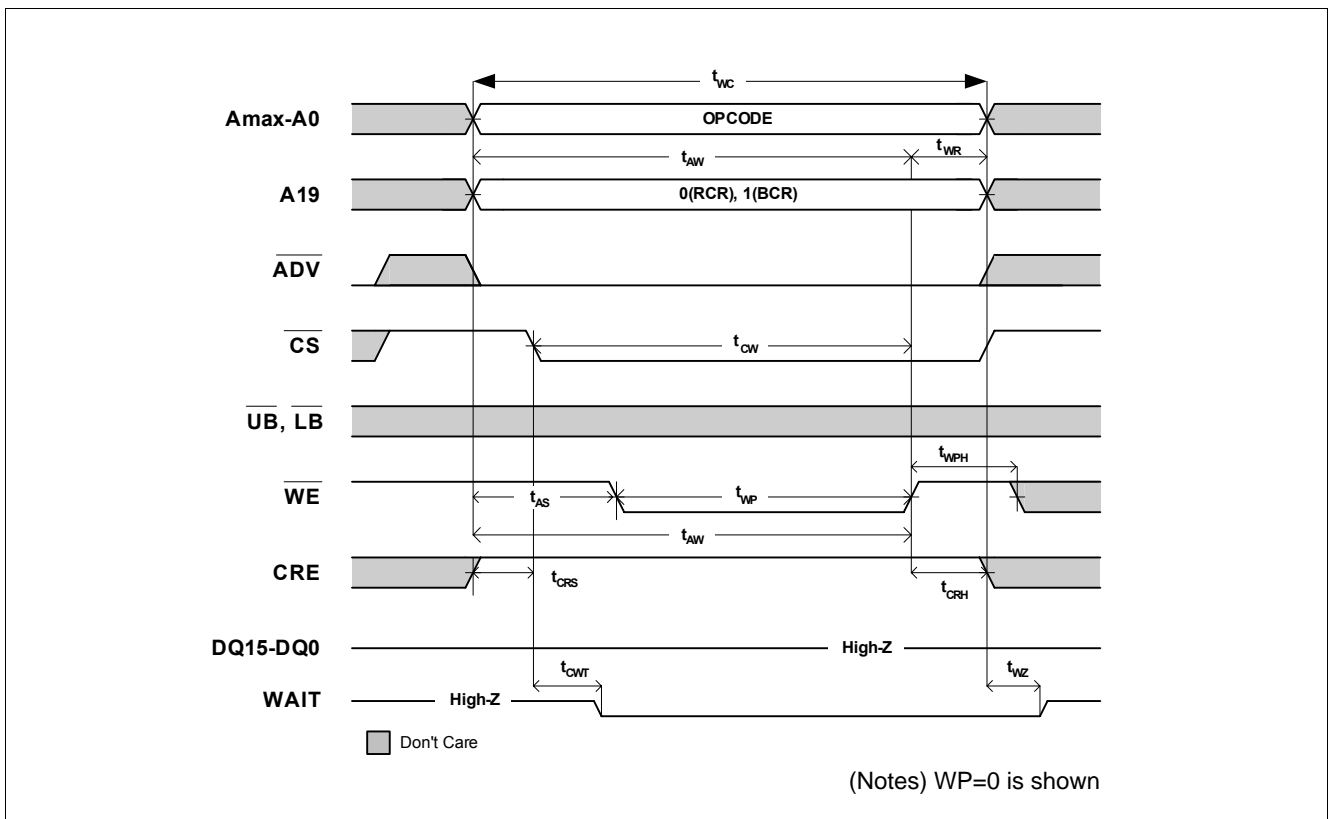
Figure 26   Asynchronous Write to Control Register ($\overline{OE}$ = V_{IH} or V_{IL})

Table 14   Timing Parameters - Asynchronous Write

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	70	–	85	–	ns	–
Address (incl. CRE) set-up time	t_{AS}	0	–	0	–	ns	–
Address valid to end of write	t_{AW}	70	–	85	–	ns	–
Write recovery time	t_{WR}	0	–	0	–	ns	–
Chip select pulse width low time	t_{CSL}	–	4	–	4	µs	–
Chip select to end of write	t_{CW}	70	–	85	–	ns	–
ADV setup to end of write	t_{VS}	70	–	85	–	ns	–
Byte control valid to end of write	t_{BW}	70	–	85	–	ns	–
Write pulse width	t_{WP}	45	–	55	–	ns	–
Write pulse pause	t_{WPH}	10	–	15	–	ns	–
$\overline{CS}$ high time when toggling	t_{CPH}	10	–	15	–	ns	–
$\overline{UB}$, $\overline{LB}$ high time when toggling	t_{BPH}	10	–	15	–	ns	–
Write to output disable	t_{WHZ}	–	8	–	10	ns	–
End of write to output enable ($\overline{OE}$ = low)	t_{OW}	5	–	5	–	ns	–
Write data setup time	t_{DS}	20	–	25	–	ns	–
Write data hold time	t_{DH}	0	–	0	–	ns	–
CRE setup time to Chip Select low	t_{CRS}	0	–	0	–	ns	–
CRE hold time from $\overline{WE}$ high	t_{CRH}	0	–	0	–	ns	–
$\overline{CS}$ low to WAIT valid	t_{CWT}	1	7.5	1	7.5	ns	–
$\overline{CS}$ high to WAIT high-Z	t_{WZ}	0	8	0	8	ns	–

Note: The AC parameter is measured with default drive strength, 1/2.

2.9 NOR-Flash-Type Mode

[Disclaimer]

Amax for 64Mbit CellularRAM is A21. A22 is for 128Mbit density.

In NOR-Flash mode the CellularRAM applies the NOR-Flash protocol to perform read and write accesses to the memory. Read accesses can be executed in synchronous burst mode, while write accesses are executed in asynchronous mode using $\overline{\text{ADV}}$ as address latch strobe signal.

2.9.1 Synchronous Read Mode

[Disclaimer]

WAIT signal of all synchronous timings below is shown in the case of WC=0 (at delay) and WP=0 (active low) though it is not default state.

Detailed description about burst operation including latency mode/code, BL, Wrap, WAIT function, etc. is available in **"Bus Control Register" on Page 25**. Proper setting of BCR has to be preceded to any burst operation.

In synchronous read mode all operations are referred to the rising clock signal edge. Refresh cycles or row boundary crossings are indicated by the WAIT output signal which stalls the processor for this period. Row boundary crossing is not permitted in case of BCR.bit14 = 1 (fixed latency mode).
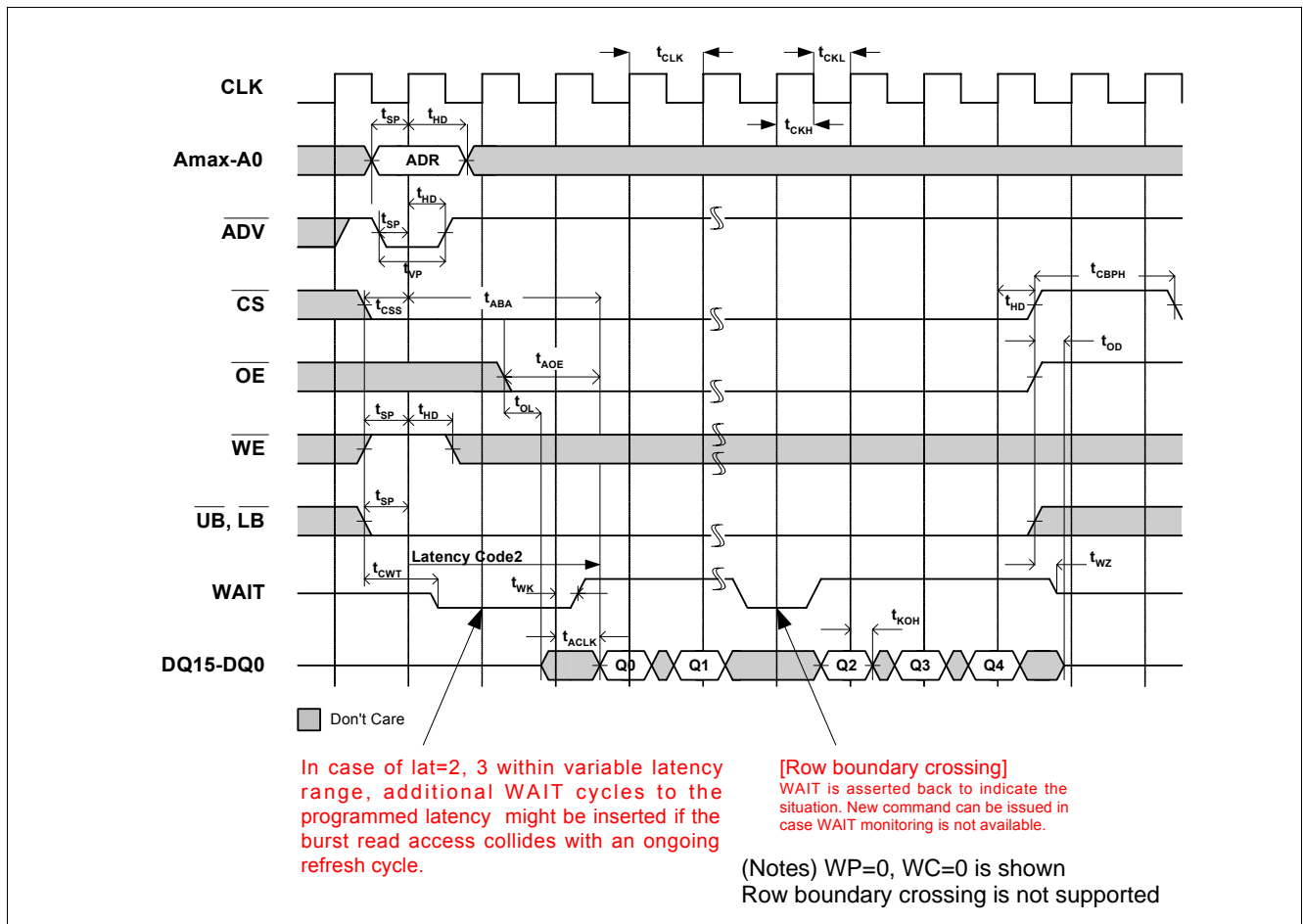
Figure 27   Synchronous Read Burst (CRE = V_{IL})

2.9.2 Burst Suspend

While in synchronous burst operation, the bus interface may need to be assigned to other memory transaction sharing the same bus. Burst suspend mode is used to fulfill this operation. Keeping $\overline{CS}$ low (WAIT stays asserted indicating valid data output on DQ pins, though they are tri-stated), burst suspend can be initiated with halted CLK. CLK can stay at either high or low state.

As specified, duration of keeping $\overline{CS}$ low can not exceed t_{CSL} maximum, which is 4 µs, so that internal refresh operation is able to run properly. In this event of exceeding t_{CSL} maximum, termination of burst by bringing $\overline{CS}$ to high is strongly recommended instead of using burst suspend mode, then reissuing of the discontinued burst command is required.
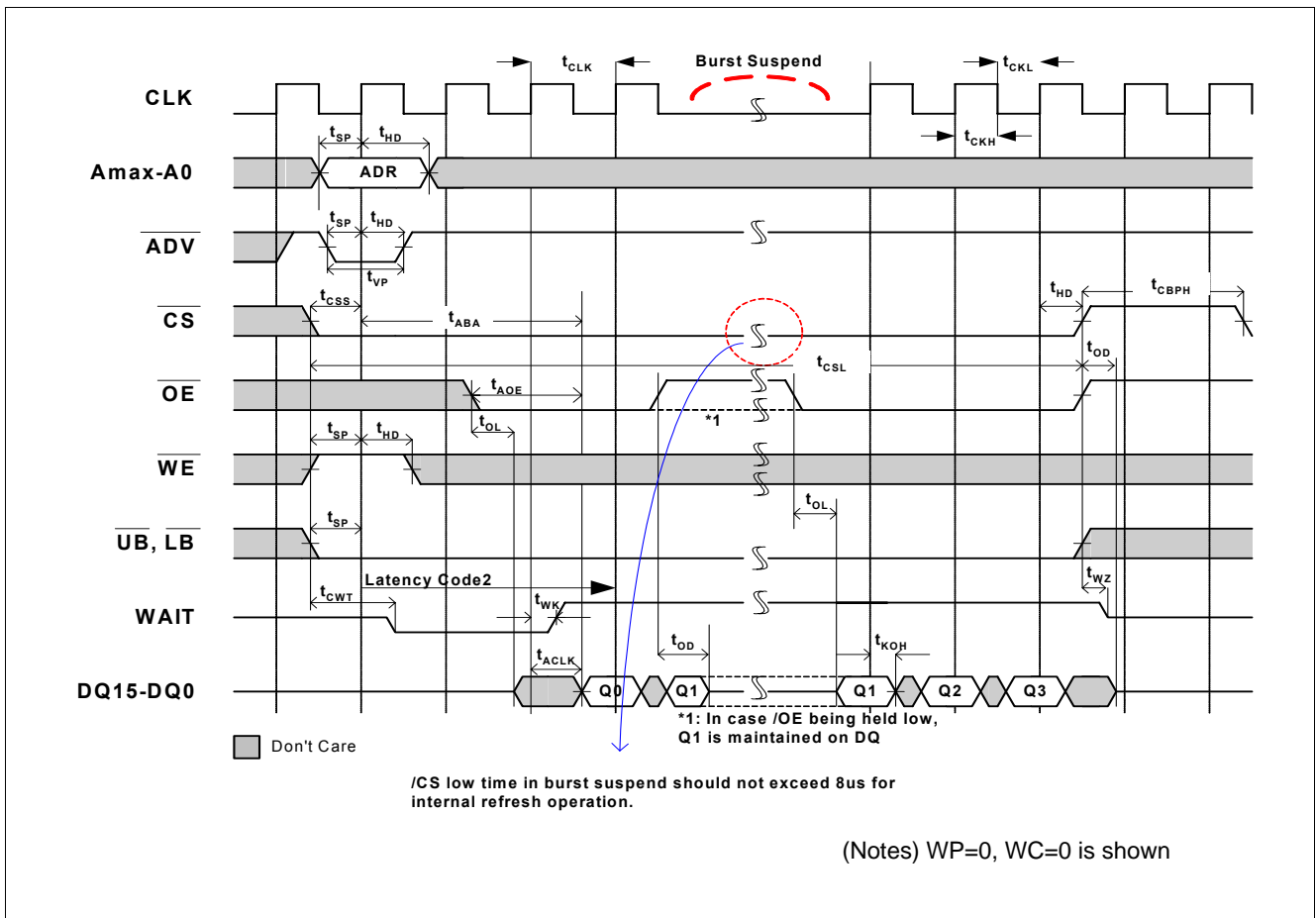
Figure 28   Burst Suspend (CRE = V_{IL})

2.9.3 Synchronous Control Register Read

The content of RCR, BCR, or RIDR is readable via DQ pins by CRE-controlled FCR command. A19 and A18 selects the register to be accessed. It is identical to single-bit read access in burst operation, but the latency is always the same as being programmed in BCR, though it is in variable latency mode. Refresh is not performed during burst_init phase of this command, so that $\overline{CS}$ should not exceed $t_{CSL,max}$ limit.
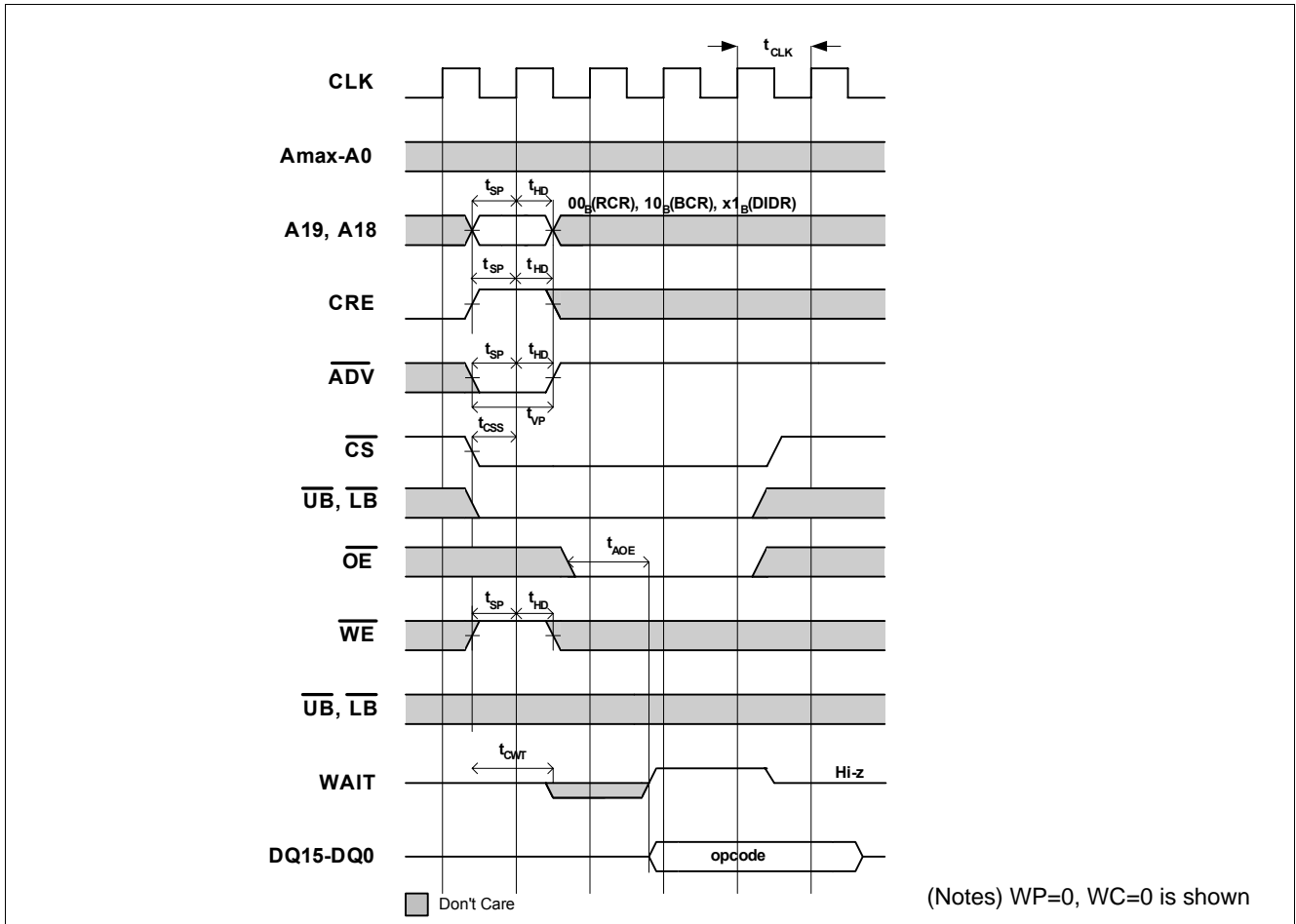
Figure 29   Synchronous Control Register Read

In the timing diagram, the timing between CRE and $\overline{WE}$ has to be carefully controlled since the overlap of CRE high and $\overline{WE}$ low may accidentally program the control register. Asynchronous command of operation is still valid when the synchronous command is prepared. Please avoid the time when both CRE high and $\overline{WE}$ low is met.

In the same manner, the time when both $\overline{CS}$ and $\overline{WE}$ low has to be avoided at the set up of synchronous read command for normal burst or control register access to avoid accidental asynchronous write operation.

Table 15   Timing Parameters - Synchronous Read Burst

Parameter		Symbol	9.6		12.5		15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock period frequency (Variable latency)	Lat = 3	f_{CLK3V}	–	104	–	80	–	66	MHz	–
	Lat = 2	f_{CLK2V}	–	66	–	66	–	40	MHz	–
Clock period (Variable latency)	Lat = 3	t_{CLK3V}	9.6	–	12.5	–	15	–	ns	–
	Lat = 2	t_{CLK2V}	15	–	15	–	25	–	ns	–
Clock period frequency (Fixed latency)	Lat = 6	f_{CLK6F}	–	104	–	80	–	66	MHz	–
	Lat = 5	f_{CLK5F}	–	75	–	75	–	52	MHz	–
	Lat = 4	f_{CLK4F}	–	66	–	66	–	40	MHz	–
	Lat = 3	f_{CLK3F}	–	52	–	52	–	33	MHz	–
	Lat = 2	f_{CLK2F}	–	33	–	33	–	20	MHz	–
Clock period (Fixed latency)	Lat = 6	t_{CLK6F}	9.6	–	12.5	–	15	–	ns	–
	Lat = 5	t_{CLK5F}	13.3	–	13.3	–	19.2	–	ns	–
	Lat = 4	t_{CLK4F}	15	–	15	–	25	–	ns	–
	Lat = 3	t_{CLK3F}	19.2	–	19.2	–	30	–	ns	–
	Lat = 2	t_{CLK2F}	30	–	30	–	50	–	ns	–
Clock high time		t_{CKH}	3	–	4	–	5	–	ns	–
Clock low time		t_{CKL}	3	–	4	–	5	–	ns	–
Clock rise/fall time		t_T	–	1.6	–	1.8	–	2	ns	–
Input setup time to CLK (except $\overline{CS}$)		t_{SP}	3	–	4	–	5	–	ns	–
Input hold time from CLK		t_{HD}	2	–	2	–	2	–	ns	–
$\overline{ADV}$ pulse width low		t_{VP}	5	–	6	–	7	–	ns	–
Burst read 1st access delay from CLK		t_{ABA}	–	36	–	39	–	56	ns	[1]
$\overline{CS}$ low setup to CLK		t_{CSS}	3	–	4	–	5	–	ns	
Chip select pulse width low time		t_{CSL}	–	4	–	4	–	4	µs	–
$\overline{CS}$ pulse width high		t_{CBPH}	5	–	6	–	8	–	ns	–
$\overline{OE}$ or $\overline{LB}/\overline{UB}$ low to output low-Z		t_{OL}	3	–	3	–	3	–	ns	–
$\overline{CS}$, $\overline{OE}$, or $\overline{LB}/\overline{UB}$ high to output high-Z		t_{OD}	0	8	0	8	0	8	ns	–
$\overline{OE}$ low to output delay		t_{AOE}	–	20	–	20	–	25	ns	–
$\overline{CS}$ low to WAIT valid		t_{CWT}	1	7.5	1	7.5	1	7.5	ns	–
$\overline{CS}$ high to WAIT high-Z		t_{WZ}	0	8	0	8	0	8	ns	–
CLK to WAIT valid		t_{WK}	–	7	–	9	–	11	ns	–
CLK to output delay		t_{ACLK}	–	7	–	9	–	11	ns	–
Output hold from CLK		t_{KOH}	2	–	2	–	2	–	ns	–

1)   This is based on the use of variable latency. In case of refresh collision to the first access, more WAIT cycles will be added.
Note: The AC parameter is measured with default drive strength, 1/2.

2.9.4 Asynchronous Write with Address Latch ($\overline{ADV}$) Control

In asynchronous write mode, the synchronous clock is switched off and CLK has to be held low. The access protocol is shown with $\overline{ADV}$-latching scheme and it can be applied to write operation in SRAM-type mode.

WAIT is always asserted as BCR. Bit 10 is programmed as to $\overline{CS}$ low time, so that the controller should ignore WAIT during asynchronous mode operation.
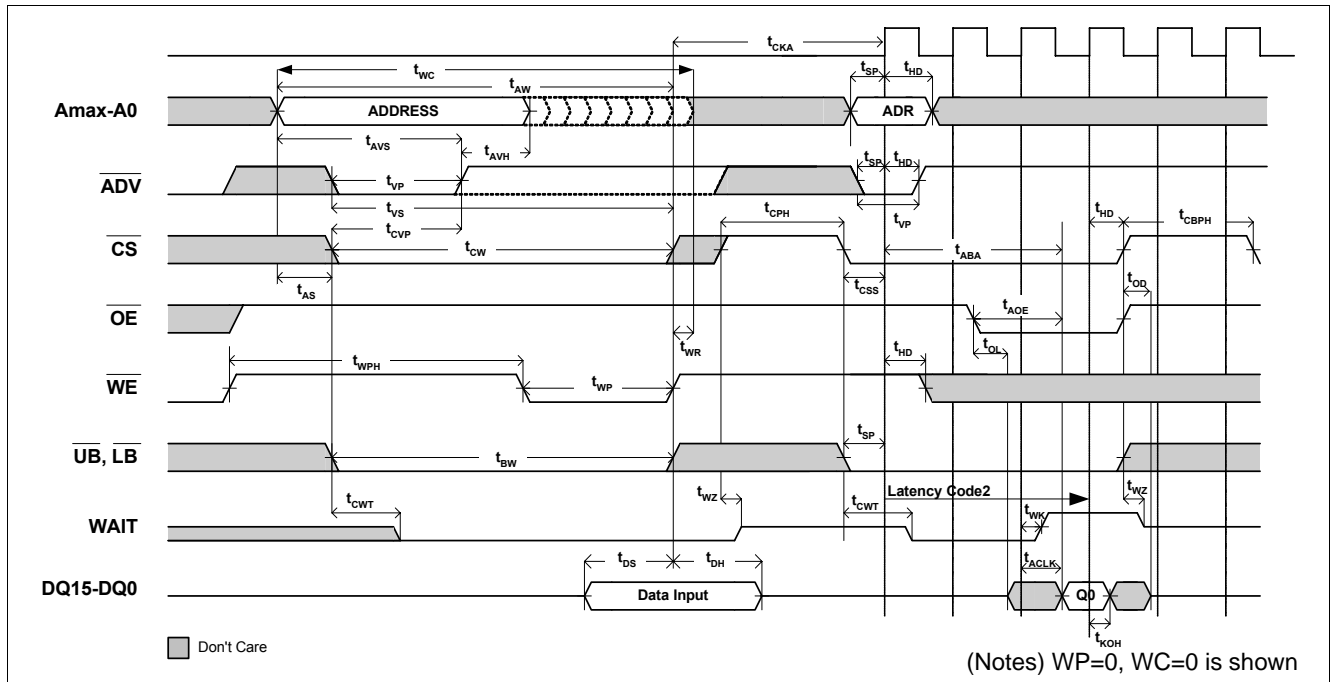
Figure 30   Asynchronous Write with Address Latch ($\overline{ADV}$) Control (followed by single-burst read)
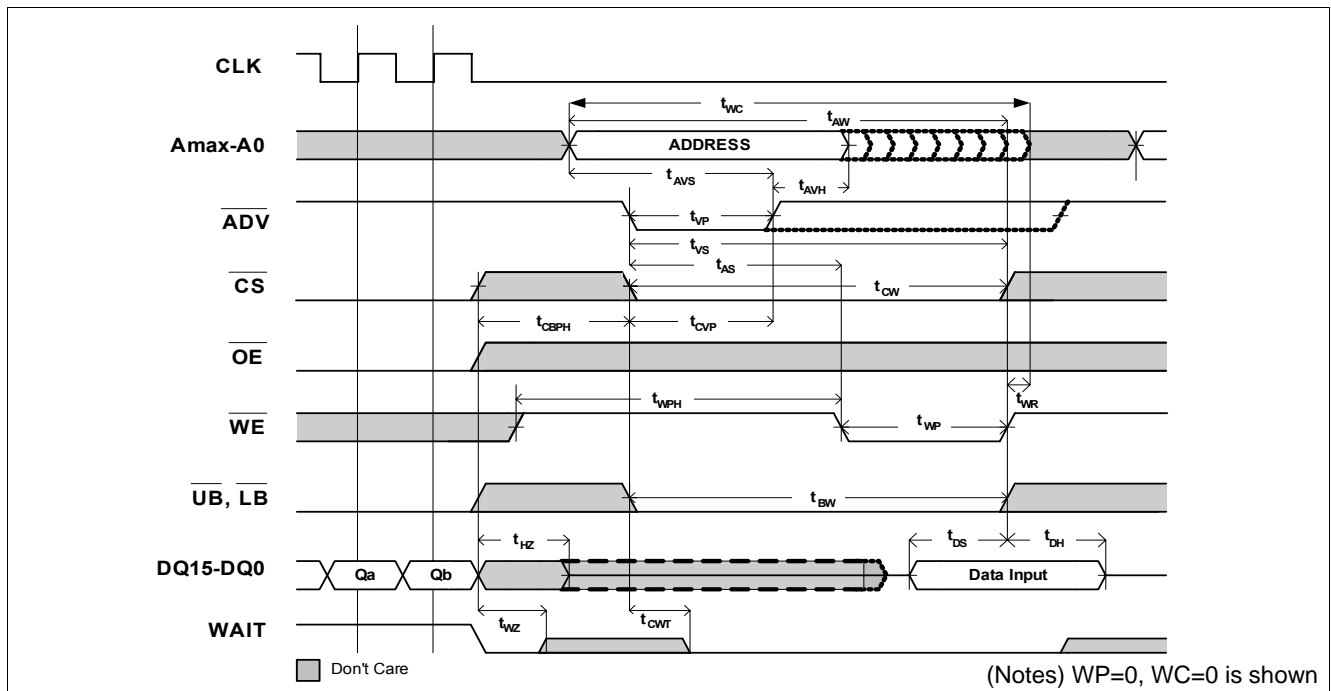
Figure 31   Asynchronous Write with Address Latch ($\overline{ADV}$) Control

Asynchronous write operation may be executed in a conjuction with a read burst operation. Bringing $\overline{CS}$ high is recommended to stop a read burst if it is on-going.

However it is allowed to let asynchronous write operation follow a read burst while $\overline{CS}$ is held low and CLK is stopped at low. By $\overline{ADV}$ being pulled low with valid write timing as in **Figure 31**, asynchronous write operation can be done. Please note that the on-going burst is terminated before write operation is initiated when $\overline{ADV}$ goes low.

The programming of control register in NOR-Flash-type mode is performed in the similar manner as asynchronous write with $\overline{ADV}$ control except CRE being held high during the code input operation. Note that CRE has to meet set-up (t_{CRS}) and hold time (t_{CRH}) of valid state (= High) in reference to $\overline{ADV}$ rising edge. $\overline{ADV}$ may be kept low for entire operation or go high to latch valid control register information at its rising edge.
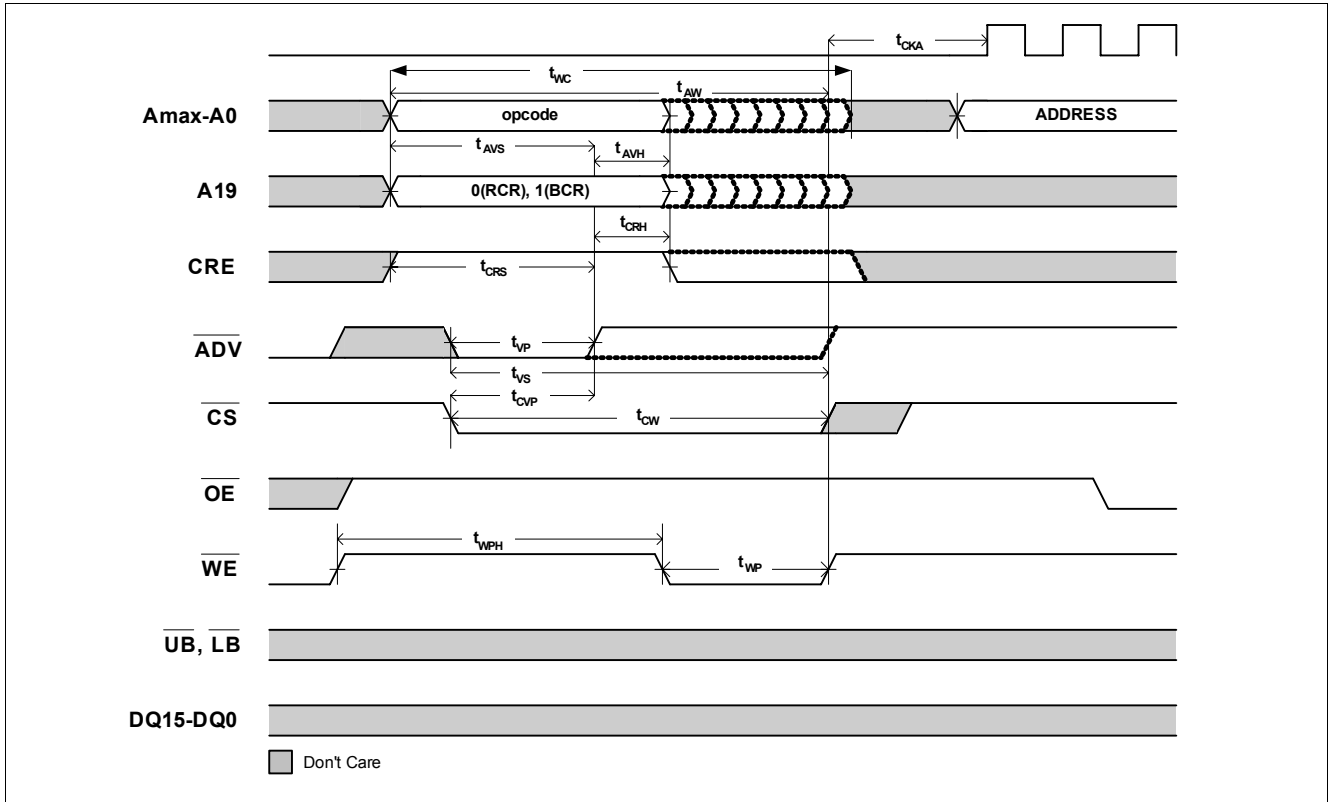
Figure 32   Asynchronous Write To Control Register in NOR-Flash Mode

Table 16   Timing Parameters - Asynchronous Write With $\overline{ADV}$ Control

Parameter	Symbol	9.6, 12.5		15		Unit	Notes
		Min.	Max.	Min.	Max.		
$\overline{WE}$ high to CLK valid	t_{CKA}	25	–	35	–	ns	–
Write cycle time	t_{WC}	70	–	85	–	ns	–
Address setup time to write start	t_{AS}	0	–	0	–	ns	–
Address setup to $\overline{ADV}$ high	t_{AVS}	5	–	5	–	ns	–
Address hold from $\overline{ADV}$ high	t_{AVH}	2	–	2	–	ns	–
Address to end of write	t_{AW}	70	–	85	–	ns	–
$\overline{ADV}$ pulse width low	t_{VP}	5	–	7	–	ns	–
$\overline{ADV}$ low hold time for $\overline{CS}$ low	t_{CVP}	7	–	7	–	ns	–
$\overline{ADV}$ setup to end of write	t_{VS}	70	–	85	–	ns	–
$\overline{CS}$ to end of write	t_{CW}	70	–	85	–	ns	–
$\overline{UB}/\overline{LB}$ to end of write	t_{BW}	70	–	85	–	ns	–
Write pulse width low	t_{WP}	45	–	55	–	ns	–
Write pulse width high	t_{WPH}	10	–	15	–	ns	–
$\overline{CS}$ high time (synch_read)	t_{CBPH}	5	–	8	–	ns	–
$\overline{CS}$ high time (asynch_write, mixed)	t_{CPH}	10	–	15	–	ns	–
Write recovery time	t_{WR}	0	–	0	–	ns	1
Data setup to $\overline{WE}$ high	t_{DS}	20	–	25	–	ns	–
Data hold from $\overline{WE}$ high	t_{DH}	0	–	0	–	ns	–
CRE setup to $\overline{ADV}$ high	t_{CRS}	5	–	5	–	ns	–
CRE hold from $\overline{ADV}$ high	t_{CRH}	2	–	2	–	ns	–
WAIT valid from $\overline{CS}$ low	t_{CWT}	1	7.5	1	7.5	ns	–
$\overline{CS}$ high to WAIT high-Z	t_{WZ}	0	8	0	8	ns	–
Chip select pulse width low time	t_{CSL}	–	4	–	4	µs	–

Note: 1. t_{WR} is valid only when $\overline{ADV}$ latch of address does not take place until the end of write.

Note: The AC parameter is measured with default drive strength, 1/2.

2.10 Synchronous Mode

[Disclaimer]

Amax for 64Mbit CellularRAM is A21. A22 is for 128Mbit density.

WAIT signal of all synchronous timings below is shown in the case of WC=0 (at delay) and WP=0 (active low) though it is not default state.

Detailed description about burst operation including latency mode/code, BL, Wrap, WAIT function, etc. is available in **"Bus Control Register" on Page 25**. Proper setting of BCR has to be preceded to any burst operation.

In synchronous mode, read and write operations are synchronized to the clock. Refresh cycles or row boundary crossings are indicated to the host system by asserting the WAIT signal which in turn stalls the processor. Row boundary crossing is not permitted in fixed latency mode setting (BCR.bit14 = 1). WAIT polarity, WAIT timing, synchronicity to the falling/rising clock edge, the burst length and further options are user configurable and can be programmed via the bus configuration register (BCR).

2.10.1 Synchronous Read Mode Including Burst Suspend

Refer to **Section 2.9.1** and **Section 2.9.2**. All the timing and parameters are same as described in read operation for NOR-Flash-Type mode.

2.10.2 Synchronous Write Mode

In synchronous write mode, $\overline{UB}$ and $\overline{LB}$ are used as byte control of data input mask. At the rising edge of CLK, their state is sampled and determined whether the coupled byte (DQ15-8 for $\overline{UB}$ and DQ7-0 for $\overline{LB}$) is updated by input data. Proper set-up time and hold time to CLK should be met. As discussed in **Section 2.4.1.3**, synchronous burst write always works with fixed latency concept, therefore, t_{CSL} maximum, which is 4 µs, has to be observed.
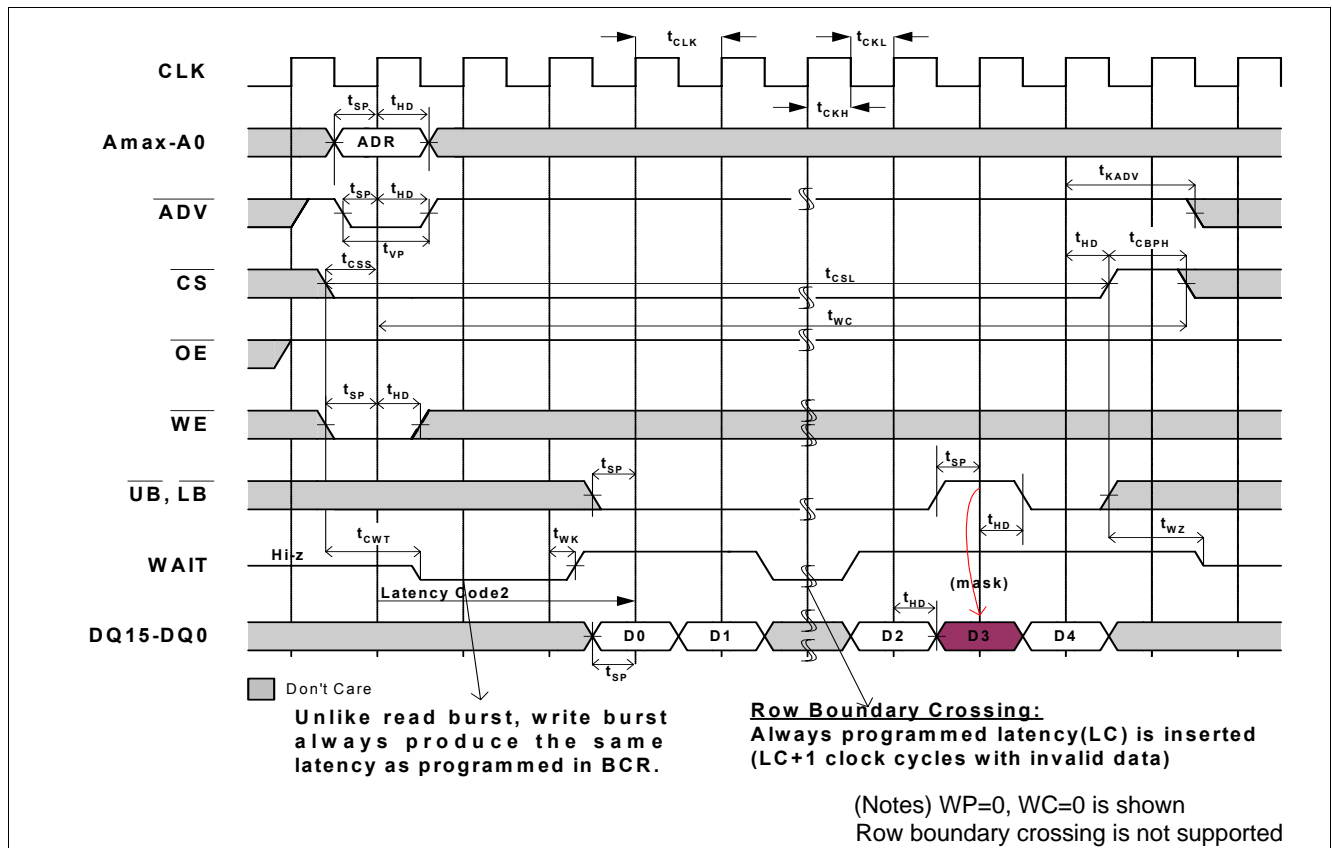
Figure 33   Synchronous Write Burst (CRE = V_{IL})

t_{KADV} has to be observed to ensure the completion of write operation and recovery. This parameter defines the time required from the last data-in to new burst start. t_{KADV} applies to only when the new burst_init command is either write burst in variable latency mode or read burst in fixed latency mode so that the refresh operation is properly performed in case. This parameter does not apply to the burst interrupt case when $\overline{CS}$ stays low.

Though maximum of t_{CSS} is not specified when a write burst command is asserted, it is strongly recommended not to exceed it 20ns. However, in case of longer, extended t_{CSS} timing being in use, the special care has to be taken to the address line update as to $\overline{WE}$ low-going time. **Figure 34** illustrates the case for details. Address set-up time, t_{AS} is still valid in this range since the command is identified as asynchronous command until the valid clock edge comes in to start burst operation. The update of address line after $\overline{WE}$ low-going is not permitted.
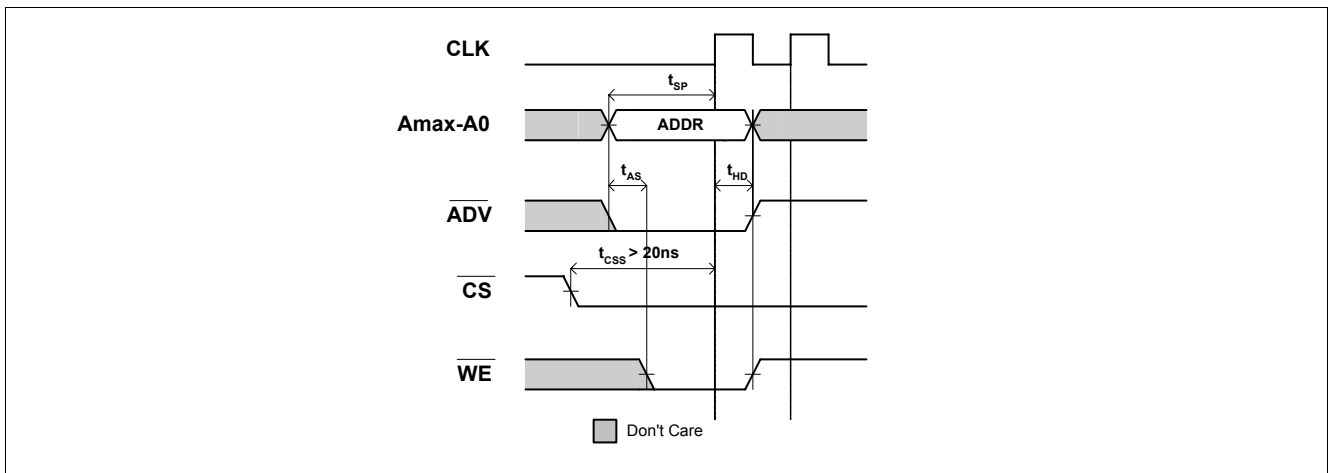
Figure 34   Synchronous Write command with extended t_{CSS}

Burst suspend mode is also available during a write burst. Please refer to **Section 2.9.2** for details.

Figure 35   Synchronous Write to Control Register

Figure 36   Synchronous Write Burst Followed by Synchronous Read Burst
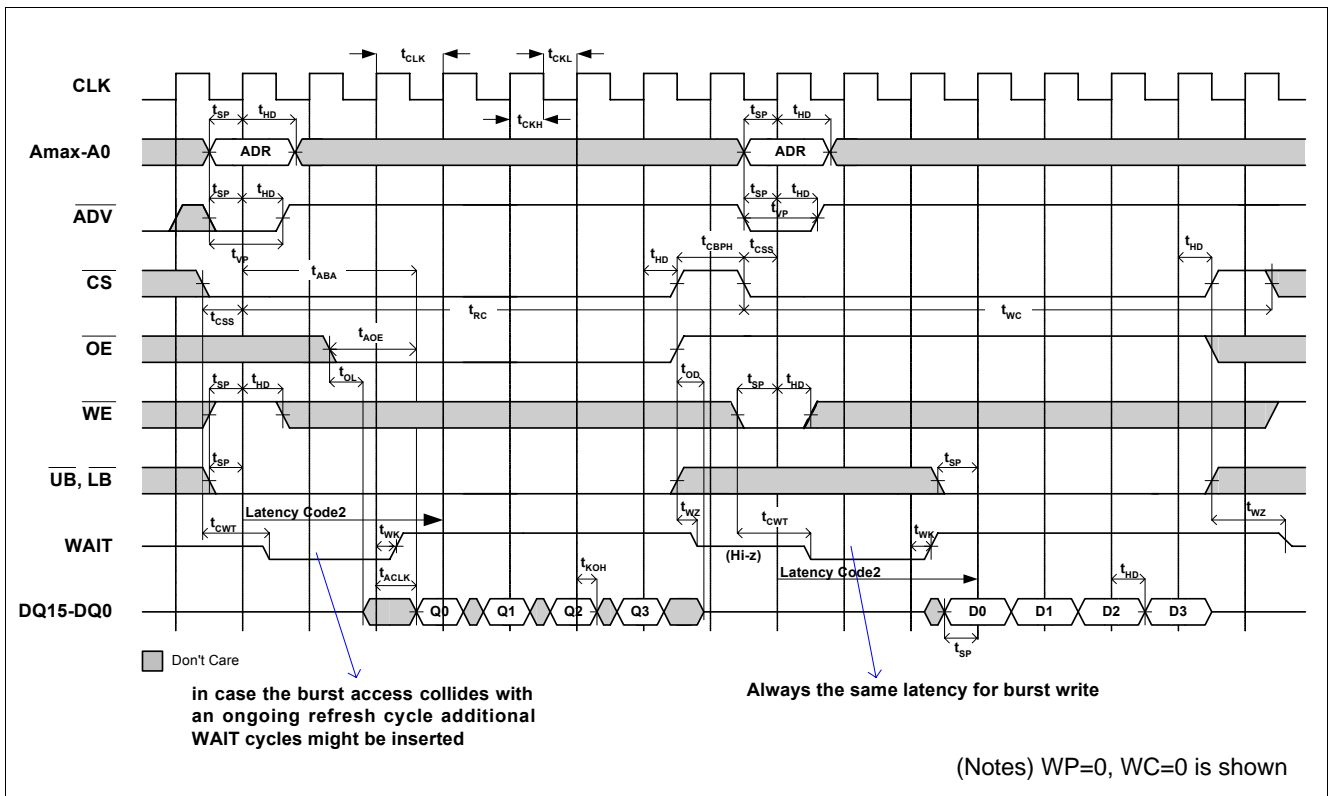
Figure 37   Synchronous Read Burst Followed by Synchronous Write Burst

Table 17   Timing Parameters - Synchronous Read/Write Burst

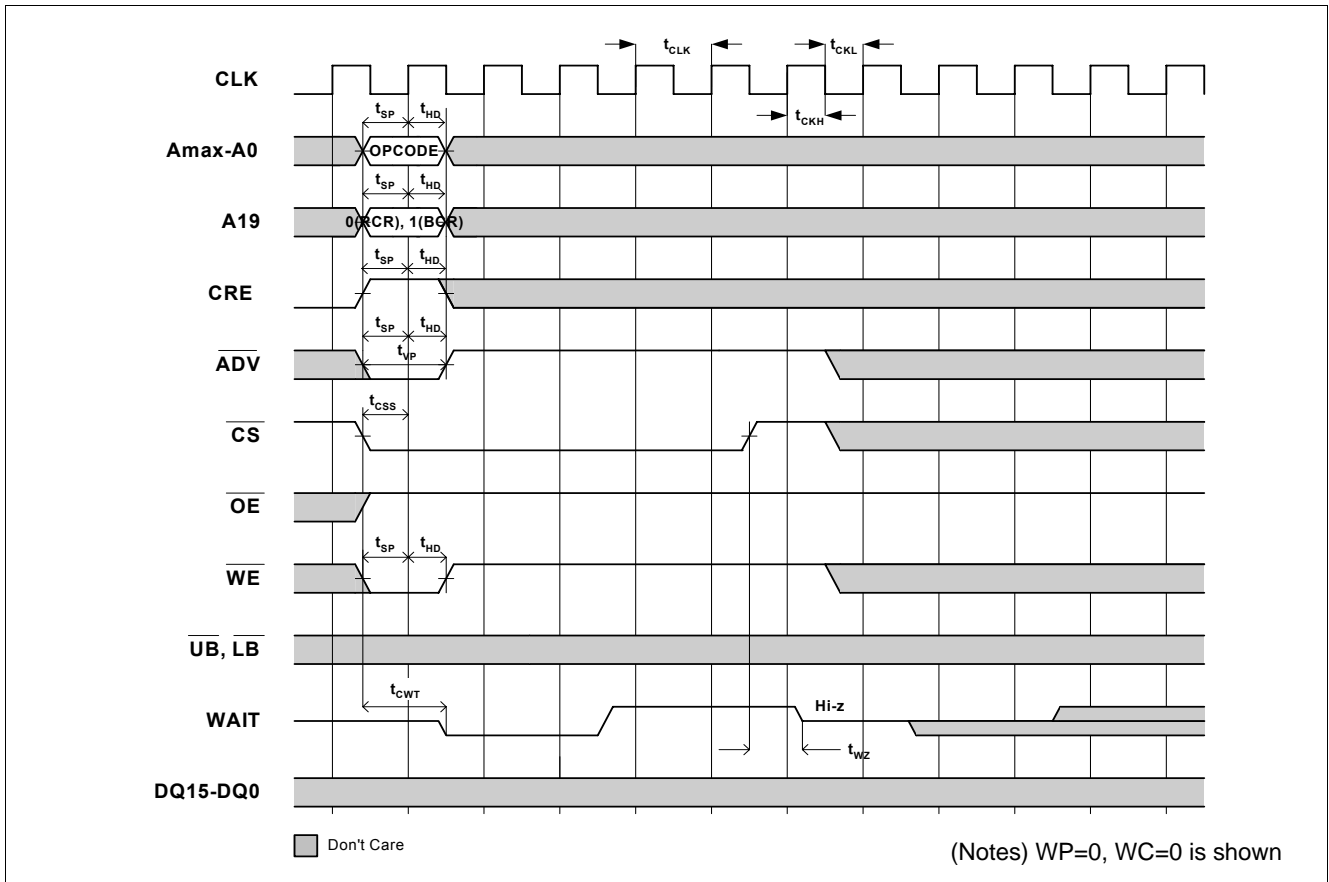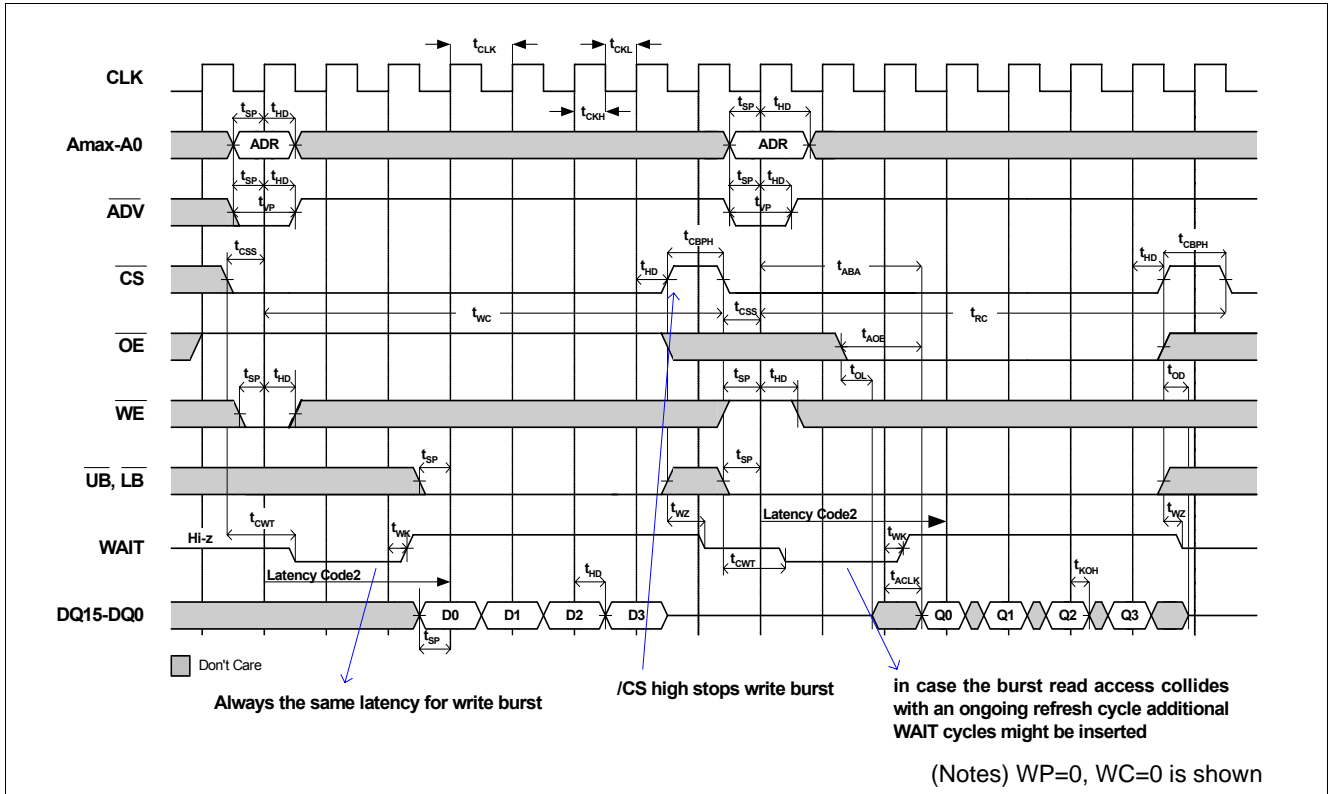| Parameter		Symbol	9.6		12.5		15		Unit	Notes
			Min.	Max.	Min.	Max.	Min.	Max.		
Clock period frequency (Variable latency)	Lat = 3	f_{CLK3V}	–	104	–	80	–	66	MHz	–
	Lat = 2	f_{CLK2V}	–	66	–	66	–	40	MHz	–
Clock period (Variable latency)	Lat = 3	t_{CLK3V}	9.6	–	12.5	–	15	–	ns	–
	Lat = 2	t_{CLK2V}	15	–	15	–	25	–	ns	–
Clock period frequency (Fixed latency)	Lat = 6	f_{CLK6F}	–	104	–	80	–	66	MHz	–
	Lat = 5	f_{CLK5F}	–	75	–	75	–	52	MHz	–
	Lat = 4	f_{CLK4F}	–	66	–	66	–	40	MHz	–
	Lat = 3	f_{CLK3F}	–	52	–	52	–	33	MHz	–
	Lat = 2	f_{CLK2F}	–	33	–	33	–	20	MHz	–
Clock period (Fixed latency)	Lat = 6	t_{CLK6F}	9.6	–	12.5	–	15	–	ns	–
	Lat = 5	t_{CLK5F}	13.3	–	13.3	–	19.2	–	ns	–
	Lat = 4	t_{CLK4F}	15	–	15	–	25	–	ns	–
	Lat = 3	t_{CLK3F}	19.2	–	19.2	–	30	–	ns	–
	Lat = 2	t_{CLK2F}	30	–	30	–	50	–	ns	–
Clock high time		t_{CKH}	3	–	4	–	5	–	ns	–
Clock low time		t_{CKL}	3	–	4	–	5	–	ns	–
Clock rise/fall time		t_T	–	1.6	–	1.8	–	2	ns	–
Input setup time to CLK (except $\overline{CS}$)		t_{SP}	3	–	4	–	5	–	ns	–
Input hold time from CLK		t_{HD}	2	–	2	–	2	–	ns	–
$\overline{ADV}$ pulse width low		t_{VP}	5	–	6	–	7	–	ns	–
Burst read 1st access delay from CLK		t_{ABA}	–	36	–	39	–	56	ns	[1]
$\overline{CS}$ low setup to CLK		t_{CSS}	3	–	4	–	5	–	ns	[2]
Chip select pulse width low time		t_{CSL}	–	4	–	4	–	4	µs	–
$\overline{CS}$ pulse width high		t_{CBPH}	5	–	6	–	8	–	ns	–
$\overline{OE}$ or $\overline{LB}/\overline{UB}$ low to output low-Z		t_{OL}	3	–	3	–	3	–	ns	–
$\overline{CS}$, $\overline{OE}$, or $\overline{LB}/\overline{UB}$ high to output high-Z		t_{OD}	0	8	0	8	0	8	ns	–
$\overline{OE}$ low to output delay		t_{AOE}	–	20	–	20	–	25	ns	–
$\overline{CS}$ low to WAIT valid		t_{CWT}	1	7.5	1	7.5	1	7.5	ns	–
$\overline{CS}$ high to WAIT high-Z		t_{WZ}	0	8	0	8	0	8	ns	–
CLK to WAIT valid		t_{WK}	–	7	–	9	–	11	ns	–
CLK to output delay		t_{ACLK}	–	7	–	9	–	11	ns	–
Output hold from CLK		t_{KOH}	2	–	2	–	2	–	ns	–
Last Data-in to new $\overline{ADV}$ low		t_{KADV}	15	–	15	–	15	–	ns	[3]

1) This is based on the use of variable latency. In case of refresh collision to the first access, more WAIT cycles will be added.
2) Maximum value is recommended not to exceed 20ns. In case of longer than 20ns, no address change is permitted after $\overline{WE}$ goes low to set up a write burst command.
3) This applies to only when the next burst_init command is either write burst in variable latency mode or read burst in fixed latency mode. Burst write interrupted by any burst (while $\overline{CS}$ is low) does not ask for t_{KADV}.

Note: The AC parameter is measured with default drive strength, 1/2.

2.11   General AC Input/Output Reference Waveform

The input timings refer to a midlevel of $V_{DDQ}/2$ while as output timings refer to midlevel $V_{DDQ}/2$. The rising and falling edges are 10 - 90% and < 2 ns.

3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 18   Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		Min.	**Max.**		
Operating temperature range	T_C	-30	+85	°C	–
Storage temperature range	T_{STG}	-55	+150	°C	–
Soldering peak temperature (10 s)	T_{Sold}	–	260	°C	–
Voltage of V_{DD} supply relative to V_{SS}	V_{DD}	-0.3	+2.5	V	–
Voltage of V_{DDQ} supply relative to V_{SS}	V_{DDQ}	-0.3	+2.5	V	–
Voltage of any input relative to V_{SS}	V_{IN}	-0.3	+2.8	V	–
Power dissipation	P_D	–	180	mW	–
Short circuit output current	I_{OUT}	-50	+50	mA	–

Attention: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.

3.2 Recommended Power & DC Operation Ratings

All values are recommended operating conditions unless otherwise noted.

Table 19   Recommended DC Operating Conditions

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	**Typ.**	**Max.**		
Power supply voltage, core	V_{DD}	1.70	1.8	1.95	V	–
Power supply voltage, 1.8 V I/Os	V_{DDQ}	1.70	1.8	1.95	V	–
Input high voltage	V_{IH}	$V_{DDQ} - 0.4$	–	$V_{DDQ} + 0.2$	V	1)
Input low voltage	V_{IL}	-0.2	–	0.4	V	2)

1)   Input signals may overshoot no higher than V_{DDQ}+1.0V. The area above V_{DDQ} should not exceed 2V-ns.

2)   Input signals may undershoot no lower than -1.0V. The area below V_{SSQ} should not exceed 2V-ns.

Table 20   DC Characteristics

Parameter	Symbol	Limit Values			Unit	Notes
		Min.	**Typ.**	**Max.**		
Output high voltage (I_{OH} = -0.2 mA)	V_{OH}	$V_{DDQ} \times 0.8$	–	–	V	–
Output low voltage (I_{OL} = 0.2 mA)	V_{OL}	–	–	$V_{DDQ} \times 0.2$	V	–
Input leakage current	I_{LI}	–	–	1	µA	–
Output leakage current	I_{LO}	–	–	1	µA	–

Table 21   Operating Characteristics

Parameter	Symbol	9.6		12.5		15		Unit	Test Condition	Notes
		Min.	Max.	Min.	Max.	Min.	Max.			
Operating Current • Async read/write random @t_{RCmin} • Async read/write random @t_{RC}=1μs • Async Page read • Burst Initial access • Sync burst (continuous) Read • Sync burst (continuous) Write	I_{DD1} I_{DD1L} I_{DD1P} I_{DD2} I_{DD3R} I_{DD3W}	– – – – – –	25 5 18 40 30 35	– – – – – –	25 5 18 35 25 30	– – – – – –	20 5 15 30 20 25	mA	$V_{in} = V_{DD}$ or V_{SS}, Chip enabled, $I_{out} = 0$ 50% of Data switching	1) 2)
Stand-By Current	I_{SB}	–	140	–	140	–	140	μA	$V_{in} = V_{DD}$ or V_{SS},Chip deselected, (Full array)	–

Parameter	Symbol	All Speed Grades		Unit	Test Condition	Notes
		Typ.	Max.			
Deep Power Down Current	I_{DPD}	10	25	μA	$V_{in} = V_{DD}$ or V_{SS}	–

1)   The specification assumes the output disabled.

2)   It is measured as page address <3:0> is applied sequentially (0000_B-0001_B-0010_B-...-1111_B-0000_B-...).

3.3   Output Test Conditions
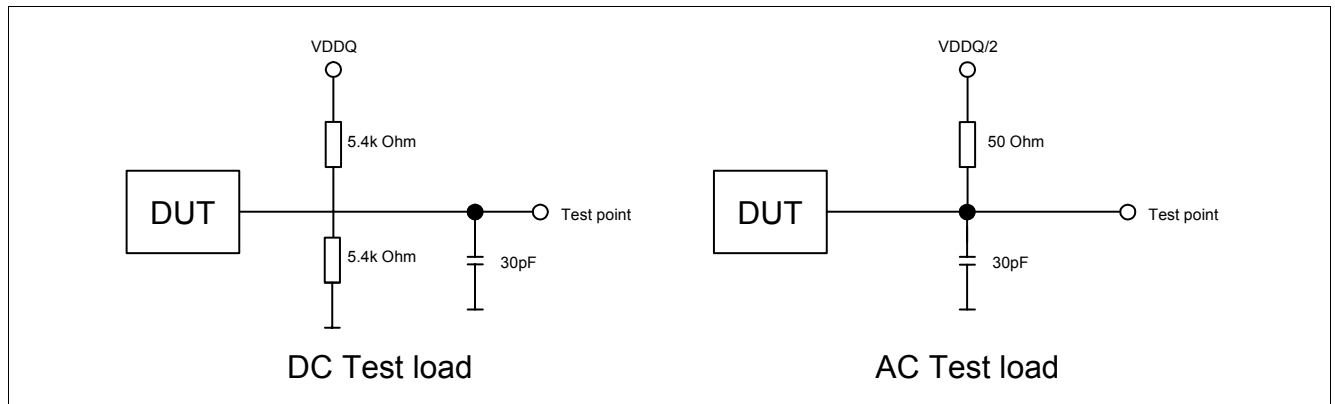
Figure 38   DC / AC Output Test Circuit

Please refer to section **Section 2.11**.

3.4   Pin Capacitances

Table 22   Pin Capacitances

Pin	Limit Values		Unit	Condition
	Min.	Max.		
A21 - A0, $\overline{CS}$, $\overline{OE}$, $\overline{WE}$, $\overline{UB}$, $\overline{LB}$, CRE, $\overline{ADV}$	2.0	6.0	pF	T_A = +25 °C freq. = 1 MHz V_{pin} = 0 V (sampled, not 100% tested)
CLK	2.0	6.0	pF	
DQ15 - DQ0	2.5	6.0	pF	
WAIT	2.5	6.0	pF	

4 Package Outlines

6.00 ± 0.10

Ball A1 indicator

8.00 ± 0.10

1.00 MAX

C

SEATING PLANE

⌀ 0.10 C

0.23 typ

Top View

Ball A1
54X ϕ 0.35
(pre-reflow diameter is 0.35)

6.00 typ

0.75 typ

0.75 typ

3.75 typ

NOTE:
1. All dimensions in mm
2. Primary Datum C and seating plane are
defined by high points of solder balls.

Balls View
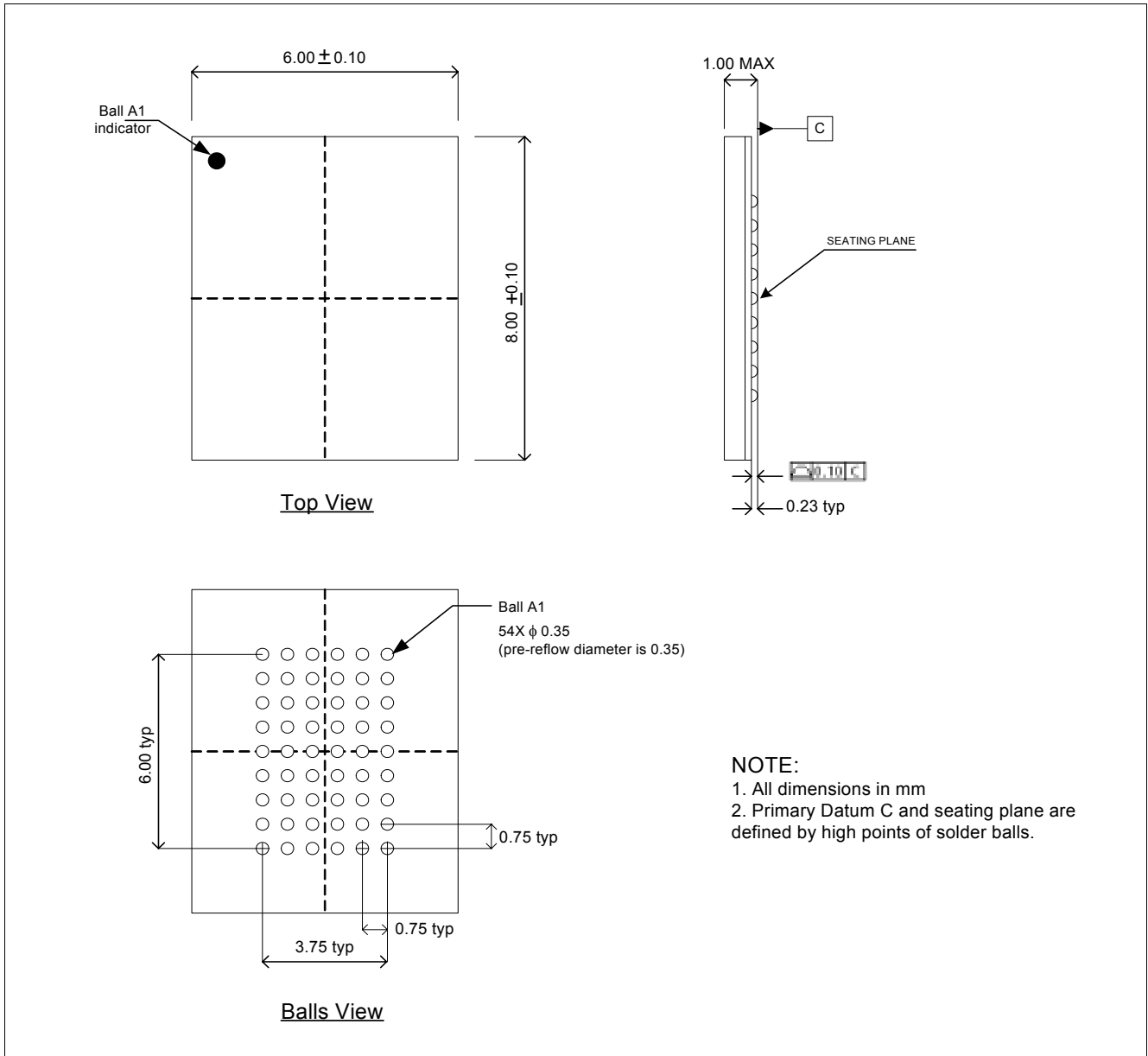
Figure 39   PG-VFBGA-54 (Plastic Very Thin Fine Pitch Ball Grid Array Package - Green Package)

You can find all of our packages, sorts of packing and others in our
Infineon Internet Page "Products": **http://www.infineon.com/products**.

SMD = Surface Mounted Device

Dimensions in mm

5 Appendix : S/W Register Entry Mode ("4-cycle method")

Other than CRE-controlled SCR and FCR operation, CellularRAM supports software (S/W) method as an alternative to access the control registers. Since S/W register entry mode consists of 4 consecutive access cycles to top memory location (all addresses are "1"), it is often referred as "4-cycle method". 4-cycles starts from 2 back-to-back read cycles (initializing command identification) followed by one write cycle (command identification completed and which control register is accessed is known), then final write cycle for configuring the selected control register by the given input or read cycle to check the content of the register through DQ pins. It does function the configuration of control register bits like the way with dedicated pin, CRE method, but there are a few differences from CRE-controlled method as follow;

- Register read mode (checking content) is supported with S/W register entry as well as register write (program).
- The mode bits for control register are supplied through DQ <15:0> instead of address pins in CRE-controlled. Though each register has 22-bits (A<21:0>) for 64M CellularRAM, only low 16-bit registers becomes valid during S/W method.
- Only asynchronous read and write is allowed for consecutive 4 access cycles to top address. No synchronous timing is supported. If this entry mode is used in synchronous mode, then clock should stop running and stay at low level.
- Instead of A19 or A18 state, the selection of the control register, BCR or RCR, or DIDR is done with the state of DQ<15:0> given at 3rd cycle. ("00$_H$" for RCR, "01$_H$" for BCR, "02$_H$" for DIDR)
- The method is realized by the device exactly when 2 consecutive read cycles to top memory location is followed by write cycle to the same location, so that any exceptional cycle combination - not only access mode, but also the number of cycles - will fail in invoking the register entry mode properly.
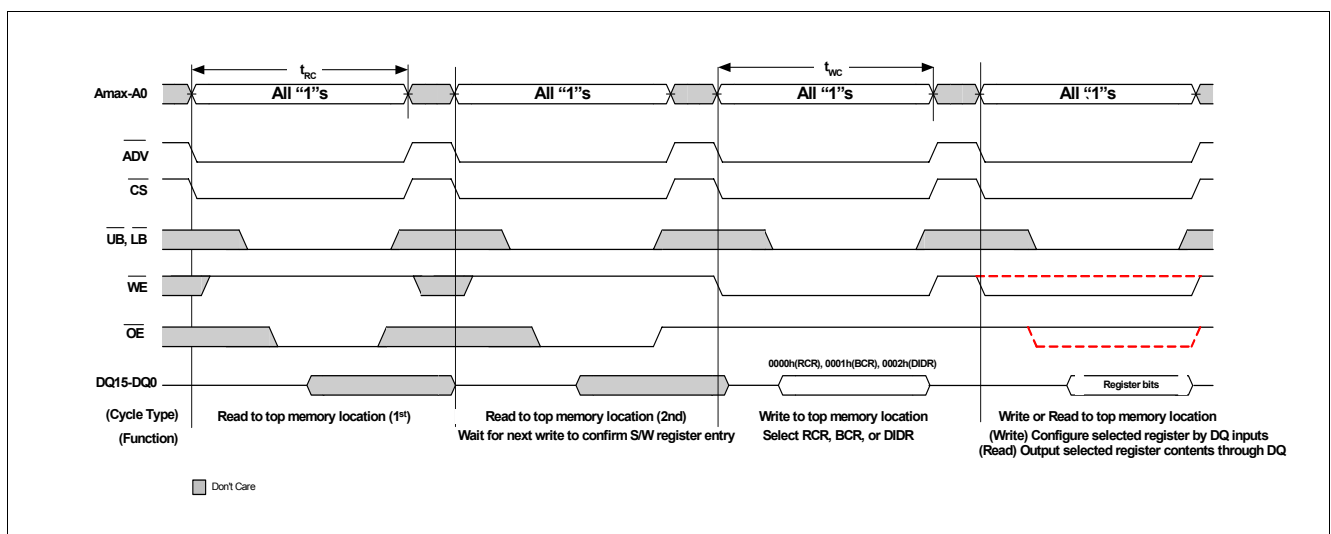
Figure 40   S/W Register Entry timing (Address input = 3FFFFF$_H$)

As depicted in **Figure 40**, 4-cycle operation requires the following timing requirement which are not applied to normal asynchronous read or write cycles.

- $\overline{CS}$ has to toggle in every cycle to distinguish 4 consecutive cycles.
- Address input of top memory location has to be maintained until the completion of each cycle by simply holding all address signals high or latching them by $\overline{ADV}$ until $\overline{CS}$ goes high.

Appendix : S/W Register Entry Mode ("4-cycle method")

DQ bus: DQ15 ---- DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0

Control Register: 0 ---- 0 PM (TCSR)* DPD 0 PASR

Page Mode Bit

A7	page mode
0	disabled (def.)
1	enabled

Deep Power Down Mode

A4	DPD
0	enabled
1	disabled (def.)

Temperature-Compensated Self-Refresh (no effect)

Partial Array Self Refresh

A2	A1	A0	refreshed memory area
0	0	0	entire memory array (def.)
0	0	1	lower 1/2 of memory array
0	1	0	lower 1/4 of memory array
0	1	1	lower 1/8 of memory array
1	0	0	zero
1	0	1	upper 1/2 of memory array
1	1	0	upper 1/4 of memory array
1	1	1	upper 1/8 of memory array

Figure 41   RCR Mapping in S/W Register Entry

DQ Bus: DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ9 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0

Control Register: OM LM Latency Code WP 0 WC 0 0 IMP BW Burst Length

Operation Mode

A15	opmode
0	sync mode
1	async./ page mode (def)

Latency Mode   Latency Code

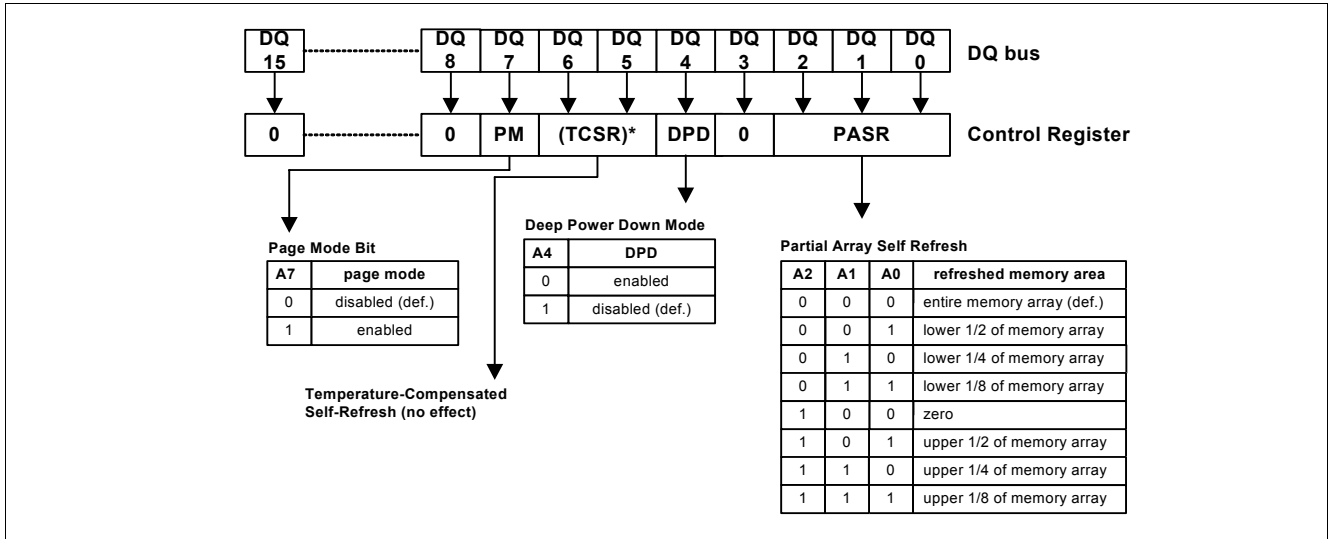|	A14	A13	A12	A11	latency
Variable	0	0	1	0	code2
Variable	0	0	1	1	code3 (def)
Variable	0	All others			reserved
Fixed	1	0	1	0	code2
Fixed	1	0	1	1	code3
Fixed	1	1	0	0	code4
Fixed	1	1	0	1	code5
Fixed	1	1	1	0	code6
Fixed	1	All others			reserved

(note) setting of bit.6 has no effect

WAIT Configuration

A8	timing
0	at delay
1	one data cycle in advance (def)

WAIT Polarity

A10	polarity
0	active low
1	active high (def)

Output Impedance

A5	A4	Drive strength
0	0	full drive
1	0	1/4 drive
0	1	1/2 drive (def)
1	1	reserved

Burst Length

A2	A1	A0	Length
0	0	1	4
0	1	0	8
0	1	1	16
1	0	0	32
1	1	1	continuous (def)
all others reserved			

Burst Wrap

A3	wrap mode
0	wrap
1	no wrap (def)

Figure 42   BCR Mapping in S/W Register Entry

Device ID Register (DIDR) : Read-Only

PS | Design Vesion | Density | Generation | Manufacturer's ID

By 0002$_H$

DQ15 DQ14 DQ13 DQ12 DQ11 DQ10 DQ9 DQ8 DQ7 DQ6 DQ5 DQ4 DQ3 DQ2 DQ1 DQ0

0_B : 128-word
1_B : 256-word

0000_B : A
0001_B : B
0010_B : C
0011_B : D
(and so on)

000_B : 16M
001_B : 32M
010_B : 64M
011_B : 128M
100_B : 256M

DQ<7:5>	Generation
001_B	1.0
010_B	1.5
011_B	2.0

DQ<4:0>	Vendor
00010_B	Infineon
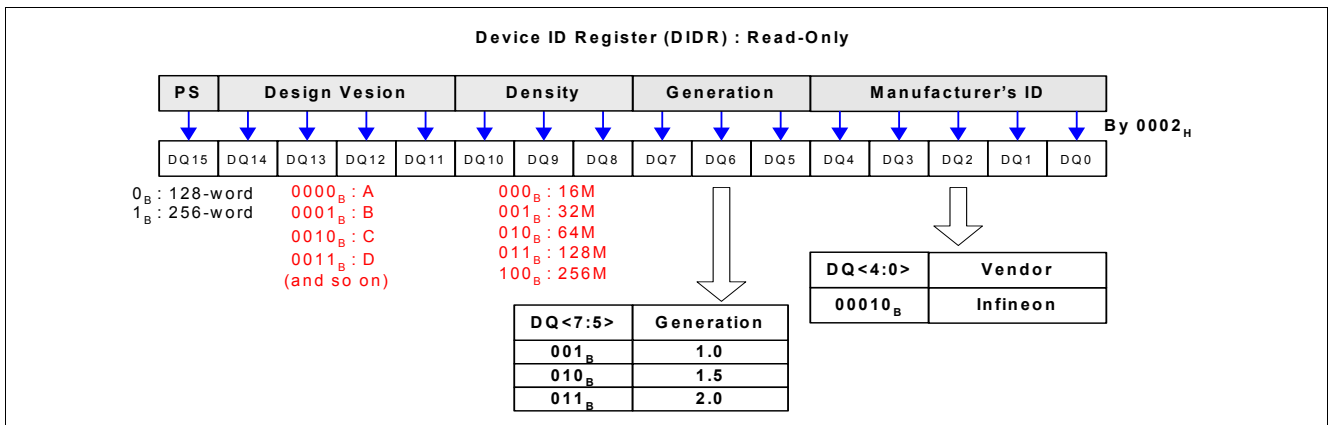
Figure 43   DIDR Mapping in S/W Register Read