

## V850E/MS1™ 32-BIT SINGLE-CHIP MICROCONTROLLERS

The  $\mu$ PD703101A-33 and  $\mu$ PD703102A-33 are members of the V850 Family™ of 32-bit single-chip microcontrollers designed for real-time control operations. These microcontrollers provide on-chip features, including a 32-bit CPU core, ROM, RAM, an interrupt controller, real-time pulse unit, serial interface, A/D converter, and DMA controller.

The  $\mu$ PD703100A-33 and  $\mu$ PD703100A-40 are ROM less versions of the  $\mu$ PD703101A-33 and  $\mu$ PD703102A-33.

The  $\mu$ PD703100-33,  $\mu$ PD703100-40,  $\mu$ PD703101-33, and  $\mu$ PD703102-33 are also available as products having a 5.0 V power supply for external pins.

**Detailed function descriptions are provided in the following user's manuals. Be sure to read them before designing.**

**V850E/MS1 User's Manual Hardware: U12688E**

**V850E/MS1 User's Manual Architecture: U12197E**

### FEATURES

- Number of instructions: 81
- Minimum instruction execution time: 25 ns (@ 40 MHz operation) .....  $\mu$ PD703100A-40  
30 ns (@ 33 MHz operation) .....  $\mu$ PD703100A-33, 703101A-33, 703102A-33
- General-purpose registers: 32 bits  $\times$  32
- Instruction set optimized for control applications
- Internal memory ROM: None ( $\mu$ PD703100A-33, 703100A-40), 96 KB ( $\mu$ PD703101A-33), 128 KB ( $\mu$ PD703102A-33)  
RAM: 4 KB
- Advanced on-chip interrupt controller
- Real-time pulse unit suitable for control operations
- Powerful serial interface (on-chip dedicated baud rate generator)
- On-chip clock generator
- 10-bit resolution A/D converter: 8 channels
- DMA controller: 4 channels
- Power saving functions

### APPLICATIONS

- Office automation equipment: Printers, facsimile machines, PPCs, etc.
- Multimedia equipment: Digital still cameras, video printers, etc.
- Consumer equipment: Single-lens reflex cameras, etc.
- Industrial equipment: Motor controllers, NC machine tools, etc.

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

## ★ ORDERING INFORMATION

Part Number	Package	Maximum Operating Frequency	Internal ROM
$\mu$ PD703100AF1-33-FA1	157-pin plastic FBGA (14 × 14)	33 MHz	None
$\mu$ PD703100AGJ-33-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	None
$\mu$ PD703100AGJ-40- UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	40 MHz	None
$\mu$ PD703101AF1-33-xxx-FA1	157-pin plastic FBGA (14 × 14)	33 MHz	96 KB
$\mu$ PD703101AGJ-33-xxx- UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	96 KB
$\mu$ PD703102AF1-33-xxx-FA1	157-pin plastic FBGA (14 × 14)	33 MHz	128 KB
$\mu$ PD703102AGJ-33-xxx- UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	33 MHz	128 KB

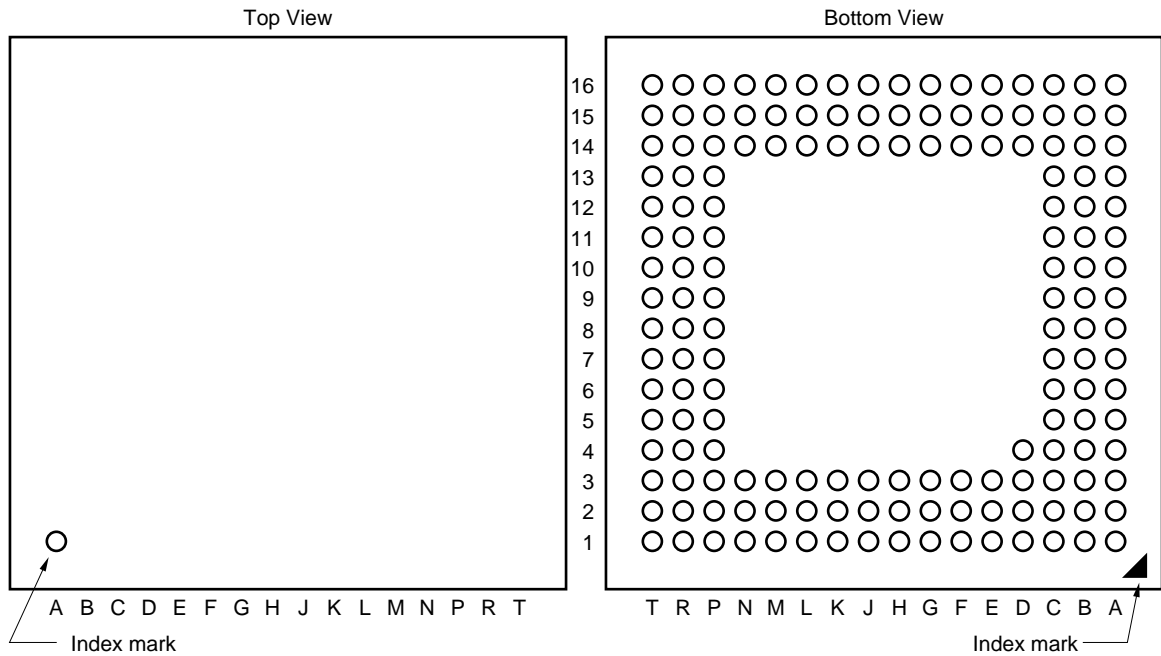
**Remark** xxx indicates ROM code suffix.

**PIN CONFIGURATION (TOP VIEW)**

**157-pin plastic FGBA (14 × 14)**

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- μPD703100AF1-33-FA1
- μPD703101AF1-33-xxx-FA1
- μPD703102AF1-33-xxx-FA1



(1/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
A1	—	B1	INTP103/DMARQ3/P07	C1	INTP101/DMARQ1/P05
A2	D0/P40	B2	D1/P41	C2	INTP102/DMARQ2/P06
A3	D2/P42	B3	D3/P43	C3	V <sub>SS</sub>
A4	D4/P44	B4	D5/P45	C4	V <sub>SS</sub>
A5	D6/P46	B5	D7/P47	C5	HV <sub>DD</sub>
A6	D8/P50	B6	D9/P51	C6	V <sub>SS</sub>
A7	D10/P52	B7	D11/P53	C7	D12/P54
A8	D13/P55	B8	D14/P56	C8	D15/P57
A9	A0/PA0	B9	A1/PA1	C9	HV <sub>DD</sub>
A10	A2/PA2	B10	A3/PA3	C10	A4/PA4
A11	A5/PA5	B11	A6/PA6	C11	A7/PA7
A12	A8/PB0	B12	A9/PB1	C12	V <sub>SS</sub>
A13	A10/PB2	B13	A11/PB3	C13	A12/PB4
A14	A13/PB5	B14	A14/PB6	C14	A18/P62
A15	A15/PB7	B15	A17/P61	C15	A19/P63
A16	—	B16	A16/P60	C16	—

(2/2)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
D1	T110/P03	K1	T112/P103	P14	RESET
D2	INTP100/DMARQ0/P04	K2	INTP120/TC0/P104	P15	INTP151/P125
D3	HV <sub>DD</sub>	K3	INTP121/TC1/P105	P16	INTP150/P124
D4	—	K14	HLD <sub>AK</sub> /P96	R1	AV <sub>SS</sub>
D14	V <sub>SS</sub>	K15	OE/P95	R2	ANI0/P70
D15	A21/P65	K16	BCYST/P94	R3	P21
D16	A20/P64	L1	TO120/P100	R4	SCK0/P24
E1	TO101/P01	L2	TO121/P101	R5	SCK1/P27
E2	TCLR10/P02	L3	TCLR12/P102	R6	INTP132/SI2/P36
E3	V <sub>SS</sub>	L14	V <sub>SS</sub>	R7	T113/P33
E14	HV <sub>DD</sub>	L15	REFRQ/PX5	R8	TO130/P30
E15	A23/P67	L16	HLD <sub>RQ</sub> /P97	R9	INTP141/SO3/P115
E16	A22/P66	M1	ANI5/P75	R10	TCLR14/P112
F1	INTP113/DMAAK3/P17	M2	ANI6/P76	R11	TO140/P110
F2	TO100/P00	M3	ANI7/P77	R12	MODE0
F3	V <sub>DD</sub>	M14	TO150/P120	R13	MODE1
F14	CS2/RAS2/P82	M15	WAIT/PX6	R14	MODE2
F15	CS1/RAS1/P81	M16	CLKOUT/PX7	R15	INTP153/ADTRG/P127
F16	CS0/RAS0/P80	N1	ANI2/P72	R16	INTP152/P126
G1	INTP110/DMAAK0/P14	N2	ANI3/P73	T1	—
G2	INTP111/DMAAK1/P15	N3	ANI4/P74	T2	AV <sub>REF</sub>
G3	INTP112/DMAAK2/P16	N14	T115/P123	T3	NMI/P20
G14	CS5/RAS5/IORD/P85	N15	TCLR15/P122	T4	RXD0/SI0/P23
G15	CS4/RAS4/IOWR/P84	N16	TO151/P121	T5	RXD1/SI1/P26
G16	CS3/RAS3/P83	P1	AV <sub>DD</sub>	T6	INTP131/SO2/P35
H1	TO111/P11	P2	ANI1/P71	T7	TCLR13/P32
H2	TCLR11/P12	P3	TXD0/SO0/P22	T8	INTP143/SCK3/P117
H3	T111/P13	P4	TXD1/SO1/P25	T9	INTP140/P114
H14	LCAS/LWR/P90	P5	V <sub>DD</sub>	T10	CV <sub>DD</sub>
H15	CS7/RAS7/P87	P6	INTP133/SCK2/P37	T11	X2
H16	CS6/RAS6/P86	P7	INTP130/P34	T12	X1
J1	INTP122/TC2/P106	P8	TO131/P31	T13	CV <sub>SS</sub>
J2	INTP123/TC3/P107	P9	INTP142/SI3/P116	T14	MODE3
J3	TO110/P10	P10	T114/P113	T15	—
J14	WE/P93	P11	TO141/P111	T16	—
J15	RD/P92	P12	CKSEL	—	—
J16	UCAS/UWR/P91	P13	HV <sub>DD</sub>	—	—

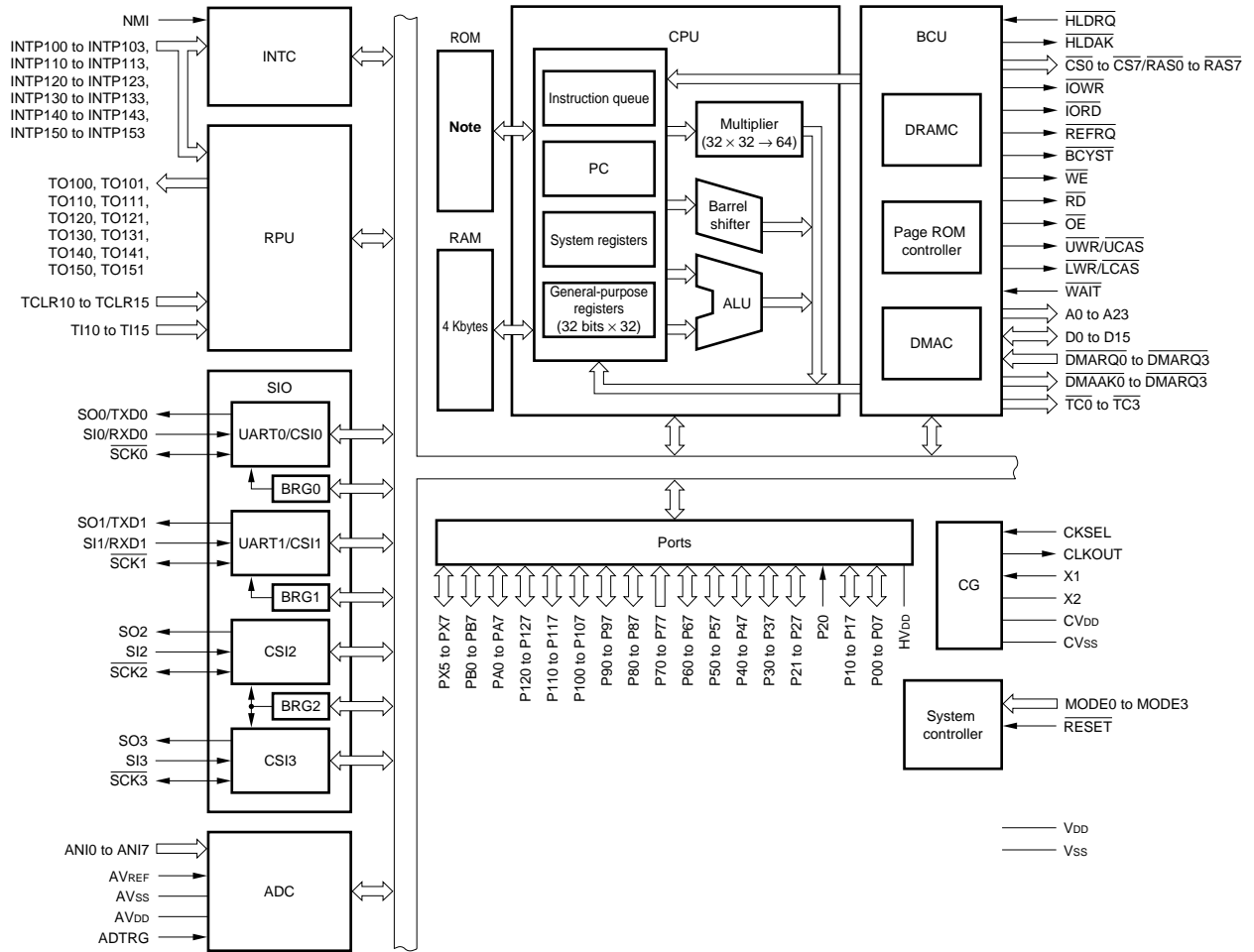
**Remark** Leave the pins numbered A1, A16, C16, D4, T1, T15, and T16 open.



**PIN IDENTIFICATION**

A0 to A23:	Address bus	P50 to P57:	Port 5
ADTRG:	AD trigger input	P60 to P67:	Port 6
ANI0 to ANI7:	Analog input	P70 to P77:	Port 7
AV <sub>DD</sub> :	Analog power supply	P80 to P87:	Port 8
AV <sub>REF</sub> :	Analog reference voltage	P90 to P97:	Port 9
AV <sub>SS</sub> :	Analog ground	P100 to P107:	Port 10
<u>BCYST</u> :	Bus cycle start timing	P110 to P117:	Port 11
CKSEL:	Clock generator operating mode select	P120 to P127:	Port 12
<u>CLKOUT</u> :	Clock output	PA0 to PA7:	Port A
<u>CS0</u> to <u>CS7</u> :	Chip select	PB0 to PB7:	Port B
CV <sub>DD</sub> :	Clock generator power supply	PX5 to PX7:	Port X
CV <sub>SS</sub> :	Clock generator ground	<u>RAS0</u> to <u>RAS7</u> :	Row address strobe
D0 to D15:	Data bus	<u>RD</u> :	Read
<u>DMAAK0</u> to <u>DMAAK3</u> :	DMA acknowledge	<u>REFRQ</u> :	Refresh request
<u>DMARQ0</u> to <u>DMARQ3</u> :	DMA request	<u>RESET</u> :	Reset
<u>HLDAK</u> :	Hold acknowledge	RXD0, RXD1:	Receive data
<u>HLD<sub>RQ</sub></u> :	Hold request	<u>SCK0</u> to <u>SCK3</u> :	Serial clock
HV <sub>DD</sub> :	Power supply for external pins	SI0 to SI3:	Serial input
INTP100 to INTP103, INTP110 to INTP113, INTP120 to INTP123, INTP130 to INTP133, INTP140 to INTP143, INTP150 to INTP153:	Interrupt request from peripherals	SO0 to SO3:	Serial output
<u>IORD</u> :	I/O read strobe	<u>TC0</u> to <u>TC3</u> :	Terminal count signal
<u>IOWR</u> :	I/O write strobe	TCLR10 to TCLR15:	Timer clear
<u>LCAS</u> :	Lower column address strobe	TI10 to TI15:	Timer input
<u>LWR</u> :	Lower write strobe	TO100, TO101, TO110, TO111, TO120, TO121, TO130, TO131, TO140, TO141, TO150, TO151:	Timer output
MODE0 to MODE3:	Mode	TXD0, TXD1:	Transmit data
NMI:	Non-maskable interrupt request	<u>UCAS</u> :	Upper column address strobe
<u>OE</u> :	Output enable	<u>UWR</u> :	Upper write strobe
P00 to P07:	Port 0	V <sub>DD</sub> :	Power supply for internal unit
P10 to P17:	Port 1	V <sub>SS</sub> :	Ground
P20 to P27:	Port 2	<u>WAIT</u> :	Wait
P30 to P37:	Port 3	<u>WE</u> :	Write enable
P40 to P47:	Port 4	X1, X2:	Crystal

INTERNAL BLOCK DIAGRAM



**Note** μPD703100A-33, 703100A-40: None  
 μPD703101A-33: 96 KB (mask ROM)  
 μPD703102A-33: 128 KB (mask ROM)

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1. DIFFERENCES AMONG PRODUCTS

Part Number / Item	μPD703100				μPD703101		μPD703102		μPD70F3102	
	-33	-40	A-33	A-40	-33	A-33	-33	A-33	-33	A-33
Internal ROM	None				96 KB (mask ROM)		128 KB (mask ROM)		128 KB (flash memory)	
Maximum operating frequency	33 MHz	40 MHz	33 MHz	40 MHz	33 MHz					
HV <sub>DD</sub>	4.5 to 5.5 V		3.0 to 3.6 V		4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V	4.5 to 5.5 V	3.0 to 3.6 V
Operation mode										
Single-chip mode 0, 1	None				Provided					
Flash memory programming mode	None								Provided	
Flash memory programming pin	None								Provided (V <sub>PP</sub> )	
Electrical specifications	Current consumption differs (refer to the data sheet of each product).									
Package	144LQFP		144LQFP 157FBGA	144LQFP	144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA	144LQFP	144LQFP 157FBGA
Others	Noise tolerance and noise radiation will differ due to the differences in circuit scale and mask layout.									

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**Remark** 144LQFP: 144-pin plastic LQFP (fine pitch) (20 × 20)  
157FBGA: 157-pin plastic FBGA (14 × 14)

2. PIN FUNCTIONS

2.1 Port Pins

(1/3)

Pin Name	I/O	Function	Alternate Function
P00	I/O	Port 0 8-bit I/O port Input/output can be specified in 1-bit units	TO100
P01			TO101
P02			TCLR10
P03			TI10
P04			INTP100/D $\overline{\text{MARQ0}}$
P05			INTP101/D $\overline{\text{MARQ1}}$
P06			INTP102/D $\overline{\text{MARQ2}}$
P07			INTP103/D $\overline{\text{MARQ3}}$
P10	I/O	Port 1 8-bit I/O port Input/output can be specified in 1-bit units	TO110
P11			TO111
P12			TCLR11
P13			TI11
P14			INTP110/D $\overline{\text{MAAK0}}$
P15			INTP111/D $\overline{\text{MAAK1}}$
P16			INTP112/D $\overline{\text{MAAK2}}$
P17			INTP113/D $\overline{\text{MAAK3}}$
P20	Input	Port 2 P20 is an input only port. When a valid edge is input, this pin operates as an NMI input. Also, bit 0 of the P2 register indicates the NMI input status. P21 to P27 are a 7-bit I/O port. Input/output can be specified in 1-bit units	NMI
P21	I/O		-
P22			TXD0/SO0
P23			RXD0/SI0
P24			SCK0
P25			TXD1/SO1
P26			RXD1/SI1
P27			SCK1
P30	I/O	Port 3 8-bit I/O port. Input/output can be specified in 1-bit units	TO130
P31			TO131
P32			TCLR13
P33			TI13
P34			INTP130
P35			INTP131/SO2
P36			INTP132/SI2
P37			INTP133/SCK2
P40 to P47	I/O	Port 4 8-bit I/O port Input/output can be specified in 1-bit units	D0 to D7

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Pin Name	I/O	Function	Alternate Function
P50 to P57	I/O	Port 5 8-bit I/O port Input/output can be specified in 1-bit units	D8 to D15
P60 to P67	I/O	Port 6 8-bit I/O port Input/output can be specified in 1-bit units	A16 to A23
P70 to P77	Input	Port 7 8-bit input-only port	ANI0 to ANI7
P80	I/O	Port 8 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{CS0}/\overline{RAS0}$
P81			$\overline{CS1}/\overline{RAS1}$
P82			$\overline{CS2}/\overline{RAS2}$
P83			$\overline{CS3}/\overline{RAS3}$
P84			$\overline{CS4}/\overline{RAS4}/\overline{IOWR}$
P85			$\overline{CS5}/\overline{RAS5}/\overline{IORD}$
P86			$\overline{CS6}/\overline{RAS6}$
P87			$\overline{CS7}/\overline{RAS7}$
P90	I/O	Port 9 8-bit I/O port Input/output can be specified in 1-bit units	$\overline{LCAS}/\overline{LWR}$
P91			$\overline{UCAS}/\overline{UWR}$
P92			$\overline{RD}$
P93			$\overline{WE}$
P94			$\overline{BCYST}$
P95			$\overline{OE}$
P96			$\overline{HLDAK}$
P97			$\overline{HLDRQ}$
P100	I/O	Port 10 8-bit I/O port Input/output can be specified in 1-bit units	TO120
P101			TO121
P102			TCLR12
P103			TI12
P104			INTP120/ $\overline{TC0}$
P105			INTP121/ $\overline{TC1}$
P106			INTP122/ $\overline{TC2}$
P107			INTP123/ $\overline{TC3}$
P110	I/O	Port 11 8-bit I/O port Input/output can be specified in 1-bit units	TO140
P111			TO141
P112			TCLR14
P113			TI14
P114			INTP140
P115			INTP141/SO3
P116			INTP142/SI3
P117			INTP143/ $\overline{SCK3}$

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Pin Name	I/O	Function	Alternate Function
P120	I/O	Port 12 8-bit I/O port Input/output can be specified in 1-bit units	TO150
P121			TO151
P122			TCLR15
P123			TI15
P124			INTP150
P125			INTP151
P126			INTP152
P127			INTP153/ADTRG
PA0	I/O	Port A 8-bit I/O port Input/output can be specified in 1-bit units	A0
PA1			A1
PA2			A2
PA3			A3
PA4			A4
PA5			A5
PA6			A6
PA7			A7
PB0	I/O	Port B 8-bit I/O port Input/output can be specified in 1-bit units	A8
PB1			A9
PB2			A10
PB3			A11
PB4			A12
PB5			A13
PB6			A14
PB7			A15
PX5	I/O	Port X 3-bit I/O port Input/output can be specified in 1-bit units	REFRQ
PX6			WAIT
PX7			CLKOUT

2.2 Non-Port Pins

(1/4)

Pin Name	I/O	Function	Alternate Function
TO100	Output	Pulse signal output for timers 10 to 15	P00
TO101			P01
TO110			P10
TO111			P11
TO120			P100
TO121			P101
TO130			P30
TO131			P31
TO140			P110
TO141			P111
TO150			P120
TO151			P121
TCLR10			Input
TCLR11	P12		
TCLR12	P102		
TCLR13	P32		
TCLR14	P112		
TCLR15	P122		
TI10	Input	External count clock input for timers 10 to 15	P03
TI11			P13
TI12			P103
TI13			P33
TI14			P113
TI15			P123
INTP100	Input	External maskable interrupt request input, also used as external capture trigger input for timer 10	P04/ $\overline{\text{DMARQ0}}$
INTP101			P05/ $\overline{\text{DMARQ1}}$
INTP102			P06/ $\overline{\text{DMARQ2}}$
INTP103			P07/ $\overline{\text{DMARQ3}}$
INTP110	Input	External maskable interrupt request input, also used as external capture trigger input for timer 11	P14/ $\overline{\text{DMAAK0}}$
INTP111			P15/ $\overline{\text{DMAAK1}}$
INTP112			P16/ $\overline{\text{DMAAK2}}$
INTP113			P17/ $\overline{\text{DMAAK3}}$
INTP120	Input	External maskable interrupt request input, also used as external capture trigger input for timer 12	P104/ $\overline{\text{TC0}}$
INTP121			P105/ $\overline{\text{TC1}}$
INTP122			P106/ $\overline{\text{TC2}}$
INTP123			P107/ $\overline{\text{TC3}}$

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Pin Name	I/O	Function	Alternate Function
INTP130	Input	External maskable interrupt request input, also used as external capture trigger input for timer 13	P34
INTP131			P35/SO2
INTP132			P36/SI2
INTP133			P37/SCK2
INTP140	Input	External maskable interrupt request input, also used as external capture trigger input for timer 14	P114
INTP141			P115/SO3
INTP142			P116/SI3
INTP143			P117/SCK3
INTP150	Input	External maskable interrupt request input, also used as external capture trigger input for timer 15	P124
INTP151			P125
INTP152			P126
INTP153			P127/ADTRG
SO0	Output	Serial transmit data output (3-wire) for CSI0 to CSI3	P22/TXD0
SO1			P25/TXD1
SO2			P35/INTP131
SO3			P115/INTP141
SI0	Input	Serial receive data input (3-wire) for CSI0 to CSI3	P23/RXD0
SI1			P26/RXD1
SI2			P36/INTP132
SI3			P116/INTP142
SCK0	I/O	Serial clock I/O (3-wire) for CSI0 to CSI3	P24
SCK1			P27
SCK2			P37/INTP133
SCK3			P117/INTP143
TXD0	Output	Serial transmit data output for UART0 and UART1	P22/SO0
TXD1			P25/SO1
RXD0	Input	Serial receive data input for UART0 and UART1	P23/SI0
RXD1			P26/SI1
D0 to D7	I/O	16-bit data bus for external memory	P40 to P47
D8 to D15			P50 to P57
A0 to A7	Output	24-bit address bus for external memory	PA0 to PA7
A8 to A15			PB0 to PB7
A16 to A23			P60 to P67
LWR	Output	Lower byte write-enable signal output for external data bus	P90/LCAS
UWR	Output	Higher byte write-enable signal output for external data bus	P91/UCAS
RD	Output	Read strobe signal output for external data bus	P92
WE	Output	Write enable signal output for DRAM	P93
OE	Output	Output enable signal output for DRAM	P95

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Pin Name	I/O	Function	Alternate Function
$\overline{\text{LCAS}}$	Output	Column address strobe signal output for DRAM's lower data	P90/ $\overline{\text{LWR}}$
$\overline{\text{UCAS}}$	Output	Column address strobe signal output for DRAM's higher data	P91/ $\overline{\text{UWR}}$
$\overline{\text{RAS0}}$ to $\overline{\text{RAS3}}$	Output	Low address strobe signal output for DRAM	P80/ $\overline{\text{CS0}}$ to P83/ $\overline{\text{CS3}}$
$\overline{\text{RAS4}}$			P84/ $\overline{\text{CS4}}$ / $\overline{\text{IOWR}}$
$\overline{\text{RAS5}}$			P85/ $\overline{\text{CS5}}$ / $\overline{\text{IORD}}$
$\overline{\text{RAS6}}$			P86/ $\overline{\text{CS6}}$
$\overline{\text{RAS7}}$			P87/ $\overline{\text{CS7}}$
$\overline{\text{BCYST}}$	Output	Strobe signal output indicating start of bus cycle	P94
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	Output	Chip select signal output	P80/ $\overline{\text{RAS0}}$ to P83/ $\overline{\text{RAS3}}$
$\overline{\text{CS4}}$			P84/ $\overline{\text{RAS4}}$ / $\overline{\text{IOWR}}$
$\overline{\text{CS5}}$			P85/ $\overline{\text{RAS5}}$ / $\overline{\text{IORD}}$
$\overline{\text{CS6}}$			P86/ $\overline{\text{RAS6}}$
$\overline{\text{CS7}}$			P87/ $\overline{\text{RAS7}}$
$\overline{\text{WAIT}}$	Input	Control signal input for inserting waits in bus cycle	PX6
$\overline{\text{REFRQ}}$	Output	Refresh request signal output for DRAM	PX5
$\overline{\text{IOWR}}$	Output	DMA write strobe signal output	P84/ $\overline{\text{RAS4}}$ / $\overline{\text{CS4}}$
$\overline{\text{IORD}}$	Output	DMA read strobe signal output	P85/ $\overline{\text{RAS5}}$ / $\overline{\text{CS5}}$
$\overline{\text{DMARQ0}}$ to $\overline{\text{DMARQ3}}$	Input	DMA request signal input	P04/ $\overline{\text{INTP100}}$ to P07/ $\overline{\text{INTP103}}$
$\overline{\text{DMAAK0}}$ to $\overline{\text{DMAAK3}}$	Output	DMA acknowledge signal output	P14/ $\overline{\text{INTP110}}$ to P17/ $\overline{\text{INTP113}}$
$\overline{\text{TC0}}$ to $\overline{\text{TC3}}$	Output	DMA end (terminal count) signal output	P104/ $\overline{\text{INTP120}}$ to P107/ $\overline{\text{INTP123}}$
$\overline{\text{HLDAK}}$	Output	Bus hold acknowledge output	P96
$\overline{\text{HLDRQ}}$	Input	Bus hold request input	P97
ANI0 to ANI7	Input	Analog input to A/D converter	P70 to P77
NMI	Input	Non-maskable interrupt request input	P20
CLKOUT	Output	System clock output	PX7
CKSEL	Input	Input for specifying clock generator's operation mode	—
MODE0 to MODE3	Input	Specify operation modes	—
$\overline{\text{RESET}}$	Input	System reset input	—
X1	Input	Oscillator connection for system clock. Input is via X1 when using an external clock.	—
X2	—		—
ADTRG	Input	A/D converter external trigger input	P127/ $\overline{\text{INTP153}}$
$\text{AV}_{\text{REF}}$	Input	Reference voltage input for A/D converter	—
$\text{AV}_{\text{DD}}$	—	Positive power supply for A/D converter	—
$\text{AV}_{\text{SS}}$	—	Ground potential for A/D converter	—

(4/4)

Pin Name	I/O	Function	Alternate Function
CV <sub>DD</sub>	—	Positive power supply for dedicated clock generator	—
CV <sub>SS</sub>	—	Ground potential for dedicated clock generator	—
V <sub>DD</sub>	—	Positive power supply (power supply for internal units)	—
HV <sub>DD</sub>	—	Positive power supply (power supply for external pins)	—
V <sub>SS</sub>	—	Ground potential	—

**2.3 Pin I/O Circuits and Recommended Connection of Unused Pins**

Table 2-1 shows the I/O circuit type of each pin and recommended connection of unused pins. Figure 2-1 shows the various circuit types using partially abridged diagrams.

When connecting to V<sub>DD</sub> or V<sub>SS</sub> via a resistor, a resistance value in the range of 1 to 10 kΩ is recommended.

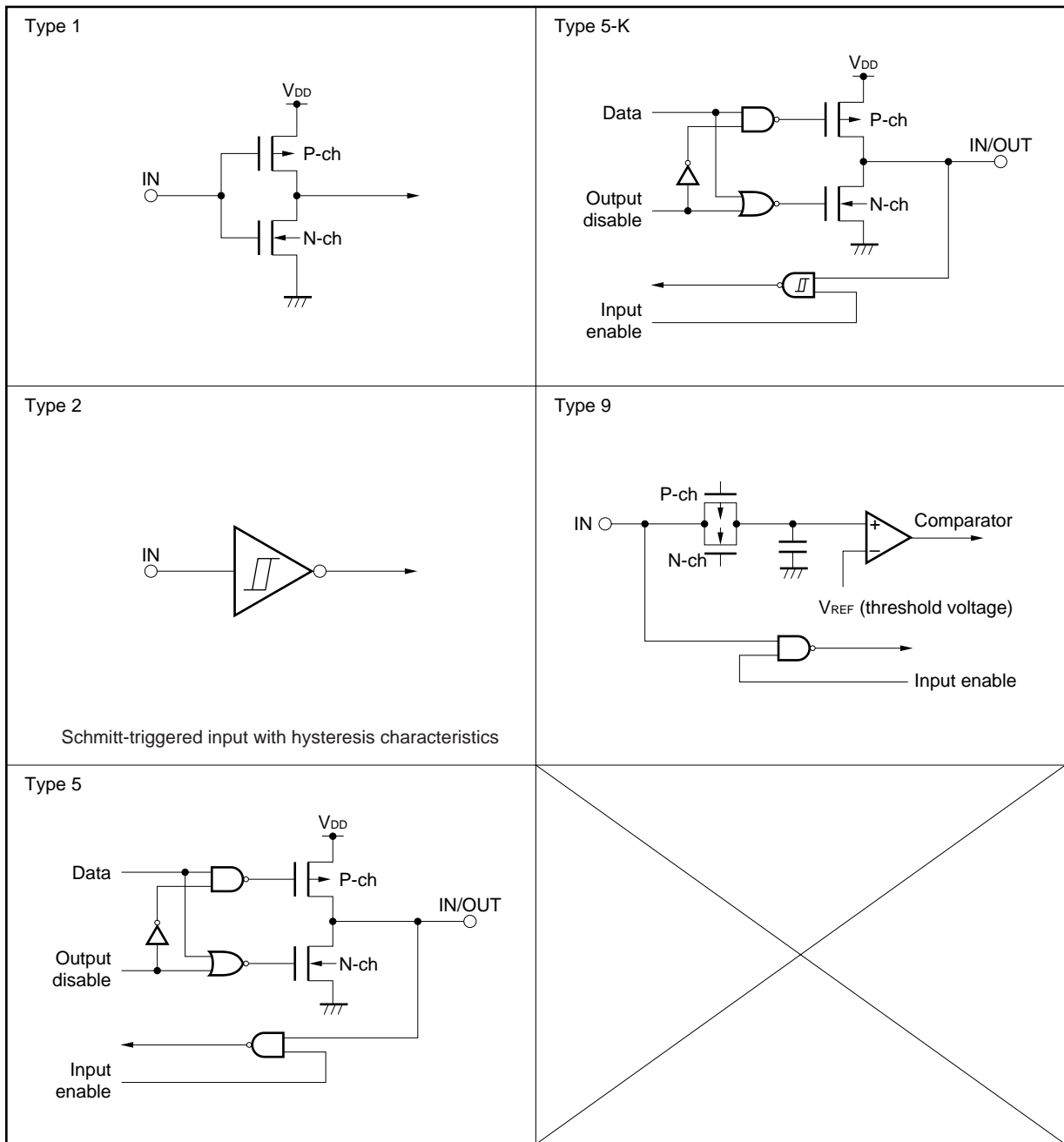
**Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (1/2)**

Pin	I/O Circuit Type	Recommended Connection of Unused Pins
P00/TO100, P01/TO101	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P02/TCLR10, P03/TI10	5-K	
P04/INTP100/D <sub>MARQ0</sub> to P07/INTP103/D <sub>MARQ3</sub>		
P10/TO110, P11/TO111	5	
P12/TCLR11, P13/TI11	5-K	
P14/INTP110/D <sub>MAAK0</sub> to P17/INTP113/D <sub>MAAK3</sub>		
P20/NMI	2	Connect directly to V <sub>SS</sub>
P21	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P22/TXD0/SO0		
P23/RXD0/SI0	5-K	
P24/SCK0		
P25/TXD1/SO1	5	
P26/RXD1/SI1	5-K	
P27/SCK1		
P30/TO130, P31/TO131	5	
P32/TCLR13, P33/TI13	5-K	
P34/INTP130		
P35/INTP131/SO2		
P36/INTP132/SI2		
P37/INTP133/SCK2		
P40/D0 to P47/D7		
P50/D8 to P57/D15		
P60/A16 to P67/A23		
P70/ANI0 to P77/ANI7	9	Connect directly to V <sub>SS</sub>
P80/ <u>CS0</u> /RAS0 to P83/ <u>CS3</u> /RAS3	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open
P84/ <u>CS4</u> /RAS4/IOWR, P85/ <u>CS5</u> /RAS5/IORD		
P86/ <u>CS6</u> /RAS6, P87/ <u>CS7</u> /RAS7		
P90/LCAS/LWR		
P91/UCAS/UWR		

Table 2-1. I/O Circuit Type of Each Pin and Recommended Connection of Unused Pins (2/2)

Pin	I/O Circuit Type	Recommended Connection of Unused Pins	
P92/RD	5	Input: Independently connect to HV <sub>DD</sub> or V <sub>SS</sub> via a resistor Output: Leave open	
P93/WE			
P94/BCYST			
P95/OE			
P96/HLDAK			
P97/HLDRQ			
P100/TO120, P101/TO121			
P102/TCLR12, P103/TI12			5-K
P104/INTP120/TC0 to P107/INTP123/TC3	5		
P110/TO140, P111/TOI41			
P112/TCLR14, P113/TI14			5-K
P114/INTP140			
P115/INTP141/SO3			
P116/INTP142/SI3			
P117/INTP143/SCK3			
P120/TO150, P121/TO151			5
P122/TCLR15, P123/TI15	5-K		
P124/INTP150 to P126/INTP152			
P127/INTP153/ADTRG			
PA0/A0 to PA7/A7	5		
PB0/A8 to PB7/A15			
PX5/REFRQ			
PX6/WAIT			
PX7/CLKOUT			
CKSEL			1
RESET	2	—	
MODE0 to MODE2		Connect to V <sub>SS</sub> via a resistor (R <sub>VPP</sub> )	
MODE3			
AV <sub>REF</sub> , AV <sub>SS</sub>	—	Connect directly to V <sub>SS</sub>	
AV <sub>DD</sub>	—	Connect directly to HV <sub>DD</sub>	

Figure 2-1. Pin I/O Circuits



**Caution** Replace  $V_{DD}$  with  $HV_{DD}$  when referencing the circuit diagrams shown above.

## 3. ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ )

Parameter	Symbol	Conditions	Rating	Unit	
Power supply voltage	$V_{DD}$	$V_{DD}$ pin	-0.5 to +4.6	V	
	$HV_{DD}$	$HV_{DD}$ pin, $HV_{DD} \geq V_{DD}$	-0.5 to +4.6	V	
	$CV_{DD}$	$CV_{DD}$ pin	-0.5 to +4.6	V	
	$CV_{SS}$	$CV_{SS}$ pin	-0.5 to +0.5	V	
	$AV_{DD}$	$AV_{DD}$ pin	-0.5 to $HV_{DD} + 0.5$	V	
	$AV_{SS}$	$AV_{SS}$ pin	-0.5 to +0.5	V	
Input voltage	$V_I$	X1 pin, except MODE3 pin	-0.5 to $HV_{DD} + 0.5$	V	
		MODE3 pin	-0.5 to $V_{DD} + 0.5$	V	
Clock input voltage	$V_K$	X1, $V_{DD} = 3.0$ to $3.6$ V	-0.5 to $V_{DD} + 1.0$	V	
Output current, low	$I_{OL}$	1 pin	4.0	mA	
		Total of all pins	100	mA	
Output current, high	$I_{OH}$	1 pin	-4.0	mA	
		Total of all pins	-100	mA	
Output voltage	$V_O$	$HV_{DD} = 3.0$ V to $3.6$ V	-0.5 to $HV_{DD} + 0.5$	V	
Analog input voltage	$V_{IAN}$	P70/ANI0 to P77/ANI7 pins	$AV_{DD} > HV_{DD}$	-0.5 to $HV_{DD} + 0.5$	V
			$HV_{DD} \geq AV_{DD}$	-0.5 to $AV_{DD} + 0.5$	V
A/D converter reference input voltage	$AV_{REF}$	$AV_{DD} > HV_{DD}$	-0.5 to $HV_{DD} + 0.5$	V	
		$HV_{DD} \geq AV_{DD}$	-0.5 to $AV_{DD} + 0.5$	V	
Operating ambient temperature	$T_A$	$\mu$ PD703100A-40	-40 to +70	$^\circ\text{C}$	
		$\mu$ PD703100A-33, 703101A-33, 703102A-33	-40 to +85	$^\circ\text{C}$	
Storage temperature	$T_{stg}$		-65 to +150	$^\circ\text{C}$	

- Caution**
- Do not directly connect the output (or I/O) pins to each other, or to  $V_{DD}$ ,  $V_{CC}$ , and GND. Open-drain or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.
  - Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

Capacitance (T<sub>A</sub> = 25°C, V<sub>DD</sub> = HV<sub>DD</sub> = CV<sub>DD</sub> = V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C <sub>i</sub>	f <sub>c</sub> = 1 MHz Unmeasured pins returned to 0 V.			15	pF
Input/output capacitance	C <sub>io</sub>				15	pF
Output capacitance	C <sub>o</sub>				15	pF

Operating Conditions

Operation Mode	Internal Operating Clock Frequency (ϕ)		Operating Ambient Temperature (T <sub>A</sub> )	Power Supply Voltage (V <sub>DD</sub> , HV <sub>DD</sub> )
Direct mode	μPD703100A-40	2 to 40 MHz	-40 to +70°C	3.0 to 3.6 V
	μPD703100A-33, 703101A-33, 703102A-33	2 to 33 MHz	-40 to +85°C	
PLL mode <sup>Note 1</sup>	μPD703100A-40	20 to 40 MHz <sup>Note 2</sup>	-40 to +70°C	
	μPD703100A-33, 703101A-33, 703102A-33	20 to 33 MHz <sup>Note 3</sup>	-40 to +85°C	

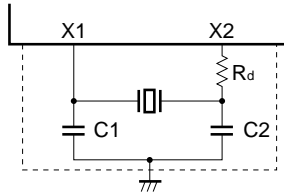
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- Notes**
1. The internal operating clock frequency in the PLL mode is the value when operating at ×5 multiplication. Operation is also possible at a frequency of 20 MHz or lower when used at 1 or 1/2 multiplication by setting the CKDIV<sub>n</sub> bit (n = 0, 1) of the CKC register.
  2. The input clock frequency used in PLL mode should be 4.0 to 8.0 MHz.
  3. The input clock frequency used in PLL mode should be used by 4.0 to 6.6 MHz.

**Recommended Oscillators**

- (a) Ceramic resonator (T<sub>A</sub> = -40 to +70°C ...  $\mu$ PD703100A-40,  
T<sub>A</sub> = -40 to +85°C ...  $\mu$ PD703100A-33, 703101A-33, 703102A-33)

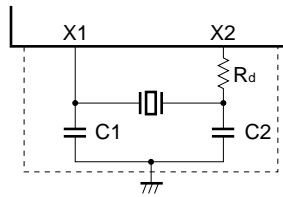
★ (i) Murata Mfg. Co., Ltd.



Type	Product Name	Oscillation Frequency f <sub>xx</sub> (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.) T <sub>OST</sub> (ms)
			C1 (pF)	C2 (pF)	R <sub>d</sub> (kΩ)	MIN. (V)	MAX. (V)	
Surface mount	CSAC4.00MGC040	4.0	100	100	0	3.0	3.6	0.5
	CSTCC4.00MG0H6	4.0	On-chip	On-chip	0	3.0	3.6	0.3
	CSAC5.00MGC040	5.0	100	100	0	3.0	3.6	0.4
	CSTCC5.00MG0H6	5.0	On-chip	On-chip	0	3.0	3.6	0.2
	CSAC6.60MT	6.6	30	30	0	3.0	3.6	0.2
	CSTCC6.60MG0H6	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSAC8.00MT	8.0	30	30	0	3.0	3.6	0.2
	CSTCC8.00MG0H6	8.0	On-chip	On-chip	0	3.0	3.6	0.3
Lead	CSA4.00MG040	4.0	100	100	0	3.0	3.6	0.5
	CST4.00MGW040	4.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA5.00MG040	5.0	100	100	0	3.0	3.6	0.5
	CST5.00MGW040	5.0	On-chip	On-chip	0	3.0	3.6	0.5
	CSA6.60MTZ	6.6	30	30	0	3.0	3.6	0.1
	CST6.60MTW	6.6	On-chip	On-chip	0	3.0	3.6	0.1
	CSA8.00MTZ	8.0	30	30	0	3.0	3.6	0.1
	CST8.00MTW	8.0	On-chip	On-chip	0	3.0	3.6	0.1

- Cautions**
1. Connect the oscillator as close to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the  $\mu$ PD703100A-33, 703100A-40, 703101A-33, 703102A-33 and the resonators.

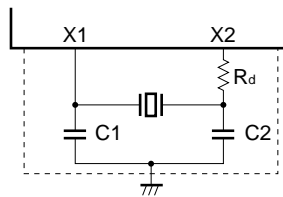
(ii) TDK Corporation ( $T_A = -40$  to  $+85^\circ\text{C}$ )



Type	Product Name	Oscillation Frequency $f_{xx}$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
			C1 (pF)	C2 (pF)	$R_d$ (k $\Omega$ )	MIN. (V)	MAX. (V)	$T_{OST}$ (ms)
TDK	CCR4.0MC3	4.0	On-chip	On-chip	0	3.0	3.6	0.17
	CCR5.0MC3	5.0	On-chip	On-chip	0	3.0	3.6	0.15
	CCR8.0MC5	8.0	On-chip	On-chip	0	3.0	3.6	0.11

- Cautions**
1. Connect the oscillator as close to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the  $\mu$ PD703100A-33, 703100A-40, 703101A-33, 703102A-33 and the resonators.

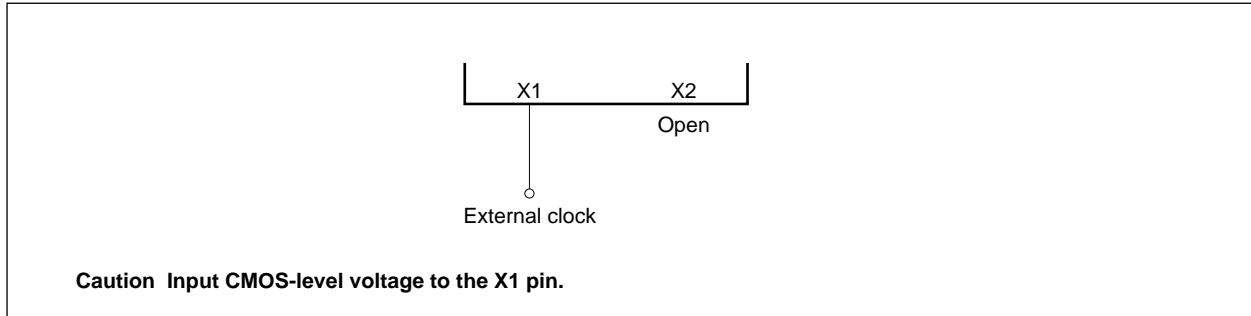
(iii) Kyocera Corporation ( $T_A = -20$  to  $+80^\circ\text{C}$ )



Type	Product Name	Oscillation Frequency $f_{xx}$ (MHz)	Recommended Circuit Constant			Oscillation Voltage Range		Oscillation Stabilization Time (MAX.)
			C1 (pF)	C2 (pF)	$R_d$ (k $\Omega$ )	MIN. (V)	MAX. (V)	$T_{OST}$ (ms)
Kyocera	PBRC5.00BR-A	5.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.00BR-A	6.0	On-chip	On-chip	0	3.0	3.6	0.06
	PBRC6.60BR-A	6.6	On-chip	On-chip	0	3.0	3.6	0.06

- Cautions**
1. Connect the oscillator as close to the X1 and X2 pins as possible.
  2. Do not wire any other signal lines in the area indicated by the broken lines.
  3. Thoroughly evaluate the matching between the  $\mu$ PD703100A-33, 703100A-40, 703101A-33, 703102A-33 and the resonators.

- (b) External clock input ( $T_A = -40$  to  $+70^\circ\text{C}$  ...  $\mu$ PD703100A-40,  
 $T_A = -40$  to  $+85^\circ\text{C}$  ...  $\mu$ PD703100A-33, 703101A-33, 703102A-33)



#### Cautions when turning on/off the power

The  $\mu$ PD703100A-33, 703100A-40, 703101A-33, and 703102A-33 are configured with power supply pins for the internal unit ( $V_{DD}$ ) and for an external pin ( $HV_{DD}$ ).

The operation guaranteed range is  $V_{DD} = HV_{DD} = 3.0$  to  $3.6$  V. The input and output state of ports may be undefined when the voltage exceeds this range.

DC Characteristics (T<sub>A</sub> = -40 to +70°C ...  $\mu$ PD703100A-40,  
 T<sub>A</sub> = -40 to +85°C ...  $\mu$ PD703100A-33,  $\mu$ PD703101A-33,  $\mu$ PD703102A-33,  
 V<sub>DD</sub> = HV<sub>DD</sub> = CV<sub>DD</sub> = 3.0 to 3.6 V, V<sub>SS</sub> = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V <sub>IH</sub>	Except <b>Note 1</b>	0.65HV <sub>DD</sub>		HV <sub>DD</sub> + 0.3	V	
		<b>Note 1</b>	0.8HV <sub>DD</sub>		HV <sub>DD</sub> + 0.3	V	
Input voltage, low	V <sub>IL</sub>	Except <b>Note 1</b> and <b>Note 2</b>	-0.5		0.2HV <sub>DD</sub>	V	
		<b>Note 1</b>	-0.5		0.15HV <sub>DD</sub>	V	
Clock input voltage, high	V <sub>XH</sub>	X1 pin	Direct mode	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
			PLL mode	0.8V <sub>DD</sub>		V <sub>DD</sub> + 0.3	V
Clock input voltage, low	V <sub>XL</sub>	X1 pin	Direct mode	-0.3		0.15V <sub>DD</sub>	V
			PLL mode	-0.3		0.15V <sub>DD</sub>	V
Schmitt-triggered input threshold voltage	HV <sub>T</sub> <sup>+</sup>	<b>Note 1</b> , rising edge		2.0		V	
	HV <sub>T</sub> <sup>-</sup>	<b>Note 1</b> , falling edge		1.0		V	
Schmitt-triggered input hysteresis width	HV <sub>T</sub> <sup>+</sup> -HV <sub>T</sub> <sup>-</sup>	<b>Note 1</b>	0.3			V	
Output voltage, high	V <sub>OH</sub>	I <sub>OH</sub> = -1.0 mA	0.8HV <sub>DD</sub>			V	
Output voltage, low	V <sub>OL</sub>	I <sub>OL</sub> = 2.5 mA			0.15HV <sub>DD</sub>	V	
Input leakage current, high	I <sub>LIH</sub>	V <sub>I</sub> = HV <sub>DD</sub> and except <b>Note 2</b>			10	μA	
Input leakage current, low	I <sub>LIL</sub>	V <sub>I</sub> = 0 V and except <b>Note 2</b>			-10	μA	
Output leakage current, high	I <sub>LOH</sub>	V <sub>O</sub> = HV <sub>DD</sub>			10	μA	
Output leakage current, low	I <sub>LOL</sub>	V <sub>O</sub> = 0 V			-10	μA	

**Notes 1.** P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3, P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/SCK2, P104/INTP120/TC0 to P107/INTP123/TC3, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/SCK3, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, MODE0 to MODE2, RESET

**2.** When the P70/ANI0 to P77/ANI7 pins are used as analog input.

**Remarks 1.** TYP. values are reference values for when T<sub>A</sub> = 25°C, V<sub>DD</sub> = CV<sub>DD</sub> = HV<sub>DD</sub> = 3.3 V.

**2.** Direct mode: f<sub>x</sub> = 2 to 40 MHz ( $\mu$ PD703100A-40)

★ f<sub>x</sub> = 2 to 33 MHz ( $\mu$ PD703100A-33, 703101A-33, 703102A-33)

PLL mode: f<sub>x</sub> = 20 to 40 MHz ( $\mu$ PD703100A-40)

★ f<sub>x</sub> = 20 to 33 MHz ( $\mu$ PD703100A-33, 703101A-33, 703102A-33)

DC Characteristics ( $T_A = -40$  to  $+70^\circ\text{C}$  ...  $\mu$ PD703100A-40,  
 $T_A = -40$  to  $+85^\circ\text{C}$  ...  $\mu$ PD703100A-33,  $\mu$ PD703101A-33,  $\mu$ PD703102A-33,  
 $V_{DD} = CV_{DD} = HV_{DD} = 3.0$  to  $3.6$  V,  $V_{SS} = 0$  V)

Parameter		Symbol	Condition		MIN.	TYP.	MAX.	Unit
★ Power supply current	During normal operation	$I_{DD1}$				$2.5 \times f_x$	$4.0 \times f_x + 5.0$	mA
	HALT mode	$I_{DD2}$				$1.2 \times f_x$	$2.7 \times f_x$	mA
	IDLE mode	$I_{DD3}$				2.0	5.0	mA
	STOP mode	$I_{DD4}$	PLL mode	$\mu$ PD703100A-40		1.5	5.0	mA
	$\mu$ PD703100A-33, 703101A-33, 703102A-33				5.0	150	$\mu$ A	

**Remarks 1.** TYP. values are reference values for when  $T_A = 25^\circ\text{C}$ ,  $V_{DD} = CV_{DD} = HV_{DD} = 3.3$  V.

**2.** Direct mode:  $f_x = 2$  to  $40$  MHz ( $\mu$ PD703100A-40)

★  $f_x = 2$  to  $33$  MHz ( $\mu$ PD703100A-33, 703101A-33, 703102A-33)

PLL mode:  $f_x = 20$  to  $40$  MHz ( $\mu$ PD703100A-40)

★  $f_x = 20$  to  $33$  MHz ( $\mu$ PD703100A-33, 703101A-33, 703102A-33)

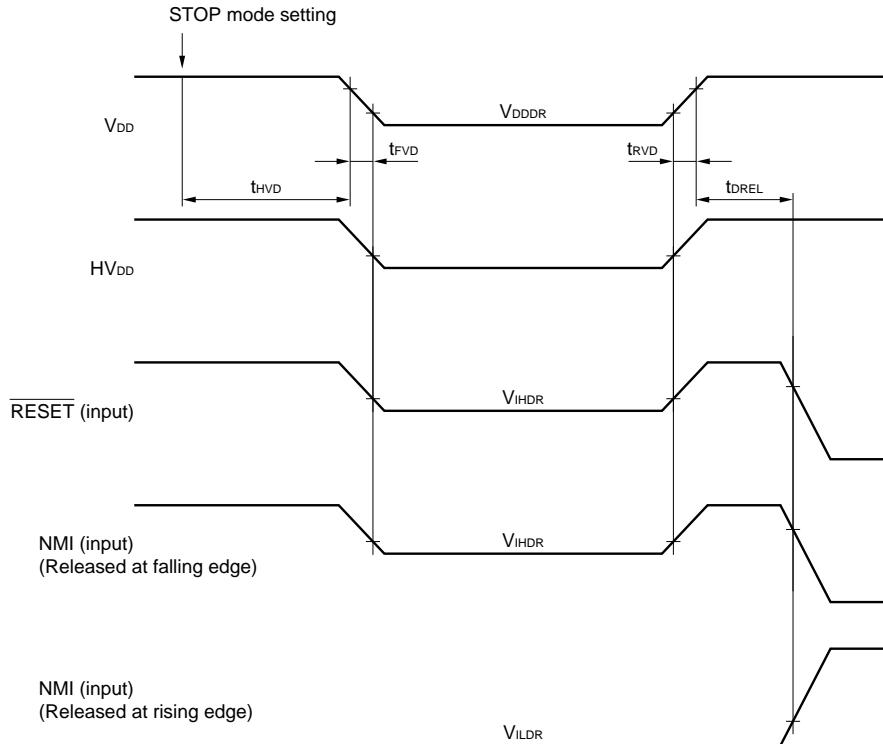
**Data Retention Characteristics** ( $T_A = -40$  to  $+70^\circ\text{C}$  ...  $\mu$ PD703100A-40,  
 $T_A = -40$  to  $+85^\circ\text{C}$  ...  $\mu$ PD703100A-33,  $\mu$ PD703101A-33,  $\mu$ PD703102A-33)

★

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	$V_{DDDR}$	STOP mode, $V_{DD} = V_{DDDR}$	1.5		3.6	V
Data retention current	$I_{DDDR}$	$V_{DD} = V_{DDDR}$	$\mu$ PD703100A-40		5.0	mA
			$\mu$ PD703100A-33, 703101A-33, 703102A-33		150	$\mu$ A
Power supply voltage rise time	$t_{RVD}$		200			$\mu$ s
Power supply voltage fall time	$t_{FVD}$		200			$\mu$ s
Power supply voltage hold time (from STOP mode setting)	$t_{HVD}$		0			ms
STOP mode release signal input time	$t_{DREL}$		0			ns
Data retention high-level input voltage	$V_{IHDR}$	<b>Note</b>	$0.8HV_{DDDR}$		$V_{DDDR}$	V
Data retention low-level input voltage	$V_{ILDR}$	<b>Note</b>	0		$0.2V_{DDDR}$	V

**Note** P04/INTP100/ $\overline{\text{DMARQ0}}$  to P07/INTP103/ $\overline{\text{DMARQ3}}$ , P14/INTP110/ $\overline{\text{DMAAK0}}$  to P17/INTP113/ $\overline{\text{DMAAK3}}$ , P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/SCK2, P104/INTP120/TC0 to P107/INTP123/TC3, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/SCK3, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, MODE0 to MODE2, RESET

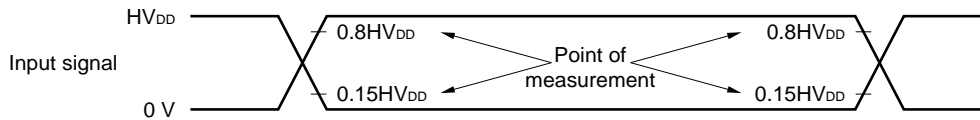
**Remark** TYP. values are reference values for when  $T_A = 25^\circ\text{C}$ .



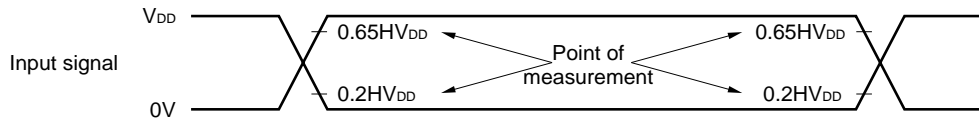
AC Characteristics ( $T_A = -40$  to  $+70^\circ\text{C}$  ...  $\mu$ PD703100A-40,  
 $T_A = -40$  to  $+85^\circ\text{C}$  ...  $\mu$ PD703100A-33,  $\mu$ PD703101A-33,  $\mu$ PD703102A-33,  
 $V_{DD} = HV_{DD} = CV_{DD} = 3.0$  to  $3.6$  V,  $V_{SS} = 0$  V, output pin load capacitance:  $C_L = 50$  pF)

AC test input measurement points

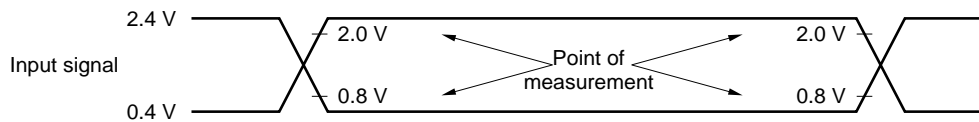
- (a) P04/INTP100/DMARQ0 to P07/INTP103/DMARQ3, P14/INTP110/DMAAK0 to P17/INTP113/DMAAK3, P34/INTP130, P35/INTP131/SO2, P36/INTP132/SI2, P37/INTP133/SCK2, P104/INTP120/TC0 to P107/INTP123/TC3, P114/INTP140, P115/INTP141/SO3, P116/INTP142/SI3, P117/INTP143/SCK3, P124/INTP150 to P126/INTP152, P127/INTP153/ADTRG, P02/TCLR10, P12/TCLR11, P32/TCLR13, P102/TCLR12, P112/TCLR14, P122/TCLR15, P03/TI10, P13/TI11, P33/TI13, P103/TI12, P113/TI14, P123/TI15, P20/NMI, P23/RXD0/SI0, P24/SCK0, P26/RXD1/SI1, P27/SCK1, MODE0 to MODE2, RESET



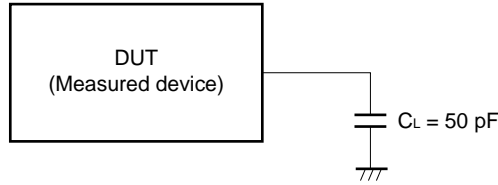
- (b) Pins other than those listed in (a) above



AC test output measurement points



Load condition

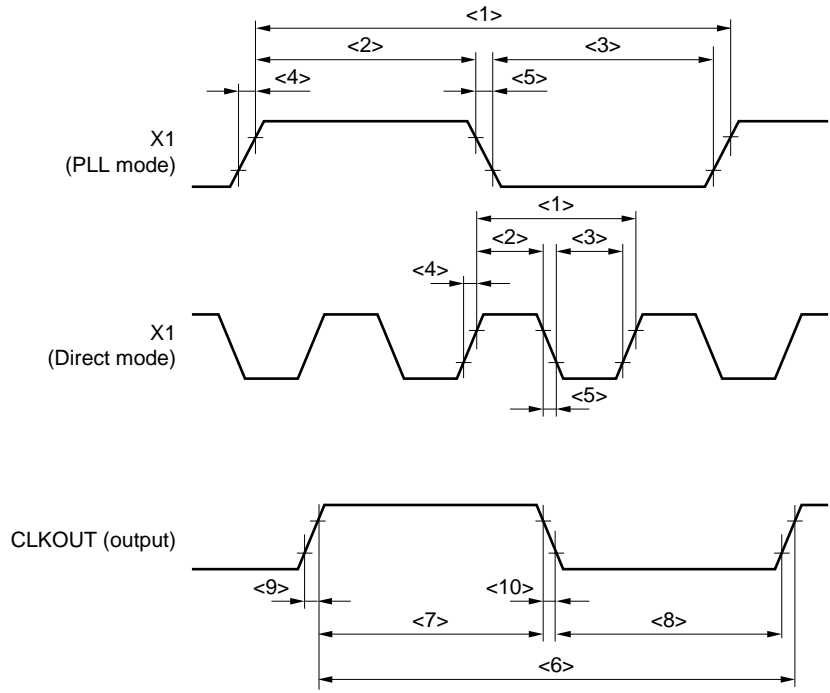


**Caution** In cases where the load capacitance is greater than 50 pF due to the circuit configuration, insert a buffer or other element to reduce the device's load capacitance to below 50 pF.

(1) Clock timing

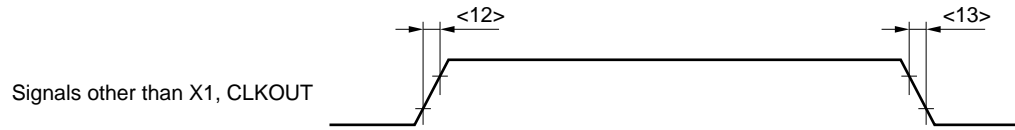
Parameter	Symbol	Conditions	MIN.	MAX.	Unit	
X1 input cycle	<1>	Direct mode	μPD703100A-40	12.5	250	ns
			μPD703100A-33, 703101A-33, 703102A-33,	15	250	ns
		PLL mode	μPD703100A-40	125	250	ns
			μPD703100A-33, 703101A-33, 703102-A33	150	250	ns
X1 input high-level width	<2>	Direct mode	5		ns	
		PLL mode	50		ns	
X1 input low-level width	<3>	Direct mode	5		ns	
		PLL mode	50		ns	
X1 input rise time	<4>	Direct mode		4	ns	
		PLL mode		10	ns	
X1 input fall time	<5>	Direct mode		4	ns	
		PLL mode		10	ns	
CLKOUT output cycle	<6>	μPD703100A-40	25	500	ns	
		μPD703100A-33, 703101A-33, 703102A-33	30	500	ns	
CLKOUT input high-level width	<7>	t <sub>WKH</sub>	0.5T – 7		ns	
CLKOUT input low-level width	<8>	t <sub>WKL</sub>	0.5T – 4		ns	
CLKOUT input rise time	<9>	t <sub>KR</sub>		5	ns	
CLKOUT input fall time	<10>	t <sub>KF</sub>		5	ns	

**Remark** T = t<sub>CYK</sub>



(2) Output waveform (other than X1, CLKOUT)

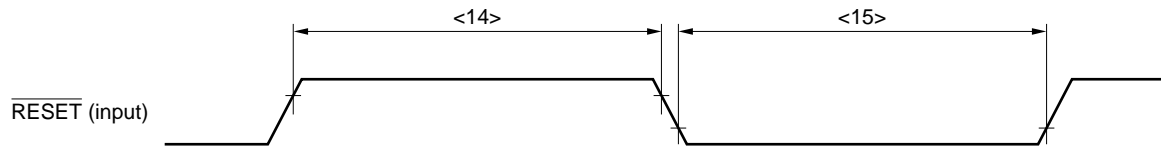
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output rise time	<12>	t <sub>OR</sub>			5	ns
Output fall time	<13>	t <sub>OF</sub>			5	ns



(3) Reset timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
RESET high-level width	<14>	t <sub>WRSH</sub>		500		ns
RESET low-level width	<15>	t <sub>WRSL</sub>	When power supply is on, and STOP mode has been released	500 + T <sub>OS</sub>		ns
			Other than when power supply is on, and STOP mode has been released	500		ns

**Remark** T<sub>OS</sub>: Oscillation stabilization time



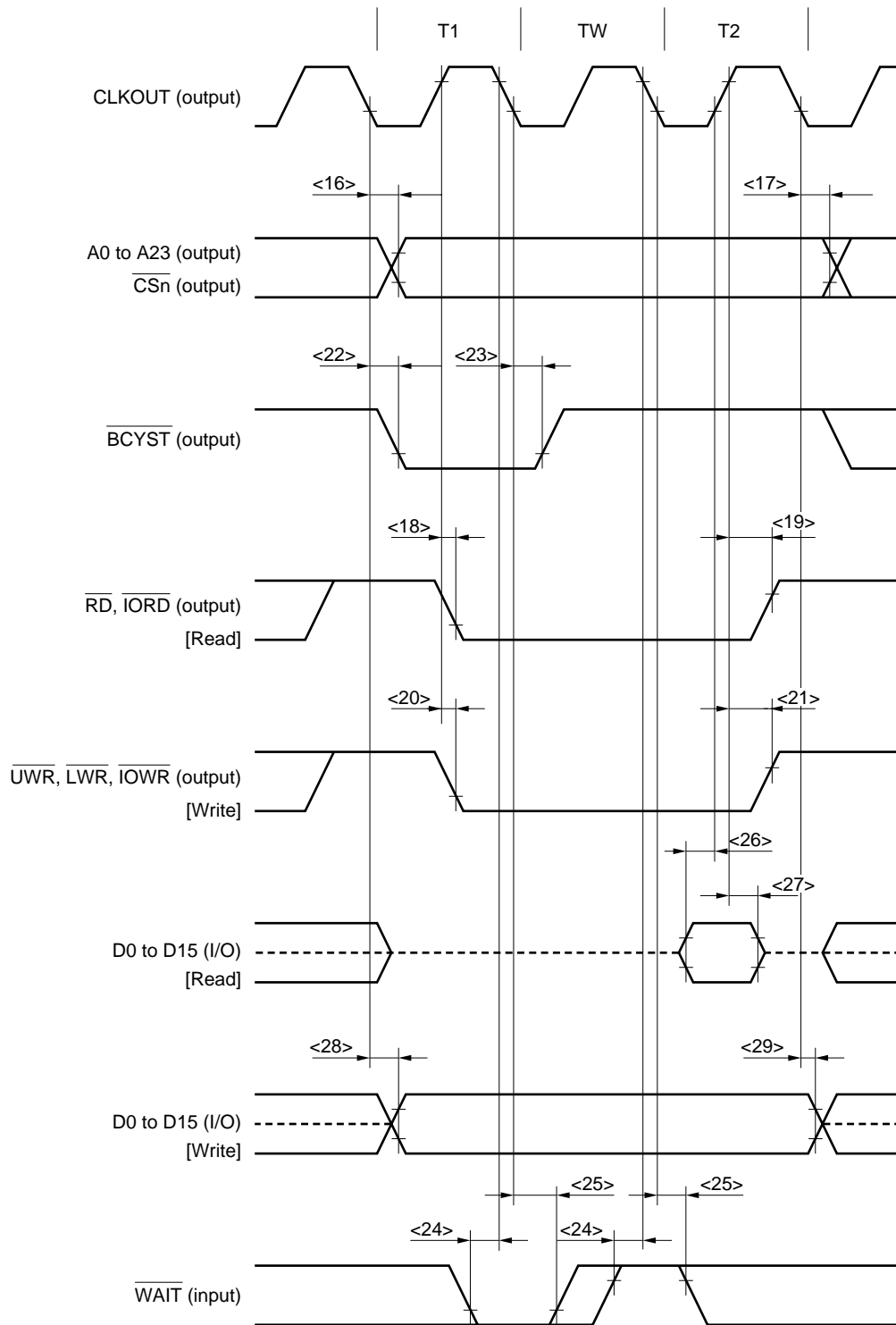
(4) SRAM, external ROM, external I/O access timing

(a) Access timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Address, $\overline{CSn}$ output delay time (from CLKOUT↓)	<16> $t_{DKA}$		2	10	ns
Address, $\overline{CSn}$ output hold time (from CLKOUT↓)	<17> $t_{HKA}$		2	10	ns
$\overline{RD}$ , $\overline{IORD}$ ↓ delay time (from CLKOUT↑)	<18> $t_{DKRDL}$		2	14	ns
$\overline{RD}$ , $\overline{IORD}$ ↑ delay time (from CLKOUT↑)	<19> $t_{HKRDH}$		2	14	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↓ delay time (from CLKOUT↑)	<20> $t_{DKWRL}$		2	10	ns
$\overline{UWR}$ , $\overline{LWR}$ , $\overline{IOWR}$ ↑ delay time (from CLKOUT↑)	<21> $t_{HKWRH}$		2	10	ns
$\overline{BCYST}$ ↓ delay time (from CLKOUT↓)	<22> $t_{DKBSL}$		2	10	ns
$\overline{BCYST}$ ↑ delay time (from CLKOUT↓)	<23> $t_{HKBSH}$		2	10	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	<24> $t_{SWK}$		10		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	<25> $t_{HKW}$		2		ns
Data input setup time (to CLKOUT↑)	<26> $t_{SKID}$		10		ns
Data input hold time (from CLKOUT↑)	<27> $t_{HKID}$		2		ns
Data output delay time (from CLKOUT↓)	<28> $t_{DKOD}$		2	10	ns
Data output hold time (from CLKOUT↓)	<29> $t_{HKOD}$		2	10	ns

- Remarks**
1. Maintain at least one of the data input hold times, either  $t_{HKID}$  or  $t_{HRDID}$ .
  2. n = 0 to 7

(a) Access timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3. n = 0 to 7

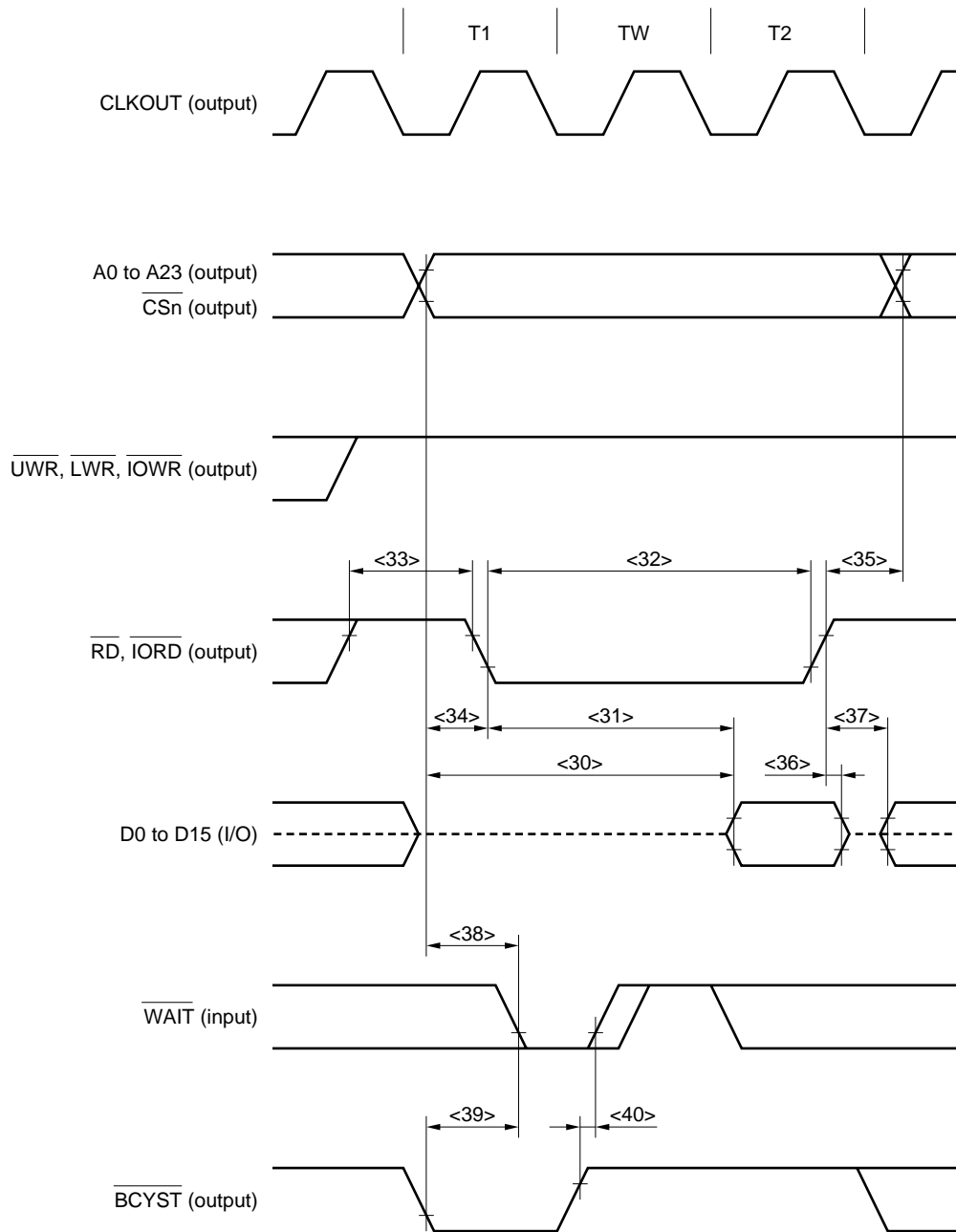
(b) Read timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to address)	<30> $t_{SAID}$			$(1.5 + w_D + w) T - 20$	ns
Data input setup time (to $\overline{RD}$ )	<31> $t_{SRDID}$			$(1 + w_D + w) T - 24$	ns
$\overline{RD}$ , $\overline{IORD}$ low-level width	<32> $t_{WRDL}$		$(1 + w_D + w) T - 10$		ns
$\overline{RD}$ , $\overline{IORD}$ high-level width	<33> $t_{WRDH}$		$T - 10$		ns
Delay time from address, $\overline{CSn}$ to $\overline{RD}$ , $\overline{IORD}\downarrow$	<34> $t_{DARD}$		$0.5T - 10$		ns
Delay time from $\overline{RD}$ , $\overline{IORD}\uparrow$ to address	<35> $t_{DRDA}$		$(0.5 + i) T - 5$		ns
Data input hold time (from $\overline{RD}$ , $\overline{IORD}\uparrow$ )	<36> $t_{HRDID}$		0		ns
Delay time from $\overline{RD}$ , $\overline{IORD}\uparrow$ to data output	<37> $t_{DRDOD}$		$(0.5 + i) T - 10$		ns
$\overline{WAIT}$ setup time (to address)	<38> $t_{SAW}$	<b>Note</b>		$T - 20$	ns
$\overline{WAIT}$ setup time (to $\overline{BCYST}\downarrow$ )	<39> $t_{SBSW}$	<b>Note</b>		$T - 20$	ns
$\overline{WAIT}$ hold time (to $\overline{BCYST}\uparrow$ )	<40> $t_{HBSW}$	<b>Note</b>	0		ns

**Note** For the first  $\overline{WAIT}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

- Remarks**
1.  $T = t_{CYK}$
  2.  $w$ : Number of waits due to  $\overline{WAIT}$
  3.  $w_D$ : Number of waits due to the DWC1 and DWC2 registers
  4.  $i$ : Number of idle states that are inserted when a write cycle follows a read cycle
  5. Maintain at least one of the data input hold times, either  $t_{HKID}$  or  $t_{HRDID}$ .
  6.  $n = 0$  to 7

(b) Read timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3.  $n = 0$  to 7

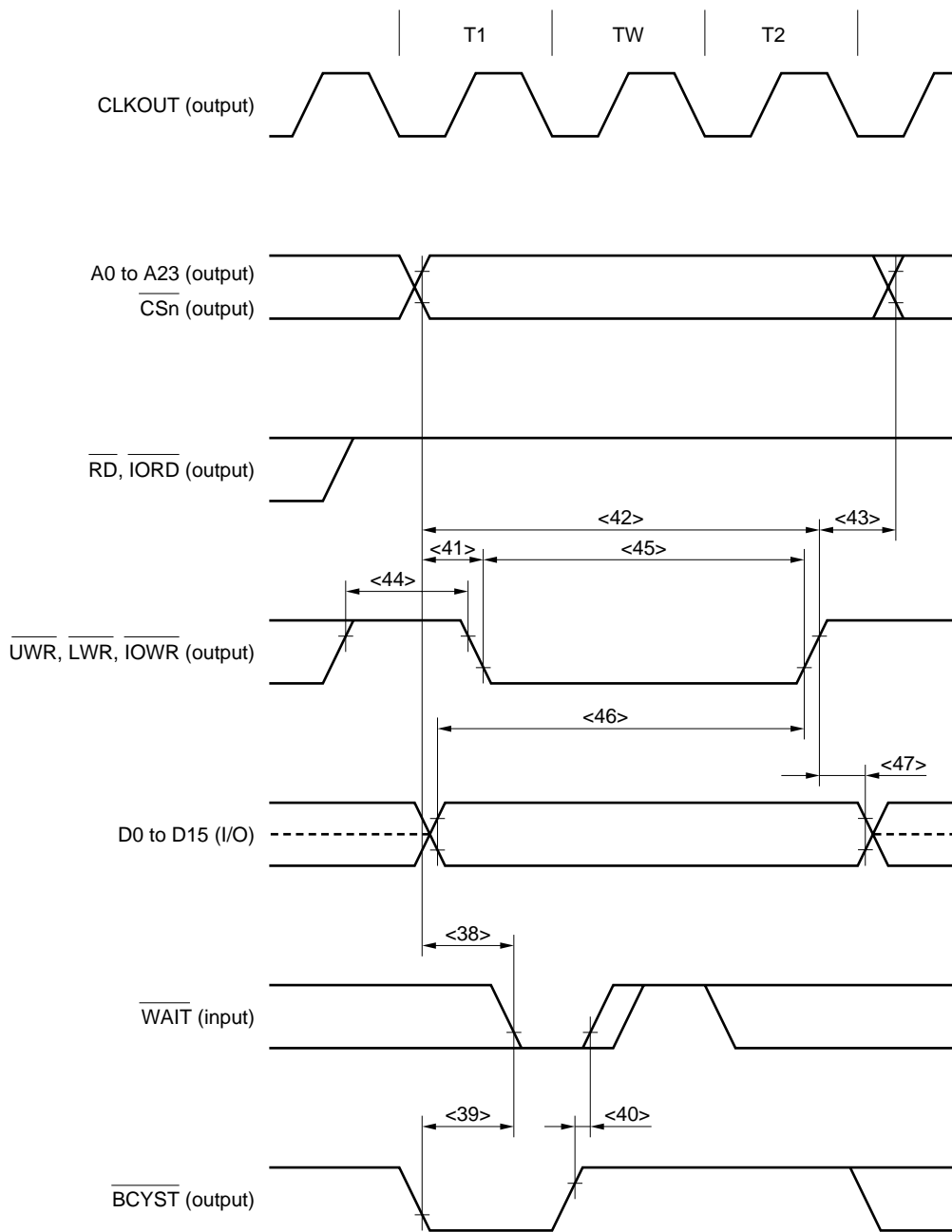
(c) Write timing (SRAM, external ROM, external I/O) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to address)	<38> $t_{\text{SAW}}$	<b>Note</b>		$T - 20$	ns
$\overline{\text{WAIT}}$ setup time (to $\overline{\text{BCYST}}\downarrow$ )	<39> $t_{\text{SBSW}}$	<b>Note</b>		$T - 20$	ns
$\overline{\text{WAIT}}$ hold time (from $\overline{\text{BCYST}}\uparrow$ )	<40> $t_{\text{HBSW}}$	<b>Note</b>	0		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\downarrow$	<41> $t_{\text{DAWR}}$		$0.5T - 5$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<42> $t_{\text{SAWR}}$		$(1.5 + w_D + w) T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ to address	<43> $t_{\text{DWRA}}$		$0.5T - 5$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ high-level width	<44> $t_{\text{WWRH}}$		$T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}$ low-level width	<45> $t_{\text{WWRL}}$		$(1 + w_D + w) T - 10$		ns
Data output setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<46> $t_{\text{SODWR}}$		$(1.5 + w_D + w) T - 10$		ns
Data output hold time (from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ , $\overline{\text{IOWR}}\uparrow$ )	<47> $t_{\text{HWROD}}$		$0.5T - 5$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

- Remarks**
1.  $T = t_{\text{CYK}}$
  2.  $w$ : Number of waits due to  $\overline{\text{WAIT}}$
  3.  $w_D$ : Number of waits due to the DWC1 and DWC2 registers
  4.  $n = 0$  to 7

(c) Write timing (SRAM, external ROM, external I/O) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero.
  2. The broken lines indicate high impedance.
  3. n = 0 to 7

(d) DMA flyby transfer timing (SRAM → external I/O transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24>	t <sub>SWK</sub>	10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25>	t <sub>HKW</sub>	2		ns
$\overline{\text{RD}}$ low-level width	<32>	t <sub>WRDL</sub>	$(1 + w_D + w_F + w) T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33>	t <sub>WRDH</sub>	$T - 10$		ns
Delay time from address, $\overline{\text{CS}}_n$ to $\overline{\text{RD}}\downarrow$	<34>	t <sub>DARD</sub>	$0.5T - 5$		ns
Delay time from $\overline{\text{RD}}\uparrow$ to address	<35>	t <sub>DRDA</sub>	$(0.5 + i) T - 5$		ns
Delay time from $\overline{\text{RD}}\uparrow$ to data output	<37>	t <sub>DRDOD</sub>	$(0.5 + i) T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	t <sub>SAW</sub>	<b>Note</b>	$T - 20$	ns
$\overline{\text{WAIT}}$ setup time (to BCYST↓)	<39>	t <sub>SBSW</sub>	<b>Note</b>	$T - 20$	ns
$\overline{\text{WAIT}}$ hold time (from BCYST↑)	<40>	t <sub>HBSW</sub>	<b>Note</b>	0	ns
Delay time from address to $\overline{\text{IOWR}}\downarrow$	<41>	t <sub>DAWR</sub>	$0.5T - 5$		ns
Address setup time (to $\overline{\text{IOWR}}\uparrow$ )	<42>	t <sub>SAWR</sub>	$(1.5 + w_D + w) T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<43>	t <sub>DWRA</sub>	$0.5T - 5$		ns
$\overline{\text{IOWR}}$ high-level width	<44>	t <sub>WWRH</sub>	$T - 10$		ns
$\overline{\text{IOWR}}$ low-level width	<45>	t <sub>WWRL</sub>	$(1 + w_D + w) T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{RD}}\uparrow$	<48>	t <sub>DWRRD</sub>	W <sub>F</sub> = 0	0	ns
			W <sub>F</sub> = 1	$T - 10$	ns
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{IOWR}}\downarrow$	<49>	t <sub>DDAWR</sub>	$0.5T - 10$		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{DMAAK}}_m\uparrow$	<50>	t <sub>DWRDA</sub>	$(0.5 + w_F) T - 10$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

**Remarks 1.** T = t<sub>cyk</sub>

**2.** w: Number of waits due to  $\overline{\text{WAIT}}$

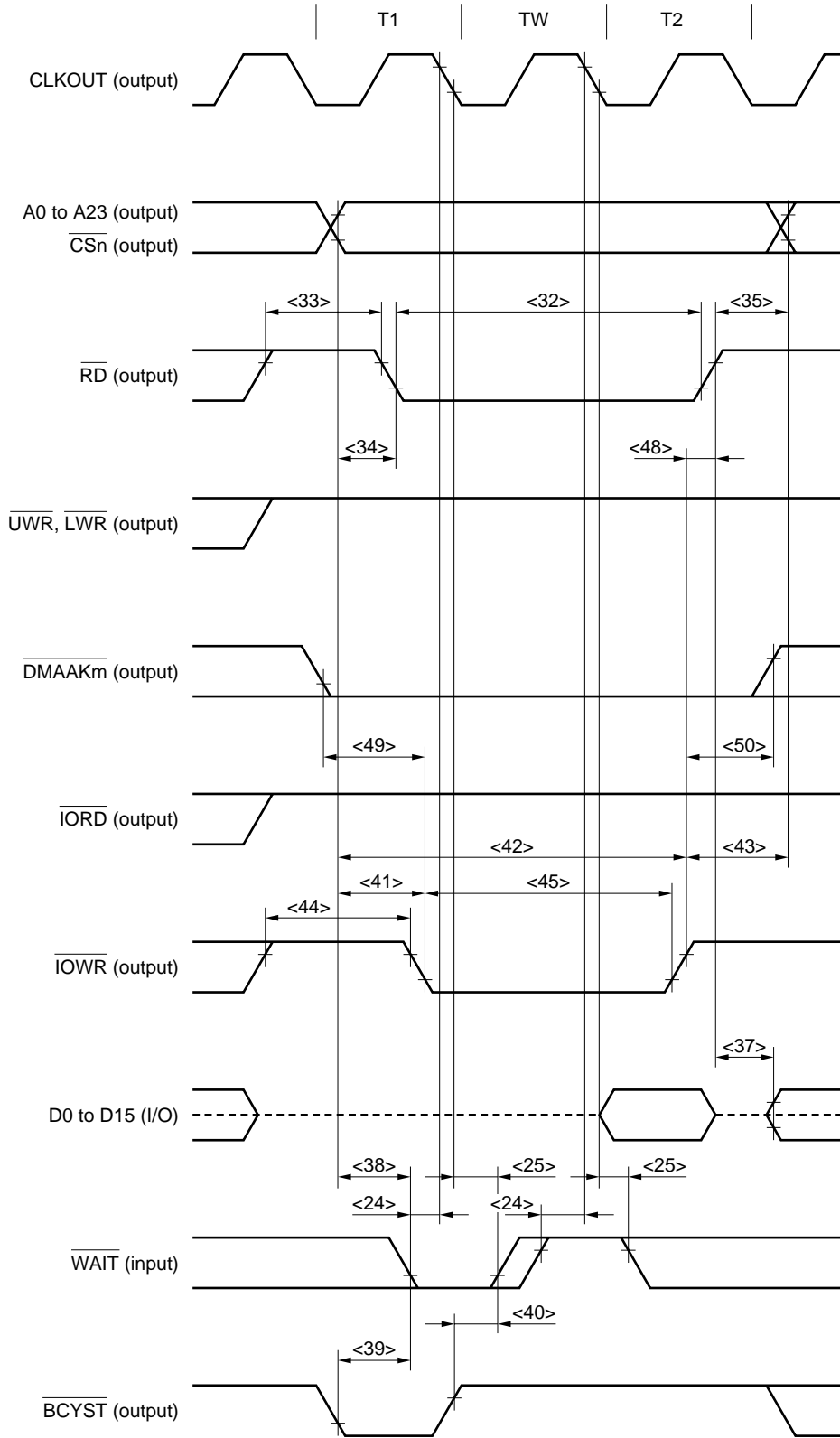
**3.** w<sub>D</sub>: Number of waits due to the DWC1 and DWC2 registers

**4.** w<sub>F</sub>: Number of waits that are inserted for a source-side access during a DMA flyby transfer

**5.** i: Number of idle states that are inserted when a write cycle follows a read cycle

**6.** n = 0 to 7, m = 0 to 3

(d) DMA flyby transfer timing (SRAM  $\rightarrow$  external I/O transfer) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and  $w_F = 0$ .
  2. The broken lines indicate high impedance.
  3.  $n = 0$  to 7,  $m = 0$  to 3

(e) DMA flyby transfer timing (external I/O → SRAM transfer) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24>	t <sub>SWK</sub>	10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25>	t <sub>HKW</sub>	2		ns
$\overline{\text{IORD}}$ low-level width	<32>	t <sub>WRDL</sub>	$(1 + w_D + w_F + w) T - 10$		ns
$\overline{\text{IORD}}$ high-level width	<33>	t <sub>WRDH</sub>	$T - 10$		ns
Delay time from address, CS <sub>n</sub> to IORD↓	<34>	t <sub>DARD</sub>	$0.5T - 5$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to address	<35>	t <sub>DRDA</sub>	$(0.5 + i) T - 5$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to data output	<37>	t <sub>DRDOD</sub>	$(0.5 + i) T - 10$		ns
$\overline{\text{WAIT}}$ setup time (to address)	<38>	t <sub>SAW</sub>	<b>Note</b>	$T - 20$	ns
$\overline{\text{WAIT}}$ setup time (to BCYST↓)	<39>	t <sub>SBSW</sub>	<b>Note</b>	$T - 20$	ns
$\overline{\text{WAIT}}$ hold time (from BCYST↑)	<40>	t <sub>HBSW</sub>	<b>Note</b>	0	ns
Delay time from address to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}\downarrow$	<41>	t <sub>DAWR</sub>	$0.5T - 5$		ns
Address setup time (to $\overline{\text{UWR}}$ , $\overline{\text{LWR}}\uparrow$ )	<42>	t <sub>SAWR</sub>	$(1.5 + w_D + w) T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ to address	<43>	t <sub>DWRA</sub>	$0.5T - 5$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ high-level width	<44>	t <sub>WWRH</sub>	$T - 10$		ns
$\overline{\text{UWR}}$ , $\overline{\text{LWR}}$ low-level width	<45>	t <sub>WWRL</sub>	$(1 + w_D + w) T - 10$		ns
Delay time from $\overline{\text{UWR}}$ , $\overline{\text{LWR}}\uparrow$ to $\overline{\text{IORD}}\uparrow$	<48>	t <sub>DWRRD</sub>	W <sub>F</sub> = 0	0	ns
			W <sub>F</sub> = 1	$T - 10$	ns
Delay time from $\overline{\text{DMAAK}}_m\downarrow$ to $\overline{\text{IORD}}\downarrow$	<51>	t <sub>DDARD</sub>	$0.5T - 10$		ns
Delay time from $\overline{\text{IORD}}\uparrow$ to $\overline{\text{DMAAK}}_m\uparrow$	<52>	t <sub>DRDDA</sub>	$0.5T - 10$		ns

**Note** For the first  $\overline{\text{WAIT}}$  sampling when the number of waits due to the DWC1 and DWC2 registers is zero.

**Remarks 1.**  $T = t_{CYK}$

**2.** w: Number of waits due to  $\overline{\text{WAIT}}$

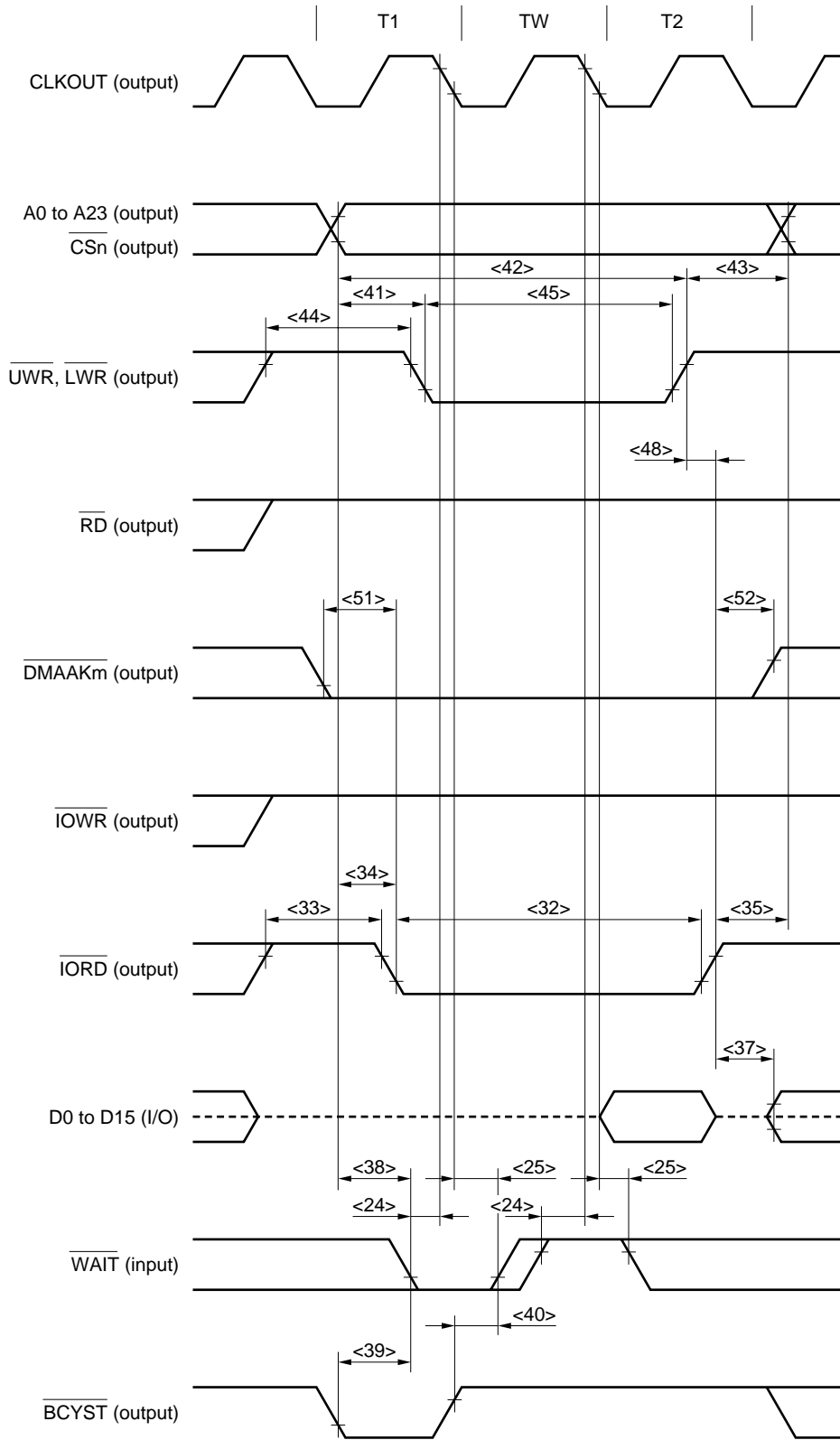
**3.** w<sub>D</sub>: Number of waits due to the DWC1 and DWC2 registers

**4.** w<sub>F</sub>: Number of waits that are inserted for a source-side access during a DMA flyby transfer

**5.** i: Number of idle states that are inserted when a write cycle follows a read cycle

**6.** n = 0 to 7, m = 0 to 3

(e) DMA flyby transfer timing (external I/O  $\rightarrow$  SRAM transfer) (2/2)



- Remarks**
1. This is the timing when the number of waits due to the DWC1 and DWC2 registers is zero and  $w_F = 0$ .
  2. The broken lines indicate high impedance.
  3.  $n = 0$  to 7,  $m = 0$  to 3

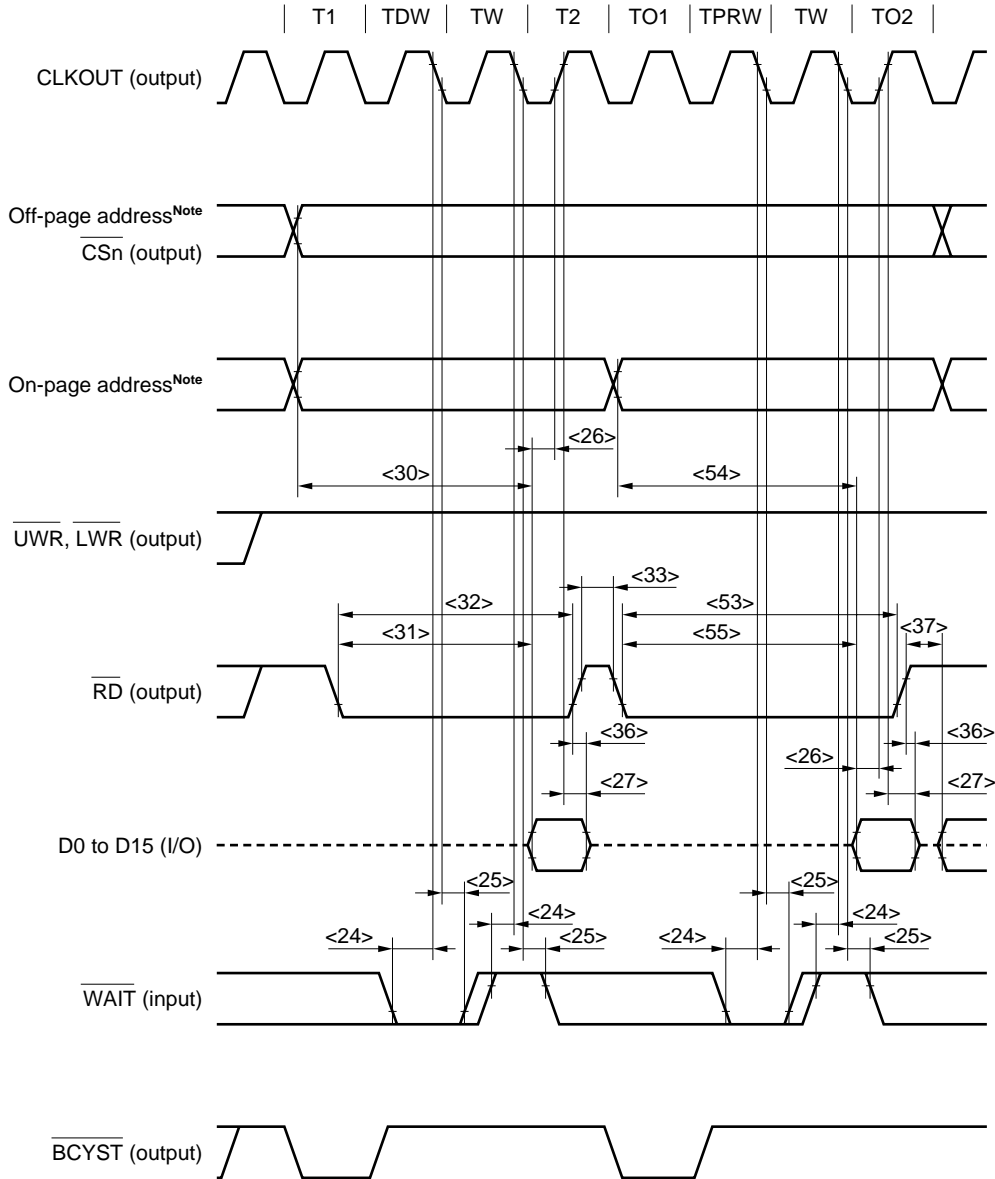
(5) Page ROM access timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24> $t_{\text{SWK}}$		10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25> $t_{\text{HKW}}$		2		ns
Data input setup time (to CLKOUT↑)	<26> $t_{\text{SKID}}$		10		ns
Data input hold time (from CLKOUT↑)	<27> $t_{\text{HKID}}$		2		ns
Off-page data input setup time (to address)	<30> $t_{\text{SAID}}$			$(1.5 + w_D + w) T - 20$	ns
Off-page data input setup time (to $\overline{\text{RD}}$ )	<31> $t_{\text{SRDID}}$			$(1 + w_D + w) T - 24$	ns
Off-page $\overline{\text{RD}}$ low-level width	<32> $t_{\text{WRDL}}$		$(1 + w_D + w) T - 10$		ns
$\overline{\text{RD}}$ high-level width	<33> $t_{\text{WRDH}}$		$0.5T - 10$		ns
Data input hold time (from $\overline{\text{RD}}$ )	<36> $t_{\text{HRDID}}$		0		ns
Delay time from $\overline{\text{RD}}\uparrow$ to data output	<37> $t_{\text{DRDOD}}$		$(0.5 + i) T - 10$		ns
On-page $\overline{\text{RD}}$ low-level width	<53> $t_{\text{WORDL}}$		$(1.5 + w_{\text{PR}} + w) T - 10$		ns
On-page data input setup time (to address)	<54> $t_{\text{SOAID}}$			$(1.5 + w_{\text{PR}} + w) T - 20$	ns
On-page data input setup time (to $\overline{\text{RD}}$ )	<55> $t_{\text{SORID}}$			$(1.5 + w_{\text{PR}} + w) T - 24$	ns

Remarks 1.  $T = t_{\text{CYK}}$

2.  $w$ : Number of waits due to  $\overline{\text{WAIT}}$
3.  $w_D$ : Number of waits due to the DWC1 and DWC2 registers
4.  $w_{\text{PR}}$ : Number of waits due to the PRC register
5.  $i$ : Number of idle states that are inserted when a write cycle follows a read cycle
6. Maintain at least one of the data input hold times  $t_{\text{HKID}}$  and  $t_{\text{HRDID}}$ .

(5) Page ROM access timing (2/2)



**Note** The on-page and off-page addresses are as follows.

PRC Register			On-Page Addresses	Off-Page Addresses
MA5	MA4	MA3		
0	0	0	A0, A1	A2 to A23
0	0	1	A0 to A2	A3 to A23
0	1	1	A0 to A3	A4 to A23
1	1	1	A0 to A4	A5 to A23

- Remarks**
- This is the timing for the following case.  
 Number of waits due to the DWC1 and DWC2 registers (TDW): 1  
 Number of waits due to the PRC register (TPRW): 1
  - The broken lines indicate high impedance.
  - n = 0 to 7

(6) DRAM access timing

(a) Read timing (high-speed page DRAM access, normal access: off-page) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24> $t_{\text{SWK}}$		10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25> $t_{\text{HKW}}$		2		ns
Data input setup time (to CLKOUT↑)	<26> $t_{\text{SKID}}$		10		ns
Data input hold time (from CLKOUT↑)	<27> $t_{\text{HKID}}$		2		ns
Delay time from $\overline{\text{OE}}\uparrow$ to data output	<37> $t_{\text{DRDOD}}$		$(0.5 + i) T - 10$		ns
Row address setup time	<56> $t_{\text{ASR}}$		$(0.5 + \text{WRP}) T - 10$		ns
Row address hold time	<57> $t_{\text{RAH}}$		$(0.5 + \text{WRH}) T - 10$		ns
Column address setup time	<58> $t_{\text{ASC}}$		$0.5T - 10$		ns
Column address hold time	<59> $t_{\text{CAH}}$		$(1.5 + \text{WDA} + \text{w}) T - 10$		ns
Read/write cycle time	<60> $t_{\text{RC}}$		$(3 + \text{WRP} + \text{WRH} + \text{WDA} + \text{w}) T - 10$		ns
$\overline{\text{RAS}}$ precharge time	<61> $t_{\text{RP}}$		$(0.5 + \text{WRP}) T - 5$		ns
$\overline{\text{RAS}}$ pulse time	<62> $t_{\text{RAS}}$		$(2.5 + \text{WRH} + \text{WDA} + \text{w}) T - 10$		ns
$\overline{\text{RAS}}$ hold time	<63> $t_{\text{RSH}}$		$(1.5 + \text{WDA} + \text{w}) T - 10$		ns
Column address read time for $\overline{\text{RAS}}$	<64> $t_{\text{RAL}}$		$(2 + \text{WDA} + \text{w}) T - 10$		ns
$\overline{\text{CAS}}$ pulse width	<65> $t_{\text{CAS}}$		$(1 + \text{WDA} + \text{w}) T - 10$		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66> $t_{\text{CRP}}$		$(1 + \text{WRP}) T - 10$		ns
$\overline{\text{CAS}}$ hold time	<67> $t_{\text{CSH}}$		$(2 + \text{WRH} + \text{WDA} + \text{w}) T - 10$		ns
$\overline{\text{WE}}$ setup time	<68> $t_{\text{RCS}}$		$(2 + \text{WRP} + \text{WRH}) T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}\uparrow$ )	<69> $t_{\text{RRH}}$		$0.5T - 10$		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}\uparrow$ )	<70> $t_{\text{RCH}}$		$T - 10$		ns
$\overline{\text{CAS}}$ precharge time	<71> $t_{\text{CPN}}$		$(2 + \text{WRP} + \text{WRH}) T - 5$		ns
Output enable access time	<72> $t_{\text{OEA}}$			$(2 + \text{WRP} + \text{WRH} + \text{WDA} + \text{w}) T - 20$	ns
$\overline{\text{RAS}}$ access time	<73> $t_{\text{RAC}}$			$(2 + \text{WRH} + \text{WDA} + \text{w}) T - 20$	ns
Access time from column address	<74> $t_{\text{AA}}$			$(1.5 + \text{WDA} + \text{w}) T - 20$	ns
$\overline{\text{CAS}}$ access time	<75> $t_{\text{CAC}}$			$(1 + \text{WDA} + \text{w}) T - 20$	ns

Remarks 1.  $T = t_{\text{CYK}}$

2. w: Number of waits due to  $\overline{\text{WAIT}}$

3. WRP: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

4. WRH: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

5. WDA: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

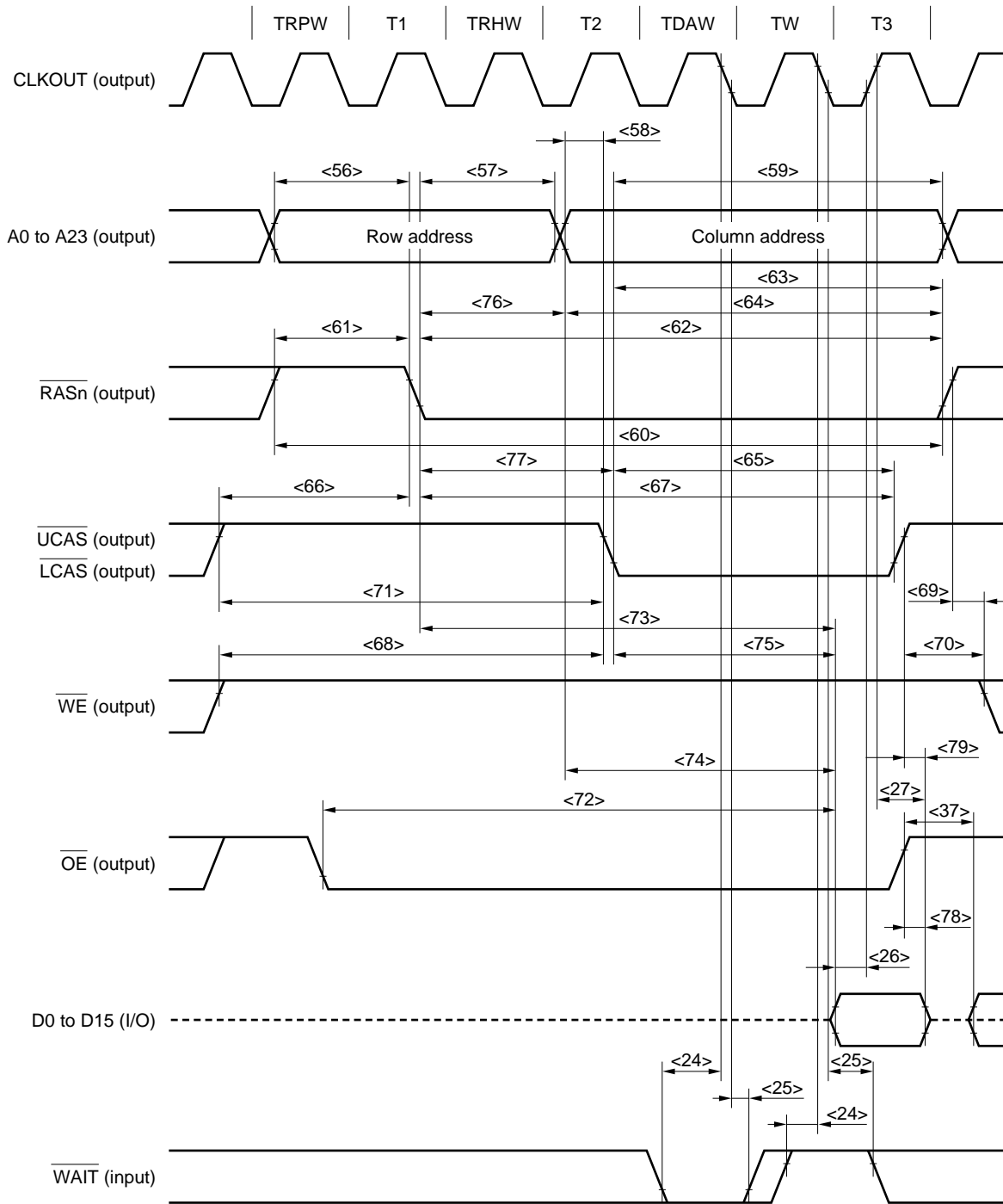
6. i: Number of idle states that are inserted when a write cycle follows a read cycle

(a) Read timing (high-speed page DRAM access, normal access: off-page) (2/3)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RAS}}$ column address delay time	<76>	t <sub>RAD</sub>		(0.5 + w <sub>RH</sub> ) T - 10		ns
$\overline{\text{RAS}}$ - $\overline{\text{CAS}}$ delay time	<77>	t <sub>RCD</sub>		(1 + w <sub>RH</sub> ) T - 10		ns
Output buffer turn-off delay time (from $\overline{\text{OE}}\uparrow$ )	<78>	t <sub>OEZ</sub>		0		ns
Output buffer turn-off delay time (from $\overline{\text{CAS}}\uparrow$ )	<79>	t <sub>OFF</sub>		0		

- Remarks**
1. T = t<sub>CYK</sub>
  2. w<sub>RH</sub>: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

(a) Read timing (high-speed page DRAM access, normal access: off-page) (3/3)



- Remarks**
1. This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).  
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1  
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  2. The broken lines indicate high impedance.
  3. n = 0 to 7

[MEMO]

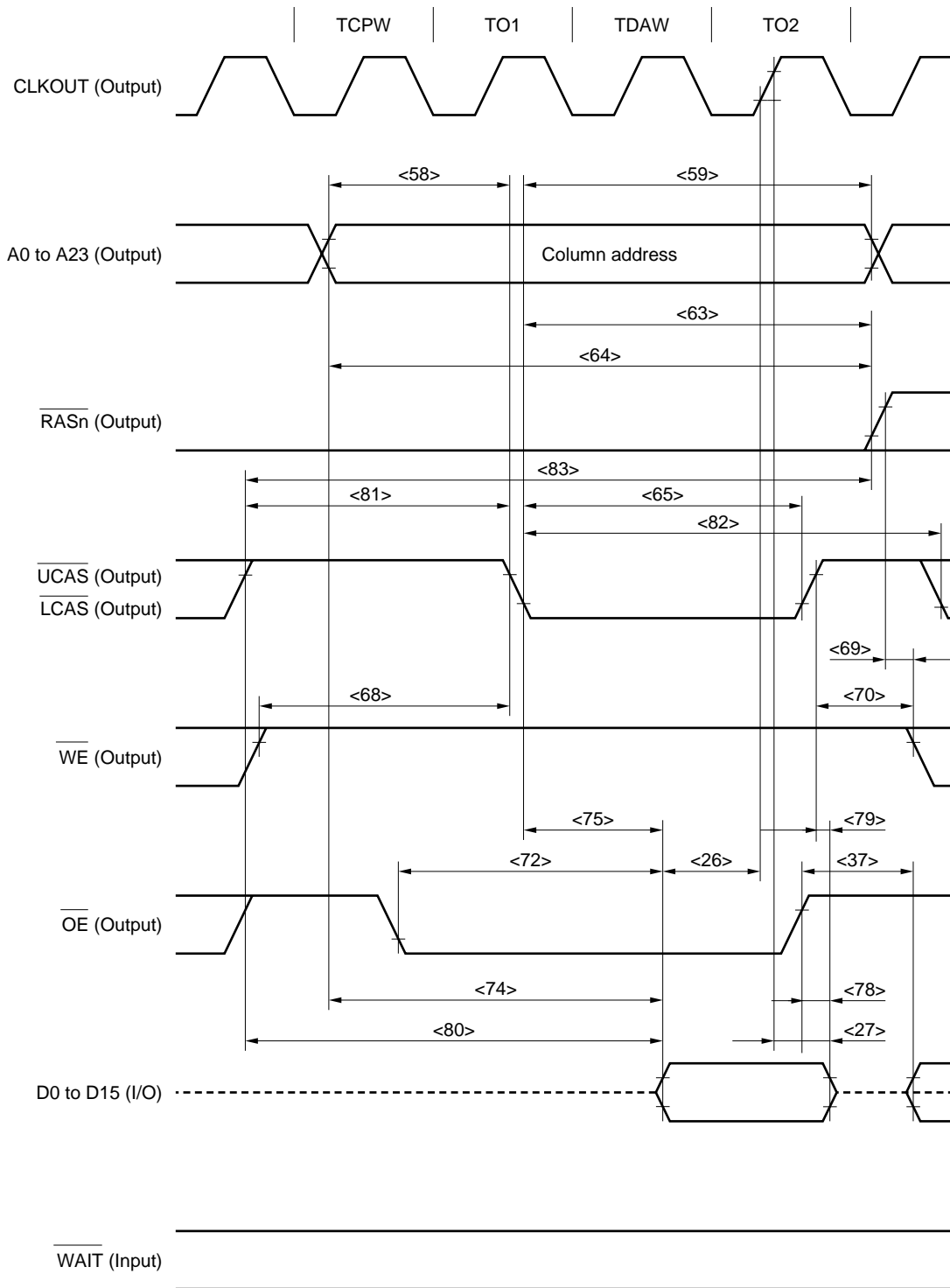
(b) Read timing (high-speed page DRAM access: on-page) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to CLKOUT ↑)	<26>	t <sub>SKID</sub>	10		ns
Data input hold time (from CLKOUT ↑)	<27>	t <sub>HKID</sub>	2		ns
Delay time from $\overline{OE}\uparrow$ to data output	<37>	t <sub>DRDOD</sub>	(0.5 + i) T – 10		ns
Column address setup time	<58>	t <sub>ASC</sub>	(0.5 + W <sub>CP</sub> ) T – 10		ns
Column address hold time	<59>	t <sub>CAH</sub>	(1.5 + W <sub>DA</sub> ) T – 10		ns
RAS hold time	<63>	t <sub>RSH</sub>	(1.5 + W <sub>DA</sub> ) T – 10		ns
Column address read time for $\overline{RAS}$	<64>	t <sub>RAL</sub>	(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 10		ns
$\overline{CAS}$ pulse width	<65>	t <sub>CAS</sub>	(1 + W <sub>DA</sub> ) T – 10		ns
$\overline{WE}$ setup time (to $\overline{CAS}\downarrow$ )	<68>	t <sub>RCS</sub>	(1 + W <sub>CP</sub> ) T – 10		ns
$\overline{WE}$ hold time (from RAS↑)	<69>	t <sub>RRH</sub>	0.5T – 10		ns
$\overline{WE}$ hold time (from $\overline{CAS}\uparrow$ )	<70>	t <sub>RCH</sub>	T – 10		ns
Output enable access time	<72>	t <sub>OEA</sub>		(1 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 20	ns
Access time from column address	<74>	t <sub>AA</sub>		(1.5 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 20	ns
$\overline{CAS}$ access time	<75>	t <sub>CAC</sub>		(1 + W <sub>DA</sub> ) T – 20	ns
Output buffer turn-off delay time (from $\overline{OE}\uparrow$ )	<78>	t <sub>OEZ</sub>	0		ns
Output buffer turn-off delay time (from $\overline{CAS}\uparrow$ )	<79>	t <sub>OFF</sub>	0		ns
Access time from $\overline{CAS}$ precharge	<80>	t <sub>ACP</sub>		(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 20	ns
$\overline{CAS}$ precharge time	<81>	t <sub>CP</sub>	(1 + W <sub>CP</sub> ) T – 5		ns
High-speed page mode cycle time	<82>	t <sub>PC</sub>	(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 10		ns
RAS hold time for $\overline{CAS}$ precharge	<83>	t <sub>RHCP</sub>	(2.5 + W <sub>CP</sub> + W <sub>DA</sub> ) T – 10		ns

**Remarks 1.** T = t<sub>CYK</sub>

- 2. W<sub>CP</sub>: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- 3. W<sub>DA</sub>: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
- 4. i: Number of idle states that are inserted when a write cycle follows a read cycle

(b) Read timing (high-speed page DRAM access: on-page) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).  
 Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  - The broken lines indicate high impedance.
  - $n = 0$  to  $7$

(c) Write timing (high-speed page DRAM access, normal access: off-page) (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24>	t <sub>SWK</sub>	10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25>	t <sub>HKW</sub>	2		ns
Row address setup time	<56>	t <sub>ASR</sub>	(0.5 + W <sub>RP</sub> ) T - 10		ns
Row address hold time	<57>	t <sub>RAH</sub>	(0.5 + W <sub>RH</sub> ) T - 10		ns
Column address setup time	<58>	t <sub>ASC</sub>	0.5T - 10		ns
Column address hold time	<59>	t <sub>CAH</sub>	(1.5 + W <sub>DA</sub> + w) T - 10		ns
Read/write cycle time	<60>	t <sub>RC</sub>	(3 + W <sub>RP</sub> + W <sub>RH</sub> + W <sub>DA</sub> + w) T - 10		ns
$\overline{\text{RAS}}$ precharge time	<61>	t <sub>RP</sub>	(0.5 + W <sub>RP</sub> ) T - 5		ns
$\overline{\text{RAS}}$ pulse time	<62>	t <sub>RAS</sub>	(2.5 + W <sub>RH</sub> + W <sub>DA</sub> + w) T - 10		ns
$\overline{\text{RAS}}$ hold time	<63>	t <sub>RSH</sub>	(1.5 + W <sub>DA</sub> + w) T - 10		ns
Column address read time (from $\overline{\text{RAS}}\uparrow$ )	<64>	t <sub>RAL</sub>	(2 + W <sub>DA</sub> + w) T - 10		ns
$\overline{\text{CAS}}$ pulse width	<65>	t <sub>CAS</sub>	(1 + W <sub>DA</sub> + w) T - 10		ns
$\overline{\text{CAS}}$ -RAS precharge time	<66>	t <sub>CRP</sub>	(1 + W <sub>RH</sub> ) T - 10		ns
$\overline{\text{CAS}}$ hold time	<67>	t <sub>CSH</sub>	(2 + W <sub>RH</sub> + W <sub>DA</sub> + w) T - 10		ns
$\overline{\text{CAS}}$ precharge time	<71>	t <sub>CPN</sub>	(2 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 5		ns
$\overline{\text{RAS}}$ column address delay time	<76>	t <sub>RAD</sub>	(0.5 + W <sub>RH</sub> ) T - 10		ns
RAS-CAS delay time	<77>	t <sub>RCD</sub>	(1 + W <sub>RH</sub> ) T - 10		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}\downarrow$ )	<84>	t <sub>WCS</sub>	(1 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 10		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}\downarrow$ )	<85>	t <sub>WCH</sub>	(1 + W <sub>DA</sub> + w) T - 10		ns
Data setup time (to $\overline{\text{CAS}}\downarrow$ )	<86>	t <sub>DS</sub>	(1.5 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 10		ns
Data hold time (from $\overline{\text{CAS}}\downarrow$ )	<87>	t <sub>DH</sub>	(1.5 + W <sub>DA</sub> + w) T - 10		ns

Remarks 1. T = t<sub>CYK</sub>

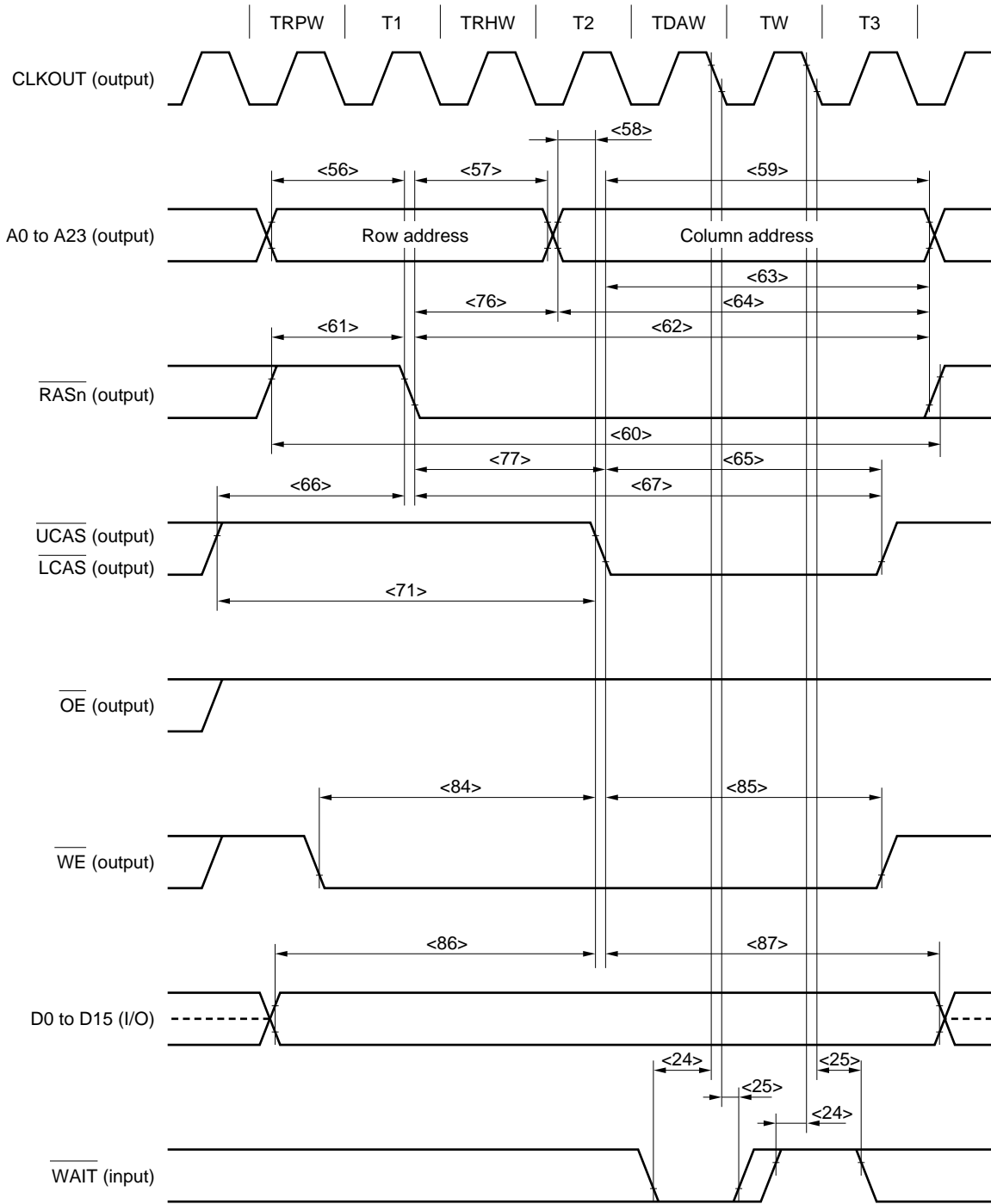
2. w: Number of waits due to  $\overline{\text{WAIT}}$

3. W<sub>RP</sub>: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

4. W<sub>RH</sub>: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

5. W<sub>DA</sub>: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

(c) Write timing (high-speed page DRAM access, normal access: off-page) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).  
 Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1  
 Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1  
 Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  - The broken lines indicate high impedance.
  - $n = 0$  to  $7$

## (d) Write timing (high-speed page DRAM access: on-page) (1/2)

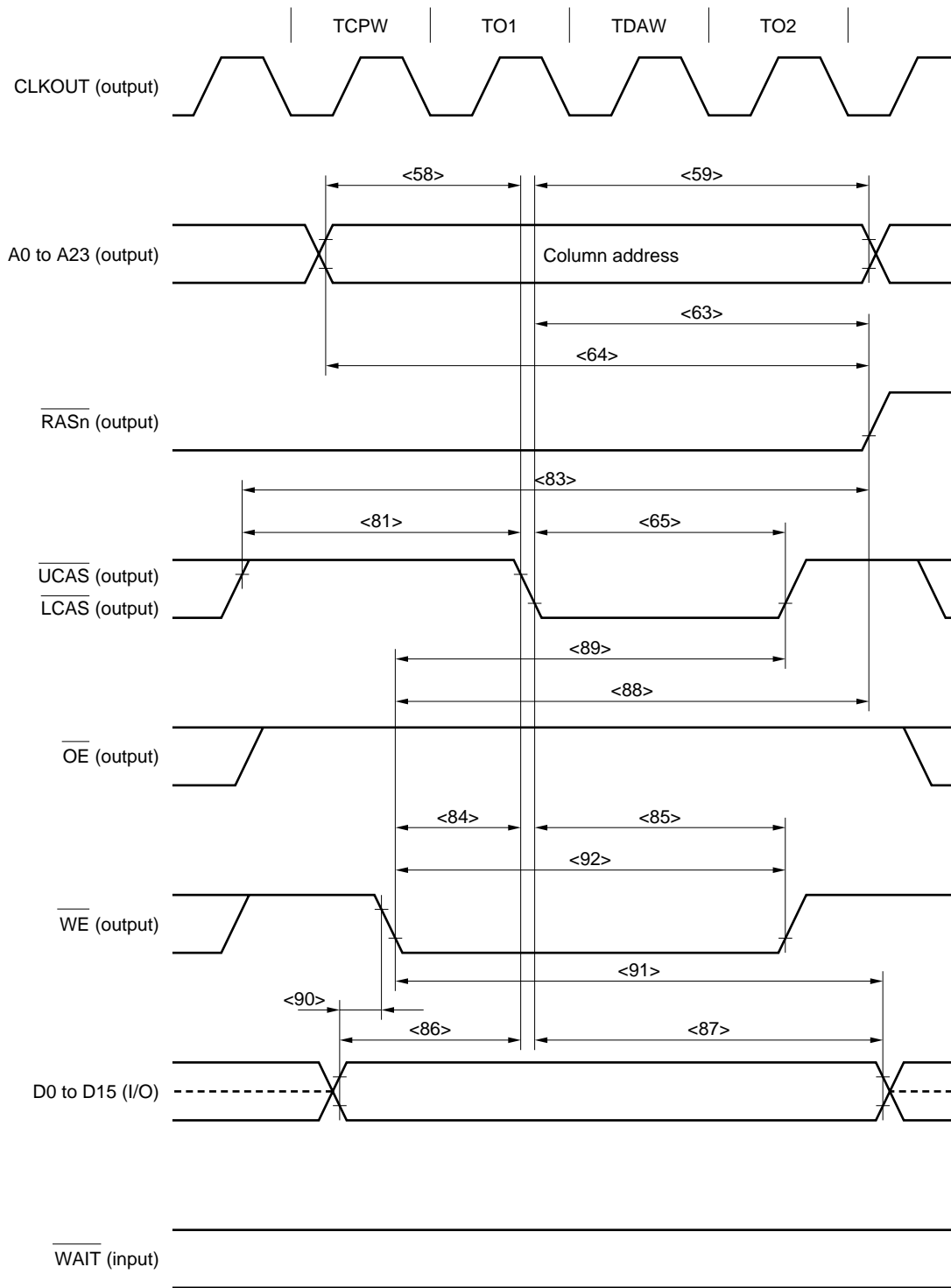
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Column address setup time	<58> $t_{ASC}$		$(0.5 + WCP) T - 10$		ns
Column address hold time	<59> $t_{CAH}$		$(1.5 + WDA) T - 10$		ns
$\overline{RAS}$ hold time	<63> $t_{RSH}$		$(1.5 + WDA) T - 10$		ns
Column address read time (from $\overline{RAS}\uparrow$ )	<64> $t_{RAL}$		$(2 + WCP + WDA) T - 10$		ns
$\overline{CAS}$ pulse width	<65> $t_{CAS}$		$(1 + WDA) T - 10$		ns
$\overline{CAS}$ precharge time	<81> $t_{CP}$		$(1 + WCP) T - 5$		ns
$\overline{RAS}$ hold time for $\overline{CAS}$ precharge	<83> $t_{RHCP}$		$(2.5 + WCP + WDA) T - 10$		ns
$\overline{WE}$ setup time (to $\overline{CAS}\downarrow$ )	<84> $t_{WCS}$	$WCP \geq 1$	$WCP T - 10$		ns
$\overline{WE}$ hold time (from $\overline{CAS}\downarrow$ )	<85> $t_{WCH}$		$(1 + WDA) T - 10$		ns
Data setup time (to $\overline{CAS}\downarrow$ )	<86> $t_{DS}$		$(0.5 + WCP) T - 10$		ns
Data hold time (from $\overline{CAS}\downarrow$ )	<87> $t_{DH}$		$(1.5 + WDA) T - 10$		ns
$\overline{WE}$ read time (from $\overline{RAS}\uparrow$ )	<88> $t_{RWL}$	$WCP = 0$	$(1.5 + WDA) T - 10$		ns
$\overline{WE}$ read time (from $\overline{CAS}\uparrow$ )	<89> $t_{CWL}$	$WCP = 0$	$(1 + WDA) T - 10$		ns
Data setup time (to $\overline{WE}\downarrow$ )	<90> $t_{DSWE}$	$WCP = 0$	$0.5T - 10$		ns
Data hold time (from $\overline{WE}\downarrow$ )	<91> $t_{DHWE}$	$WCP = 0$	$(1.5 + WDA) T - 10$		ns
$\overline{WE}$ pulse width	<92> $t_{WP}$	$WCP = 0$	$(1 + WDA) T - 10$		ns

**Remarks 1.**  $T = t_{CYK}$

**2.**  $w_{CP}$ : Number of waits due to the CPCxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13)

**3.**  $w_{DA}$ : Number of waits due to the DACxx bit of the DRCn register ( $n = 0$  to 3,  $xx = 00$  to 03, 10 to 13)

(d) Write timing (high-speed page DRAM access: on-page) (2/2)



- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
  - The broken lines indicate high impedance.
  - $n = 0$  to  $7$

(e) Read timing (EDO DRAM) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Data input setup time (to CLKOUT↑)	<26>	t <sub>SKID</sub>	10		ns
Data input hold time (from CLKOUT↑)	<27>	t <sub>HKID</sub>	2		ns
Data output delay time from OE↑	<37>	t <sub>DRDOD</sub>	(0.5 + i) T - 10		ns
Row address setup time	<56>	t <sub>ASR</sub>	(0.5 + W <sub>RP</sub> ) T - 10		ns
Row address hold time	<57>	t <sub>RAH</sub>	(0.5 + W <sub>RH</sub> ) T - 10		ns
Column address setup time	<58>	t <sub>ASC</sub>	0.5T - 10		ns
Column address hold time	<59>	t <sub>CAH</sub>	(0.5 + W <sub>DA</sub> ) T - 10		ns
RAS precharge time	<61>	t <sub>RP</sub>	(0.5 + W <sub>RP</sub> ) T - 5		ns
Column address read time (from RAS↑)	<64>	t <sub>RAL</sub>	(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 10		ns
CAS-RAS precharge time	<66>	t <sub>CRP</sub>	(1 + W <sub>RP</sub> ) T - 10		ns
CAS hold time	<67>	t <sub>CSH</sub>	(1.5 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 10		ns
WE setup time (to CAS↓)	<68>	t <sub>RCS</sub>	(2 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 10		ns
WE hold time (from RAS↑)	<69>	t <sub>RRH</sub>	0.5T - 10		ns
WE hold time (from CAS↑)	<70>	t <sub>RCH</sub>	1.5T - 10		ns
RAS access time	<73>	t <sub>RAC</sub>		(2 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 20	ns
Access time from column address	<74>	t <sub>AA</sub>		(1.5 + W <sub>DA</sub> ) T - 20	ns
CAS access time	<75>	t <sub>CAC</sub>		(1 + W <sub>DA</sub> ) T - 20	ns
Column address delay time from RAS	<76>	t <sub>RAD</sub>	(0.5 + W <sub>RH</sub> ) T - 10		ns
RAS-CAS delay time	<77>	t <sub>RCD</sub>	(1 + W <sub>RH</sub> ) T - 10		ns
Output buffer turn-off delay time (from OE)	<78>	t <sub>OEZ</sub>	0		ns
Access time from CAS precharge	<80>	t <sub>ACP</sub>		(1.5 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 20	ns
CAS precharge time	<81>	t <sub>CP</sub>	(0.5 + W <sub>CP</sub> ) T - 5		ns
RAS hold time for CAS precharge	<83>	t <sub>RHCP</sub>	(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 10		ns
Read cycle time	<93>	t <sub>HPC</sub>	(1 + W <sub>DA</sub> + W <sub>CP</sub> ) T - 10		ns
RAS pulse width	<94>	t <sub>RASP</sub>	(2.5 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 10		ns
CAS pulse width	<95>	t <sub>HCAS</sub>	(0.5 + W <sub>DA</sub> ) T - 10		ns
CAS hold time from OE	Off-page	<96>	t <sub>och1</sub>	(2 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 10	ns
	On-page	<97>	t <sub>och2</sub>	(0.5 + W <sub>DA</sub> ) T - 10	ns
Data input hold time (from CAS↓)	<98>	t <sub>DHC</sub>	0		ns

Remarks 1. T = t<sub>CYK</sub>

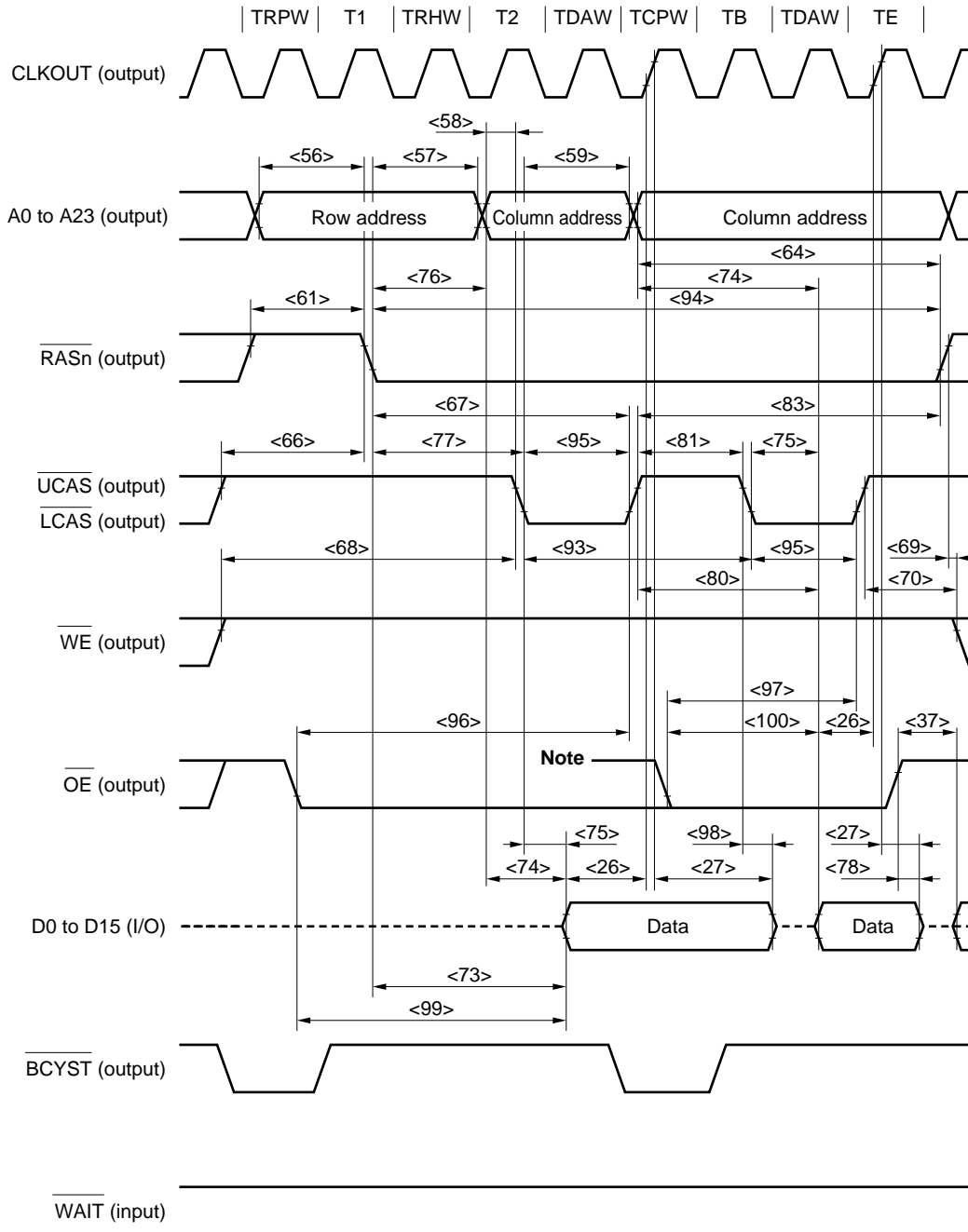
2. W<sub>RP</sub>: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
3. W<sub>RH</sub>: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
4. W<sub>DA</sub>: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
5. W<sub>CP</sub>: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
6. i: Number of idle states that are inserted when a write cycle follows a read cycle

(e) Read timing (EDO DRAM) (2/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
Output enable access time	Off-page	<99>	t <sub>OE1</sub>			(2 + W <sub>PR</sub> + W <sub>RH</sub> + W <sub>DA</sub> ) T - 20	ns
	On-page	<100>	t <sub>OE2</sub>			(1 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 20	ns

- Remarks**
1. T = t<sub>CYK</sub>
  2. W<sub>RP</sub>: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
  3. W<sub>RH</sub>: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
  4. W<sub>DA</sub>: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
  5. W<sub>CP</sub>: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

(e) Read timing (EDO DRAM) (3/3)



**Note** For on-page access from another cycle during the RASn low level signal.

- Remarks**
- This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
  - The broken lines indicate high impedance.
  - n = 0 to 7

[MEMO]

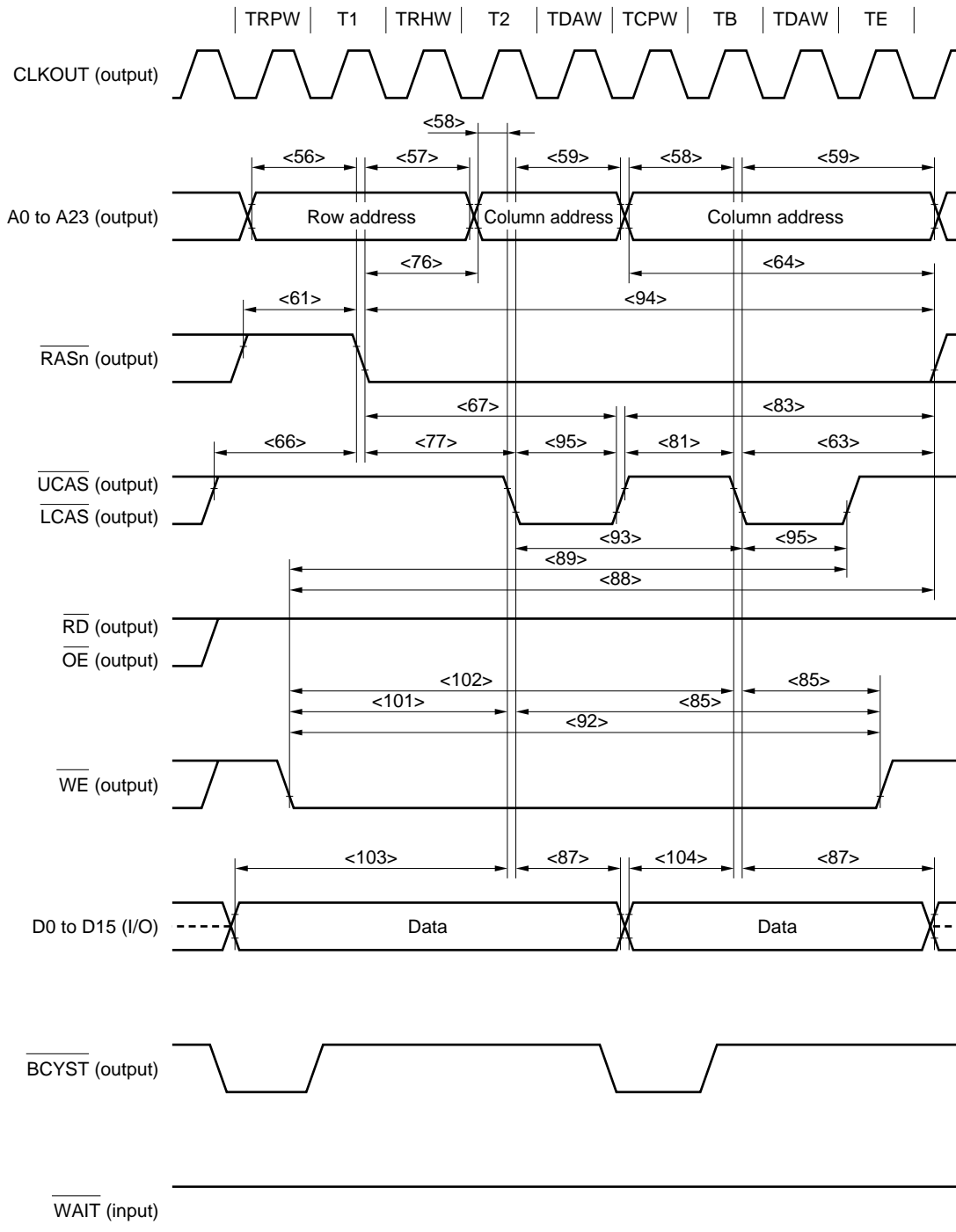
(f) Write timing (EDO DRAM) (1/2)

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Row address setup time		<56>	t <sub>ASR</sub>		(0.5 + W <sub>RP</sub> ) T - 10	ns
Row address hold time		<57>	t <sub>RAH</sub>		(0.5 + W <sub>RH</sub> ) T - 10	ns
Column address setup time		<58>	t <sub>ASC</sub>		0.5T - 10	ns
Column address hold time		<59>	t <sub>CAH</sub>		(0.5 + W <sub>DA</sub> ) T - 10	ns
RAS precharge time		<61>	t <sub>RP</sub>		(0.5 + W <sub>RP</sub> ) T - 5	ns
RAS hold time		<63>	t <sub>RSH</sub>		(1.5 + W <sub>DA</sub> ) T - 10	ns
Column address read time (from RAS↑)		<64>	t <sub>RAL</sub>		(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 10	ns
CAS-RAS precharge time		<66>	t <sub>CRP</sub>		(1 + W <sub>RP</sub> ) T - 10	ns
CAS hold time		<67>	t <sub>CSH</sub>		(1.5 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 10	ns
Column address delay time from RAS		<76>	t <sub>RAD</sub>		(0.5 + W <sub>RH</sub> ) T - 10	ns
RAS-CAS delay time		<77>	t <sub>RCD</sub>		(1 + W <sub>RH</sub> ) T - 10	ns
CAS precharge time		<81>	t <sub>CP</sub>		(0.5 + W <sub>CP</sub> ) T - 5	ns
RAS hold time for CAS precharge		<83>	t <sub>RHCP</sub>		(2 + W <sub>CP</sub> + W <sub>DA</sub> ) T - 10	ns
WE hold time (from CAS↓)		<85>	t <sub>WCH</sub>		(1 + W <sub>DA</sub> ) T - 10	ns
Data hold time (from CAS↓)		<87>	t <sub>DH</sub>		(0.5 + W <sub>DA</sub> ) T - 10	ns
WE read time (from RAS↑)	On-page	<88>	t <sub>RWL</sub>	W <sub>CP</sub> = 0	(1.5 + W <sub>DA</sub> ) T - 10	ns
WE read time (from CAS↑)	On-page	<89>	t <sub>CWL</sub>	W <sub>CP</sub> = 0	(0.5 + W <sub>DA</sub> ) T - 10	ns
WE pulse width	On-page	<92>	t <sub>WP</sub>	W <sub>CP</sub> = 0	(1 + W <sub>DA</sub> ) T - 10	ns
Write cycle time		<93>	t <sub>HPC</sub>		(1 + W <sub>DA</sub> + W <sub>CP</sub> ) T - 10	ns
RAS pulse width		<94>	t <sub>RASP</sub>		(2.5 + W <sub>RH</sub> + W <sub>DA</sub> ) T - 10	ns
CAS pulse width		<95>	t <sub>HCAS</sub>		(0.5 + W <sub>DA</sub> ) T - 10	ns
WE setup time (to CAS↓)	Off-page	<101>	t <sub>WCS1</sub>		(1 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 10	ns
	On-page	<102>	t <sub>WCS2</sub>	W <sub>CP</sub> ≥ 1	W <sub>CP</sub> T - 10	ns
Data setup time (to CAS↓)	Off-page	<103>	t <sub>DS1</sub>		(1.5 + W <sub>RP</sub> + W <sub>RH</sub> ) T - 10	ns
	On-page	<104>	t <sub>DS2</sub>		(0.5 + W <sub>CP</sub> ) T - 10	ns

Remarks 1. T = t<sub>CYK</sub>

2. W<sub>RP</sub>: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
3. W<sub>RH</sub>: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
4. W<sub>DA</sub>: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
5. W<sub>CP</sub>: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

(f) Write timing (EDO DRAM) (2/2)



- Remarks**
- This is the timing for the following case (n = 0 to 3, xx = 00 to 03, 10 to 13).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
  - The broken lines indicate high impedance.
  - n = 0 to 7

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{WAIT}}$ setup time (to CLKOUT↓)	<24>	t <sub>SWK</sub>	10		ns
$\overline{\text{WAIT}}$ hold time (from CLKOUT↓)	<25>	t <sub>HKW</sub>	2		ns
Delay time from $\overline{\text{OE}}\uparrow$ to data output	<37>	t <sub>DRDOD</sub>	(0.5 + i) T – 10		ns
Delay time from address to $\overline{\text{IOWR}}\downarrow$	<41>	t <sub>DAWR</sub>	(0.5 + WRP) T – 5		ns
Address setup time (to $\overline{\text{IOWR}}\uparrow$ )	<42>	t <sub>SAWR</sub>	(2 + WRP + WRH + WDA) T – 10		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to address	<43>	t <sub>DWRA</sub>	0.5T – 5		ns
Delay time from $\overline{\text{IOWR}}\uparrow$ to $\overline{\text{RD}}\uparrow$	<48>	WF = 0	0		ns
		WF = 1	T – 10		ns
$\overline{\text{IOWR}}$ low-level width	<50>	t <sub>WWRL</sub>	(2 + WRH + WDA + w) T – 10		ns
Row address setup time	<56>	t <sub>ASR</sub>	(0.5 + WRP) T – 10		ns
Row address hold time	<57>	t <sub>RAH</sub>	(0.5 + WRH) T – 10		ns
Column address setup time	<58>	t <sub>ASC</sub>	0.5T – 10		ns
Column address hold time	<59>	t <sub>CAH</sub>	(1.5 + WDA + WF + w) T – 10		ns
Read/write cycle time	<60>	t <sub>RC</sub>	(3 + WRP + WRH + WDA + WF + w) T – 10		ns
$\overline{\text{RAS}}$ precharge time	<61>	t <sub>RP</sub>	(0.5 + WRP) T – 5		ns
$\overline{\text{RAS}}$ hold time	<63>	t <sub>RSH</sub>	(1.5 + WDA + WF + w) T – 10		ns
Column address read time for $\overline{\text{RAS}}$	<64>	t <sub>RAL</sub>	(2 + WCP + WDA + WF + w) T – 10		ns
$\overline{\text{CAS}}$ pulse width	<65>	t <sub>CAS</sub>	(1 + WDA + WF + w) T – 10		ns
$\overline{\text{CAS}}$ - $\overline{\text{RAS}}$ precharge time	<66>	t <sub>CRP</sub>	(1 + WRP) T – 10		ns
$\overline{\text{CAS}}$ hold time	<67>	t <sub>CSH</sub>	(2 + WRH + WDA + WF + w) T – 10		ns
$\overline{\text{WE}}$ setup time (to $\overline{\text{CAS}}\downarrow$ )	<68>	t <sub>RCS</sub>	(2 + WRP + WRH) T – 10		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{RAS}}\uparrow$ )	<69>	t <sub>RRH</sub>	0.5T – 10		ns
$\overline{\text{WE}}$ hold time (from $\overline{\text{CAS}}\uparrow$ )	<70>	t <sub>RCH</sub>	1.5T – 10		ns
$\overline{\text{CAS}}$ precharge time	<71>	t <sub>CPN</sub>	(2 + WRP + WRH) T – 5		ns

Remarks 1. T = t<sub>cyk</sub>

2. w: Number of waits due to  $\overline{\text{WAIT}}$

3. WRP: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

4. WRH: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

5. WDA: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

6. WCP: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

7. WF: Number of waits that are inserted for a source-side access during a DMA flyby transfer

8. i: Number of idle states that are inserted when a write cycle follows a read cycle

(g) DMA flyby transfer timing (DRAM (EDO, high-speed page) → external I/O transfer) (2/3)

Parameter		Symbol	Conditions	MIN.	MAX.	Unit
Delay time from $\overline{\text{RAS}}$ to column address		<76>	t <sub>RAD</sub>		$(0.5 + \text{WRH}) T - 10$	ns
$\overline{\text{RAS}}$ -CAS delay time		<77>	t <sub>RCD</sub>		$(1 + \text{WRH}) T - 10$	ns
Output buffer turn-off delay time (from $\overline{\text{OE}} \uparrow$ )		<78>	t <sub>OEZ</sub>		0	ns
Output buffer turn-off delay time (from $\overline{\text{CAS}} \uparrow$ )		<79>	t <sub>OFF</sub>		0	ns
$\overline{\text{CAS}}$ precharge time		<81>	t <sub>CP</sub>		$(0.5 + \text{WCP}) T - 5$	ns
High-speed page mode cycle time		<82>	t <sub>PC</sub>		$(2 + \text{WCP} + \text{WDA} + \text{WF} + \text{W}) T - 10$	ns
$\overline{\text{RAS}}$ hold time for CAS precharge		<83>	t <sub>RHCP</sub>		$(2.5 + \text{WCP} + \text{WDA} + \text{WF} + \text{W}) T - 10$	ns
$\overline{\text{RAS}}$ pulse width		<94>	t <sub>RASP</sub>		$(2.5 + \text{WRH} + \text{WDA} + \text{WF} + \text{W}) T - 10$	ns
$\overline{\text{OE}} \rightarrow \overline{\text{CAS}}$ hold time (from $\overline{\text{CAS}} \uparrow$ )	Off-page	<96>	t <sub>OCH1</sub>		$(2.5 + \text{WRP} + \text{WRH} + \text{WDA} + \text{WF} + \text{W}) T - 10$	ns
	On-page	<97>	t <sub>OCH2</sub>		$(1.5 + \text{WCP} + \text{WDA} + \text{WF} + \text{W}) T - 10$	ns
Delay time from $\overline{\text{DMAAKm}} \downarrow$ to $\overline{\text{CAS}} \downarrow$		<105>	t <sub>DDACS</sub>		$(1.5 + \text{WRH}) T - 10$	ns
Delay time from $\overline{\text{IOWR}} \downarrow$ to $\overline{\text{CAS}} \downarrow$		<106>	t <sub>DRDCS</sub>		$(1 + \text{WRH}) T - 10$	ns

**Remarks** 1. T=t<sub>cyk</sub>

2. w: Number of waits due to  $\overline{\text{WAIT}}$
3. WCP: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
4. WDA: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
5. WRH: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
6. WRP: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
7. WF: Number of waits that are inserted for a source-side access during a DMA flyby transfer
8. m = 0 to 3



(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (1/3)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
WAIT setup time (to CLKOUT↓)	<24>	t <sub>SWK</sub>	10		ns
WAIT hold time (from CLKOUT↓)	<25>	t <sub>HKW</sub>	2		ns
IORD low-level width	<32>	t <sub>WRDL</sub>	(2 + WRH + WDA + WF + w) T - 10		ns
IORD high-level width	<33>	t <sub>WRDH</sub>	T - 5		ns
Delay time from address to IORD↑	<34>	t <sub>DARD</sub>	0.5T - 5		ns
Delay time from IORD↑ to address	<35>	t <sub>DRDA</sub>	(0.5 + i) T - 5		ns
Row address setup time	<56>	t <sub>ASR</sub>	(0.5 + WRP) T - 10		ns
Row address hold time	<57>	t <sub>RAH</sub>	(0.5 + WRH) T - 10		ns
Column address setup time	<58>	t <sub>ASC</sub>	0.5T - 10		ns
Column address hold time	<59>	t <sub>CAH</sub>	(1.5 + WDA + WF) T - 10		ns
Read/write cycle time	<60>	t <sub>RC</sub>	(3 + WRP + WRH + WDA + WF + w) T - 10		ns
RAS precharge time	<61>	t <sub>RP</sub>	(0.5 + WRP) T - 5		ns
RAS hold time	<63>	t <sub>RSH</sub>	(1.5 + WDA + WF) T - 10		ns
Column address read time for RAS	<64>	t <sub>RAL</sub>	(2 + WCP + WDA + WF + w) T - 10		ns
CAS pulse width	<65>	t <sub>CAS</sub>	(1 + WDA + WF) T - 10		ns
CAS-RAS precharge time	<66>	t <sub>CRP</sub>	(1 + WRP) T - 10		ns
CAS hold time	<67>	t <sub>CSH</sub>	(2 + WRH + WDA + WF + w) T - 10		ns
CAS precharge time	<71>	t <sub>CPN</sub>	(2 + WRP + WRH + w) T - 5		ns
Delay time from RAS to column address	<76>	t <sub>RAD</sub>	(0.5 + WRH) T - 10		ns
RAS-CAS delay time	<77>	t <sub>RCD</sub>	(1 + WRH + w) T - 10		ns
CAS precharge time	<81>	t <sub>CP</sub>	(0.5 + WCP + w) T - 5		ns
High-speed page mode cycle time	<82>	t <sub>PC</sub>	(2 + WCP + WDA + WF + w) T - 10		ns
RAS hold time for CAS precharge	<83>	t <sub>RHCP</sub>	(2.5 + WCP + WDA + w) T - 10		ns
WE hold time (from CAS↓)	<85>	t <sub>WCH</sub>	(1 + WDA) T - 10		ns
WE read time (from RAS↑)	<88>	t <sub>RWL</sub>	WCP = 0 (1.5 + WDA + w) T - 10		ns
WE read time (from CAS↑)	<89>	t <sub>CWL</sub>	WCP = 0 (1 + WDA + w) T - 10		ns
WE pulse width	<92>	t <sub>WP</sub>	WCP = 0 (1 + WDA + w) T - 10		ns
RAS pulse width	<94>	t <sub>RASP</sub>	(2.5 + WRH + WDA + WF + w) T - 10		ns

Remarks

1. T = t<sub>cyk</sub>
2. w: Number of waits due to WAIT
3. WRH: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
4. WDA: Number of waits due to the DACxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
5. WRP: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
6. WCP: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)
7. WF: Number of waits that are inserted for a source-side access during a DMA flyby transfer
8. i: Number of idle states that are inserted when a write cycle follows a read cycle
9. n = 0 to 7

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (2/3)

Parameter		Symbol		Conditions	MIN.	MAX.	Unit
WE setup time (to CAS↓)	Off-page	<101>	tWCS1	WCP = 0	$(1 + WRH + WRP + w) T - 10$		ns
	On-page	<102>	tWCS2	WCP ≥ 1	$WCP T - 10$		ns
Delay time from DMAAKm↓ to CAS↓		<105>	tDDACS		$(1.5 + WRH + w) T - 10$		ns
Delay time from IORD↓ to CAS↓		<106>	tDRDCS		$(1 + WRH + w) T - 10$		ns
Delay time from WE↑ to IORD↑		<107>	tDWERD	WF = 0	0		ns
				WF = 1	$T - 10$		ns

Remarks 1. T = tCYK

2. w: Number of waits due to WAIT

3. WRH: Number of waits due to the RHCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

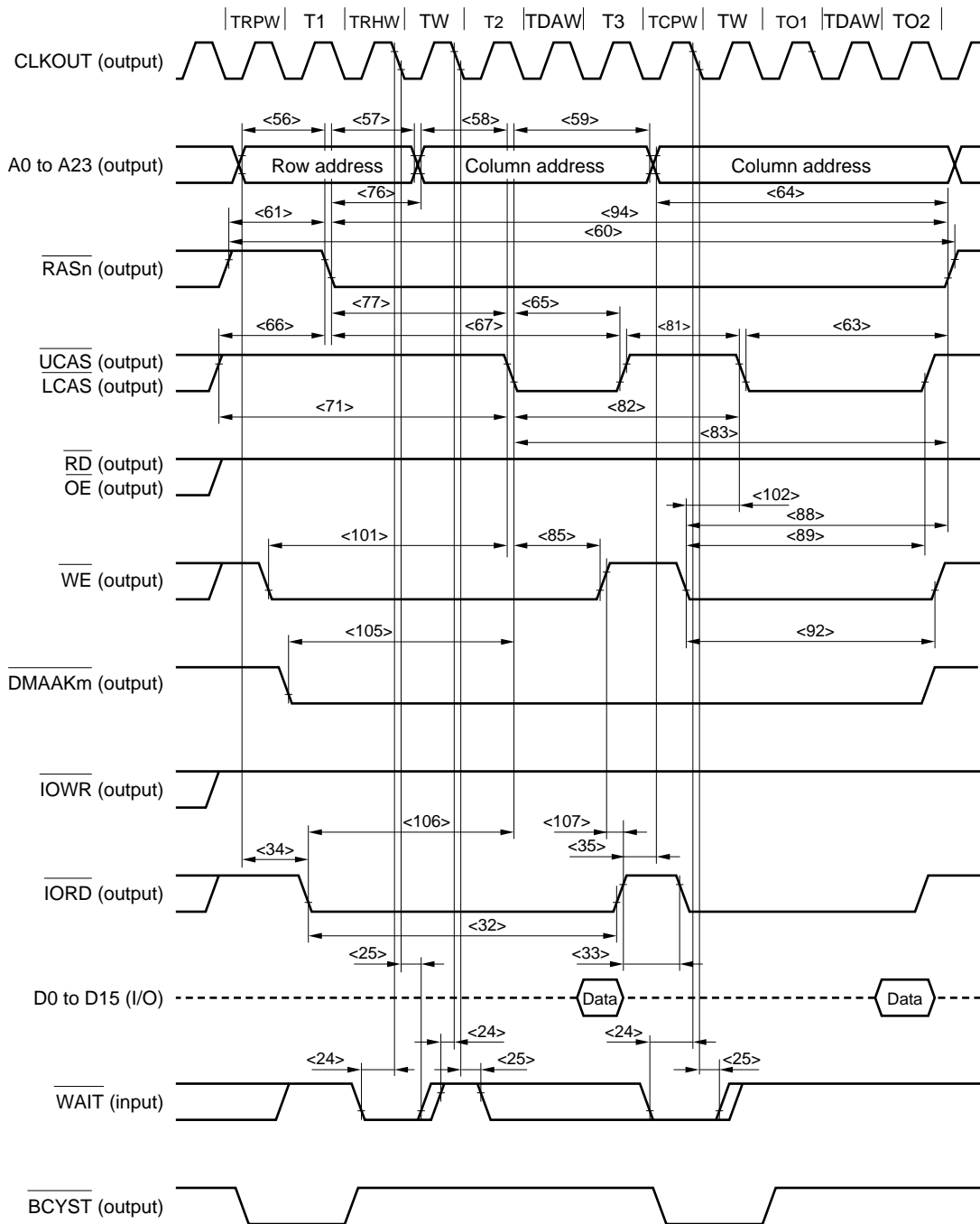
4. WRP: Number of waits due to the RPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

5. WCP: Number of waits due to the CPCxx bit of the DRCn register (n = 0 to 3, xx = 00 to 03, 10 to 13)

6. WF: Number of waits that are inserted for a source-side access during a DMA flyby transfer

7. m = 0 to 3

(h) DMA flyby transfer timing (external I/O → DRAM (EDO, high-speed page) transfer) (3/3)



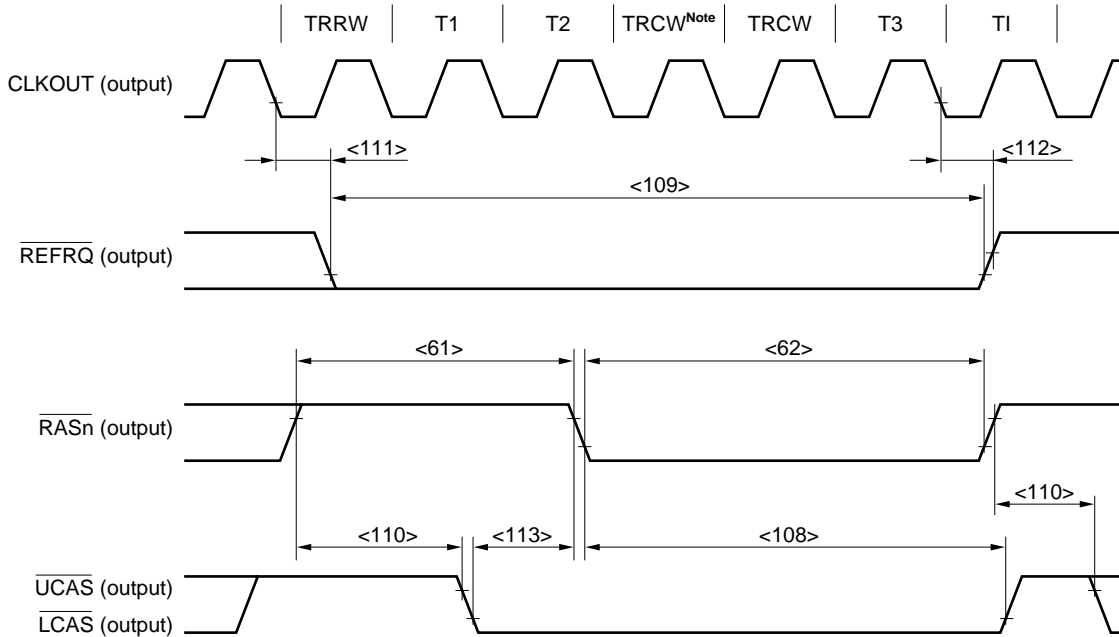
- Remarks**
- This is the timing for the following case ( $n = 0$  to  $3$ ,  $xx = 00$  to  $03$ ,  $10$  to  $13$ ).
    - Number of waits due to the RPCxx bit of the DRCn register (TRPW): 1
    - Number of waits due to the RHCxx bit of the DRCn register (TRHW): 1
    - Number of waits due to the DACxx bit of the DRCn register (TDAW): 1
    - Number of waits due to the CPCxx bit of the DRCn register (TCPW): 1
    - Number of waits that are inserted for a source-side access during a DMA flyby transfer: 0
  - The broken lines indicate high impedance.
  - $n = 0$  to  $7$ ,  $m = 0$  to  $3$

(i) CBR refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
RAS precharge time	<61> $t_{RP}$		$(1.5 + W_{RRW}) T - 5$		ns
RAS pulse width	<62> $t_{RAS}$		$(1.5 + W_{RCW}^{Note}) T - 10$		ns
CAS hold time	<108> $t_{CHR}$		$(1.5 + W_{RCW}^{Note}) T - 10$		ns
REFRQ pulse width	<109> $t_{WRFL}$		$(3 + W_{RRW} + W_{RCW}^{Note}) T - 10$		ns
RAS precharge CAS hold time	<110> $t_{RPC}$		$(0.5 + W_{RRW}) T - 10$		ns
REFRQ active delay time (from CLKOUT↓)	<111> $t_{DKRF}$		2	10	ns
REFRQ inactive delay time (from CLKOUT↓)	<112> $t_{HKRF}$		2	10	ns
CAS setup time	<113> $t_{CSR}$		$T - 10$		ns

**Note** At least one clock cycle is inserted by default for  $w_{RCW}$  regardless of the settings of bits RCW0 to RCW2 of the RWC register.

- Remarks**
1.  $T = t_{CYK}$
  2.  $w_{RRW}$ : Number of waits due to the RRW0 and RRW1 bits of the RWC register
  3.  $w_{RCW}$ : Number of waits due to the RCW0 to RCW2 bits of the RWC register



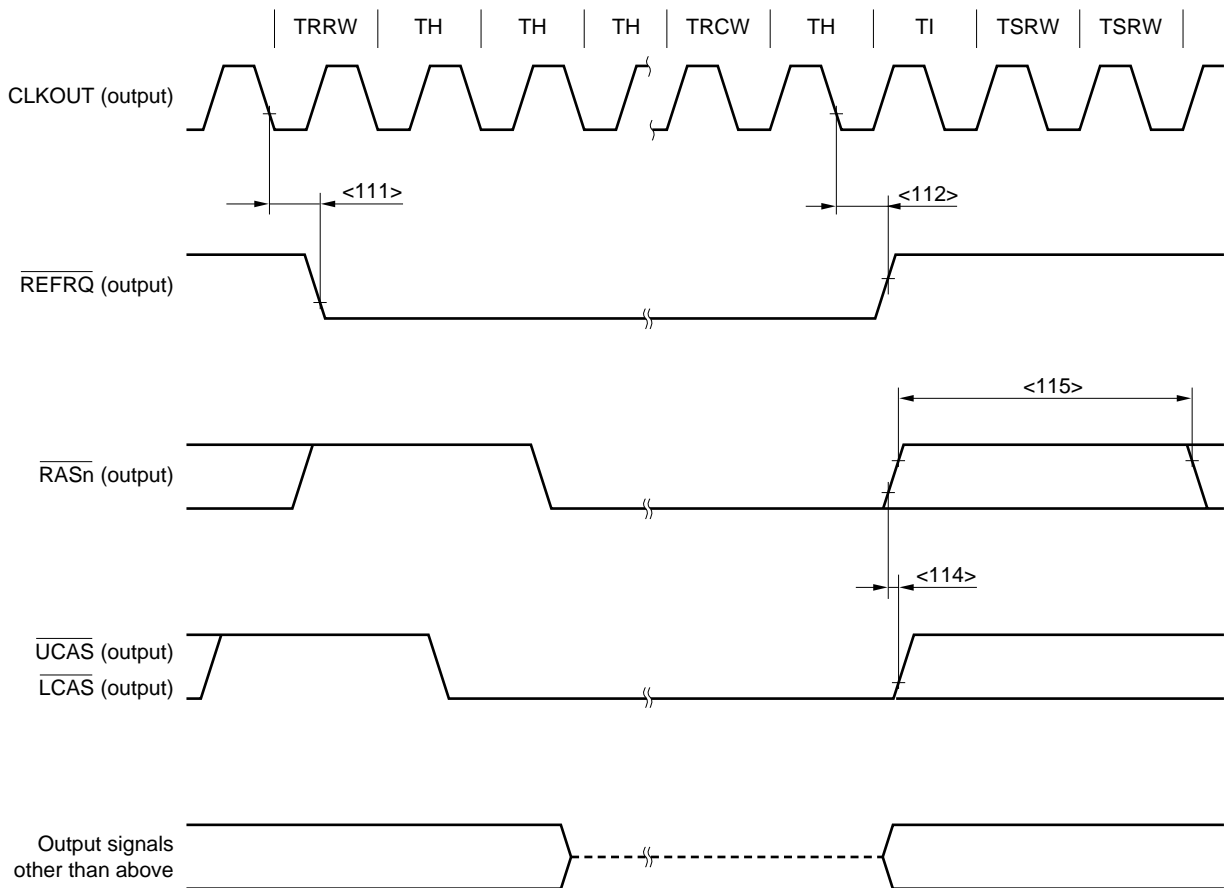
**Note** This TRCW is always inserted regardless of the settings of bits RCW0 to RCW2 of the RWC register.

- Remarks**
1. This is the timing for the following case.  
 Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1  
 Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 2
  2.  $n = 0$  to 7

(j) CBR self-refresh timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{REFRQ}}$ active delay time (from CLKOUT↑)	<111>	$t_{DKRF}$	2	10	ns
$\overline{\text{REFRQ}}$ inactive delay time (from CLKOUT↑)	<112>	$t_{HKRF}$	2	10	ns
$\overline{\text{CAS}}$ hold time	<114>	$t_{CHS}$	-5		ns
$\overline{\text{RAS}}$ precharge time	<115>	$t_{RPS}$	$(1 + 2w_{SRW}) T - 10$		ns

- Remarks**
- $T = t_{CYK}$
  - $w_{SRW}$ : Number of waits due to the SRW0 to SRW2 bits of the RWC register

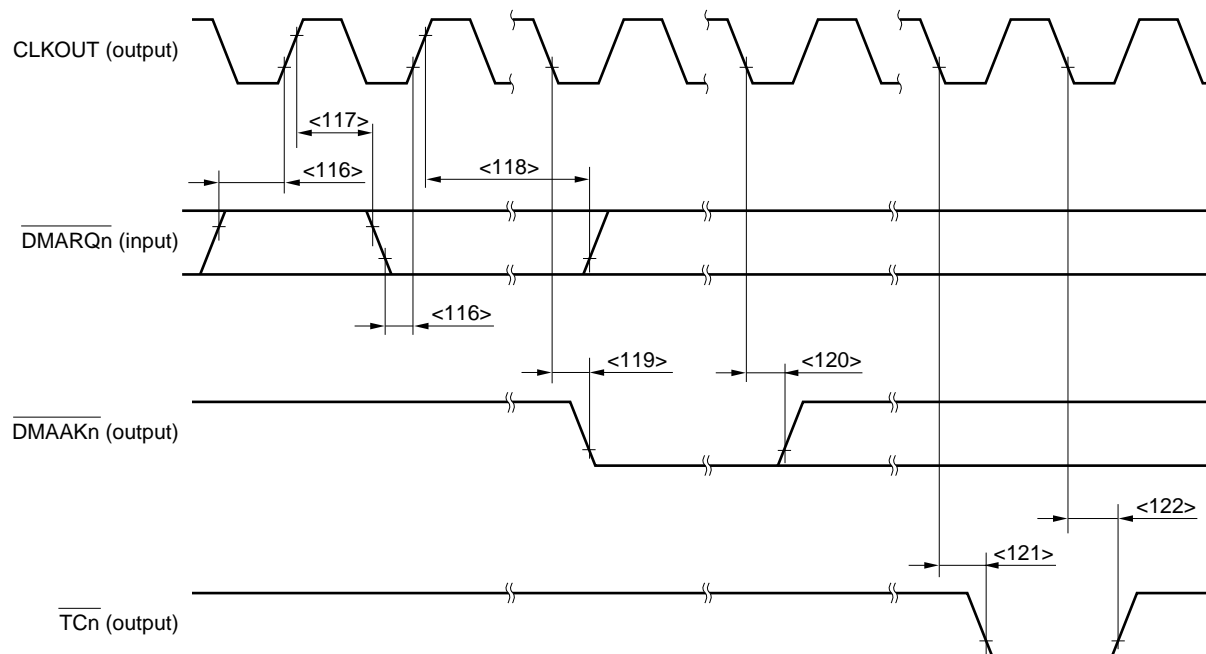


- Remarks**
- This is the timing for the following case.  
 Number of waits due to the RRW0 and RRW1 bits of the RWC register (TRRW): 1  
 Number of waits due to the RCW0 to RCW2 bits of the RWC register (TRCW): 1  
 Number of waits due to the SRW0 to SRW2 bits of the RWC register (TSRW): 2
  - The broken lines indicate high impedance.
  - $n = 0$  to 7

(7) DMAC timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{DMARQn}}$ setup time (to CLKOUT↑)	<116> $t_{\text{SDRK}}$		10		ns
$\overline{\text{DMARQn}}$ hold time (from CLKOUT↑)	<117> $t_{\text{HKDR1}}$		2		ns
	<118> $t_{\text{HKDR2}}$		Until $\overline{\text{DMAAKn}}\downarrow$		ns
$\overline{\text{DMAAKn}}$ output delay time (from CLKOUT↓)	<119> $t_{\text{DKDA}}$		2	10	ns
$\overline{\text{DMAAKn}}$ output hold time (from CLKOUT↓)	<120> $t_{\text{HKDA}}$		2	10	ns
$\overline{\text{TCn}}$ output delay time (from CLKOUT↓)	<121> $t_{\text{DKTC}}$		2	10	ns
$\overline{\text{TCn}}$ output hold time (from CLKOUT↓)	<122> $t_{\text{HKTC}}$		2	10	ns

Remark n = 0 to 3



Remark n = 0 to 3

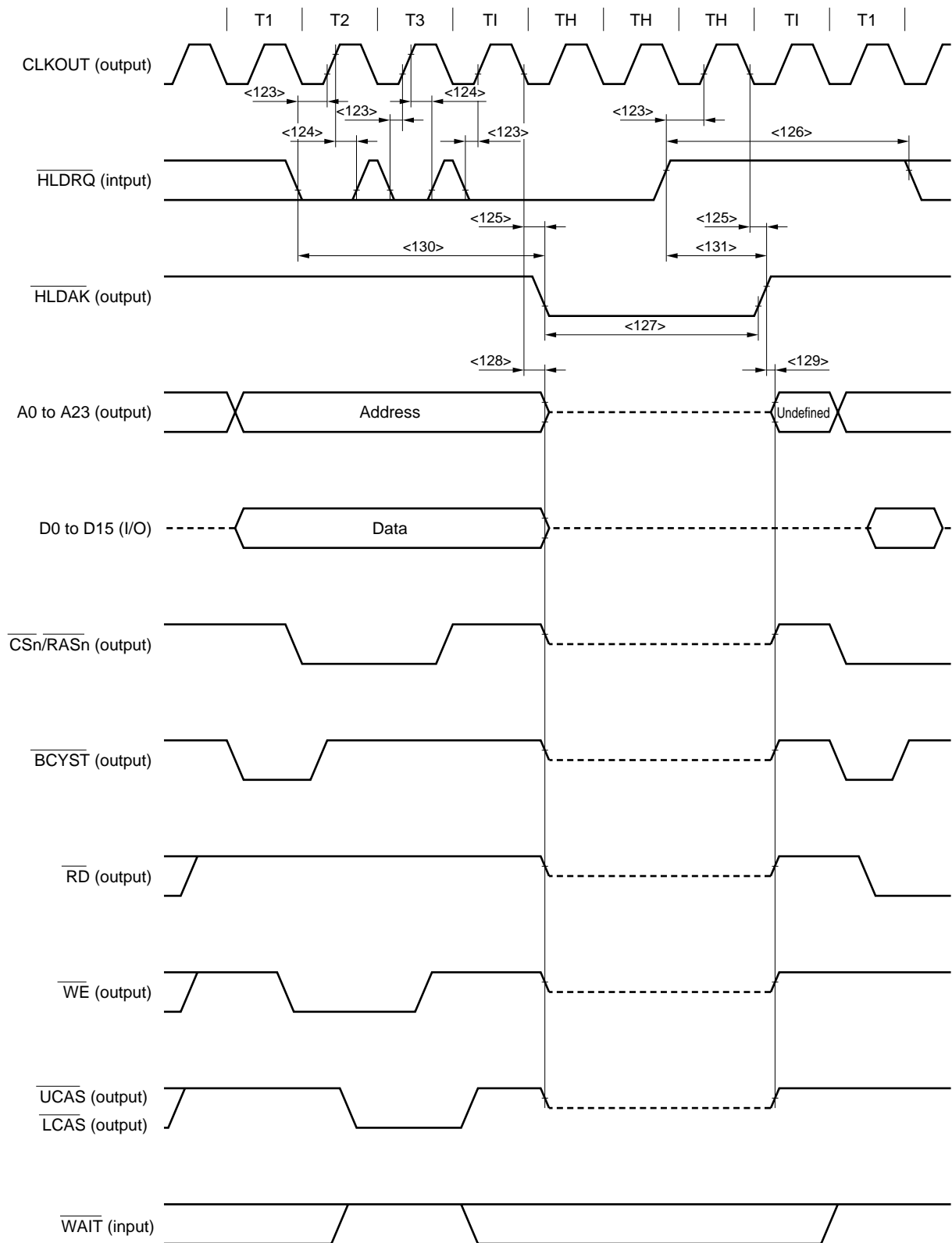
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## (8) Bus hold timing (1/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{\text{HLDRQ}}$ setup time (to $\text{CLKOUT}\uparrow$ )	<123> $t_{\text{SHRK}}$		10		ns
$\overline{\text{HLDRQ}}$ hold time (from $\text{CLKOUT}\uparrow$ )	<124> $t_{\text{HKHR}}$		5		ns
Delay time from $\text{CLKOUT}\downarrow$ to $\overline{\text{HLDAK}}$	<125> $t_{\text{DKHA}}$		2	10	ns
$\overline{\text{HLDRQ}}$ high-level width	<126> $t_{\text{WHQH}}$		$T + 17$		ns
$\overline{\text{HLDAK}}$ low-level width	<127> $t_{\text{WHAL}}$		$T - 8$		ns
Delay time from $\text{CLKOUT}\downarrow$ to bus float	<128> $t_{\text{DKCF}}$			10	ns
Delay time from $\overline{\text{HLDAK}}\uparrow$ to bus output	<129> $t_{\text{DHAC}}$		0		ns
Delay time from $\overline{\text{HLDRQ}}\downarrow$ to $\overline{\text{HLDAK}}\downarrow$	<130> $t_{\text{DHQA1}}$		2.5T		ns
Delay time from $\overline{\text{HLDRQ}}\uparrow$ to $\overline{\text{HLDAK}}\uparrow$	<131> $t_{\text{DHQA2}}$		0.5T	1.5T	ns

**Remark** T =  $t_{\text{CYK}}$

(8) Bus hold timing (2/2)

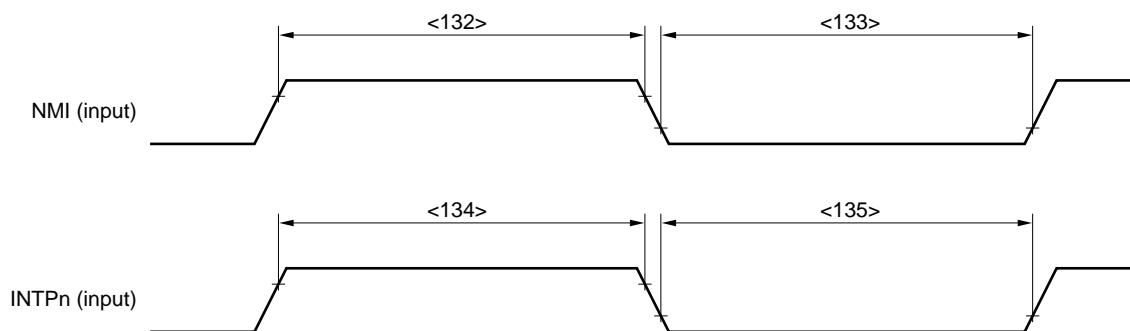


- Remarks**
1. The broken lines indicate high impedance.
  2. n = 0 to 7

(9) Interrupt timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
NMI high-level width	<132>	t <sub>WNH</sub>		500		ns
NMI low-level width	<133>	t <sub>WNL</sub>		500		ns
INTPn high-level width	<134>	t <sub>WTH</sub>		4T + 10		ns
INTPn low-level width	<135>	t <sub>WTL</sub>		4T + 10		ns

- Remarks**
- n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153
  - T = t<sub>cyk</sub>

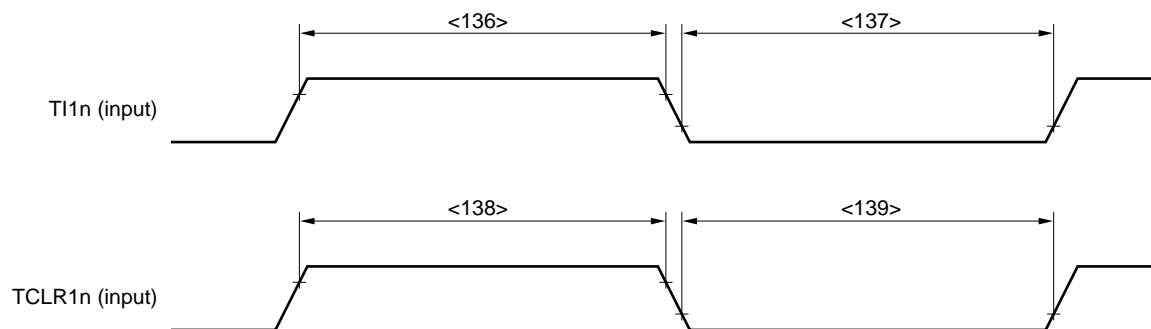


**Remark** n = 100 to 103, 110 to 113, 120 to 123, 130 to 133, 140 to 143, or 150 to 153

(10) RPU timing

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
TI1n high-level width	<136>	t <sub>WTIH</sub>		3T + 18		ns
TI1n low-level width	<137>	t <sub>WTIL</sub>		3T + 18		ns
TCLR1n high-level width	<138>	t <sub>WTCH</sub>		3T + 18		ns
TCLR1n low-level width	<139>	t <sub>WTCL</sub>		3T + 18		ns

- Remarks**
- n = 0 to 5
  - T = t<sub>cyk</sub>

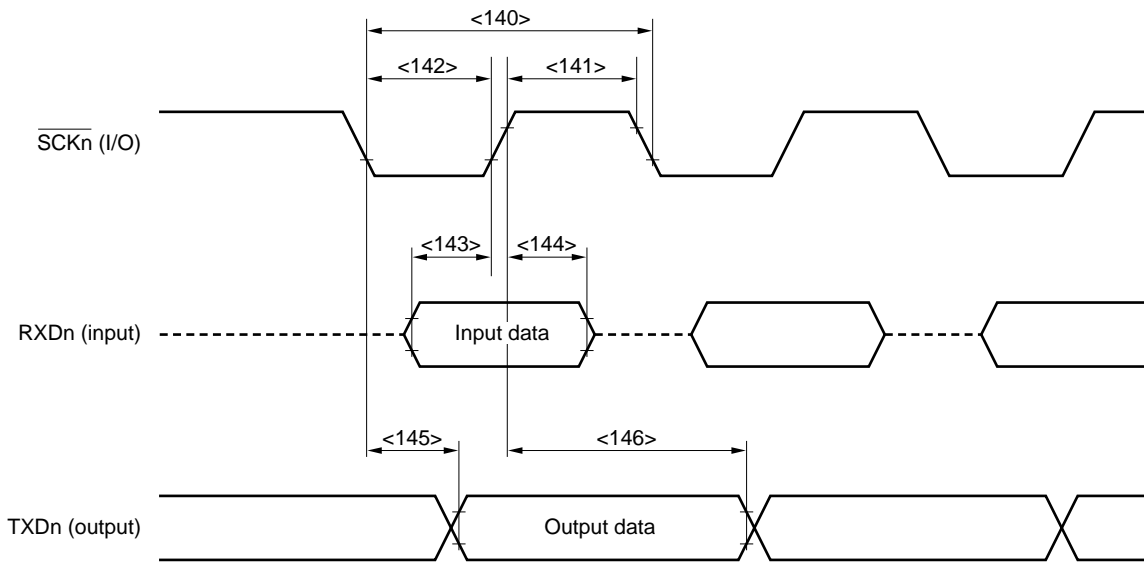


**Remark** n = 0 to 5

(11) UART0, UART1 timing (clocked or master mode only)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCKn cycle	<140>	$t_{CYSK0}$	250		ns
SCKn high-level width	<141>	$t_{WSK0H}$	$0.5t_{CYSK0} - 20$		ns
SCKn low-level width	<142>	$t_{WSK0L}$	$0.5t_{CYSK0} - 20$		ns
RxDn setup time (to SCKn↑)	<143>	$t_{SRXSK}$	30		ns
RxDn hold time (from SCKn↑)	<144>	$t_{HSKRX}$	0		ns
TxDn output delay time (from SCKn↓)	<145>	$t_{DSKTX}$		20	ns
TxDn output hold time (from SCKn↑)	<146>	$t_{HDKTX}$	$0.5t_{CYSK0} - 5$		ns

Remark n = 0, 1



- Remarks
1. The broken lines indicate high impedance.
  2. n = 0, 1

(12) CSI0 to CSI3 timing

(a) Master mode

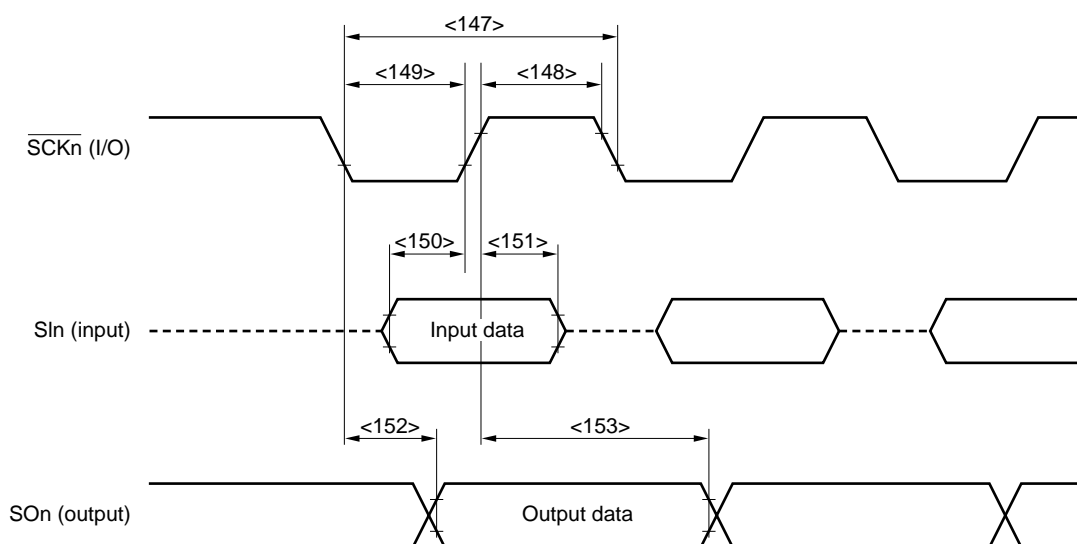
Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147> $t_{CYSK1}$	Output	100		ns
$\overline{SCKn}$ high-level width	<148> $t_{WSK1H}$	Output	$0.5t_{CYSK1} - 20$		ns
$\overline{SCKn}$ low-level width	<149> $t_{WSK1L}$	Output	$0.5t_{CYSK1} - 20$		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<150> $t_{SSISK}$		30		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<151> $t_{HSKSI}$		0		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<152> $t_{DSKSO}$			20	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<153> $t_{HSKSO}$		$0.5t_{CYSK1} - 5$		ns

Remark n = 0 to 3

(b) Slave mode

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
$\overline{SCKn}$ cycle	<147> $t_{CYSK1}$	Input	100		ns
$\overline{SCKn}$ high-level width	<148> $t_{WSK1H}$	Input	30		ns
$\overline{SCKn}$ low-level width	<149> $t_{WSK1L}$	Input	30		ns
SIn setup time (to $\overline{SCKn}\uparrow$ )	<150> $t_{SSISK}$		10		ns
SIn hold time (from $\overline{SCKn}\uparrow$ )	<151> $t_{HSKSI}$		10		ns
SOn output delay time (from $\overline{SCKn}\downarrow$ )	<152> $t_{DSKSO}$			30	ns
SOn output hold time (from $\overline{SCKn}\uparrow$ )	<153> $t_{HSKSO}$		$t_{WSK1H}$		ns

Remark n = 0 to 3



- Remarks
1. The broken lines indicate high impedance.
  2. n = 0 to 3

**A/D Converter Characteristics** ( $T_A = -40$  to  $+70^\circ\text{C}$  ...  $\mu$ PD703100A-40,  
 $T_A = -40$  to  $+85^\circ\text{C}$  ...  $\mu$ PD703100A-33,  $\mu$ PD703101A-33,  $\mu$ PD703102A-33,  
 $V_{DD} = HV_{DD} = CV_{DD} = 3.0$  to  $3.6$  V,  $V_{SS} = 0$  V,  
 $V_{DD} - 0.5$  V  $\leq AV_{DD} \leq V_{DD}$ , output pin load capacitance:  $C_L = 50$  pF)

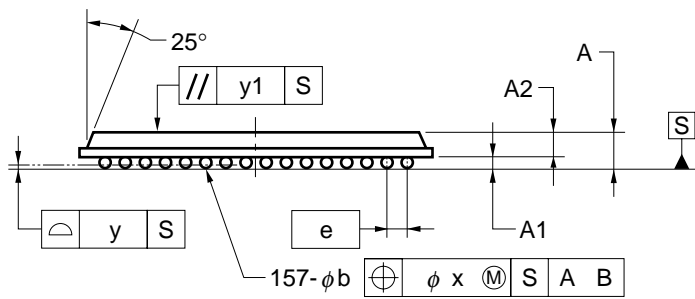
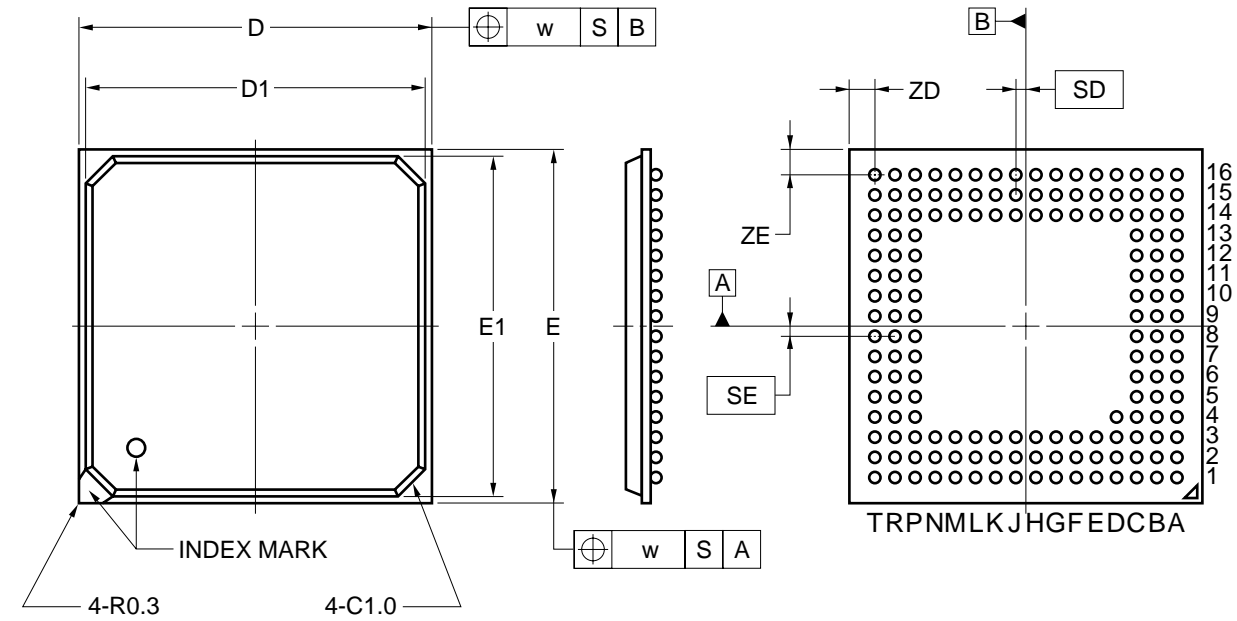
★

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	–		10			bit
Overall error	–				$\pm 5$	LSB
Quantization error	–				$\pm 1/2$	LSB
Conversion time	$t_{CONV}$		5		10	$\mu$ s
Sampling time	$t_{SAMP}$		Conversion clock <sup>Note/6</sup>			ns
Zero-scale error	–				$\pm 5$	LSB
Full-scale error	–				$\pm 5$	LSB
Nonlinearity error	–				$\pm 3$	LSB
Analog input voltage	$V_{IAN}$		-0.3		$AV_{REF} + 0.3$	V
Analog input resistance	$R_{AN}$			1.0		M $\Omega$
$AV_{REF}$ input voltage	$AV_{REF}$	$AV_{REF} = AV_{DD}$	3.0		$AV_{DD}$	V
$AV_{REF}$ input current	$AI_{REF}$				2.0	mA
$AV_{DD}$ current	$AI_{DD}$				5.0	mA

**Note** The conversion clock is the number of clocks set by the ADM1 register.

4. PACKAGE DRAWINGS

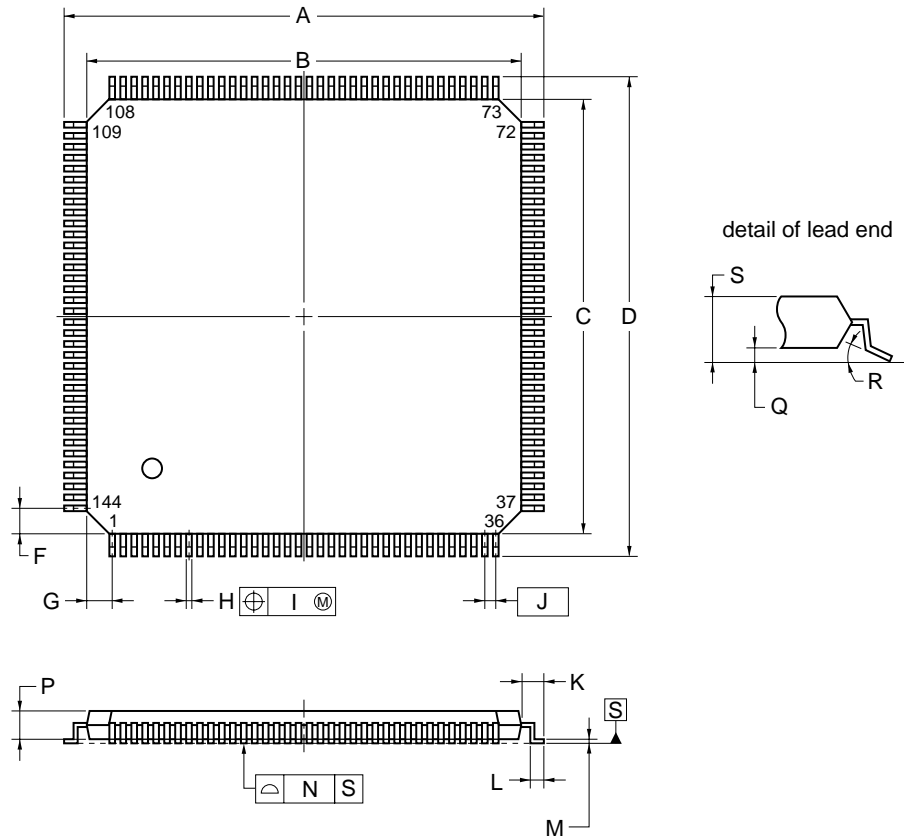
157-PIN PLASTIC FBGA (14x14)



ITEM	MILLIMETERS
D	14.0±0.1
D1	13.4
E	14.0±0.1
E1	13.4
w	0.20
e	0.8
A	1.31±0.15
A1	0.35±0.10
A2	0.96
b	0.5 <sup>+0.05</sup> <sub>-0.10</sub>
x	0.08
y	0.10
y1	0.2
SD	0.4
SE	0.4
ZD	1.0
ZE	1.0

S157F1-80-FA1

★ 144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	0.17 <sup>+0.03</sup> <sub>-0.07</sub>
N	0.08
P	1.4
Q	0.10±0.05
R	3°+4° -3°
S	1.5±0.1

**S144GJ-50-UEN**

**5. RECOMMENDED SOLDERING CONDITIONS**

This product should be soldered and mounted under the following recommended conditions.

For details of the recommended soldering conditions, refer to the document **Semiconductor Device Mounting Technology Manual (C10535E)**.

For soldering methods and conditions other than those recommended below, contact an NEC sales representative.

**Table 5-1. Surface Mounting Type Soldering Conditions**

- (1) μPD703100AF1-33-FA1: 157-pin plastic FBGA (14 × 14)
- μPD703101AF1-33-xxx-FA1: 157-pin plastic FBGA (14 × 14)
- μPD703102AF1-33-xxx-FA1: 157-pin plastic FBGA (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 230°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-103-2
★ VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds max. (at 200°C or higher), count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

- ★ (2) μPD703100AGJ-33-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
- μPD703100AGJ-40-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
- μPD703101AGJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
- μPD703102AGJ-33-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	IR35-103-2
★ VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds max. (at 200°C or higher), count: Two times or less, Exposure limit: 3 days <sup>Note</sup> (after that, prebake at 125°C for 10 hours)	VP15-103-2
Partial heating	Pin temperature: 300°C max., Time: 3 seconds max. (per pin row)	—

**Note** After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

[MEMO]

## NOTES FOR CMOS DEVICES

## ① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

## ② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

## ③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Related Documents**  $\mu$ PD70F3102-33 Data Sheet (U13844E)  
 $\mu$ PD703100-33, 703100-40, 703101-33, 703102-33 Data Sheet (U13995E)  
 $\mu$ PD70F3102A-33 Data Sheet (U13845E)

**Reference Materials** Electrical Characteristics for Microcomputer (U15170J<sup>Note</sup>)

**Note** This document number is that of Japanese version.

**The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.**

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- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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