SANDCRAFT

ENGINES FOR THE DIGITAL AGE™

PRELIMINARY

SR71040A

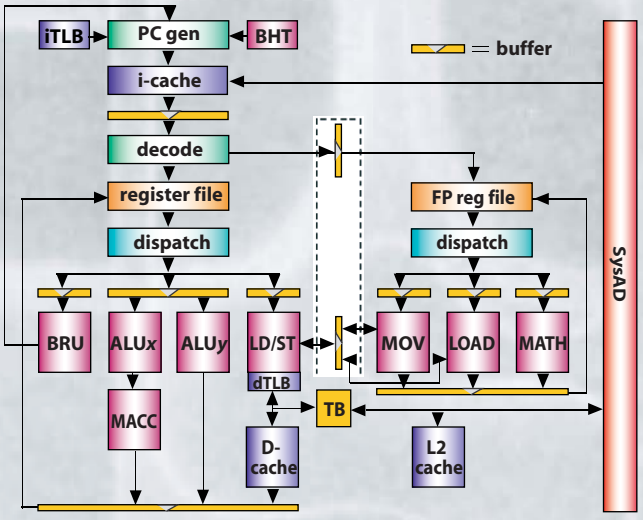
MIPS64™ SUPERSCALAR MICROPROCESSOR

The SR71040A microprocessor is a MIPS64-™ compatible processor based on the proven 0.15u SR71010A design.

The product provides a low cost, high-performance MIPS64-compatible processor to enable a new class of processor-based embedded systems, and also to provide an upgrade path for users of R4000- and R5000-class processors in low- to mid-range embedded systems.

The SR71040A microprocessor comprises the following features:

- 600 to 800MHz two-way superscalar 9 stage pipeline with out of order executions and hardware branch prediction.
- Primary instruction and data caches are both 16KB, and 2-way set associative
- On-chip secondary cache is 128KB and is 4-way set associative
- 133MHz SysAD bus interface
- IEEE 754 compatible floating point unit
- The SR71040A is available in two speed grades of 600MHz and 800MHz in a 256 pin TBGA package.



SR71040A Architecture Block Diagram

High performance architecture
- Fully MIPS64 Instruction Set Architecture (ISA) compliant

True 2-way superscalar architecture
- Dual fetch, dual dispatch, up to 6-issue, up to 6-execute, dual-commit
- Maximum operation rate of pipeline: 2 instructions per cycle
- Out-of-order issue and dispatch
- In-order retires

9-stage pipeline for high clock frequency
- Optimized pipeline bypass architecture for minimizing instruction interdependent stalls

Intelligent dynamic branch prediction
- Bi-modal 3Kbit table, Branch predictor
- Keeps pipeline full and minimizes branch mis-predict penalties
- Speculative execution down predicted paths
- Maximizes sustainable performance

Low power consumption
- Fully static design
- Clock enabled registers for improved power management
- Dynamic activation of sense amps. in caches

High-performance system interface
- Compatible with R4xxx/5xxx/7xxx SysAD interface
- 133 MHz with split transactions and out-of-order return

High-performance floating point
- Fully MIPS64 compliant
- IEEE - 754 compatible
- Decoupled from Integer pipeline

Extended features:
- 10 interrupts, 64 dual-entry TLB
- Variable page sizes from 4 KBytes to 256 MBytes
- JTAG interface compatible with IEEE 1149.1

Cache Hierarchy

Primary Instruction Cache - (L1)
- 16 KB, 16 byte line
- 2-way set associative
- Line Locking

Primary Data Cache - (L1)
- 16 KB, 16 byte line
- 2-way set associative
- Line Locking
- Write Back, Write Through (Write-Allocate/No-Write-Allocate), Bypass L2-L3

Secondary Unified Cache - (L2)
- 128 KB on chip
- 4-way set associative
- 32-byte line, line locking

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SR71040 - 600-800 MHz

Core frequency	600MHz - 800 MHz
Instruction cache	16 KByte (2 way)
Data cache	16 KByte (2 way)
L2 cache	128 KByte (4 way)
SR71040A-XXX-2T	256 TBGA 600 - 800 MHz

Interface bus width (MIPS SysAD)	64-bit
Interface bus frequency	up to 133 MHz
Process	0.13um
Core VCC	1.2V
I/O VCC	3.3V or 2.5V

SR71040A-XXX-YY

- SR71040A: SandCraft Designator
- XXX: CPU Speed
- YY: Package Size, Package Type

DEVELOPMENT TOOLS

Compilers:	RedHat (Cygnus)
Operating system:	Wind River, Linux
Simulation tools:	SandCraft
Development boards:	SandCraft, Marvell

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