THOMSON-CSF
SEMICONDUCTEURS SPECIFIQUES

TH7426A/27A

NEAR INFRARED InGaAs LINEAR IMAGE SENSOR 300 PIXELS

DESCRIPTION

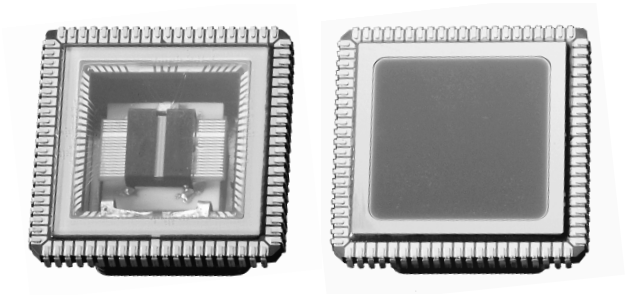
These devices are based on a 300 InGaAs photodiode linear array, with a 26µm pitch, using an in line pixel layout or a staggered pixel layout.

Two 150:1 CCD multiplexor chips, offering memory and delayed readout capability, are hybridized on both sides of the photodiode array so as to build a complete module.

Specially designed to allow an accurate butting, those modules could be tied together on request so as to provide an array extension with only one dead pixel at the splice.

These devices are also available in a full CMOS interface version :

TH74KA26A/TH74KA27A or TH74KB26A/TH74KB27A.



MAIN FEATURES

- Near infrared spectral response: 0.8µm to 1.7µm
- Room temperature operation
- Low noise
- High detectivity, wide dynamic range (>10 000)
- High linearity, high Modulation Transfer Function (MTF)
- High output data rate : up to 6 MHz
- Intrinsic antiblooming
- Built in thermoelectric cooler and temperature sensor available
- Accurate mechanical indexes (ready to mount)

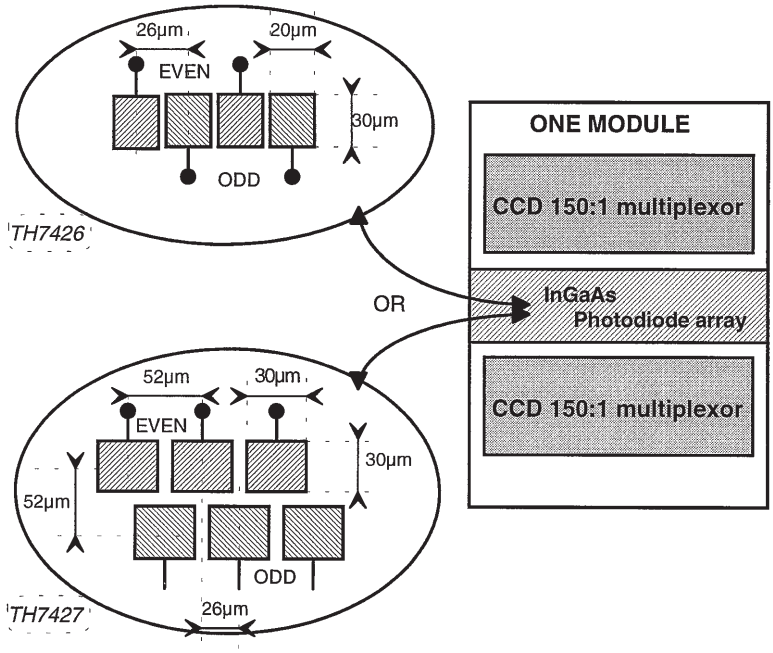
APPLICATIONS

- Suited for Near Infrared imaging
- Thermal imaging in the 200°C to 800°C range
- High resolution multichannel spectrometry
- Fluorescence free Raman spectrophotometry
- On-line inspection and monitoring

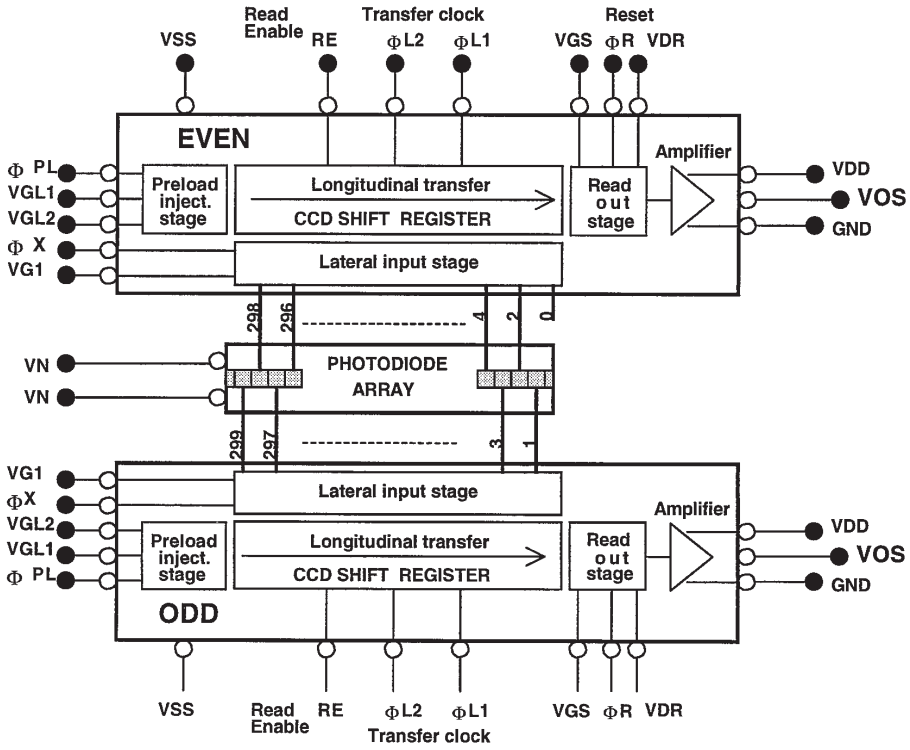
SELECTION GUIDE

REFERENCE	PIXEL COUNT	LAYOUT	PIXEL AREA	PITCH	NUMBER OF VIDEO OUTPUTS
TH7426A	299	In line	20x30µm²	26µm	2
TH7427A	299	Staggered	30x30µm²	26µm	2
TH7428A	599	In line	20x30µm²	26µm	4
TH7429A	599	Staggered	30x30µm²	26µm	4

GEOMETRICAL CHARACTERISTICS



ELEMENT BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Supply voltages (compare to Vss, at any pin)	0 to +20V
Transient voltages (compare to Vss, at any pin)	0 to +25V
DC current (at any pin),	10mA
Except - thermoelectric cooler pins	6A
- temperature sensor	+/-3mA
Operating temperature (temperature variation limited to 6°C/min)	-40 to +85°C
Storage temperature (temperature variation limited to 6°C/min)	-40 to +85°C
Electrostatic discharge sensitivity, MIL-STD-883 method 3015	device Class 1

Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent devices failure. Functionality at or above these limits is not implied. Exposure to maximum ratings for extended periods may affect device reliability.

To avoid any performance degradation,the device must be handled with grounded bracelet and stored in the conductive packing used for shipment.

TABLE 1 - ELECTRO-OPTICAL CHARACTERISTICS

15°C internal operating temperature, 3ms integration time, typical voltage input (otherwise specified).

Parameter	Symbol	TH 7426			TH 7427			Unit	Remarks
		Min.	Typ.	Max.	Min	Typ.	Max.		
Dark voltage signal mean isolated pixels (photodiode dark current)	 V_D (I_D)		 3 0.6	 100 		 4 0.8	 120 	 mV mV pA	 See Fig. 6 See note (1)
Noise in darkness (rms) mean isolated pixels	 σV_D		 200	 1		 200	 1.2	 µV mV	
Absolute photo response mean non uniformity non linearity over 1.5V range	 R PRNU 		 10 1	 +/-10 		 15 1	 +/-10 	 Vcm²/µJ % %	 See Fig. 3-4-5
Spectral response Cut-off wavelength Temperature shift	 λc dλc/dT	 1.66	 1.68 1.1	 1.73	 1.66	 1.68 1.1	 173	 µm nm/°C	 At 50% R(λ) max
Modulation transfer function across array along array	 MTF	 0.35 0.55	 0.50 0.68	 0.54 0.73	 0.35 0.35	 0.50 0.50	 0.54 0.54		At 19.2 lp/mm See note (2)
Output saturation voltage	Vsat	2.5			2.5			V	Depends on preload level. See Fig. 7
Noise equivalent power at λ=1.65µm	NEP		0.35 40 6.7			0.35 40 4.4		fW fW nWcm^{-2}	BW=1Hz BW=167Hz BW=167Hz
Specific detectivity at λ=1.65µm	D*		5.10^{12} 8.10^{11}			6.10^{12} 1.10^{12}		cmHz$^{1/2}$W^{-1} cmHz$^{1/2}$W^{-1}	BW=1Hz BW=167Hz
Electron to voltage conversion factor Quantum efficiency	Fc QE		0.26 0.8			0.26 0.8		µV/e e/ph	 See Fig. 5
Image grade (number of blemishes)	J K O E			1 5 10 NA			1 5 10 NA		See note (3) Electrical sample

Note : 1 Already taken into account in mean V_D ($V_D = \frac{Id\ TI\ Fc}{q}$; TI=Integration time ; q = 1.6 10^{-19} C)

Note : 2 "Maximum value" is the theoretical value computed using the corresponding diode size

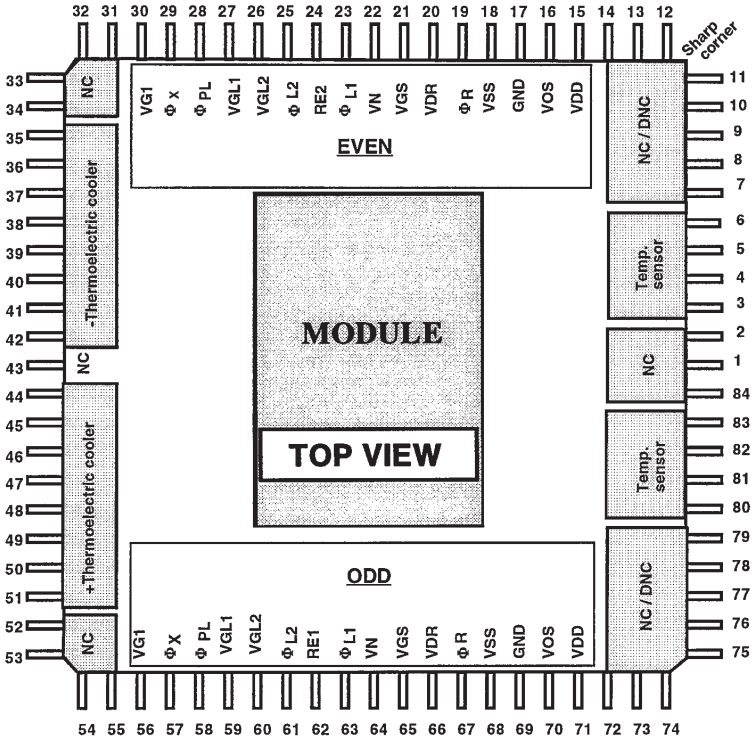
Note : 3 a pixel is considered as a blemish if :

- its dark voltage is higher than isolated pixel max value
- or - its noise is higher than isolated pixel noise max value
- or - its PRNU is higher than +/- 10 %

TABLE 2 - CONNECTION DIAGRAMS

Pin n°	EVEN Module #	Symbol	Designation	Pin n°	ODD Module #	Symbol	Designation
1...2		NC	Not connected	44...51		TC+	Thermoelectric cooler (positive node) see notes (2) (3)
3...6		TS	Temperature sensor see note (3)	52...55		NC	Not connected
7...9		NC	Not connected	56	O	VG1	Lateral skimming gate bias
10		DNC	Do not connect see note (4)	57	O	ϕX	Photodiode lateral transfer clock
11...14		NC	Not connected	58	O	ϕPL	Electrical injection clock
15	E	VDD	Output amplifier drain & RE supplies	59	O	VGL1	Preload skimming gate bias
16	E	VOS	Video output signal (pixels 0-298)	60	O	VGL2	Preload storage gate bias
17	E	GND	Video ground	61	O	ϕL2	Shift register clock 2 (gated by RE)
18	E	VSS	CCD substrate bias (phases return)	62	O	RE	Read enable control signal (pixels 1-299)
19	E	ϕR	CCD reset clock	63	O	ϕL1	Shift register clock 1
20	E	VDR	Reset bias	64	O	VN	Photodiode substrate bias see note (1)
21	E	VGS	Output gate bias	65	O	VGS	Output gate bias
22	E	VN	Photodiode substrate bias see note (1)	66	O	VDR	Reset bias
23	E	ϕL1	Shift register clock 1	67	O	ϕR	CCD reset clock
24	E	RE	Read enable control signal (pixels 0-298)	68	O	VSS	CCD substrate bias (phases return)
25	E	ϕL2	Shift register clock 2 (gated by RE)	69	O	GND	Video ground
26	E	VGL2	Preload storage gate bias	70	O	VOS	Video output signal (pixels 1-299)
27	E	VGL1	Preload skimming gate bias	71	O	VDD	Output amplifier drain & RE supplies
28	E	ϕPL	Electrical injection clock	72...75		NC	Not connected
29	E	ϕX	Photodiode lateral transfer clock	76		DNC	Do not connect see note (4)
30	E	VG1	Lateral skimming gate bias	77...79		NC	Not connected
31...34		NC	Not connected	80...83		TS	Temperature sensor see note (3)
35...42		TC-	Thermoelectric cooler (negative node) see notes (2) (3)	84		NC	Not connected
43		NC	Not connected				

Notes : 1 Pin 22 and 64 are internally connected together.
Notes : 2 In each group every pins must be connected and tied together in order to lower pin current density
Notes : 3 Not connected on non cooled package
Notes : 4 DNC (Do Not Connect). Pins which are internally connected and must not be used.



PIN DESCRIPTION

Odd and Even channels are fully independent, therefore same pin function will be found on odd and even sides.

Φ_{PL} This is the preload injection stage electrical input. Each Φ_{PL} pulse down overfills preload storage capacitance with electrons. Φ_{PL} is connected to a diode cathode which anode is internally tied to Vss.

V_{GL1} This is the preload stage skimming gate. Its bias determines the voltage up to which preload storage capacitance will be biased. Thus it drives preload level.

V_{GL2} This is the storage capacitance grid bias. It determines the bottom voltage of preload storing well, while V_{GL1} determines its top level. Preload capacitance thus is charged up proportionately to (V_{GL2} - V_{GL1}) bias difference.

Φ_{L1} This is the main register storage grid clock. Charges are stored under Φ_{L1} when transfer is disabled (RE at low level). Φ_{L1} is also used for lateral transfers to input nodes.

Φ_{L2} This is the main register transfer grid clock. Φ_{L2} is used to isolate Φ_{L1} content during lateral transfers. The main register is beginning and ending with Φ_{L2} which therefore controls main register access and outputs. Φ_{L2} is gated by RE input, it is internally pulled down when RE is low, preventing transfers, preload injection, read out and isolating each Φ_{L1} well.

RE This is the “Read Enable” input. When high, it allows Φ_{L2} input connection to main register, when low, main register corresponding grids are pulled down whatever Φ_{L2} input level is.
This input helps to serially read out two or more multiplexors with one single Φ_{L2} signal for all. Data are stored into the main register as long as RE is low, thus read out can occur later on.

Φ_X This is the lateral transfer grid command. Lateral transfer is allowed when Φ_X is at high level. Φ_X is common to all input nodes, all photodiode information is collected at the same time.

V_{G1} This is the lateral input stage skimming grid bias. This grid determines photodiodes reset bias, always the same from integration time to integration time. After photodiode reset (input node capacitance reset) extra charges leading to overcrossing V_{G1} level are skimmed back into Φ_{L1} main register wells.

V_N This is the InGaAs photodiode common cathode bias. V_N is available on odd and ev en side, however, both pins are connected together, to photodiode substrate.

V_{GS} This is main register output grid bias. It is used to isolate read out capacitance from main register. It allows charges to be read out when Φ_{L2} is at low level.

V_{DR} This is the read out capacitance reset bias. After each single read out, read out capacitance is cleared off (reset) to V_{DR} level, during Φ_R clock high state.

V_{DD} This is the output amplifier power supply (high side). It also supplies the “Read Enable” switching device which explains that I_{DD} is different whether RE is at high or low level.

G_{ND} This is the output amplifier low side power supply. G_{ND} is linked to V_{SS} through a diode, G_{ND} being the cathode node. Thus G_{ND} must always be more positive than or equal to Vss.
It must be noticed that “RE” switching device is powered from V_{DD} to V_{SS}. G_{ND} is specific to output amplifier.

V_{OS} This is the amplifier output.

V_{SS} This is the CCD multiplexor substrate bias. All applied biases and clock levels must be more positive or equal to V_{SS} .

T_S These are the internal temperature sensor connections. Temperature sensor is floating with respect to all other pin connections. Pins 3 to 6 are internally connected together as well as pin 80 to 83.

TC+ This is the internal thermoelectric cooler positive input (current enters) (all pins must be externally connected in order to lower current density into each pin).

TC- This is the internal thermoelectric cooler negative input (current goes out). Thermoelectric cooler connections are floating, with respect to all other pins. All pins must be externally connected in order to lower individual pin current density. It is advised to avoid pulsed current regulations to drive TE cooler, since it may result in EMC troubleshooting inside component cavity.

FUNCTIONAL DESCRIPTION

Individual InGaAs diodes are reversed bias. The cathode node is common to all diodes and connected to a fixed potential Vn. The anode of each diode is wire bonded to a lateral entrance of the readout CCD stage.

These diodes behave as capacitors whose leakage current depends on dark current and illumination. This current tends to decrease the voltage across the capacitor. Each diode capacity is first preloaded with a calibrated amount of negative charges (Qb). After an integration time (TI), the amount of removed charges (QI) figures out the cumulated light absorption. So the measurement of the remaining charge amount (Qs) in the diode capacitor gives access to QI (QI = Qb - Qs). This is called “Vidicon” readout mode.

CCD multiplexors fulfill all those operations. They provide preloading and readout functions for the separate odd and even pixel groups. The main CCD features consist in a two phase register (ϕ_{L1} and ϕ_{L2}) with longitudinal and lateral transfer capability. Following is a description of how those devices keep photodiodes under control and capture pixel signals.

Four main functions can be considered :

- Preload

The potential gap between the two gates [V_{GL1}-V_{GL2}] defines a potential well for preload calibration (Qb), its filling and spilling occurs using an injection diode ϕ_{PL}.

- Main register charge handling

At each individual transfer step, Qs moves out of the 150th stage, while Qb moves in the first stage. The longitudinal register stage requires a series of at least 150 steps to complete the preloading cycle. This transfer operation is inhibited if RE (read enable) input is maintained at a low level.

- Photodiode information collection (and reset)

The lateral input stage consists in 150 input diodes, each of them directly wire bonded to one photodiode, and controlled under a single common biasing gate V_{G1} and a lateral transfer gate ϕ_X.

At the end of integration time (see timing diagram Figure 1) :

- the preload charges Qb, stored in the register, are transferred simultaneously to the 150 photodiodes when ϕ_X is at high level and ϕ_{L1} at low level, allowing the photodiode reset.

- charges in excess (identified as Qs) are collected back to the register by forcing ϕ_{L1} at high level. At this step the register current information is the mirror image of the collected photo signal and, all photodiodes are reseted while a new TI starts.

To isolate each stage from the other one, ϕ_{L2} must be at low level during all lateral transfer operations.

- Data read-out

At the end of the photodiode reset operation :

- if RE is forced to low level (Timing Diagram - Figure 1), all Qs information remain stored in the register and so, readout is delayed .According to this situation a next photodiode reset procedure can’t be operated until the full longitudinal transfer takes place (150 steps minimum).

- if RE is activated or always at high level (Timing Diagram - Figure 2), each stored charge is transferred to the readout capacitance; this continuous readout mode is recommended for long integration time.

Qs conversion into voltage is supported by the readout stage capacitance, linked to a low output impedance amplifier. This capacitance is reset at V_{DR} bias, before each pixel readout operation (high level ϕ_R).

Due to the “Vidicon” read out mode, Qb level needs adjustment so as to provide enough carriers to sustain photocurrent and dark current during the integration time. Pixel antiblooming is also resulting from “Vidicon mode” since photodiodes cannot consume more electrons than Qb.

Antismearing (frame to frame antiblooming) efficiency depends on the photodiode reset conditions, reverse bias recovering need a minimum Qb condition such as :

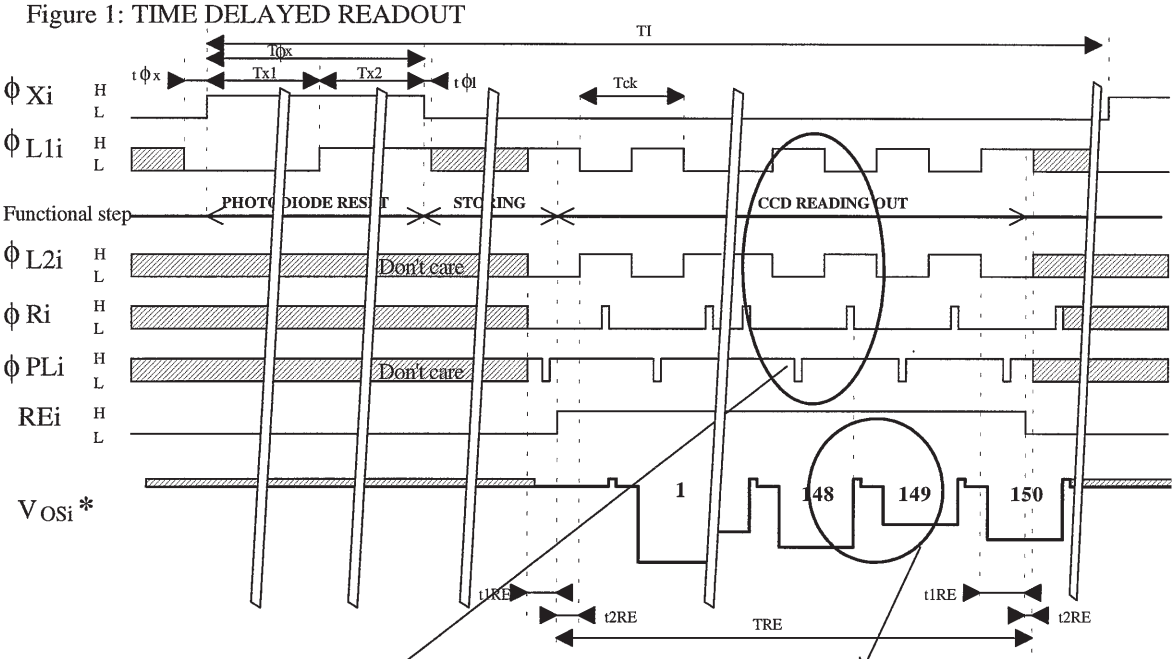
$$Qb > Clat \cdot V_D$$

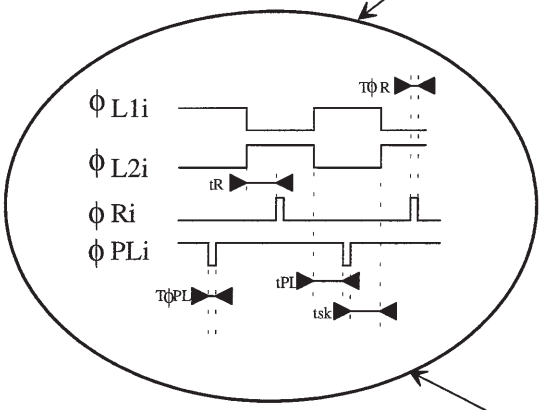
where : - Clat is the individual lateral input node capacitance, Clat ~1.5 pF (including photodiode, bonding pads...)

- V_D is the photodiode bias : $V_D = V_N - 0.78V_{G1} - 8.7$

MULTIPLEXOR TIMING DIAGRAM

Figure 1: TIME DELAYED READOUT





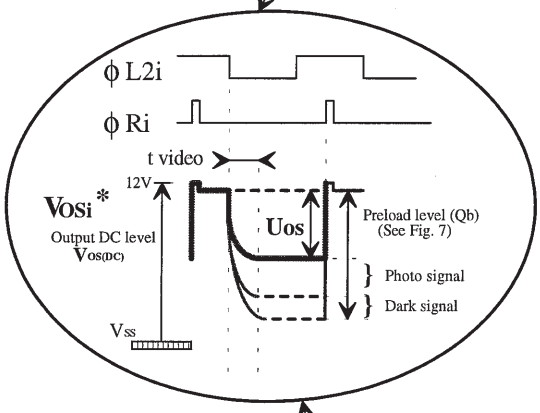
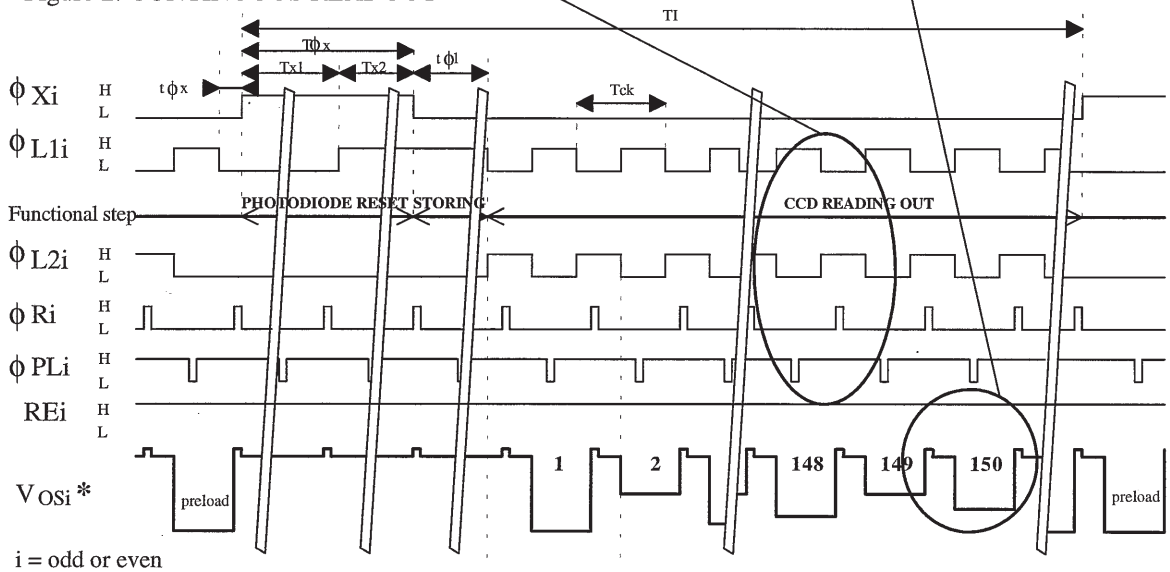


Figure 2: CONTINUOUS READOUT



* First Even output data is always at preload level (multiplexor corresponding input is not connected — See “Element Block Diagram”)

TABLE 3 - STATIC CHARACTERISTICS

Symbol	Pin n° EVEN/ODD	Function	Value			Unit	Note
			Min	Typ	Max		
V_{DD}	15/71	Output amplifier	17.5	18	18.5	V	(1)
I_{DD}		with Read Enable disabled with Read Enable activated		0.7 1.1		mA mA	(2)
V_{DR}	20/66	Reset bias	15.3	15.5	16.5	V	(1)
V_N	22/64 internally connected	Photodiode substrate bias	11	11.3	11.5	V	
G_{ND}	17/69	Video ground	0		2	V	(3)
V_{SS}	18/68	Register substrate				V	
V_{G1}	30/56	Lateral skimming gate	1.9	2	2.1	V	
V_{GL1}	27/59	Preload skimming gate	2.8	3	5	V	(4)
V_{GL2}	26/60	Preload storage gate	3	4	5	V	(4)
V_{GS}	21/65	Register output gate	6.2	6.5	7	V	

Note : 1 V_{DD}-V_{DR} >1.8V
Note : 2 For each V_{DD} Pin
Note : 3 Recommendation: tied to V_{SS} or, for best operation, hold at +0.5V above V_{SS}
Note : 4 V_{GL1} and V_{GL2} are used to calibrate preloading level see Fig. 7; to minimise noise effect, it is recommended to get V_{GL1} and V_{GL2} from the same low noise supply.

TABLE 4 - DYNAMIC CHARACTERISTICS

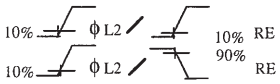
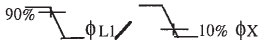
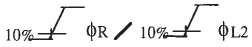
Symbol	Pin n° EVEN/ODD	Function	Value			Unit	Note
			Min	Typ	Max		
Φ_{L1} low high	23/63	Longitudinal transfer stage (120 pF typical)	0.1 9	0.3 9.5	0.7 10.5	V V	
Φ_{L2} low high	25/61	(120 pF typical if all RE enabled)	0.1 9	0.3 9.5	0.7 10.5	V V	
Φ_{PL} low high	28/58	Preload injection diode (10 pF typ.)	5.8 9.5	6 12	6.7 12.5	V V	
Φ_R low high	19/67	Read out reset gate (10 pF typ.)	0.1 11.5	0.3 12	0.7 12.5	V V	
Φ_X low high	29/57	Lateral transfer stage (10 pF typ.)	0.1 7.8	0.3 8	0.7 8.2	V V	
RE low high	24/62	Read enable (15 pF typ.)	0.1 (Φ_{L2} high +2,5V)	0.2	0.4 15	V V	

TABLE 5 - MISCELLANEOUS DATA

Symbol	Pin n°	Function	Value			Unit	Note
			Min	Typ	Max		
I_{TH}	35 to 42 44 to 51	Thermo cooler		3	6	A	(5)
$V_{OS(DC)}$	16,7	Video signal DC level (wrt Vss)		12		V	(7)
Z_O		Output impedance		1.2		KΩ	(7)
Rpt (at 0°C)	3 to 6 80 to 83	Temperature sensor resistance (recommended max. current 1 mA)		100		Ω	(6)
F_P		Transfer frequency		0.5	3	MHz	

Note : 5 See Fig. 8a, 8b, 8c, 8d.
Note : 6 See Fig. 9.
Note : 7 Short circuit to Gnd or Vss exceeding 1 min duration may permanently damage the device

TABLE 6 - TIMING AND SWITCHING CHARACTERISTICS

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
INTEGRATION TIME	TI	0.05	3		ms	
CLOCK PERIOD	Tck	0.33	2		µs	(3)
READ ENABLE Duration	TRE		$149.5Tck+t1_{RE}+t2_{RE}$		µs	
Rise time or fall time	tr/tf		25	250	ns	(4)
Delay 	t1RE	0	120		ns	
Set-up RE 	t2RE	150	850		ns	
LATERAL TRANSFER Duration	TΦx	5	22		µs	
Φx rise time or fall time	tr/tf		25	150	ns	(4)
Φ1 low level hold time	Tx1	1	1.7		µs	
Φ2 low level hold time	Tx2	4	20		µs	
Delay 	tΦx	100	980		ns	
Readout delay 	tΦ1	100	200		ns	
LONGITUDINAL TRANSFER ΦL1 rise time or fall time	tr/tf		25	150	ns	(4)
ΦL2 rise time or fall time	tr/tf		25	150	ns	(4)
Preload duration	TΦPL	35	240		ns	
Preload rise time or fall time	tr/tf		25	50	ns	(4)
Preload delay 	tPL	0	80		ns	
Skimming time 	tsk	70	500		ns	(1)
READOUT DIODE RESET Duration	TΦR	35	240		ns	(2)
Rise time or fall time	tr/tf		25	120	ns	(4)
Delay 	tR	0	10		ns	(2)
VIDEO SIGNAL SET-UP TIME	t_{video}		100		ns	

Note : 1 Better if no clock transition occurs during “tsk” time.
Note : 2 tR + TΦR < ΦL2 high level duration.
Note : 3 Duty cycle: 50%
Note : 4 Rise time (tr) and fall time (tf) specified between 10% and 90%

ELECTRO-OPTICAL TYPICAL CHARACTERISTICS

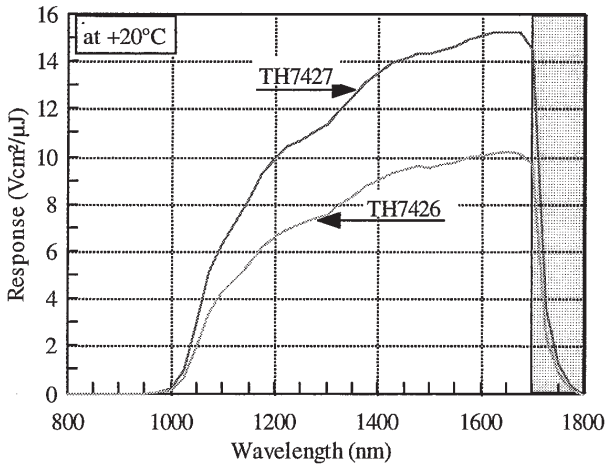


Figure 3 : Silicon Window typical spectral response

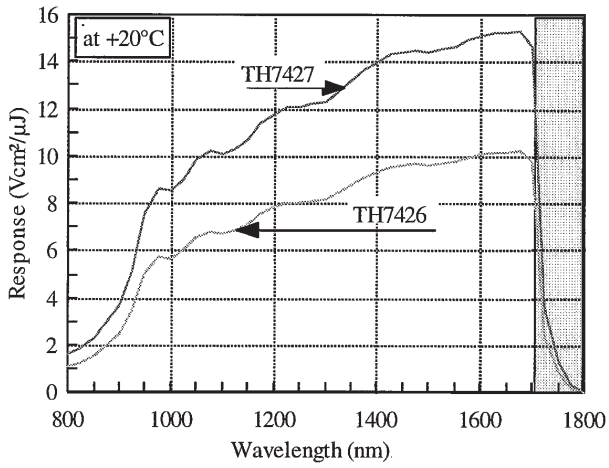


Figure 4 : Clear window typical spectral response

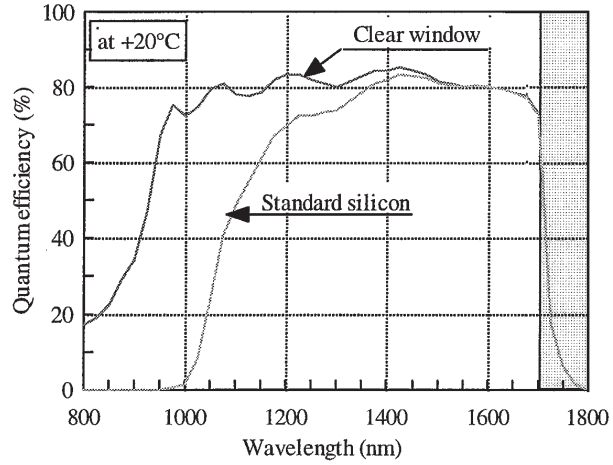


Figure 5 : Clear window & Silicon window quantum efficiency

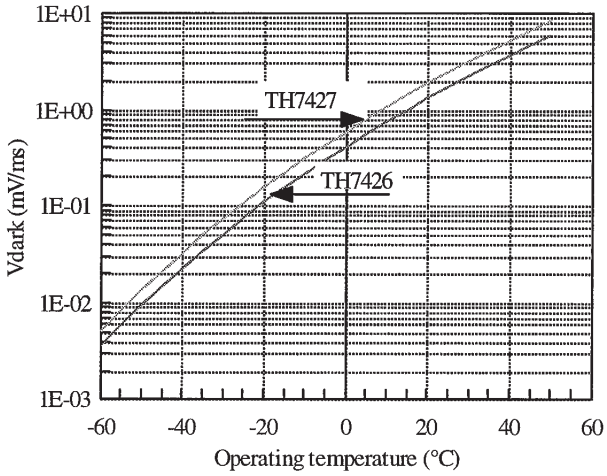
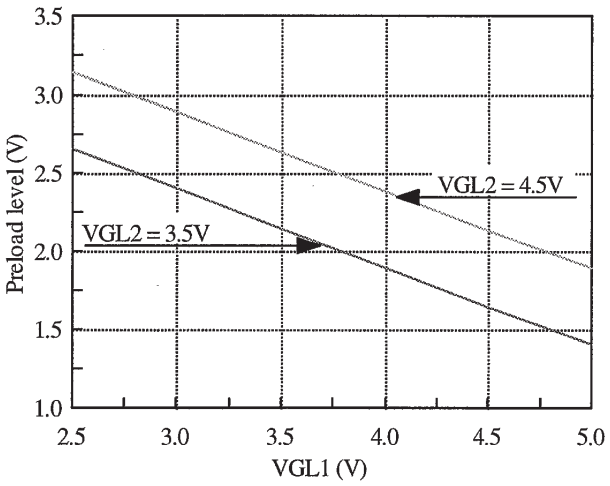


Figure 6 : Dark voltage per 1ms integration time vs internal operating temperature



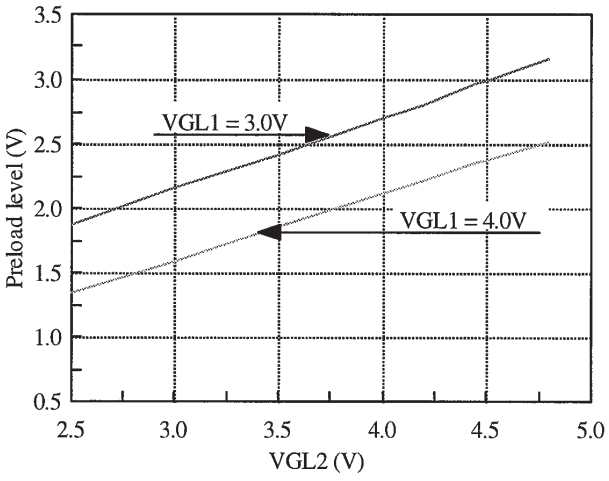


Figure 7 : Typical preload voltage vs V_{GL1} and V_{GL2} gate voltages

THERMAL CHARACTERISTICS (single stage TE cooled package -subvariant N- only)

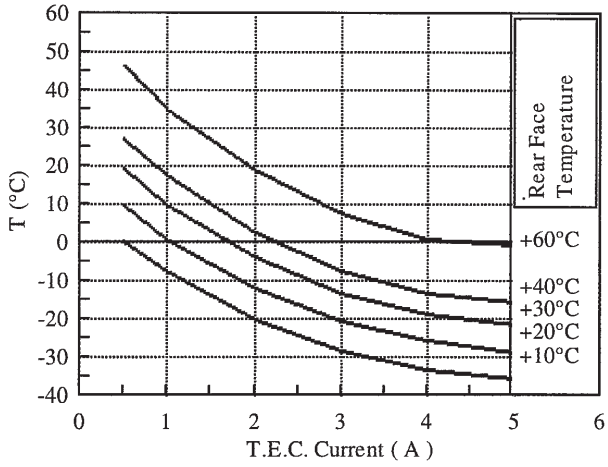


Figure 8a : Internal temperature vs Thermo-electric cooler current

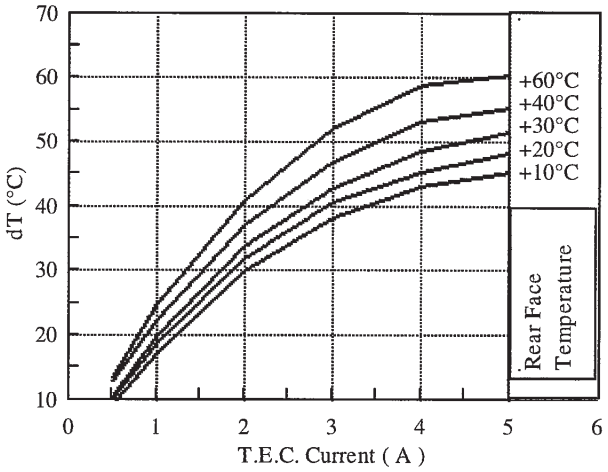


Figure 8b : Internal to rear face temperature gap vs Thermo-electric cooler current

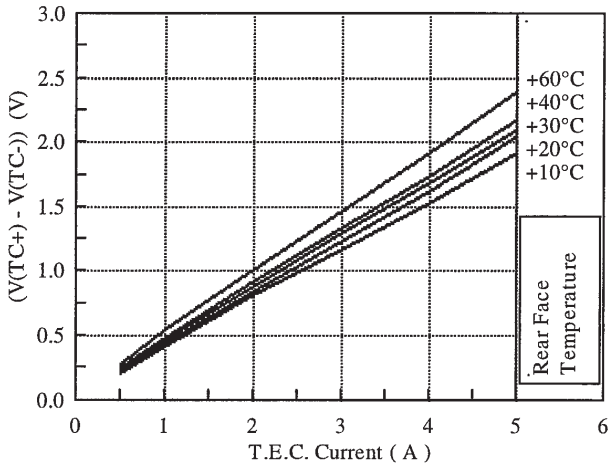


Figure 8c : Thermo-electric cooler voltage vs. Thermo-electric cooler current

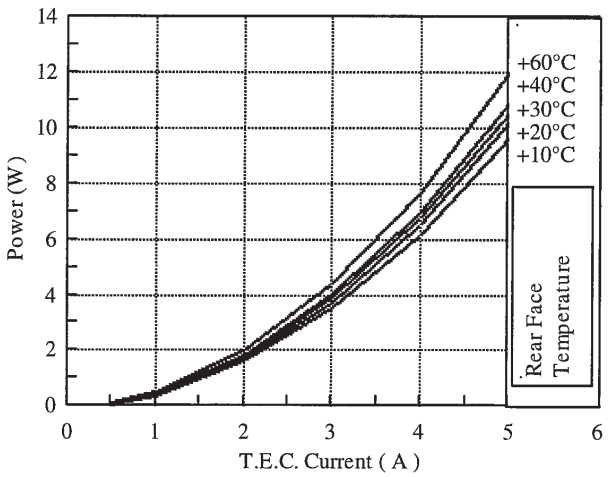


Figure 8d : Rear face power dissipation vs. Thermo-electric cooler current

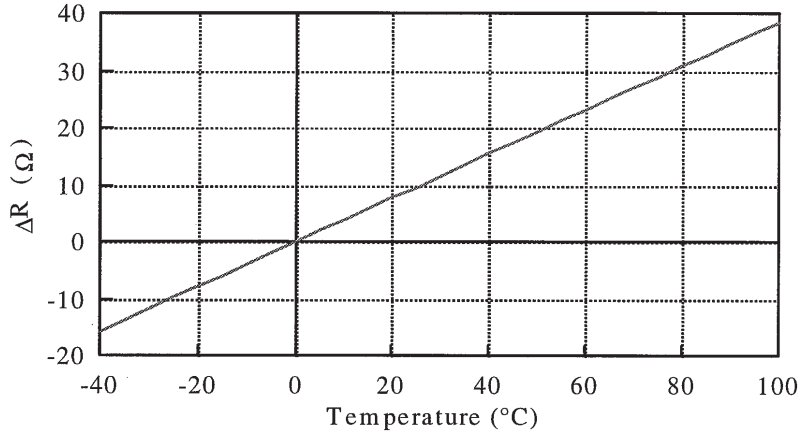


Figure 9 : Pt resistance variation R = R(T°C) - R(0°C) vs. temperature

T°C<0 $Rpt = 100 \{1+[3.90802\ 10^{-3}\ T] - [0.580195\ 10^{-6}\ T^2] - [4.7350\ 10^{-12}(T-100)\ T^3]\}$

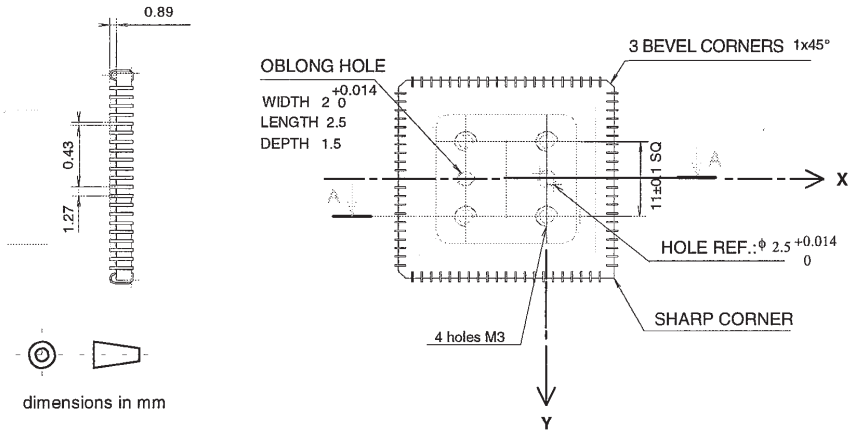
T°C>0 $Rpt = 100 \{1+[3.90802\ 10^{-3}\ T] - [0.580195\ 10^{-6}\ T^2]\}$

OUTLINE DRAWING

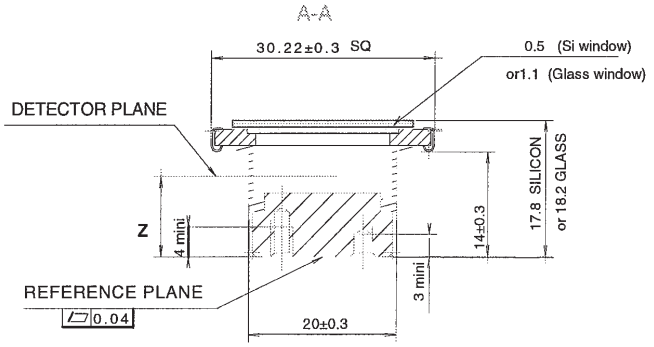
In the standard version devices are hermetically sealed in a Jlead 84 like package with a near IR transparent window (see next drawing). The package basement includes a thermoelectric cooler and a temperature sensor, see Figures 8-9 for thermal characteristics.

Silicon, with an antireflective coating is the window material. An optional version used an AR coated glass and an additional frame (numerical aperture f/3) to prevent parasitic lateral visible light.

The photodiode array location is mechanically indexed upon the package rear face (opposite to the window) for fast accurate mounting.

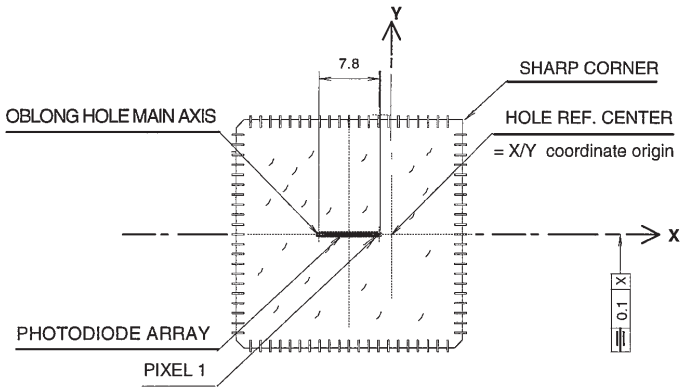


Z ARRAY LOCATION
Z (optic) = 15.56±0.15
both windows



X, Y ARRAY LOCATION

Pixel 1	x	y
TH7426	-1.57	0
TH7427	-1.57	-0.03



PACKAGE VARIANT (N)
(Thermoelectric cooler version)

ORDERING INFORMATION

T	H	7	4	2	6	A	V(1)	W(2)	a*	b*	c*	G	d*
T	H	7	4	2	7	A	V(1)	W(2)	a*	b*	c*	G	d*

(1) Temperature range
V = -40 to 85°C (see § c*)

(2) Package family
Ceramic Jlead type

a* **Image grade**
J, K, O, E see Table 1

b* **Package variant**
S = standard silicon window
R = clear glass window
N = non sealed removable window

c* **Package sub-variant**
(The detector temperature depends on the surrounding ambient and on device energy budget which is directly related to the built in thermo-cooler option efficiency.)

- = without thermo-electric cooler; from -40 to +15°C full performances(derated over)
N = 1 stage thermo-electric cooler; from -40 to +60°C full performances (derated over)
P = 3 stages thermo-electric cooler; from -40 to +85°C full performances

d* **Quality level**
- = standard
D/T = industrial level
B/T = military levels
S = space level

APPLICATION INFORMATION

- Preload generation

Preload is fed up when Φ_{PL} is at low level. This process needs few time to be completed (>35 ns). Then skimming is needed to calibrate Qb. This step needs as much as possible time. Therefore it is recommended to activate Φ_{PL} as soon as Φ_{L2} is at low level, in order to spend most of Φ_{L2} low level duration for skimming.

Qb depends on (V_{GL2} - V_{GL1}) difference, thus noise on Qb may result from differential fluctuations between V_{GL1} and V_{GL2}. It is therefore recommended to get V_{GL1} and V_{GL2} biases on each side (Odd or Even) from the same power supply line.

- Preload level adjustment

Preload level must be chosen so as to covered both expected maximum signal and dark current resulting signal. It must be noticed that the “Vidicon mode” implies output signal has the largest amplitude in darkness (since most of Qb is to be readout).

Since output signal treatment difficulty may arise from its large amplitude it is better to reduce as much as possible its dynamic, thus to reduce preload level to the minimum required.

From Figure 6, dark voltage can be deduced, photosignal is computed from Figures 3 & 4 and application data (light flux, integration time). Preload must be 200 mV in excess to dark voltage and maximum photosignal sum. Preload can be adjusted with (V_{GL2} - V_{GL1}) biases, as indicated in Figure 7, however it is recommended to act first on V_{GL2}. Direct read out of preload level is possible in forcing Φ_X at low level avoiding lateral transfer and photodiode read out.

TH7426A/27A maximum preload is about 2.5 V (corresponding to 10^7 electrons).

- Photodiode information collection

As explained this operation needs two steps :

a). Qb injection into input nodes.

b). Skimming back into main register of extra charges.

Step a) needs at least 1 µs to be completed (TX1). However, step b) is a longer process, which duration influences lateral transfer efficiency. It has been measured that 20 µs is needed for less than 1 % transfer non efficiency which raises to 2 % for 4 µs skimming time (TX2).
Thus it is recommended to allow as long as possible skimming time, compatible with application requirement.

- Output signal format

Figures 1 and 2 give details on output signal. Each reset (Φ_R) pulse pulls up the output at reset level related to VDR bias. Using typical biases, reset level reaches about 12 volts with respect to Vss. Notice that Φ_R must be pulsed only when Φ_{L2} is at high level.

Just after reset pulse, output level is stabilizing to a steady level called “floating diode level”. This level is the very reset level to be taken into account for useful signal amplitude measurement. It is about 200 mV lower than reset level.

Then on Φ_{L2} falling edge, charges coming from main register last stage arrive. Consequently, output signal drops down. The new steady level reached, counted from “floating diode” level represents the useful information - Uos -

Uos amplitude is maximum when no lateral transfer has occurred, since it represents preload level. In darkness, after photodiode read out (lateral transfer) Uos is reduced by dark voltage signal. Under illumination Uos is still smaller until saturation occurs (whole preload consumption), in this situation “floating diode” level is maintained until next pixel readout.

- Read enable operation

RE input simplifies device operation since it allows to use continuous Φ_{L2} clocks. However, one can force RE at high level and generate external Φ_{L2} interruption during Φ_X transfer. In this case, first pixel data will be read out at first falling edge of Φ_{L2}. After 150 Φ_{L2} periods all pixel data will have been read out, on 151^{st} Φ_{L2} period, output will be unused preload and so on until next Φ_X cycle.

When using RE input, it must be noticed that RE duration must at least allow 150 main register transfers (Φ_{L2} periods) in order to guaranty that all main register stages contain a preload (Qb) before next Φ_X cycle. Otherwise all photodiodes will not be properly reset at next Φ_X cycle.

When RE is low, output signal is continuously at floating diode level, with Φ_R transparencies.

- Interlacing odd even

As odd and even sides are fully separated, it is possible to drive odd and even side with 180° phase shifted Φ_{L1} and Φ_{L2} (Φ_{PL} , Φ_R with same phase with respect to their Φ_{L2}), Φ_X being identicals. In this manner Odd output signals will be delayed by half a Tck period with respect to Even outputs allowing, after common sampling, natural multiplexing and double pixel data rate. This opportunity is presented in application hints (Figures 10 to 12).

- Mechanical mounting

Accurate mechanical references are provided in N and P subvariant packages (see ordering information and outline drawings). If optics are mechanically referred to these packages rear face, no tuning strategy could be implemented for scale manufacturing.

APPLICATION HINTS

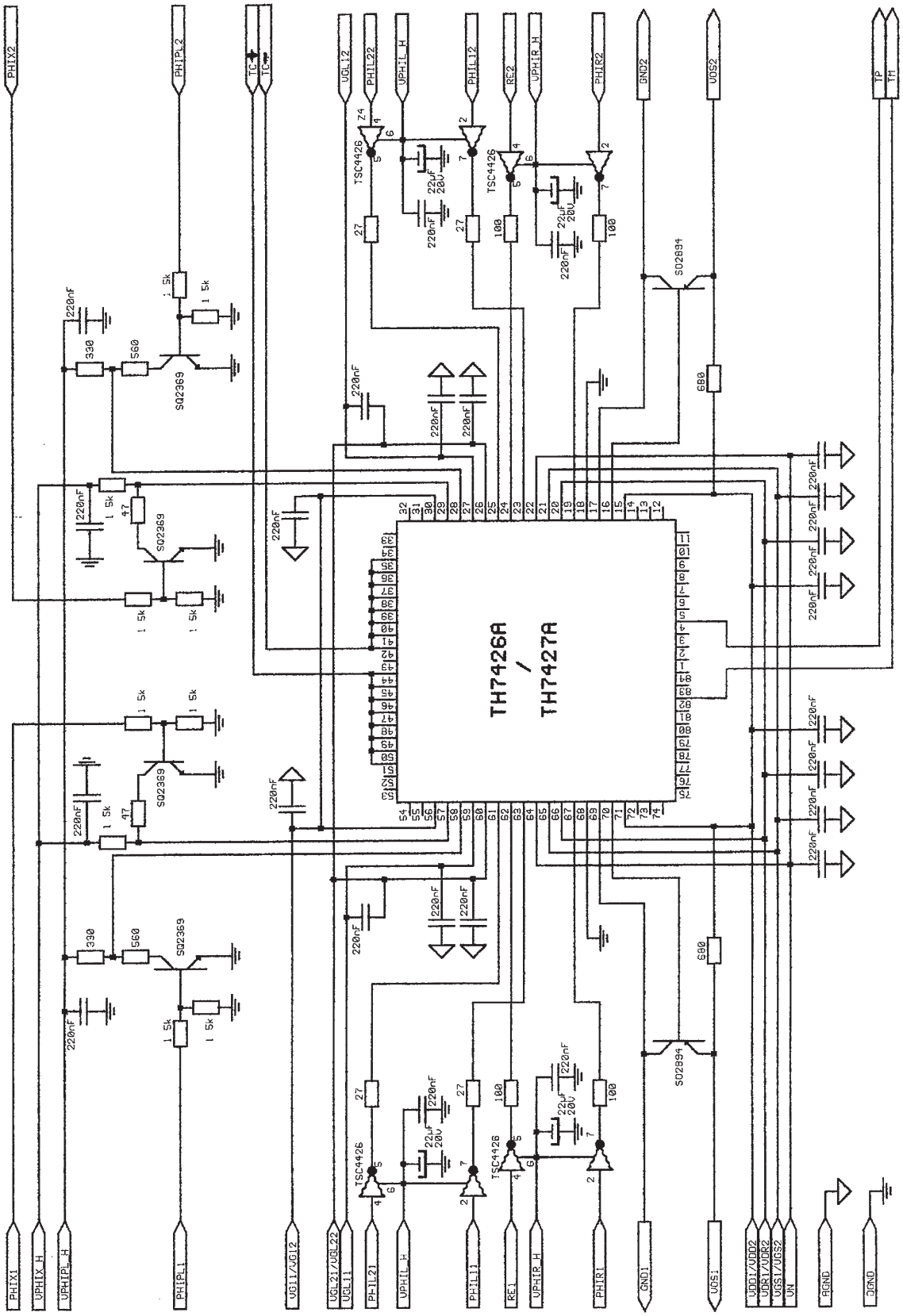


Figure 10 : Application hint : device operation

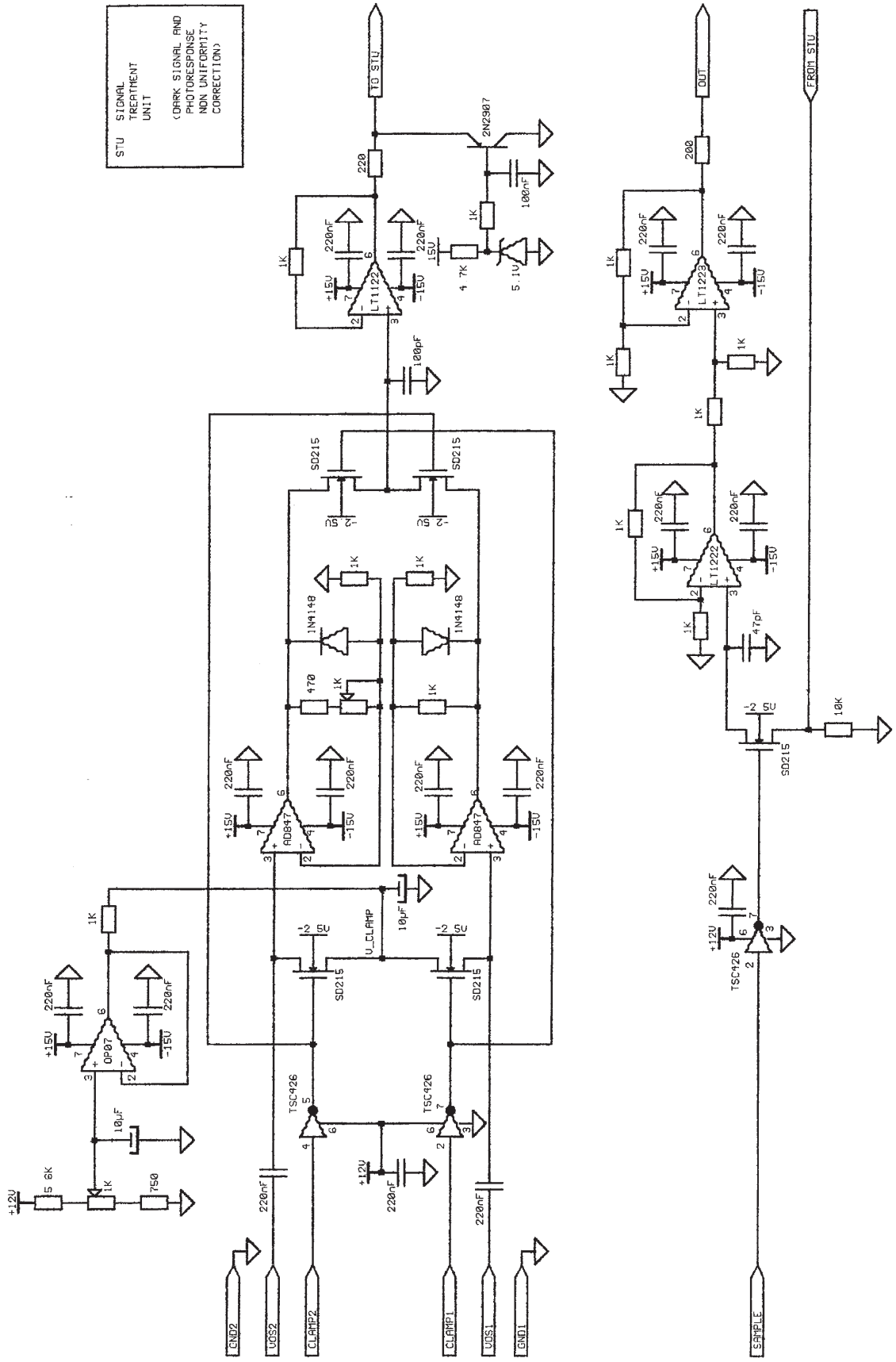
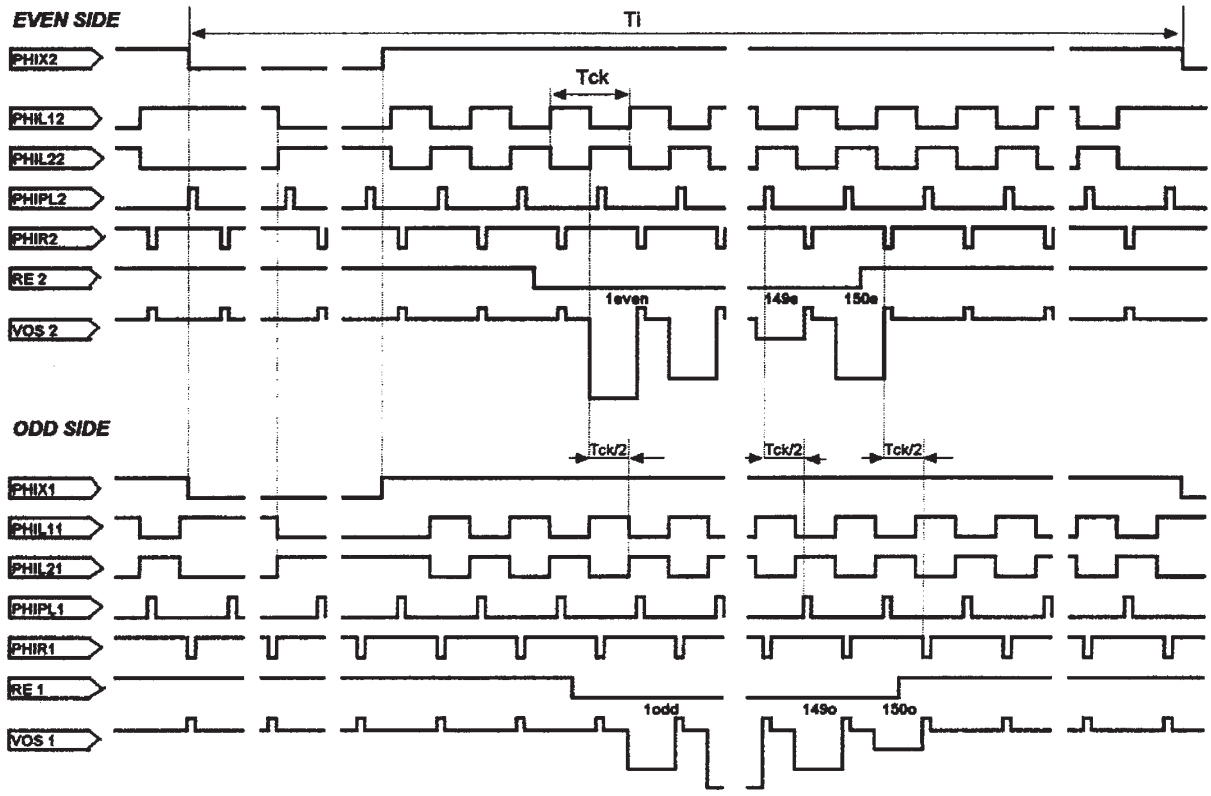
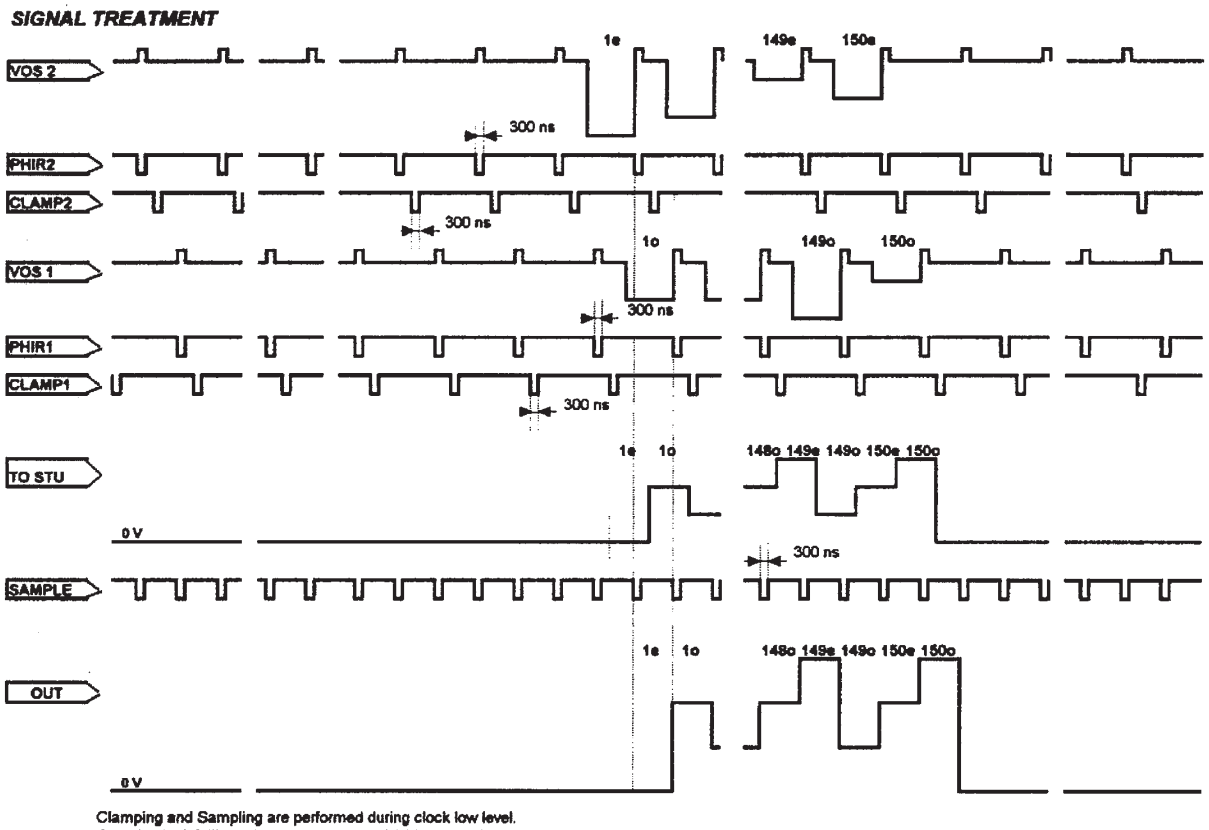


Figure 11 : Application hint : signal treatment



Even readout register clocks (PHIR2, PHIPL2, PHIL12, PHIL22, RE2) are delayed (of Tck/2) with respect to even clocks (PHIR1, PHIPL1, PHIL11, PHIL21, RE1)
PHIX1 and PHIX2 are identical.



Clamping and Sampling are performed during clock low level.
Sample clock falling edge corresponds to PHIR1 and PHIR2 falling edge.

Figure 12 : Timing diagramm for figure 10 &11 (Output data : 1 MHz)

NOTE

This product is manufactured by THOMSON-CSF SEMICONDUCTEURS SPECIFIQUES - 38521 SAINT-EGREVE / FRANCE.

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