

# MC100EP16VC

## 3.3V / 5V ECL Differential Receiver/Driver with High Gain and Enable Output

The EP16VC is a world-class differential receiver/driver. The device is functionally equivalent to the EP16 and LVEP16 devices but with high gain and enable output.

The EP16VC provides an  $\overline{EN}$  input which is synchronized with the data input (D) signal in a way that provides glitchless gating of the QHG and  $\overline{QHG}$  outputs.

When the  $\overline{EN}$  signal is LOW, the input is passed to the outputs and the data output equals the data input. When the data input is HIGH and  $\overline{EN}$  goes HIGH, it will force the QHG LOW and the  $\overline{QHG}$  HIGH on the next negative transition of the data input. If the data input is LOW when the  $\overline{EN}$  goes HIGH, the next data transition to a HIGH is ignored and QHG remains LOW and  $\overline{QHG}$  remains HIGH. The next positive transition of the data input is not passed on to the data outputs under these conditions. The QHG and  $\overline{QHG}$  outputs remain in their disabled state as long as the  $\overline{EN}$  input is held HIGH. The  $\overline{EN}$  input has no influence on the  $\overline{Q}$  output and the data input is passed on (inverted) to this output whether  $\overline{EN}$  is HIGH or LOW. This configuration is ideal for crystal oscillator applications where the oscillator can be free running and gated on and off synchronously without adding extra counts to the output.

The  $V_{BB}$  pin, an internally generated voltage supply, is available to this device only. For single-ended input conditions, the unused differential input is connected to  $V_{BB}$  as a switching reference voltage.  $V_{BB}$  may also rebias AC coupled inputs. When used, decouple  $V_{BB}$  and  $V_{CC}$  via a 0.01  $\mu$ F capacitor and limit current sourcing or sinking to 0.5 mA. When not used,  $V_{BB}$  should be left open.

The 100 Series contains temperature compensation.

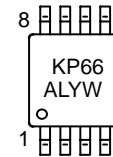
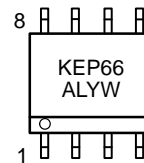
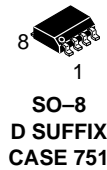
- 310 ps Typical Prop Delay  $\overline{Q}$ , 380 ps Typical Prop Delay QHG,  $\overline{QHG}$
- Gain > 200
- Maximum Frequency > 3 GHz Typical
- PECL Mode Operating Range:  $V_{CC} = 3.0$  V to 5.5 V with  $V_{EE} = 0$  V
- NECL Mode Operating Range:  $V_{CC} = 0$  V with  $V_{EE} = -3.0$  V to -5.5 V
- Open Input Default State
- QHG Output Will Default LOW with D Inputs Open or at  $V_{EE}$
- $V_{BB}$  Output



ON Semiconductor™

<http://onsemi.com>

### MARKING DIAGRAMS\*



K = MC100  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

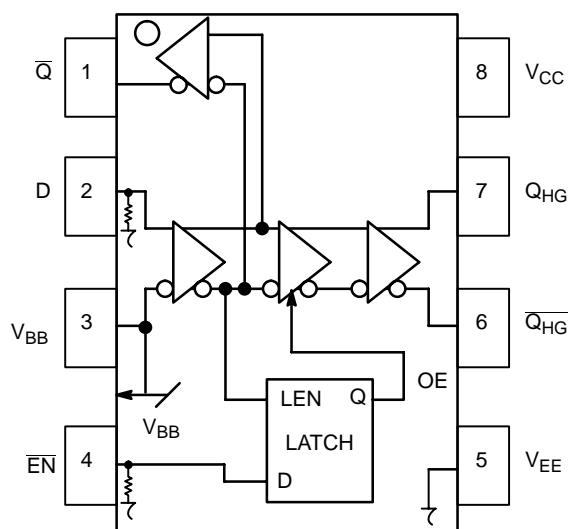
\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100EP16VCD	SO-8	98 Units/Rail
MC100EP16VCDR2	SO-8	2500 Tape & Reel
MC100EP16VCDT	TSSOP-8	100 Units/Rail
MC100EP16VCDTR2	TSSOP-8	2500 Tape & Reel

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

# MC100EP16VC



## PIN DESCRIPTION

PIN	FUNCTION
D*	ECL Data Input
$\bar{Q}$	ECL Data Output
$Q_{HG}, \bar{Q}_{HG}$	ECL High Gain Data Outputs
EN*	ECL Enable Input
$V_{BB}$	Reference Voltage Output
$V_{CC}$	Positive Supply
$V_{EE}$	Negative Supply

\* Pins will default LOW when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 k $\Omega$
Internal Input Pullup Resistor	N/A
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 4 kV > 200 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating Oxygen Index	UL-94 code V-0 A 1/8" 28 to 34
Transistor Count	167 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
$V_{CC}$	PECL Mode Power Supply	$V_{EE} = 0\text{ V}$		6	V
$V_{EE}$	NECL Mode Power Supply	$V_{CC} = 0\text{ V}$		-6	V
$V_I$	PECL Mode Input Voltage NECL Mode Input Voltage	$V_{EE} = 0\text{ V}$ $V_{CC} = 0\text{ V}$	$V_I \leq V_{CC}$ $V_I \geq V_{EE}$	6 -6	V V
$I_{out}$	Output Current	Continuous Surge		50 100	mA mA
$I_{BB}$	$V_{BB}$ Sink/Source			$\pm 0.5$	mA
TA	Operating Temperature Range			-40 to +85	$^{\circ}\text{C}$
$T_{stg}$	Storage Temperature Range			-65 to +150	$^{\circ}\text{C}$
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 SOIC	41 to 44	$^{\circ}\text{C}/\text{W}$
$\theta_{JA}$	Thermal Resistance (Junction to Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	$^{\circ}\text{C}/\text{W}$ $^{\circ}\text{C}/\text{W}$
$\theta_{JC}$	Thermal Resistance (Junction to Case)	std bd	8 TSSOP	41 to 44	$^{\circ}\text{C}/\text{W}$
$T_{sol}$	Wave Solder	<2 to 3 sec @ 248 $^{\circ}\text{C}$		265	$^{\circ}\text{C}$

2. Maximum Ratings are those values beyond which device damage may occur.

# MC100EP16VC

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 3.3\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	25	36	45	30	40	50	32	42	52	mA
$V_{OH}$	Output HIGH Voltage (Note 4)	2105	2230	2355	2105	2230	2355	2105	2230	2355	mV
$V_{OL}$	Output LOW Voltage (Note 4)	1305	1430	1555	1305	1430	1555	1305	1430	1555	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	1355		1675	1355		1675	1355		1675	mV
$V_{BB}$	Output Voltage Reference	1725	1825	1925	1700	1800	1900	1675	1775	1875	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D EN	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

3. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +0.3 V to -2.2 V.

4. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

5.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, PECL $V_{CC} = 5.0\text{ V}$ , $V_{EE} = 0\text{ V}$ (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	25	36	45	30	40	50	32	42	52	mA
$V_{OH}$	Output HIGH Voltage (Note 7)	3805	3930	4055	3805	3930	4055	3805	3930	4055	mV
$V_{OL}$	Output LOW Voltage (Note 7)	3005	3130	3255	3005	3130	3255	3005	3130	3255	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	3775		4120	3775		4120	3775		4120	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	3055		3375	3055		3375	3055		3375	mV
$V_{BB}$	Output Voltage Reference	3425	3525	3625	3400	3500	3600	3375	3475	3575	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.0		5.0	2.0		5.0	2.0		5.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D EN	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

6. Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{EE}$  can vary +2.0 V to -0.5 V.

7. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

8.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## 100EP DC CHARACTERISTICS, NECL $V_{CC} = 0\text{ V}$ ; $V_{EE} = -5.5\text{ V}$ to $-3.0\text{ V}$ (Note 9)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$I_{EE}$	Power Supply Current	25	36	45	30	40	50	32	42	52	mA
$V_{OH}$	Output HIGH Voltage (Note 10)	-1195	-1070	-945	-1195	-1070	-945	-1195	-1070	-945	mV
$V_{OL}$	Output LOW Voltage (Note 10)	-1995	-1870	-1745	-1995	-1870	-1745	-1995	-1870	-1745	mV
$V_{IH}$	Input HIGH Voltage (Single Ended)	-1225		-880	-1225		-880	-1225		-880	mV
$V_{IL}$	Input LOW Voltage (Single Ended)	-1945		-1625	-1945		-1625	-1945		-1625	mV
$V_{BB}$	Output Voltage Reference	-1575	-1475	-1375	-1600	-1500	-1400	-1625	-1525	-1425	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 11)	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	$V_{EE}+2.0$		0.0	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	D EN	0.5 -150		0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: EP circuits are designed to meet the DC specifications shown in the above table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500 lpm is maintained.

9. Input and output parameters vary 1:1 with  $V_{CC}$ .

10. All loading with 50 ohms to  $V_{CC}$ -2.0 volts.

11.  $V_{IHCMR}$  min varies 1:1 with  $V_{EE}$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

# MC100EP16VC

**AC CHARACTERISTICS**  $V_{CC} = 0\text{ V}$ ;  $V_{EE} = -3.0\text{ V}$  to  $-5.5\text{ V}$  or  $V_{CC} = 3.0\text{ V}$  to  $5.5\text{ V}$ ;  $V_{EE} = 0\text{ V}$  (Note 12)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2. $F_{max}/JITTER$ )		> 3			> 3			> 3		GHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay (Differential) $\overline{Q}$ (Differential) QHG, $\overline{QH\overline{G}}$ (Single Ended) $\overline{Q}$ (Single Ended) QHG, $\overline{QH\overline{G}}$	200 250 250 300	280 360 330 410	350 450 400 500	250 300 300 350	310 380 360 430	400 500 450 550	275 325 325 375	340 430 390 480	425 525 475 575	ps
$t_S$	Setup Time $\overline{EN} = L$ to D $\overline{EN} = H$ to D	50 100	15 60		50 100	5 40		50 100	18 10		ps
$t_H$	Hold Time $\overline{EN} = L$ to D $\overline{EN} = H$ to D	100 50	50 15		100 50	40 20		100 50	5 20		ps
$t_{SKEW}$	Duty Cycle Skew (Note 13)		5.0	20		5.0	20		5.0	20	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (See Figure 2. $F_{max}/JITTER$ )		0.2	< 1		0.2	< 1		0.2	< 1	ps
$V_{PP}$	Input Voltage Swing (Differential) HG (Differential) $\overline{Q}$	25 150	800 800	1200 1200	25 150	800 800	1200 1200	25 150	800 800	1200 1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (20% – 80%) $\overline{Q}$ QHG, $\overline{QH\overline{G}}$	200 70	300 130	400 220	250 80	350 150	450 240	250 100	350 170	500 270	ps

12. Measured using a 750 mV source, 50% duty cycle clock source. All loading with 50 ohms to  $V_{CC}-2.0\text{ V}$ .

13. Skew is measured between outputs under identical transitions. Duty cycle skew is defined only for differential operation when the delays are measured from the cross point of the inputs to the cross point of the outputs.

# MC100EP16VC

## Single Ended Input

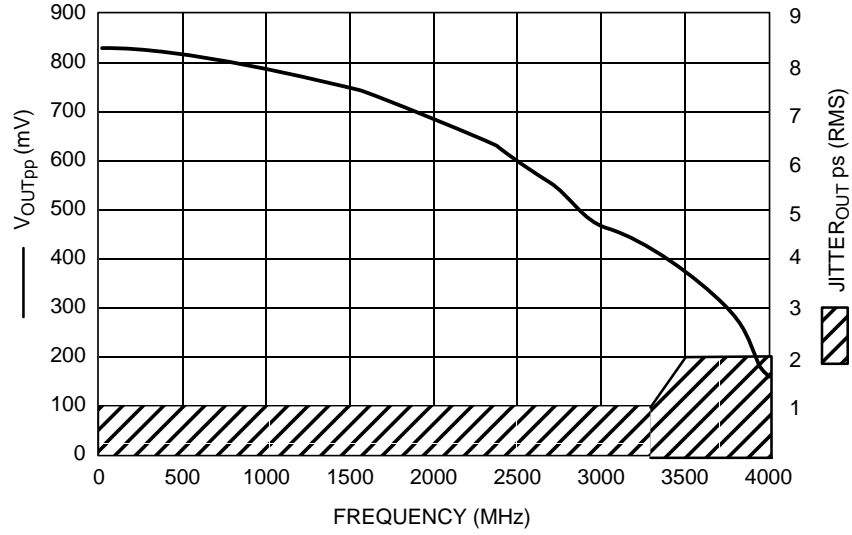


Figure 2.  $F_{max}$ /Jitter for QHG,  $\overline{QHG}$  Output

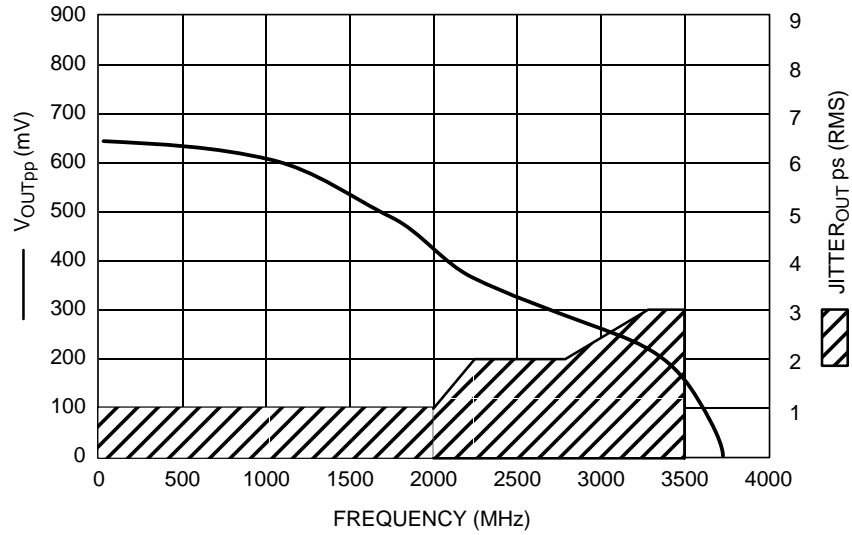


Figure 3.  $F_{max}$ /Jitter for  $\overline{Q}$  Output

# MC100EP16VC

## Differential Inputs

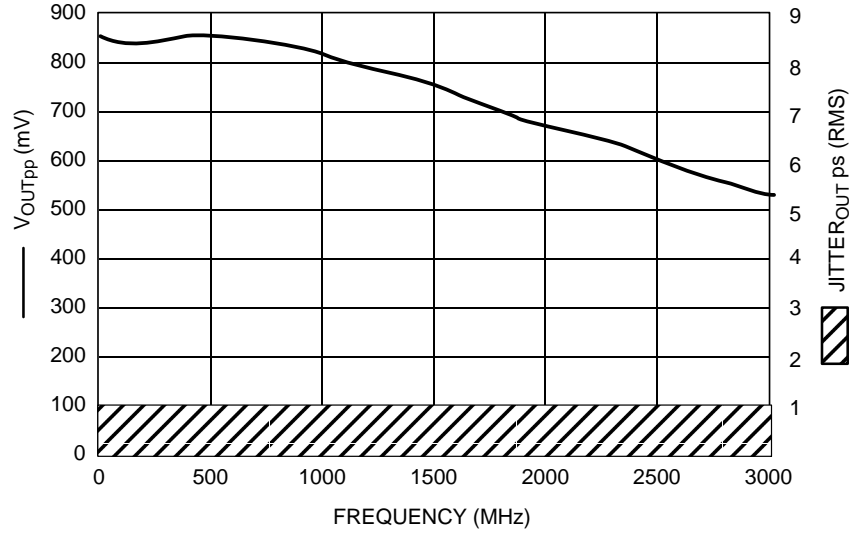


Figure 4.  $F_{max}$ /Jitter for QHG,  $\overline{QHG}$  Output

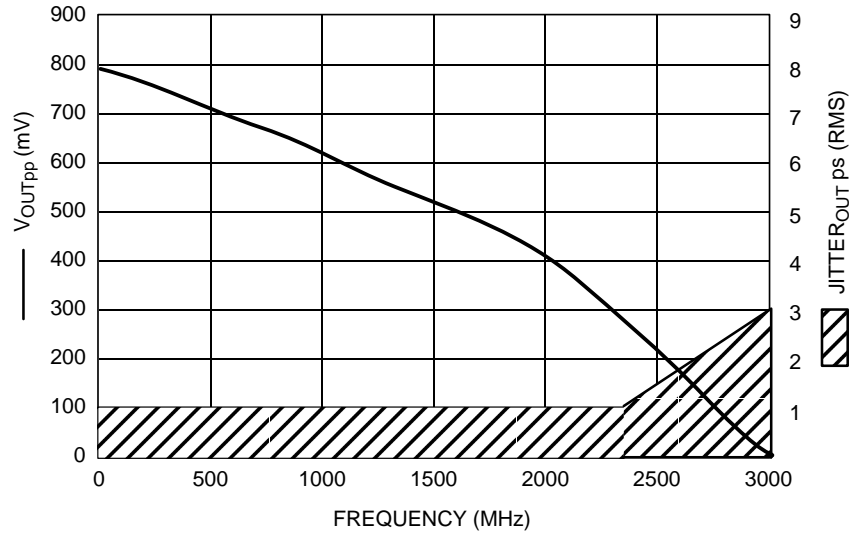
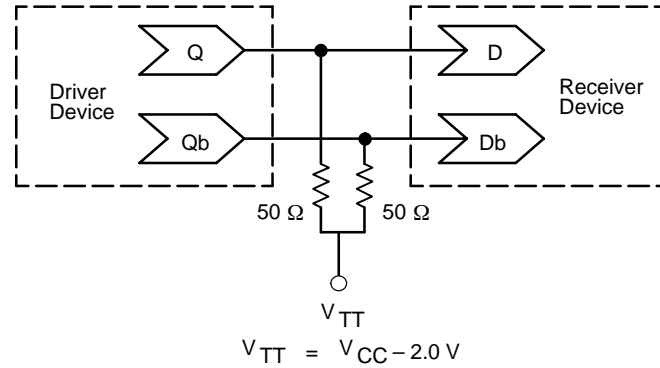


Figure 5.  $F_{max}$ /Jitter for  $\overline{Q}$  Output

## MC100EP16VC



**Figure 6. Typical Termination for Output Driver and Device Evaluation**  
(Refer to Application Note AND8020 – Termination of ECL Logic Devices.)

### Resource Reference of Application Notes

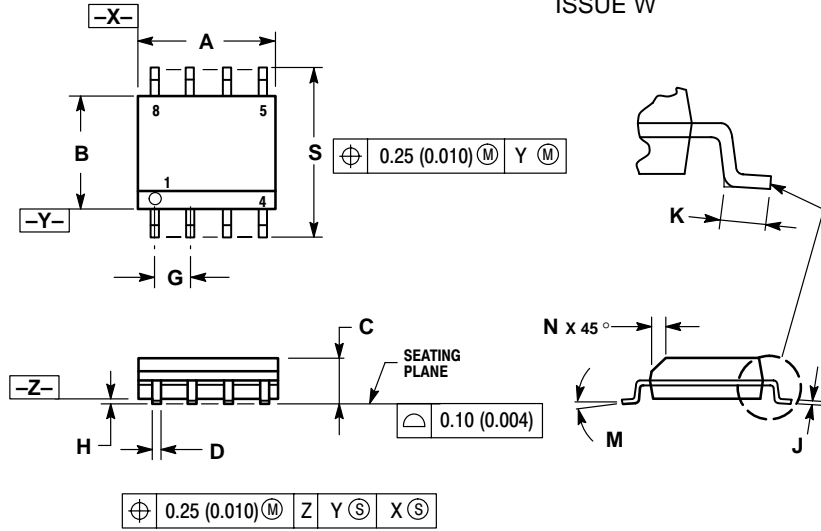
- AN1404** – ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** – ECL Clock Distribution Techniques
- AN1406** – Designing with PECL (ECL at +5.0 V)
- AN1504** – Metastability and the ECLinPS Family
- AN1568** – Interfacing Between LVDS and ECL
- AN1650** – Using Wire-OR Ties in ECLinPS Designs
- AN1672** – The ECL Translator Guide
- AND8001** – Odd Number Counters Design
- AND8002** – Marking and Date Codes
- AND8009** – ECLinPS Plus Spice I/O Model Kit
- AND8020** – Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.

# MC100EP16VC

## PACKAGE DIMENSIONS

SO-8  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751-07  
ISSUE W



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

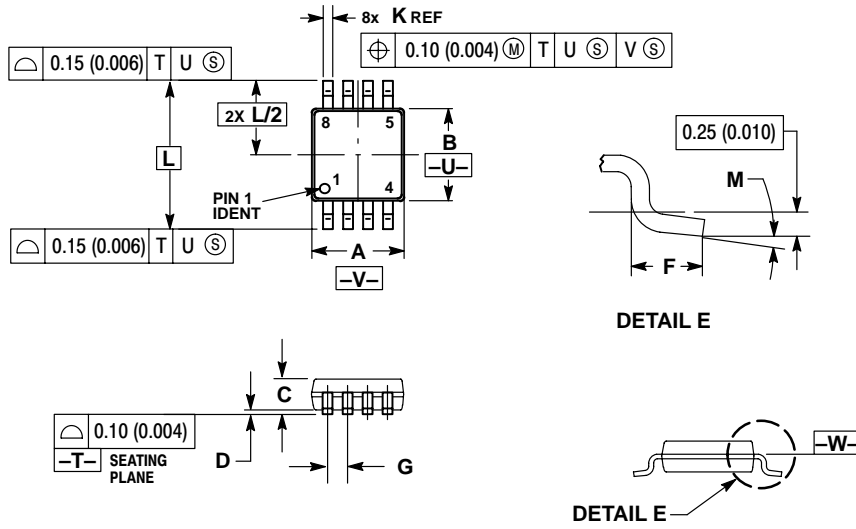
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244



# MC100EP16VC

## PACKAGE DIMENSIONS

### TSSOP-8 DT SUFFIX PLASTIC TSSOP PACKAGE CASE 948R-02 ISSUE A




- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: MILLIMETER.
  3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE  $-V-$ .

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°

**Notes**

**Notes**

# MC100EP16VC

**ON Semiconductor** and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

## PUBLICATION ORDERING INFORMATION

### Literature Fulfillment:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
**Phone:** 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
**Email:** ONlit@hibbertco.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**JAPAN:** ON Semiconductor, Japan Customer Focus Center  
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-0031  
**Phone:** 81-3-5740-2700  
**Email:** r14525@onsemi.com

**ON Semiconductor Website:** <http://onsemi.com>

For additional information, please contact your local Sales Representative.