



4-Bit Binary Counter

Features

- Function, pinout, and drive compatible with FCT and F logic
- FCT-C speed at 5.8 ns max. (Com'l)  
FCT-A speed at 7.2 ns max. (Com'l)
- Reduced  $V_{OH}$  (typically = 3.3V) versions of equivalent FCT functions
- Edge-rate control circuitry for significantly improved noise characteristics
- Power-off disable feature
- ESD > 2000V

- Matched rise and fall times
- Fully compatible with TTL input and output logic levels
- Sink current 64 mA (Com'l),  
32 mA (Mil)  
Source current 32 mA (Com'l),  
12 mA (Mil)

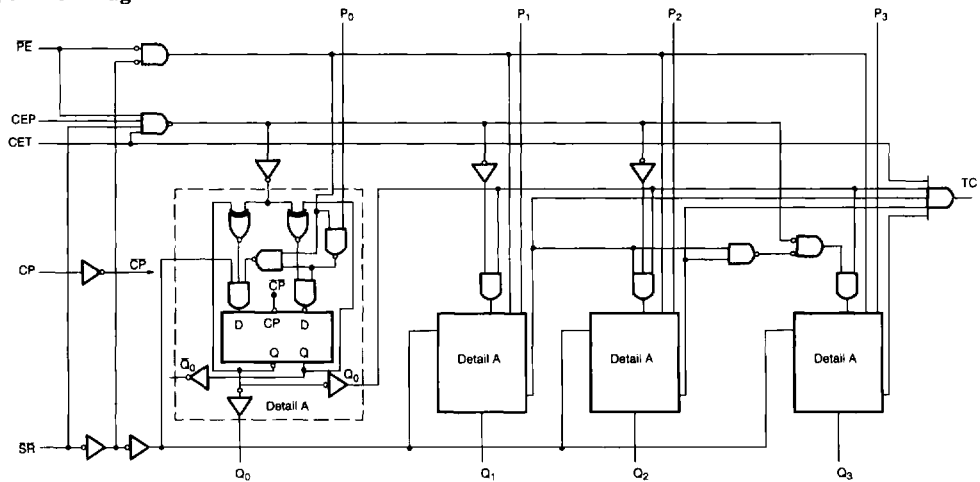
Functional Description

The FCT163T is a high-speed synchronous modulo-16 binary counter. It is synchronously presettable for

application in programmable dividers and has two types of count enable inputs plus a terminal count output for versatility in forming synchronous multi-staged counters. The FCT163T has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

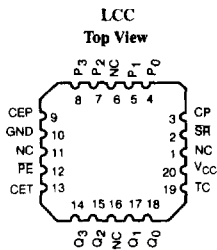
The outputs are designed with a power-off disable feature to allow for live insertion of boards.

Logic Block Diagram

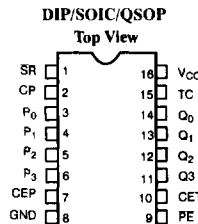


FCT163T-1

Pin Configurations



FCT163T-2



FCT163T-3

**Function Table<sup>[1]</sup>**

Inputs				Action on the Rising Clock Edge(s)
SR	PE	CET	CEP	
L	X	X	X	Reset (Clear)
H	L	X	X	Load ( $P_n \rightarrow Q_n$ )
H	H	H	H	Count (Incremental)
H	H	L	X	No Charge (Hold)
H	H	X	L	No Charge (Hold)

**Pin Description**

Name	Description
CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input (Active Rising Edge)
SR	Synchronous Reset Input (Active LOW)
P	Parallel Data Inputs
PE	Parallel Enable Input (Active LOW)
Q	Flip-Flop Outputs
TC	Terminal Count Output

**Maximum Ratings<sup>[2, 3]</sup>**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-65°C to +135°C
Supply Voltage to Ground Potential	-0.5V to +7.0V
DC Input Voltage	-0.5V to +7.0V
DC Output Voltage	-0.5V to +7.0V
DC Output Current (Maximum Sink Current/Pin)	120 mA
Power Dissipation	0.5W

Static Discharge Voltage ..... >2001V  
(per MIL-STD-883, Method 3015)

**Operating Range**

Range	Range	Ambient Temperature	V <sub>CC</sub>
Commercial	CT	0°C to +70°C	5V ± 5%
Commercial	T, AT	-40°C to +85°C	5V ± 5%
Military <sup>[4]</sup>	All	-55°C to +125°C	5V ± 10%

**Electrical Characteristics Over the Operating Range**

Parameter	Description	Test Conditions	Min.	Typ. <sup>[5]</sup>	Max.	Unit	
V <sub>OH</sub>	Output HIGH Voltage	V <sub>CC</sub> =Min., I <sub>OH</sub> =-32 mA	Com'l	2.0		V	
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-15 mA	Com'l	2.4	3.3	V	
		V <sub>CC</sub> =Min., I <sub>OH</sub> =-12 mA	Mil	2.4	3.3	V	
V <sub>OL</sub>	Output LOW Voltage	V <sub>CC</sub> =Min., I <sub>OL</sub> =64 mA	Com'l		0.3	0.55	V
		V <sub>CC</sub> =Min., I <sub>OL</sub> =32 mA	Mil		0.3	0.55	V
V <sub>IH</sub>	Input HIGH Voltage		2.0			V	
V <sub>IL</sub>	Input LOW Voltage				0.8	V	
V <sub>H</sub>	Hysteresis <sup>[6]</sup>	All inputs		0.2		V	
V <sub>IK</sub>	Input Clamp Diode Voltage	V <sub>CC</sub> =Min., I <sub>IN</sub> =-18 mA		-0.7	-1.2	V	
I <sub>I</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =V <sub>CC</sub>			5	μA	
I <sub>IH</sub>	Input HIGH Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =2.7V			±1	μA	
I <sub>IL</sub>	Input LOW Current	V <sub>CC</sub> =Max., V <sub>IN</sub> =0.5V			±1	μA	
I <sub>OS</sub>	Output Short Circuit Current <sup>[7]</sup>	V <sub>CC</sub> =Max., V <sub>OUT</sub> =0.0V	-60	-120	-225	mA	
I <sub>OFF</sub>	Power-Off Disable	V <sub>CC</sub> =0V, V <sub>OUT</sub> =4.5V			±1	μA	

**Notes:**

- H = HIGH Voltage Level. L = LOW Voltage Level. X = Don't Care.
- Unless otherwise noted, these limits are over the operating free-air temperature range.
- Unused inputs must always be connected to an appropriate logic voltage level, preferably either V<sub>CC</sub> or ground.
- T<sub>A</sub> is the "instant on" case temperature.
- Typical values are at V<sub>CC</sub>=5.0V, T<sub>A</sub>=+25°C ambient.
- This parameter is guaranteed but not tested.
- Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high-speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parametric tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

**Capacitance<sup>[6]</sup>**

Parameter	Description	Typ. <sup>[5]</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	5	10	pF
C <sub>OUT</sub>	Output Capacitance	9	12	pF

**Power Supply Characteristics**

Parameter	Description	Test Conditions	Typ. <sup>[5]</sup>	Max.	Unit
I <sub>CC</sub>	Quiescent Power Supply Current	V <sub>CC</sub> =Max., V <sub>IN</sub> ≤ 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	0.1	0.2	mA
ΔI <sub>CC</sub>	Quiescent Power Supply Current (TTL inputs HIGH)	V <sub>CC</sub> =Max., V <sub>IN</sub> =3.4V, <sup>[8]</sup> f <sub>i</sub> =0, Outputs Open	0.2	2.0	mA
I <sub>CCD</sub>	Dynamic Power Supply Current <sup>[9]</sup>	V <sub>CC</sub> =Max., One Bit Toggling, Load Mode, 50% Duty Cycle, Outputs Open, CEP=CET=PE=GND, SR=V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	0.06	0.12	mA/MHz
I <sub>C</sub>	Total Power Supply Current <sup>[10]</sup>	V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>i</sub> =5 MHz, CEP=CET=PE=GND, SR=V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	0.7	1.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, One Bit Toggling at f <sub>i</sub> =5 MHz, CEP=CET=PE=GND, SR=V <sub>CC</sub> , V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	1.2	3.4	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f <sub>i</sub> =5 MHz, CEP=CET=PE=GND, SR=V <sub>CC</sub> , V <sub>IN</sub> ≤ 0.2V or V <sub>IN</sub> ≥ V <sub>CC</sub> -0.2V	1.6	3.2 <sup>[11]</sup>	mA
		V <sub>CC</sub> =Max., f <sub>0</sub> =10 MHz, Load Mode, 50% Duty Cycle, Outputs Open, Four Bits Toggling at f <sub>i</sub> =5 MHz, CEP=CET=PE=GND, SR=V <sub>CC</sub> , V <sub>IN</sub> =3.4V or V <sub>IN</sub> =GND	2.9	8.2 <sup>[11]</sup>	mA

**Notes:**

8. Per TTL driven input (V<sub>IN</sub>=3.4V); all other inputs at V<sub>CC</sub> or GND.
9. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
10. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
I<sub>C</sub> = I<sub>CC</sub> + ΔI<sub>CC</sub>D<sub>H</sub>N<sub>T</sub> + I<sub>CCD</sub>(f<sub>0</sub>/2 + f<sub>i</sub>N<sub>i</sub>)  
I<sub>CC</sub> = Quiescent Current with CMOS input levels  
ΔI<sub>CC</sub> = Power Supply Current for a TTL HIGH input (V<sub>IN</sub>=3.4V)  
D<sub>H</sub> = Duty Cycle for TTL inputs HIGH

- N<sub>T</sub> = Number of TTL inputs at D<sub>H</sub>  
I<sub>CCD</sub> = Dynamic Current caused by an input transition pair (HLH or LHL)  
f<sub>0</sub> = Clock frequency for registered devices, otherwise zero  
f<sub>i</sub> = Input signal frequency  
N<sub>i</sub> = Number of inputs changing at f<sub>i</sub>  
All currents are in milliamps and all frequencies are in megahertz.
11. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.

**Switching Characteristics Over the Operating Range**

Parameter	Description	FCT163T				FCT163AT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial		Military		Commercial			
		Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q (PE Input HIGH)	2.0	11.5	1.5	11.0	2.0	7.5	1.5	7.2	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC (PE Input LOW)	2.0	10.0	1.5	9.5	2.0	6.5	1.5	6.2	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC	2.0	16.5	1.5	15.0	2.0	10.8	1.5	9.8	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC	1.5	9.0	1.5	8.5	1.5	5.9	1.5	5.5	ns	1, 5
t <sub>S</sub>	Set-Up Time, HIGH or LOW P to CP	5.5		4.0		4.5		4.0		ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW P to CP	2.0		1.5		2.0		1.5		ns	4
t <sub>SU</sub>	Set-Up Time HIGH or LOW PE or SR to CP	13.5		9.5		11.5		9.5		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW PE or SR to CP	1.5		1.5		1.5		1.5		ns	4
t <sub>SU</sub>	Set-Up Time HIGH or LOW CEP or CET to CP	13.0		9.5		11.0		9.5		ns	4
t <sub>H</sub>	Hold Time HIGH or LOW CEP or CET to CP	0		0		0		0		ns	4
t <sub>w</sub>	Clock Pulse Width (Load) HIGH or LOW	5.0		4.0		4.0		4.0		ns	5
t <sub>w</sub>	Clock Pulse Width(Count) HIGH or LOW	8.0		6.0		7.0		6.0		ns	5

**Notes:**

12. Minimum limits are guaranteed but not tested on Propagation Delays.

13. See "Parameter Measurement Information" in the General Information Section.

**Switching Characteristics** Over the Operating Range (continued)

Parameter	Description	FCT163CT				Unit	Fig. No. <sup>[13]</sup>
		Military		Commercial			
		Min. <sup>[12]</sup>	Max.	Min. <sup>[12]</sup>	Max.		
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to Q ( $\overline{PE}$ Input HIGH)	1.5	6.1	1.5	5.8	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC ( $\overline{PE}$ Input LOW)	1.5	5.5	1.5	5.2	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CP to TC	1.5	8.7	1.5	7.8	ns	1, 5
t <sub>PLH</sub> t <sub>PHL</sub>	Propagation Delay CET to TC	1.5	4.8	1.5	4.4	ns	1, 5
t <sub>S</sub>	Set-Up Time, HIGH or LOW P to CP	3.9		3.5		ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW P to CP	2.0		1.5		ns	4
t <sub>SU</sub>	Set-Up Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	9.0		7.6		ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	1.5		1.0		ns	4
t <sub>SU</sub>	Set-Up Time, HIGH or LOW CEP or CET to CP	8.8		7.6		ns	4
t <sub>H</sub>	Hold Time, HIGH or LOW CEP or CET to CP	0		0		ns	4
t <sub>w</sub>	Clock Pulse Width (Load) HIGH or LOW	4.0		4.0		ns	5
t <sub>w</sub>	Clock Pulse Width (Count) HIGH or LOW	6.0		5.0		ns	5

**Ordering Information**

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
5.8	CY74FCT163CTPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163CTQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163CTSOC	S1	16-Lead (300-Mil) Molded SOIC	
6.1	CY54FCT163CTDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163CTLMB	L61	20-Square Leadless Chip Carrier	
7.2	CY74FCT163ATPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163ATQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163ATSOC	S1	16-Lead (300-Mil) Molded SOIC	
7.5	CY54FCT163ATDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163ATLMB	L61	20-Square Leadless Chip Carrier	
11.0	CY74FCT163TPC	P1	16-Lead (300-Mil) Molded DIP	Commercial
	CY74FCT163TQC	Q1	16-Lead (150-Mil) Quarter Size Outline	
	CY74FCT163TSOC	S1	16-Lead (300-Mil) Molded SOIC	
11.5	CY54FCT163TDMB	D2	16-Lead (300-Mil) CerDIP	Military
	CY54FCT163TLMB	L61	20-Square Leadless Chip Carrier	

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