SL2305

Low Jitter and Skew 10 to 140 MHz Zero Delay Buffer (ZDB)

Key Features

- 10 to 140 MHz operating frequency range
- Low output clock jitter:
  - 140 ps-max c-c-j at 66 MHz
- Low output-to-output skew: 150 ps-max
- Low product-to-product skew: 400 ps-max
- 3.3 V power supply range
- Low power dissipation:
  - 14 mA-max at 66MHz
  - 26 mA-max at 133 MHz
- One input drives 5 outputs organized as 4+1
- SpreadThru™ PLL that allows use of SSCG
- Standard and High-Drive options
- Available in 8-pin SOIC and TSSOP packages
- Available in Commercial and Industrial grades

Applications

- Printers and MFPs
- Digital Copiers
- PCs and Work Stations
- DTV
- Routers, Switchers and Servers
- Digital Embeded Systems

Description

The SL2305 is a low skew, low jitter and low power Zero Delay Buffer (ZDB) designed to produce up to five (5) clock outputs from one (1) reference input clock for high speed clock distribution applications. The product has an on-chip PLL which locks to the input clock at CLKIN and receives its feedback internally from the CLKOUT pin.

The SL2305 is available with two (2) drive strength versions. The -1 is the standard-drive version and -1H is the high-drive version.

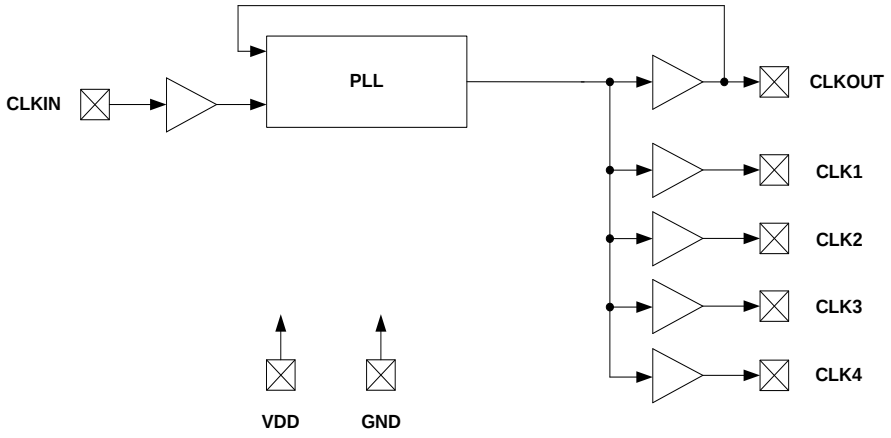
The SL2305 high-drive version operates up to 140MHz and the standard drive version -1 operates up to 100.

The SL2305 enter into Power-Down (PD) mode if the input at CLKIN is DC (0 to VDD). In this power-down state all five (5) outputs are tri-stated and the PLL is turned off leading to less than 12µA-max of power supply current draw.

Benefits

- Up to five (5) distribution of input clock
- Standard and High-Drive levels to control impedance level, frequency range and EMI
- Low jitter and skew
- Low power dissipation
- Low cost

Block Diagram



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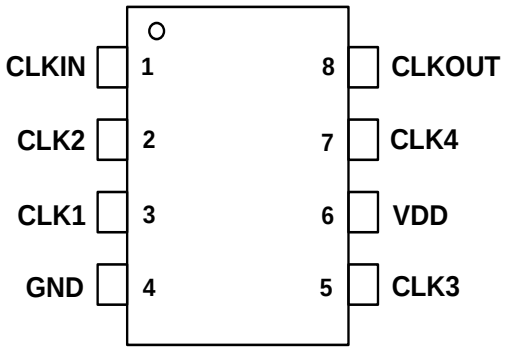
Pin Configuration



8-Pin SOIC or TSSOP

Pin Description

Pin Number	Pin Name	Pin Type	Pin Description
1	CLKIN	Input	Reference Frequency Clock Input. Weak pull-down (250kΩ).
2	CLK2	Output	Buffered Clock Output Weak pull-down (250kΩ).
3	CLK1	Output	Buffered Clock Output. Weak pull-down (250kΩ).
4	GND	Power	Power Ground.
5	CLK3	Output	Buffered Clock Output. Weak pull-down (250kΩ).
6	VDD	Power	3.3V Power Supply.
7	CLK4	Output	Buffered Clock Output. Weak pull-down (250kΩ).
8	CLKOUT	Output	Buffered Clock Output, Used for Internal Feedback to PLL Input. Weak pull-down (250kΩ).

General Description

The SL2305 is a low skew, low jitter Zero Delay Buffer with very low operating power supply current (IDD).

The product includes an on-chip high performance PLL that locks into the input reference clock and produces five (5) output clock drivers tracking the input reference clock for systems requiring clock distribution.

In addition to CLKOUT that is used for internal PLL feedback, there is a single bank with four (4) outputs, bringing the number of total available output clocks to five (5).

Input and output Frequency Range

The input and output frequency range is the same. But, the frequency range depends on the drive levels and load capacitance (CL) as given in the below Table 1.

Drive	CL(pF)	Min(MHz)	Max(MHz)
HIGH (-1H)	15	10	140
HIGH (-1H)	30	10	100
STD (-1)	15	10	100
STD (-1)	30	10	66

Table 1. Input/Output Frequency Range

If the input clock frequency is DC (0 to VDD), this is detected by an input detection circuitry and all five (5) clock outputs are forced to Hi-Z. The PLL is shutdown to save power. In this shutdown state, the product draws less than 12µA-max supply current.

SpreadThru™ Feature

If a Spread Spectrum Clock (SSC) were to be used as an input clock, the SL2305 is designed to pass the modulated Spread Spectrum Clock (SSC) signal from its CLKIN (reference) input to the output clocks. The same spread characteristics at the input are passed through the PLL and drivers without any degradation in spread percent (%), spread profile and modulation frequency.

High and Low-Drive Product Options

The SL2305 is offered with High-Drive “-1H” and Standard-Drive “-1” options. These drive options enable the users to control load levels, frequency range and EMI control. Refer to the AC electrical tables for the details.

Skew and Zero Delay

All outputs should drive the similar load to achieve output-to-output and input-to-output skew specifications given in the AC electrical tables.

However, Zero delay between input and outputs can be adjusted by changing the loading of CLKOUT relative to the other clock outputs since CLKOUT is the feedback to the PLL.

Power Supply Range (VDD)

The SL2305 is designed to operate from 3.0V (Min) to 3.6V (Max), complying with VDD=3.3V+/-10% requirement.

An internal on-chip voltage regulator is used to supply PLL constant power supply of 1.8V, leading to a consistent and stable PLL electrical performance in terms of skew, jitter and power dissipation.

Temperature Range and Packages

The SL2305 is offered with commercial temperature range of 0 to +70°C (C-Grade) and industrial temperature range of -40 to +85°C (I-Grade).

The SL2305 is available in 8-pin SOIC (150-mil) and 8-pin TSSOP (173-mil) packages.

SL23EP05

Refer to SL23EP05 for extended frequency operation from 10 to 220MHz and 2.5V to 3.3V power supply operation range.

Absolute Maximum Ratings

Description	Condition	Min	Max	Unit
Supply voltage, VDD		– 0.5	4.6	V
All Inputs and Outputs		– 0.5	VDD+0.5	V
Ambient Operating Temperature	In operation, C-Grade	0	70	°C
Ambient Operating Temperature	In operation, I-Grade	– 40	85	°C
Storage Temperature	No power is applied	– 65	150	°C
Junction Temperature	In operation, power is applied	–	125	°C
Soldering Temperature		–	260	°C
ESD Rating (Human Body Model)	JEDEC22-A114D	-4,000	4,000	V
ESD Rating (Charge Device Model)	JEDEC22-C101C	-1,500	1,500	V
ESD Rating (Machine Model)	JEDEC22-A115D	-250	250	V
Latch-up	125°C	-200	200	mA

Operating Conditions: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	3.3V Supply Voltage	3.3V+/-10%	3.0	3.6	V
TA	Operating Temperature(Ambient)	Commercial	0	70	°C
		Industrial	–40	85	°C
CLOAD	Load Capacitance	10 to 140 MHz, -1H high drive	–	15	pF
		10 to 100 MHz, -1H high drive	–	30	pF
		10 to 100MHz, -1 standard drive	–	15	pF
		10 to 66MHz, -1 standard drive	–	30	pF
CIN	Input Capacitance	CLKIN pin	–	7	pF
tpu	Power-up Time	Power-up time for all VDDs to reach minimum VDD voltage (VDD=3.0V).	0.05	100	ms
CLBW	Closed-loop bandwidth	3.3V, (typical)	1.2		MHz
ZOUT	Output Impedance	3.3V (typical), -1H high drive	22		Ω
		3.3V (typical), -1 standard drive	32		Ω

DC Electrical Specifications: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

Symbol	Description	Condition	Min	Max	Unit
VDD	Supply Voltage		3.0	3.6	V
VIL	Input LOW Voltage	CLKIN (Pin-1)	–	0.8	V
VIH	Input HIGH Voltage	CLKIN (Pin-1)	2.0	V_{DD}+0.3	V
IIL	Input LOW Current	CLKIN, 0 < VIN < 0.8V	–	25	µA
IIH	Input HIGH Current	CLKIN, VIN = VDD	–	50	µA
VOL	Output LOW Voltage (All outputs)	IOL = 8 mA (standard drive)	–	0.4	V
		IOL = 12 mA (high drive)	–	0.4	V
VOH	Output HIGH Voltage (All outputs)	IOH = –8 mA (standard drive)	2.4	–	V
		IOH = –12 mA (high drive)	2.4	–	V
IDDPD	Power Down Supply Current CLKIN=0 to VDD	C-Grade, Power-down if CLKIN=0 to VDD or input is floating	–	12	µA
		I-Grade, Power-down if CLKIN=0 to VDD or input is floating	–	25	µA
IDD1	Power Supply Current	All Outputs CL=0, 33MHz CLKIN	–	8	mA
IDD2	Power Supply Current	All Outputs CL=0, 66MHz CLKIN	–	14	mA
IDD3	Power Supply Current	All Outputs CL=0, 100MHz CLKIN	–	20	mA
IDD4	Power Supply Current	All Outputs CL=0, 133MHz CLKIN	–	26	mA
RPD	Pull-down Resistors	Pins-1/2/3/5/7/8, 250kΩ-typ	175	325	kΩ

Switching Specifications: Unless otherwise stated VDD=3.3V+/-10% and both C and I Grades

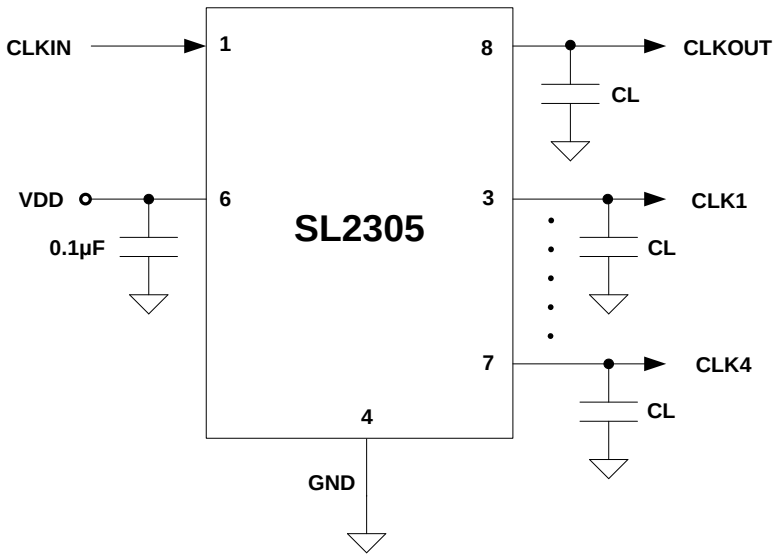
Symbol	Description	Condition	Min	Max	Unit
FMAX1	Maximum Frequency [1] (Input=Output) All Active PLL Modes	High drive (-1H). All outputs CL=15pF	10	140	MHz
		High drive (-1H), All outputs CL=30pF	10	100	MHz
		Standard drive, (-1), All outputs CL=15pf	10	100	MHz
		Standard drive, (-1), All outputs CL=30pf	10	66	MHz
INDC	Input Duty Cycle	Measured at 1.4V, Fout=66MHz, CL=15pF	30	70	%
OUTDC1	Output Duty Cycle[2]	Measured at 1.4V, Fout≥50MHz, CL=15pF	40	60	%
OUTDC2	Output Duty Cycle[2]	Measured at 1.4V, Fout≤50MHz, CL=15pF	45	55	%
tr/f	Rise, Fall Time (3.3V) [2] (Measured at: 0.8 to 2.0V)	High drive (-1H), CL=10pF	–	1.5	ns
		High drive (-1H), CL=30pF	–	1.8	ns
		Standard drive (-1), CL=10pF	–	2.2	ns
		Standard drive (-1), CL=30pF	–	2.5	ns
t1	Output-to-Output Skew[2] (Measured at VDD/2)	All outputs CL=0 or equally loaded, -1 or -1H drives	–	150	ps
t2	Product-to-Product Skew[2] (Measured at VDD/2)	All outputs CL=0 or equally loaded, -1 or -1H drives	–	400	ps
t3	Delay Time, CLKIN Rising Edge to CLKOUT Rising Edge[2]	Measured at VDD/2	–220	220	ps
tPLOCK	PLL Lock Time[2]	Time from 90% of VDD to valid clocks on all the output clocks	–	1.0	ms
CCJ	Cycle-to-cycle Jitter [2]	Fin=Fout=66 MHz, <CL=15pF, -1H drive	–	140	ps
		Fin=Fout=66 MHz, <CL=15pF, -1 drive	–	150	ps
		Fin=Fout=66 MHz, <CL=30pF, -1H drive	–	160	ps
		Fin=Fout=66 MHz, <CL=30pF, -1 drive	–	170	ps

Notes:

1. For the given maximum loading conditions. See CL in Operating Conditions Table.
2. Parameter is guaranteed by design and characterization. Not 100% tested in production.

External Components & Design Considerations

Typical Application Schematic



Comments and Recommendations

Decoupling Capacitor: A decoupling capacitor of 0.1µF must be used between VDD and VSS on the pins 6 and 4. Place the capacitor on the component side of the PCB as close to the VDD pin as possible. The PCB trace to the VDD pin and to the GND via should be kept as short as possible. Do not use vias between the decoupling capacitor and the VDD pin.

Series Termination Resistor: A series termination resistor is recommended if the distance between the outputs and the load is over 1 ½ inch. The nominal impedance of the Clock outputs are about 30 Ω. Use 20 Ω resistor in series with the output to terminate 50Ω trace impedance and place 20 Ω resistor as close to the clock outputs as possible.

Zero Delay and Skew Control: All outputs and CLKIN pins should be loaded with the same load to achieve “Zero Delay” between the CLKIN and the outputs. The CLKOUT pin is connected to CLKIN internally on-chip for internal feedback to PLL, and sees an additional 2 pF load with respect to the clock pins. For applications requiring zero input/output delay, the load at the all output pins including the CLKOUT pin must be the same. If any delay adjustment is required, the capacitance at the CLKOUT pin could be increased or decreased to increase or decrease the delay between clocks and CLKIN.

For minimum pin-to-pin skew, the external load at the clock outputs must be the same.

Switching Waveforms

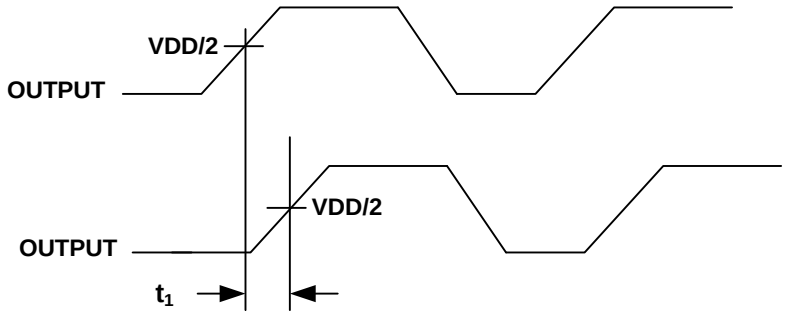


Figure 1. Output to Output Skew

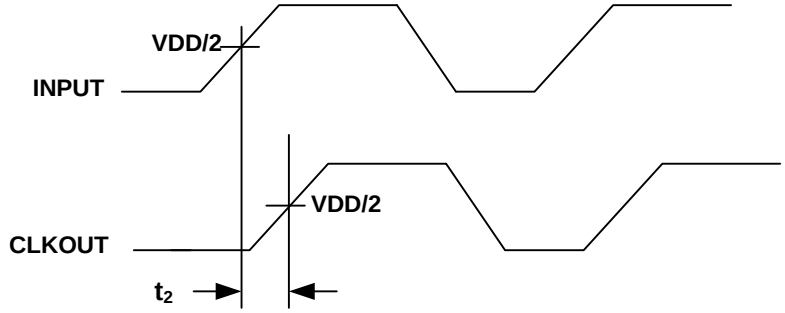


Figure 2. Input- to-Output Skew

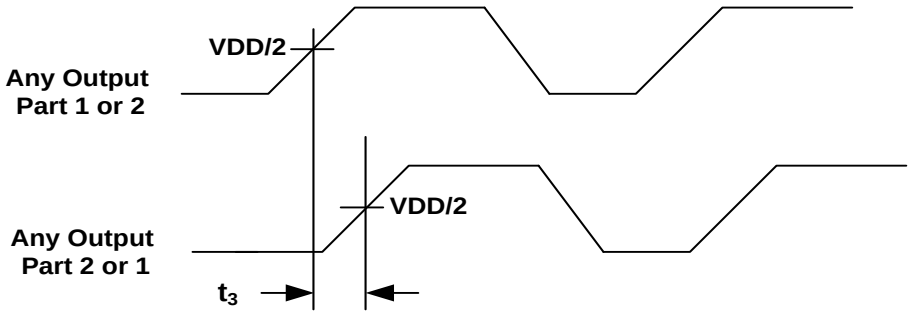
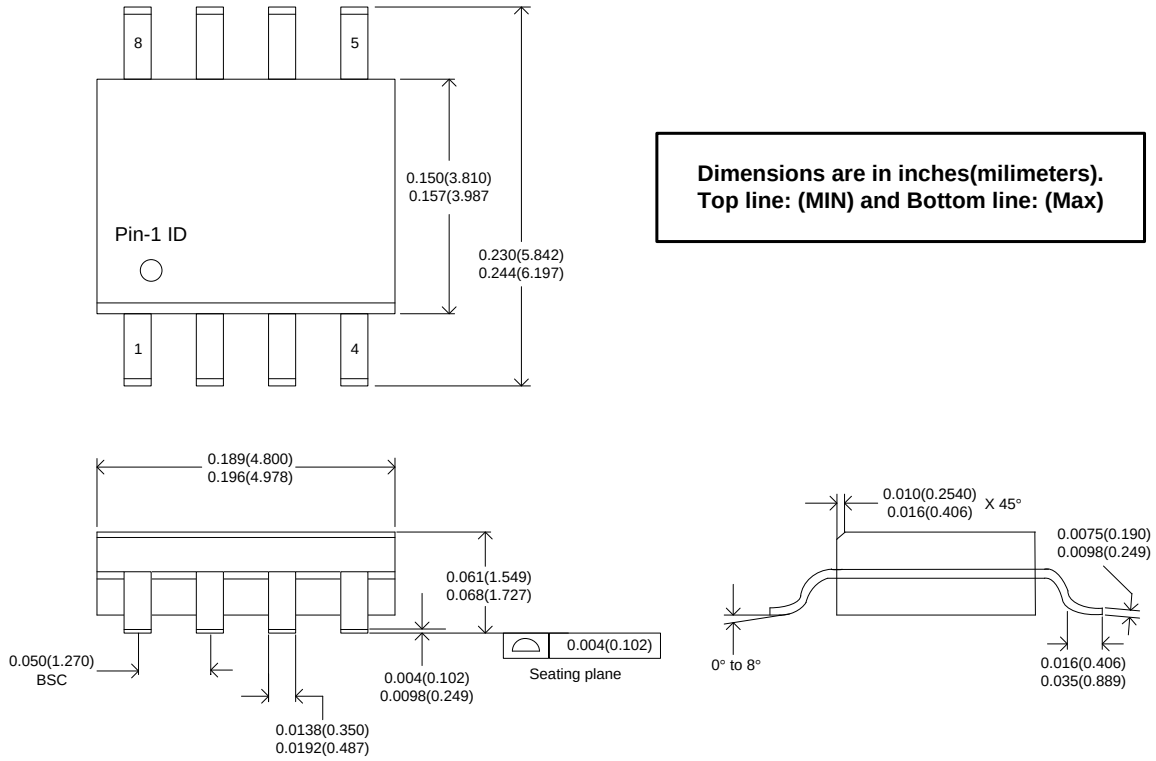


Figure 3. Part-to-Part Skew

Package Outline and Package Dimensions

8-Pin SOIC Package (150-mil)



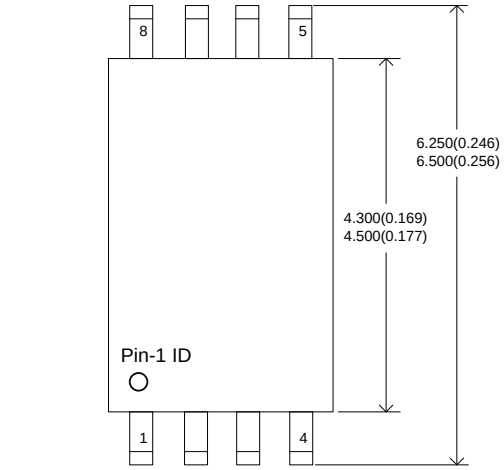
Dimensions are in inches(milimeters).
Top line: (MIN) and Bottom line: (Max)

Thermal Characteristics

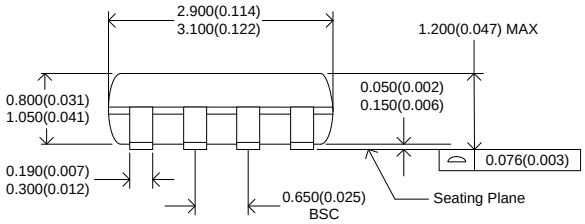
Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient	θ JA	Still air	-	150	-	°C/W
	θ JA	1m/s air flow	-	140	-	°C/W
	θ JA	3m/s air flow	-	120	-	°C/W
Thermal Resistance Junction to Case	θ JC	Independent of air flow	-	40	-	°C/W

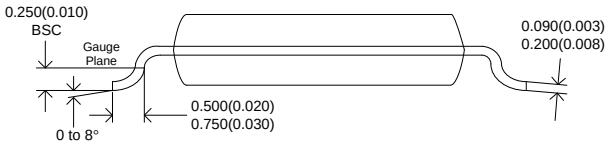
Package Outline and Package Dimensions

8-Pin TSSOP Package (4.4-mm)



Dimensions are in milimeters (inches)
Top line: (MIN) and Bottom line: (Max)





Thermal Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermal Resistance Junction to Ambient		Still air	-	110	-	°C/W
		1m/s air flow	-	100	-	°C/W
		3m/s air flow	-	80	-	°C/W
Thermal Resistance Junction to Case		Independent of air flow	-	35	-	°C/W

Ordering Information [3]

Ordering Number	Marking	Shipping Package	Package	Temperature
SL2305SC-1	SL2305SC-1	Tube	8-pin SOIC	0 to 70°C
SL2305SC-1T	SL2305SC-1	Tape and Reel	8-pin SOIC	0 to 70°C
SL2305SI-1	SL2305SI-1	Tube	8-pin SOIC	-40 to 85°C
SL2305SI-1T	SL2305SI-1	Tape and Reel	8-pin SOIC	-40 to 85°C
SL2305SC-1H	SL2305SC-1H	Tube	8-pin SOIC	0 to 70°C
SL2305SC-1HT	SL2305SC-1H	Tape and Reel	8-pin SOIC	0 to 70°C
SL2305SI-1H	SL2305SI-1H	Tube	8-pin SOIC	-40 to 85°C
SL2305SI-1HT	SL2305SI-1H	Tape and Reel	8-pin SOIC	-40 to 85°C
SL2305ZC-1	SL2305ZC-1	Tube	8-pin TSSOP	0 to 70°C
SL2305ZC-1T	SL2305ZC-1	Tape and Reel	8-pin TSSOP	0 to 70°C
SL2305ZI-1	SL2305ZI-1	Tube	8-pin TSSOP	-40 to 85°C
SL2305ZI-1T	SL2305ZI-1	Tape and Reel	8-pin TSSOP	-40 to 85°C
SL2305ZC-1H	SL2305ZC-1H	Tube	8-pin TSSOP	0 to 70°C
SL2305ZC-1HT	SL2305ZC-1H	Tape and Reel	8-pin TSSOP	0 to 70°C
SL2305ZI-1H	SL2305ZI-1H	Tube	8-pin TSSOP	-40 to 85°C
SL2305ZI-1HT	SL2305ZI-1H	Tape and Reel	8-pin TSSOP	-40 to 85°C

Notes:

3. The SL2305 products are RoHS compliant.