

### MOS FIELD EFFECT TRANSISTOR NP32N055HHE, NP32N055IHE

## SWITCHING N-CHANNEL POWER MOS FET INDUSTRIAL USE

#### **DESCRIPTION**

These products are N-Channel MOS Field Effect

Transistors designed for high current switching applications.

#### **FEATURES**

- Channel temperature 175 degree rated
- Super low on-state resistance
   R<sub>DS(on)</sub> = 25 mΩ MAX. (V<sub>GS</sub> = 10 V, I<sub>D</sub> = 16 A)
- Low Ciss: Ciss = 1100 pF TYP.
- Built-in gate protection diode

#### ORDERING INFORMATION

PART NUMBER	PACKAGE
NP32N055HHE	TO-251
NP32N055IHE	TO-252

#### ABSOLUTE MAXIMUM RATINGS (TA = 25 °C)

Drain to Source Voltage	VDSS	55	V
Gate to Source Voltage	Vgss	±20	V
Drain Current (DC)	I <sub>D(DC)</sub>	±32	Α
Drain Current (Pulse) Note1	D(pulse)	±100	Α
Total Power Dissipation (T <sub>A</sub> = 25 °C)	Рт	1.2	W
Total Power Dissipation (Tc = 25 °C)	Рт	66	W
Single Avalanche Current Note2	las	26 / 21 / 7	Α
Single Avalanche Energy Note2	Eas	6.7 / 44 / 49	mJ
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to + 175	°C

(TO-251)



(TO-252)



**Notes 1.** PW  $\leq$  10  $\mu$  s, Duty cycle  $\leq$  1 %

**2.** Starting  $T_{ch} = 25 \, ^{\circ}\text{C}$ ,  $R_G = 25 \, \Omega$ ,  $V_{GS} = 20 \, \text{V} \rightarrow 0 \, \text{V}$  (See Figure 4.)

#### THERMAL RESISTANCE

Channel to Case	Rth(ch-C)	2.27	°C/W
Channel to Ambient	Rth(ch-A)	125	°C/W

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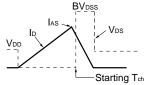


#### **ELECTRICAL CHARACTERISTICS (TA = 25 °C)**

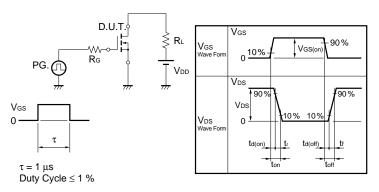
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	RDS(on)	Vgs = 10 V, ID = 16 A		19	25	mΩ
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	$V_{DS} = V_{GS}$ , $I_D = 250 \mu A$	2.0	3.0	4.0	V
Forward Transfer Admittance	yfs	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 16 A	6	12		S
Drain Leakage Current	Ipss	V <sub>DS</sub> = 55 V, V <sub>GS</sub> = 0 V			10	μΑ
Gate to Source Leakage Current	Igss	Vgs = ±20 V, Vps = 0 V			±10	μΑ
Input Capacitance	Ciss	V <sub>DS</sub> = 25 V		1100	1600	pF
Output Capacitance	Coss	V <sub>GS</sub> = 0 V		180	270	pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		95	170	pF
Turn-on Delay Time	td(on)	ID = 16 A		16	35	ns
Rise Time	tr	V <sub>GS(on)</sub> = 10 V		11	27	ns
Turn-off Delay Time	td(off)	V <sub>DD</sub> = 28 V		29	58	ns
Fall Time	tf	$R_G = 1 \Omega$		10	24	ns
Total Gate Charge	Q <sub>G</sub>	ID = 32 A		21	32	nC
Gate to Source Charge	Qgs	V <sub>DD</sub> = 44 V		6		nC
Gate to Drain Charge	Q <sub>GD</sub>	V <sub>GS</sub> = 10 V		8		nC
Body Diode Forward Voltage	VF(S-D)	IF = 32 A, VGS = 0 V		1.0		V
Reverse Recovery Time	trr	IF = 32 A, VGS = 0 V		40		ns
Reverse Recovery Charge	Qrr	di/dt = 100 A/μs		57		nC

#### **TEST CIRCUIT 1 AVALANCHE CAPABILITY**

# $\begin{array}{c} \text{D.U.T.} \\ \text{Rg} = 25 \Omega \\ \text{Vgs} = 20 \rightarrow 0 \text{ V} \\ \text{m} \end{array} \begin{array}{c} \text{D.U.T.} \\ \text{So} \\ \text{N} \end{array}$

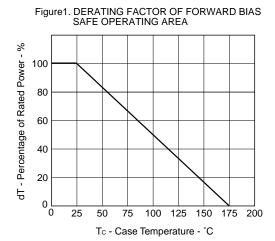


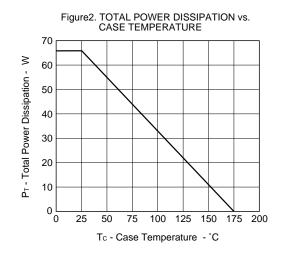
#### **TEST CIRCUIT 2 SWITCHING TIME**

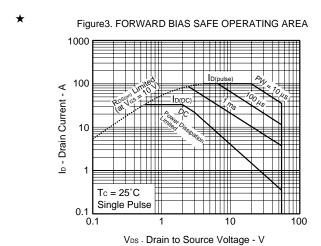


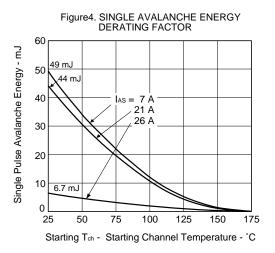
#### **TEST CIRCUIT 3 GATE CHARGE**

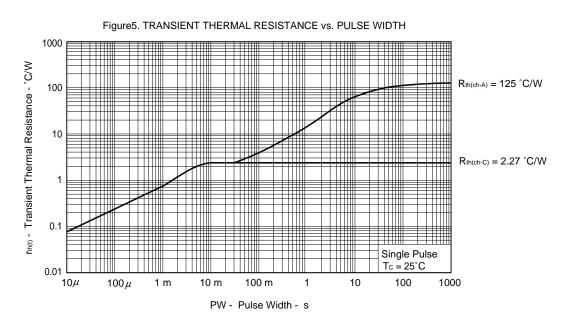
#### TYPICAL CHARACTERISTICS (TA = 25 °C)











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Figure 6. FORWARD TRANSFER CHARACTERISTICS

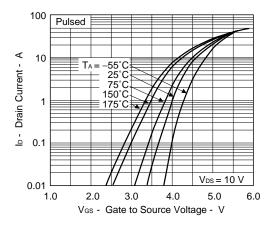


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

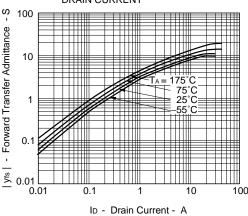


Figure7. DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE

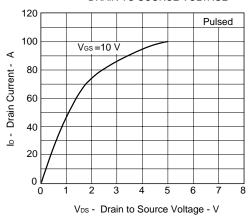


Figure 9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

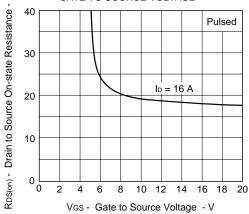
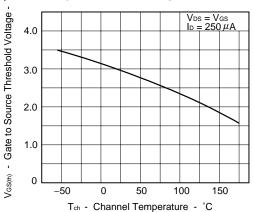
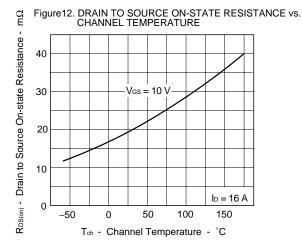
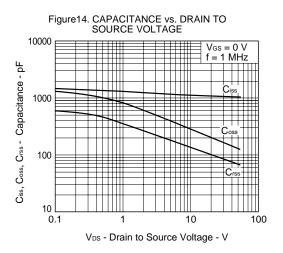
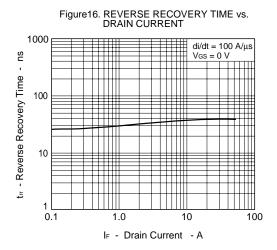


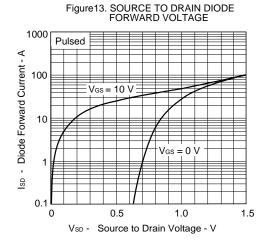
Figure 11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

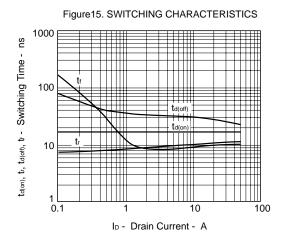












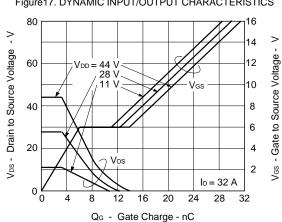
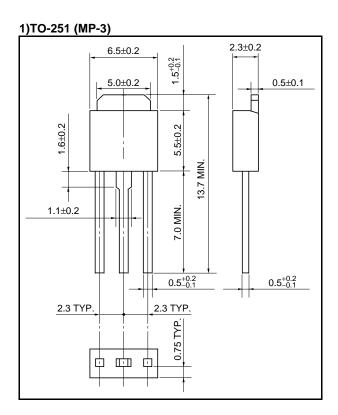
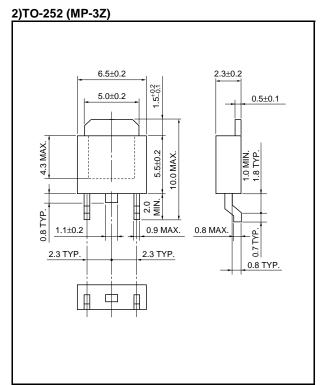


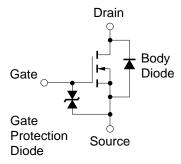
Figure 17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

#### **PACKAGE DRAWINGS (Unit:mm)**





#### **EQUIVALENT CIRCUIT**



**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

[MEMO]

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