SST111 SERIES
N-Channel JFETs

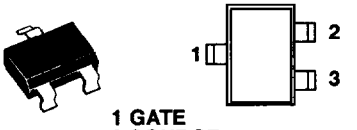
Siliconix incorporated

The SST111 Series is the surface mount equivalent of our J111 device types. Its low cost and $r_{DS(ON)}$ make it a good choice for an all-purpose analog switch, while its high g_{fs} and good high-frequency response also make this product useful in a high-gain amplifier mode. Like all SOT-23 products available from Siliconix, tape and reel capabilities exist for automated assembly. (See Section 7.)

PART NUMBER	$V_{GS(OFF)}$ MAX (V)	$r_{DS(ON)}$ MAX (Ω)	$I_{D(OFF)}$ TYP (pA)	t_{ON} TYP (ns)
SST111	-10	30	5	4
SST112	-5	50	5	4
SST113	-3	100	5	4

For further design information please consult the typical performance curves NCB.

SOT-23 TOP VIEW



1 GATE
2 SOURCE
3 DRAIN

SIMILAR PRODUCTS

- TO-92, See J111 Series
- TO-18, See 2N4391 Series
- Duals, See 2N5564 Series
- Chips, See NCB Series Die

PRODUCT MARKING	
SST111	C11
SST112	C12
SST113	C13

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C Unless Otherwise Noted)

PARAMETERS/TEST CONDITIONS	SYMBOL	LIMITS	UNITS
Gate-Drain Voltage	V_{GD}	-35	V
Gate-Source Voltage	V_{GS}	-35	
Gate Current	I_G	50	mA
Power Dissipation	P_D	350	mW
Power Derating		2.8	mW/°C
Operating Junction Temperature Range	T_J	-55 to 150	°C
Storage Temperature Range	T_{stg}	-55 to 150	
Lead Temperature ($^1/_{16}$" from case for 10 sec.)	T_L	300	

SPECIFICATIONS[a]			LIMITS							
				SST111		SST112		SST113		
PARAMETER	SYMBOL	TEST CONDITIONS	TYP[b]	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
STATIC										
Gate-Source Breakdown Voltage	$V_{(BR)GSS}$	I_G = -1 µA, V_{DS} = 0 V	-55	-35		-35		-35		V
Gate-Source Cutoff Voltage	$V_{GS(OFF)}$	V_{DS} = 5 V, I_D = 1 µA		-3	-10	-1	-5		-3	
Saturation Drain Current[c]	I_{DSS}	V_{DS} = 15 V, V_{GS} = 0 V		20		5		2		mA
Gate Reverse Current	I_{GSS}	V_{GS} = -15 V, V_{DS} = 0 V	-0.005		-1		-1		-1	nA
		T_A = 125°C	-3							
Gate Operating Current	I_G	V_{DG} = 15 V, I_D = 10 mA	-5							pA
Drain Cutoff Current	$I_{D(OFF)}$	V_{DS} = 10 V, V_{GS} = -12 V	0.005		1		1		1	nA
		T_A = 125°C	3							
Drain-Source On-Resistance	$r_{DS(ON)}$	V_{GS} = 0 V, V_{DS} = 0.1 V			30		50		100	Ω
Gate-Source Forward Voltage	$V_{GS(F)}$	I_G = 1 mA, V_{DS} = 0 V	0.7							V
DYNAMIC										
Common-Source Forward Transconductance	g_{fs}	V_{DG} = 20 V, I_D = 1 mA f = 1 kHz	6							mS
Common-Source Output Conductance	g_{os}		25							µS
Drain-Source On-Resistance	$r_{ds(ON)}$	V_{GS} = 0 V, I_D = 0 V f = 1 kHz			30		50		100	Ω
Common-Source Input Capacitance	C_{iss}	V_{DS} = 0 V, V_{GS} = -10 V f = 1 MHz	7		12		12		12	pF
Common-Source Reverse Transfer Capacitance	C_{rss}		3		5		5		5	
Equivalent Input Noise Voltage	$\bar{e}_n$	V_{DG} = 10 V, I_D = 1 mA f = 1 kHz	4							$nV/\sqrt{Hz}$
SWITCHING										
Turn-On Time	$t_{d(ON)}$	V_{DD} = 10 V, $V_{GS(ON)}$ = 0 V	2							ns
	t_r	P/N $I_{D(ON)}$ $V_{GS(OFF)}$ R_L	2							
Turn-Off Time	$t_{d(OFF)}$	SST111 12.5mA -12V 800Ω SST112 6.25mA -7V 1600Ω SST113 3.1mA -5V 3200Ω	6							
	t_f		15							

NOTES:
a. T_A = 25°C unless otherwise noted.
b. For design aid only, not subject to production testing.
c. Pulse test; PW = 300 µS, duty cycle ≤ 3%.

4