450 MHz to 6000 MHz
TruPwr Detector

ADL5504

FEATURES

True rms response detector
Excellent temperature stability
±0.25 dB rms detection accuracy vs. temperature
Over 35 dB input power dynamic range, inclusive of crest factor
RF bandwidths from 450 MHz to 6000 MHz
500 Ω input impedance
Single-supply operation: 2.5 V to 3.3 V
Low power: 1.8 mA at 3.0 V supply
RoHS compliant part

APPLICATIONS

Power measurement of W-CDMA, CDMA2000, QPSK-/QAM-based OFDM (LTE and WiMAX), and other complex modulation waveforms
RF transmitter or receiver power measurement

FUNCTIONAL BLOCK DIAGRAM

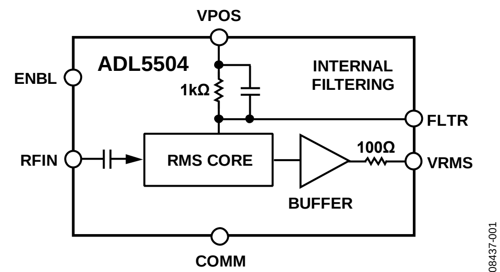

Figure 1.

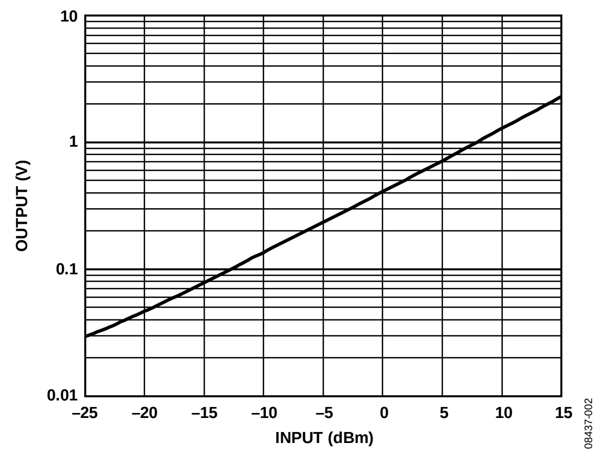

Figure 2. Output vs. Input Level, 3 V Supply, Frequency 1900 MHz

GENERAL DESCRIPTION

The ADL5504 is a TruPwr™ mean-responding (true rms) power detector for use in high frequency receiver and transmitter signal chains from 450 MHz to 6000 MHz. Requiring only a single supply between 2.5 V and 3.3 V, the detector draws less than 1.8 mA. The input is internally ac-coupled and has a nominal input impedance of 500 Ω. The rms output is a linear-responding dc voltage with a conversion gain of 1.87 V/V rms at 900 MHz.

The ADL5504 is a highly accurate, easy to use means of determining the rms of complex waveforms. It can be used for power measurements of both simple and complex waveforms but is particularly useful for measuring high crest factor (high peak-to-rms ratio) signals, such as W-CDMA, CDMA2000, WiMAX, WLAN, and LTE waveforms.

The on-chip modulation filter provides adequate averaging for most waveforms. For more complex waveforms, an external capacitor at the FLTR pin can be used for supplementary signal demodulation. An on-chip, 100 Ω series resistance at the output, combined with an external shunt capacitor, creates a low-pass filter response that reduces the residual ripple in the dc output voltage.

The ADL5504 offers excellent temperature stability across a 30 dB range and near 0 dB measurement error across temperature over the top portion of the dynamic range. In addition to its temperature stability, the ADL5504 offers low process variations that further reduce calibration complexity.

The power detector operates from −40°C to +85°C and is available in a 6-ball, 0.8 mm × 1.2 mm, wafer level chip scale package. It is fabricated on a high f_T silicon BiCMOS process.

Rev. A

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

1/11—Rev. 0 to Rev. A

Change to Filtering Section ... 13
Change to Land Pattern and Soldering Information Section ... 20

10/09—Revision 0: Initial Version

SPECIFICATIONS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = 10 nF, C_{OUT} = open, light condition ≤ 600 lux, 75 Ω input termination resistor, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
FREQUENCY RANGE	Input RFIN	450		6000	MHz
RF INPUT (f = 450 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		520‖1.00		Ω‖pF
RMS Conversion					
Dynamic Range[1]	Continuous wave (CW) input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		25		dB
±0.25 dB Error[3]			16		dB
±1 dB Error[3]			35		dB
±2 dB Error[3]			39		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−21		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.90		V/V rms
Output Intercept[4]			0.003		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.760		
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.077		
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0027		dB/°C
	−40°C < T_A < +25°C		0.0024		dB/°C
RF INPUT (f = 900 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		370‖0.80		Ω‖pF
RMS Conversion					
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		27		dB
±0.25 dB Error[3]			17		dB
±1 dB Error[3]			35		dB
±2 dB Error[3]			39		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept	1.6	1.87	2.2	V/V rms
Output Intercept[4]		−0.1	+0.004	+0.1	V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.746		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.077		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0024		dB/°C
	−40°C < T_A < +25°C		0.0018		dB/°C

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT (f = 1900 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		260‖0.68		Ω‖pF
RMS Conversion					
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		20		dB
±0.25 dB Error[3]			15		dB
±1 dB Error[3]			35		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.82		V/V rms
Output Intercept[4]			0.001		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.719		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.072		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0016		dB/°C
	−40°C < T_A < +25°C		0.0070		dB/°C
RF INPUT (f = 2600 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		240‖0.61		Ω‖pF
RMS Conversion					
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		13		dB
±0.25 dB Error[3]			10		dB
±1 dB Error[3]			35		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		15		dBm
Minimum Input Level	±1 dB error[3]		−22		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.79		V/V rms
Output Intercept[4]			−0.003		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.702		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.069		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0031		dB/°C
	−40°C < T_A < +25°C		0.0046		dB/°C
RF INPUT (f = 3500 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		200‖0.50		Ω‖pF
RMS Conversion					
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±0.25 dB Error[2]	Delta from 25°C		6		dB
±0.25 dB Error[3]			5		dB
±1 dB Error[3]			34		dB
±2 dB Error[3]			40		dB
Maximum Input Level	±0.25 dB error[3]		13		dBm
Minimum Input Level	±1 dB error[3]		−21		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		1.65		V/V rms
Output Intercept[4]			−0.006		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.639		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.060		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0037		dB/°C
	−40°C < T_A < +25°C		0.0074		dB/°C

Parameter	Test Conditions	Min	Typ	Max	Unit
RF INPUT (f = 6000 MHz)	Input RFIN to output VRMS				
Input Impedance	No termination		90‖0.31		Ω‖pF
RMS Conversion					
Dynamic Range[1]	CW input, −40°C < T_A < +85°C				
±1 dB Error[3]			25		dB
±2 dB Error[3]			34		dB
Maximum Input Level	±0.25 dB error[3]		12		dBm
Minimum Input Level	±1 dB error[3]		−16		dBm
Conversion Gain	VRMS = (gain × V_{IN}) + intercept		0.82		V/V rms
Output Intercept[4]			-0.005		V
Output Voltage, High Input Power	P_{IN} = 5 dBm, 400 mV rms		0.314		V
Output Voltage, Low Input Power	P_{IN} = −15 dBm, 40 mV rms		0.027		V
Temperature Sensitivity	P_{IN} = 0 dBm				
	25°C < T_A < 85°C		0.0108		dB/°C
	−40°C < T_A < +25°C		0.0120		dB/°C
VRMS OUTPUT	Pin VRMS				
Output Offset	No signal at RFIN		10	100	mV
Maximum Output Voltage	V_S = 3.0 V, R_{LOAD} ≥ 10 kΩ		2.5		V
Available Output Current			3		mA
Pulse Response Time	10 dB step, 10% to 90% of settling level, no filter capacitor		3		μs
ENABLE INTERFACE	Pin ENBL				
Logic Level to Enable Power, High Condition	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	1.8		V_{POS}	V
Input Current when High	2.5 V at ENBL, −40°C < T_A < +85°C		0.05	0.1	μA
Logic Level to Disable Power, Low Condition	2.5 V ≤ V_S ≤ 3.3 V, −40°C < T_A < +85°C	−0.5		+0.5	V
Power-Up Response Time[5]	C_{FLTR} = open, 0 dBm at RFIN		1		μs
	C_{FLTR} = 10 nF, 0 dBm at RFIN		8		μs
POWER SUPPLIES					
Operating Range	−40°C < T_A < +85°C	2.5		3.3	V
Quiescent Current[6]	No signal at RFIN, ENBL high input condition		1.8		mA
Disable Current[7]	ENBL input low condition		0.1	1	μA

[1] The available output swing and, therefore, the dynamic range are altered by the supply voltage; see Figure 8.
[2] Error referred to delta from 25°C response; see Figure 13 to Figure 15 and Figure 19 to Figure 21.
[3] Error referred to best-fit line at 25°C; see Figure 10 to Figure 12 and Figure 16 to Figure 18.
[4] Calculated using linear regression.
[5] The response time is measured from 10% to 90% of settling level; see Figure 31 to Figure 33.
[6] Supply current is input level-dependent; see Figure 27.
[7] Guaranteed but not tested; limits are specified at six sigma levels.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage, V_S	3.5 V
VRMS, ENBL	0 V to V_S
RFIN	1.25 V rms
Equivalent Power, Referred to 50 Ω	15 dBm
Internal Power Dissipation	150 mW
θ_{JA} (WLCSP)	260°C/W
Maximum Junction Temperature	125°C
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

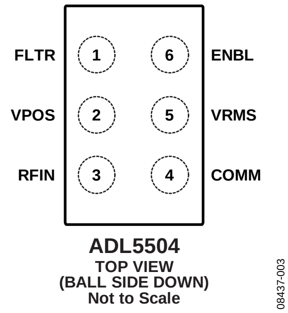

Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	FLTR	Modulation Filter. Connect an external capacitor to this pin to lower the corner frequency of the modulation filter.
2	VPOS	Supply Voltage. The operational range is 2.5 V to 3.3 V.
3	RFIN	Signal Input. This pin is internally ac-coupled after internal termination resistance. The nominal input impedance is 500 Ω.
4	COMM	Device Ground.
5	VRMS	RMS Output. This pin is a rail-to-rail voltage output with limited current drive capability. The output has an internal 100 Ω series resistance. High resistive loads and low capacitance loads are recommended to preserve output swing and allow fast response.
6	ENBL	Enable. Connect this pin to V_S for normal operation. Connect this pin to ground for disable mode.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = 3.0 V, C_{FLTR} = 10 nF, C_{OUT} = open, light condition ≤ 600 lux, 75 Ω input termination resistor; colors: black = +25°C, blue = −40°C, red = +85°C; unless otherwise noted.

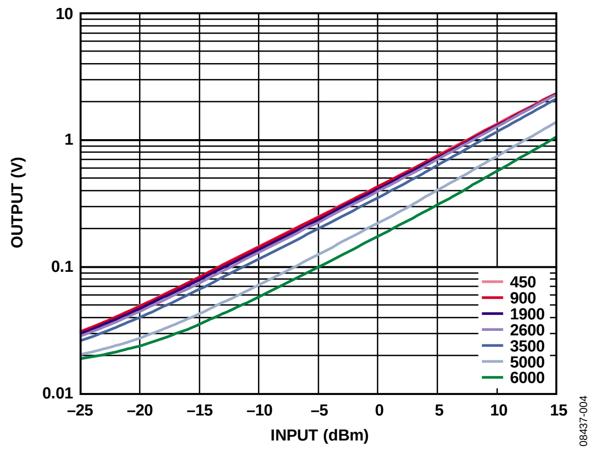

Figure 4. Output vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz Frequencies, 3.0 V Supply

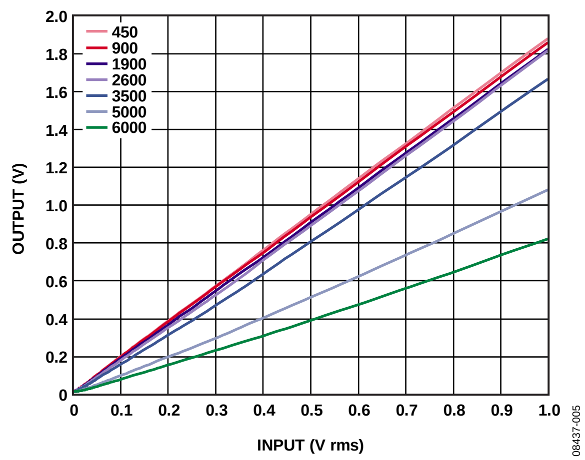

Figure 5. Output vs. Input Level (Linear Scale), 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz Frequencies, 3.0 V Supply

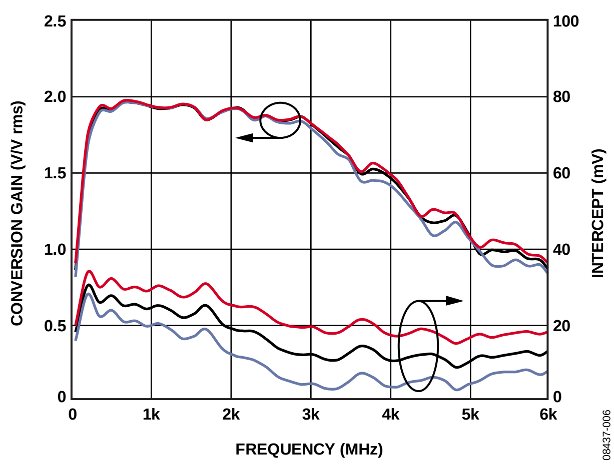

Figure 6. Conversion Gain and Intercept vs. Frequency, 3.0 V Supply at −40°C, +25°C, and +85°C

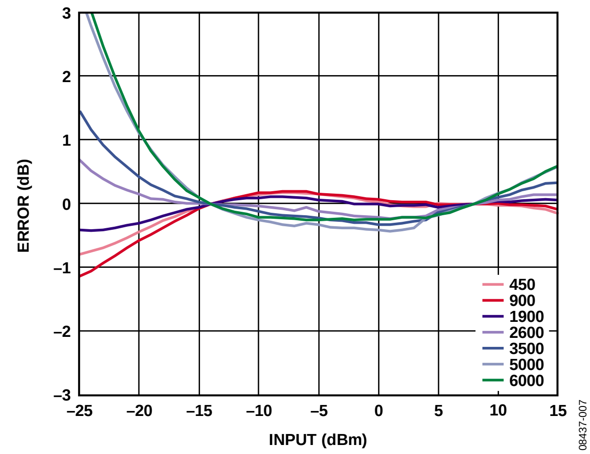

Figure 7. Linearity Error vs. Input Level, 450 MHz, 900 MHz, 1900 MHz, 2600 MHz, 3500 MHz, 5000 MHz, 6000 MHz Frequencies, 3.0 V Supply

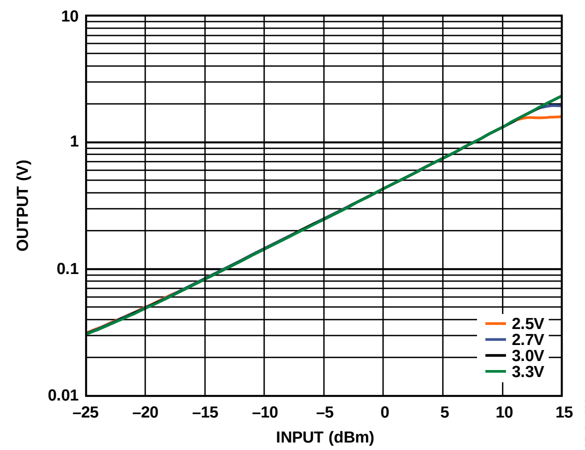

Figure 8. Output vs. Input Level, 900 MHz Frequency, 2.5 V, 2.7 V, 3.0 V, and 3.3 V Supplies

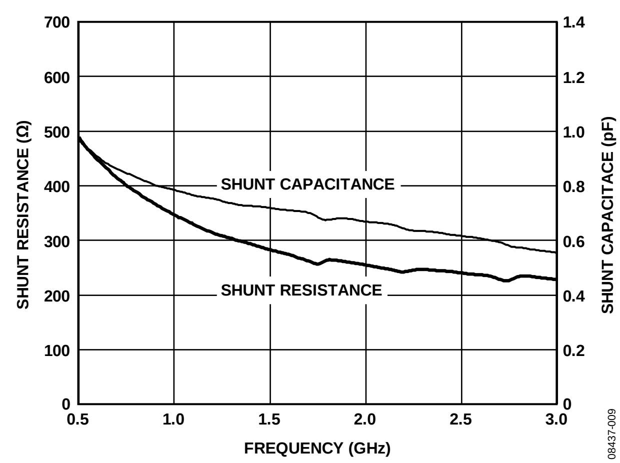

Figure 9. Input Impedance vs. Frequency, 3.0 V Supply, at −40°C, +25°C, and +85°C

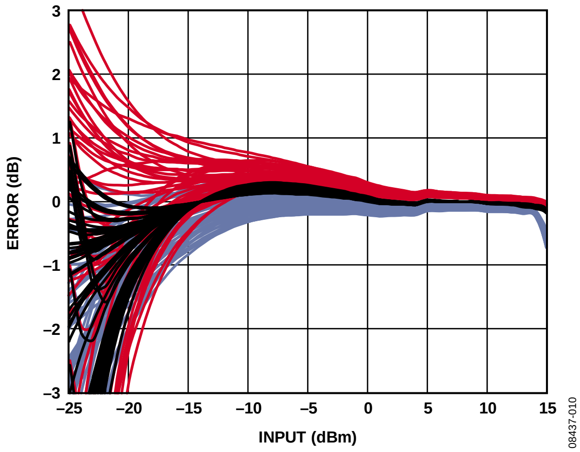

Figure 10. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 450 MHz Frequency

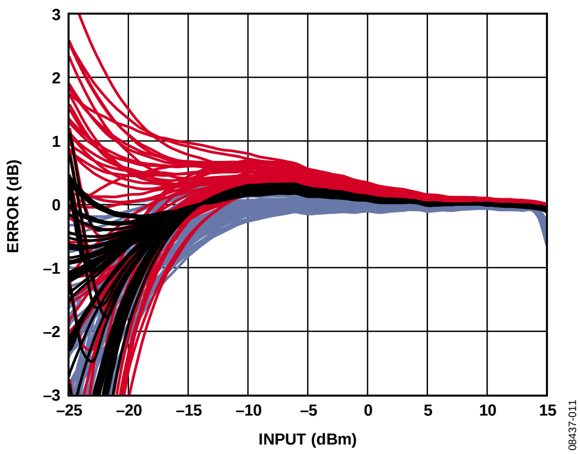

Figure 11. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 900 MHz Frequency

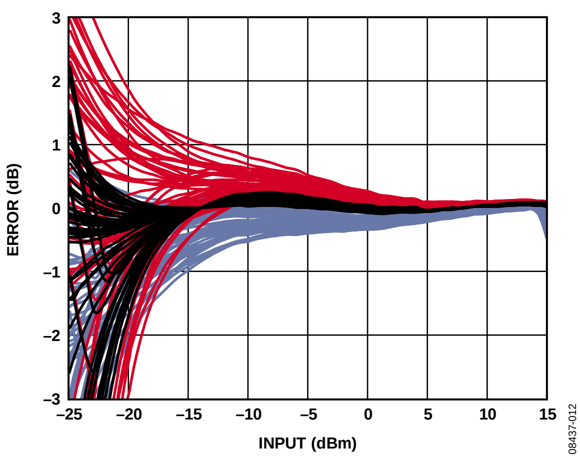

Figure 12. Output Temperature Drift from +25°C Linear Reference for 50 Devices at −40°C, +25°C, and +85°C, 1900 MHz Frequency

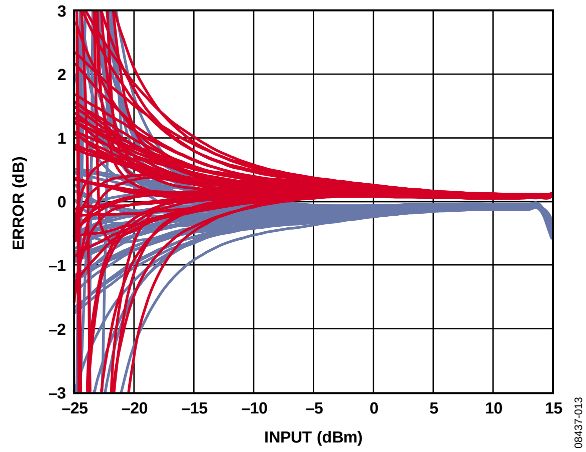

Figure 13. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 450 MHz Frequency

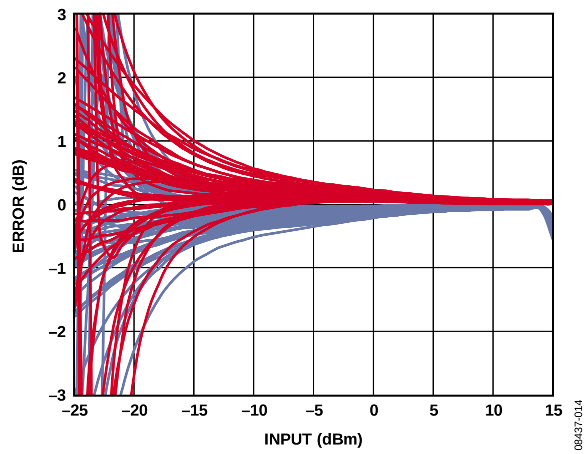

Figure 14. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 900 MHz Frequency

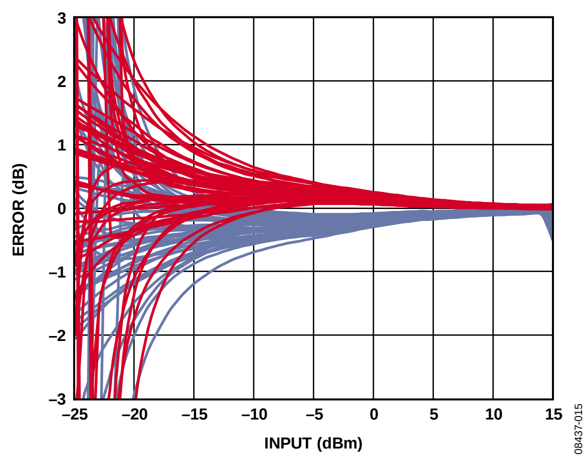

Figure 15. Output Delta from +25°C Output Voltage for 50 Devices at −40°C and +85°C, 1900 MHz Frequency

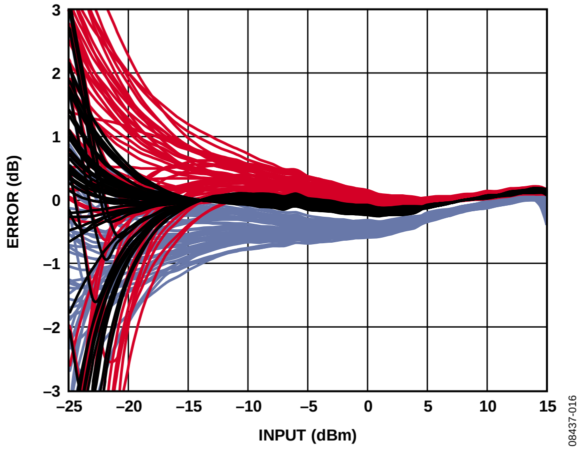

Figure 16. Output Temperature Drift from +25°C Linear Reference for 50 Devices at –40°C, +25°C, and +85°C, 2600 MHz Frequency

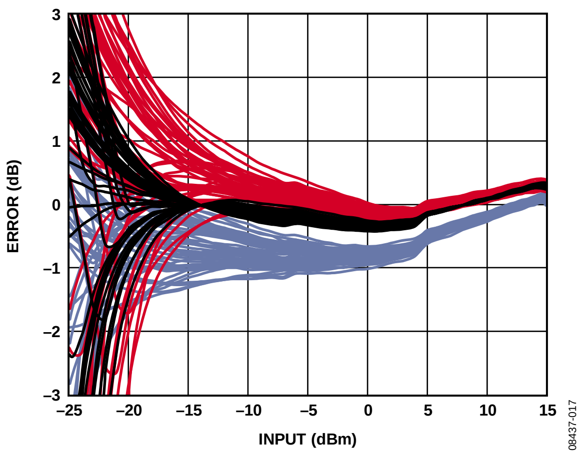

Figure 17. Output Temperature Drift from +25°C Linear Reference for 50 Devices at –40°C, +25°C, and +85°C, 3500 MHz Frequency

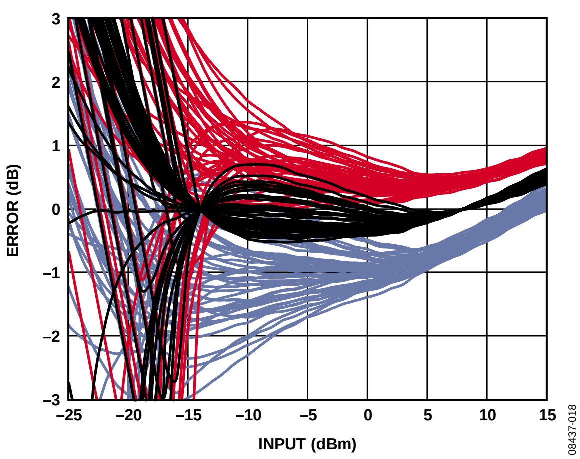

Figure 18. Output Temperature Drift from +25°C Linear Reference for 50 Devices at –40°C, +25°C, and +85°C, 6000 MHz Frequency

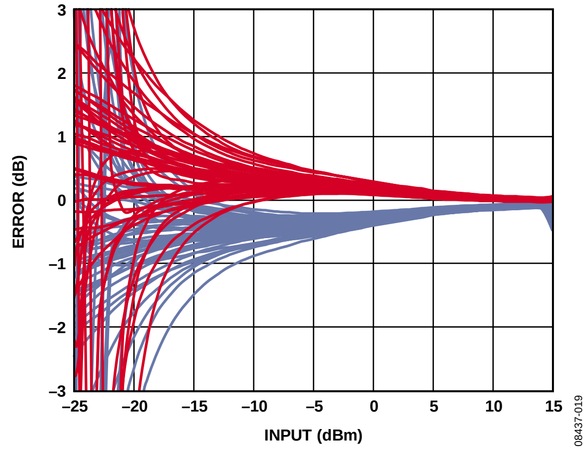

Figure 19. Output Delta from +25°C Output Voltage for 50 Devices at –40°C and +85°C, 2600 MHz Frequency

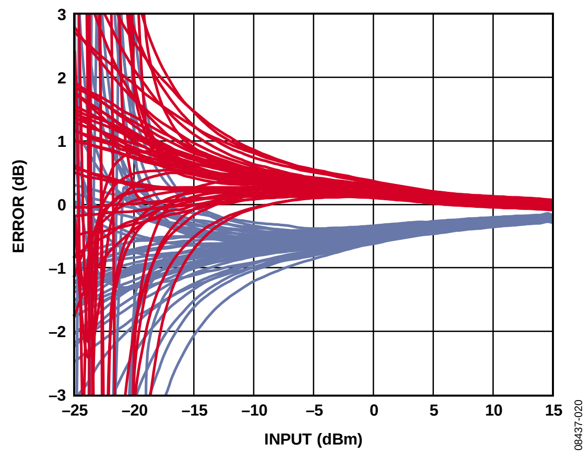

Figure 20. Output Delta from +25°C Output Voltage for 50 Devices at –40°C and +85°C, 3500 MHz Frequency

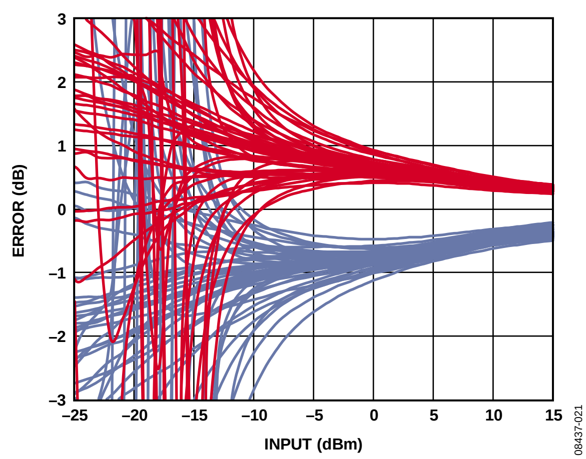

Figure 21. Output Delta from +25°C Output Voltage for 50 Devices at –40°C and +85°C, 6000 MHz Frequency

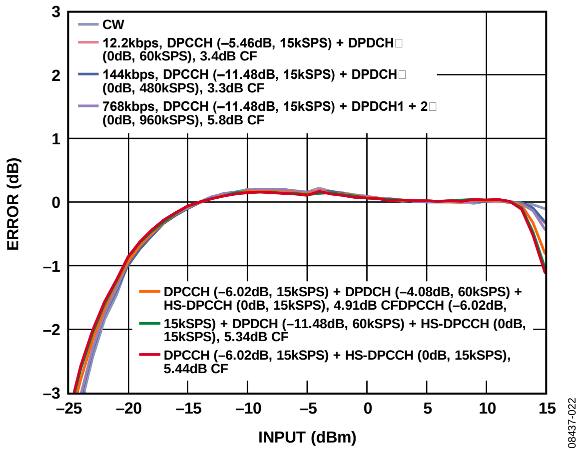

Figure 22. Error from CW Linear Reference vs. Input with Various W-CDMA Reverse Link Waveforms at 900 MHz, C_{FLTR} = 10 nF, C_{OUT} = Open

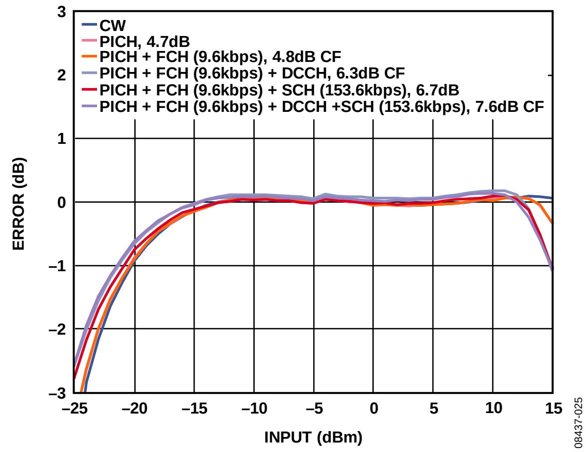

Figure 25. Error from CW Linear Reference vs. Input with Various CDMA2000 Reverse Link Waveforms at 1900 MHz, C_{FLTR} = 12 nF, C_{OUT} = Open

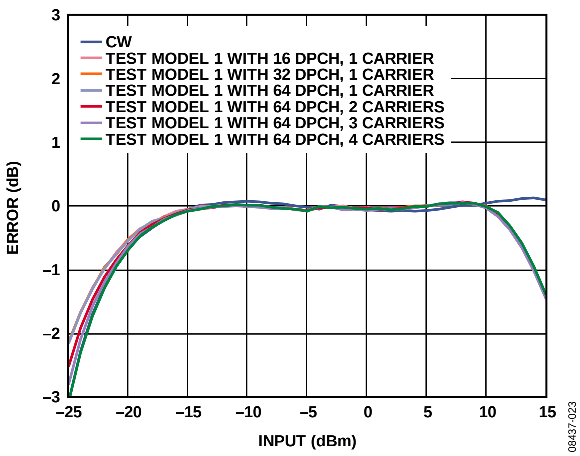

Figure 23. Error from CW Linear Reference vs. Input with Various W-CDMA Forward Link Waveforms at 2200 MHz, C_{FLTR} = 10 nF, C_{OUT} = Open

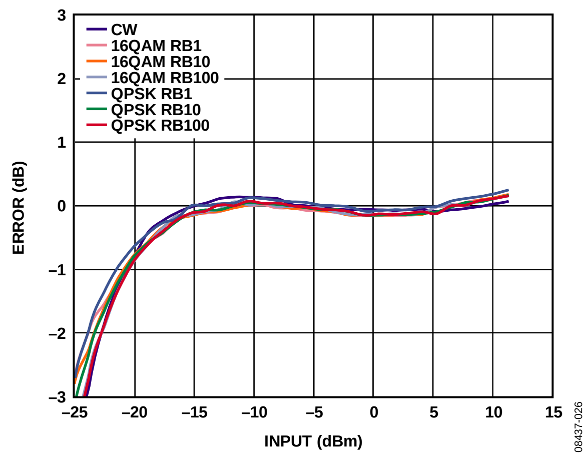

Figure 26. Error from CW Linear Reference vs. Input with Various LTE Reverse Link Waveforms at 2600 MHz, C_{FLTR} = 12 nF, C_{OUT} = Open

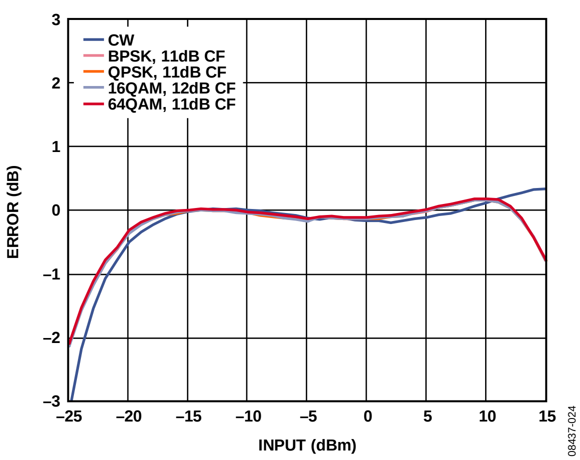

Figure 24. Error from CW Linear Reference vs. Input with Various 802.16 OFDM Waveforms at 3500 MHz, 10 MHz Signal BW, and 256 Subcarriers for All Modulated Signals, C_{FLTR} = 10 nF, C_{OUT} = Open

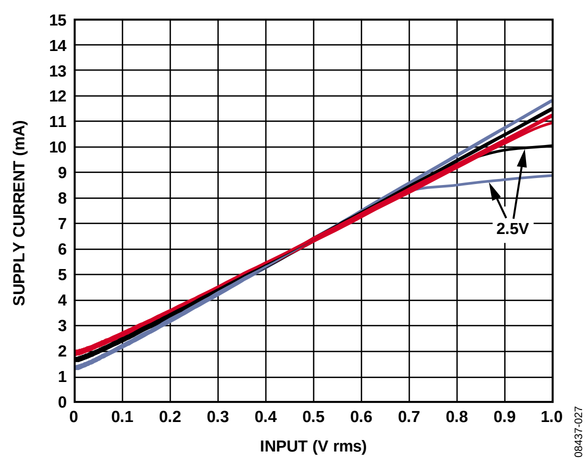

Figure 27. Supply Current vs. Input Level, 2.5 V, 3.0 V, and 3.3 V Supplies, 900 MHz Frequency, at −40°C, +25°C, and +85°C

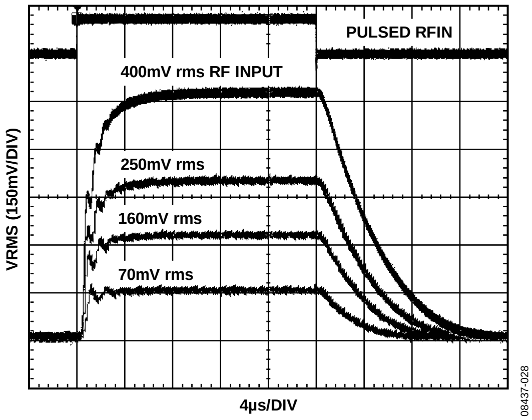

Figure 28. Output Response to Various RF Input Pulse Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} = Open, C_{OUT} = Open, R_{OUT} = Open

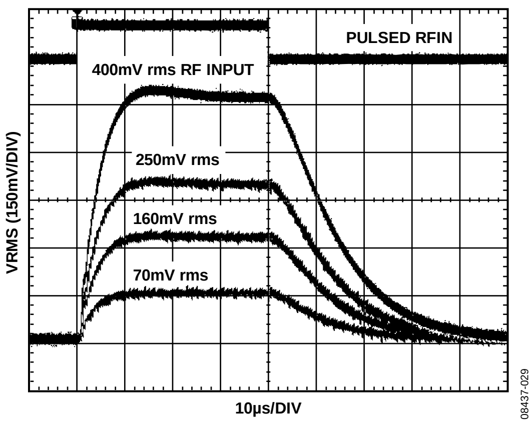

Figure 29. Output Response to Various RF Input Pulse Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} = 10 nF, C_{OUT} = Open, R_{OUT} = Open

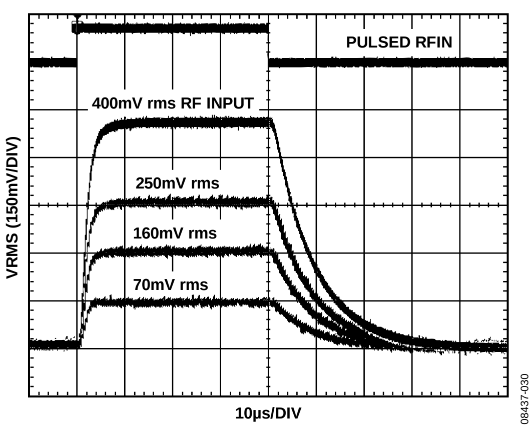

Figure 30. Output Response to Various RF Input Pulse Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} =Open, C_{OUT} = 10 nF, R_{OUT} = 1 kΩ

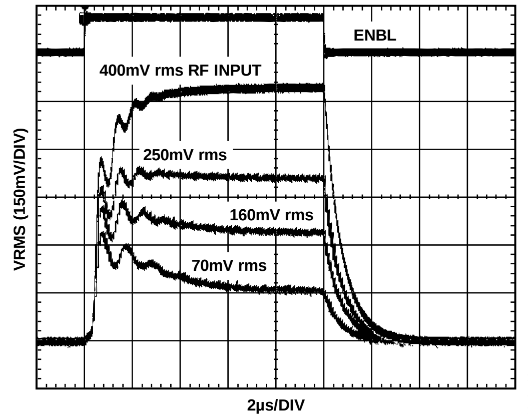

Figure 31. Output Response to Enable Gating at Various RF Input Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} = Open, C_{OUT} = Open, R_{OUT} = Open

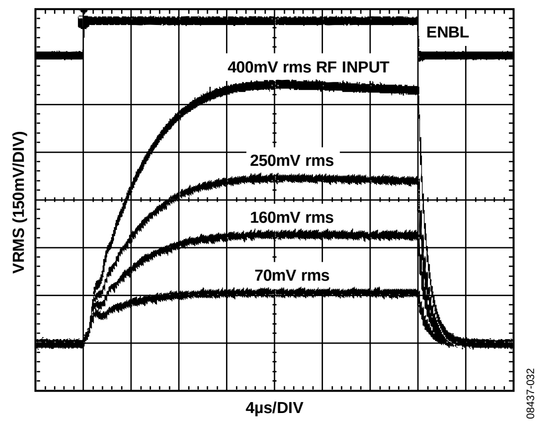

Figure 32. Output Response to Enable Gating at Various RF Input Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} = 10 nF, C_{OUT} = Open, R_{OUT} = Open

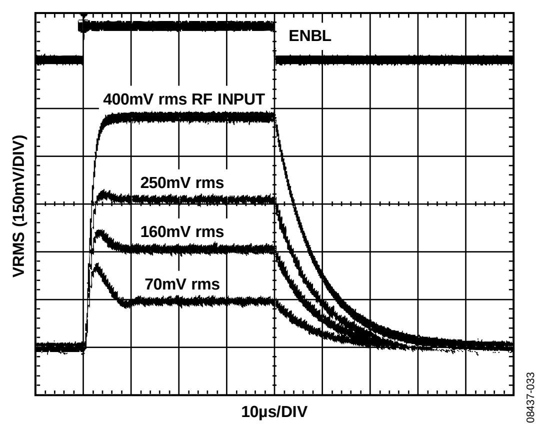

Figure 33. Output Response to Enable Gating at Various RF Input Levels, 3.0 V Supply, 900 MHz Frequency, C_{FLTR} =Open, C_{OUT} = 10 nF, R_{OUT} = 1 kΩ

CIRCUIT DESCRIPTION

The ADL5504 employs two-stage detection. The critical aspect of this technical approach is the concept of first stripping the carrier to reveal the envelope and then performing the required analog computation of rms.

RMS CIRCUIT DESCRIPTION AND FILTERING

The rms processing is executed using a proprietary translinear technique. This method is a mathematically accurate rms computing approach and allows achieving unprecedented rms accuracies for complex modulation signals irrespective of the crest factor of the input signal. An integrating filter capacitor performs the square-domain averaging. The VRMS output can be expressed as

$$VRMS = A \times \sqrt{\frac{\int_{T1}^{T2} V_{IN}^2 \times dt}{T2 - T1}}$$

Note that A is a scaling parameter that is determined by the on-chip resistor ratio, and there are no other scaling parameters involved in this computation, which means that the rms output is inherently free from any sources of error due to temperature, supply, and process variations.

FILTERING

An important aspect of rms-dc conversion is the need for averaging (the function is root-mean-square). The on-chip averaging in the square domain has a corner frequency of approximately 140 kHz and is sufficient for common modulation signals, such as CDMA-, CDMA2000-, WCDMA-, and QPSK-/ QAM-based OFDM (for example, LTE, WLAN, and WiMAX).

For improved accuracy with more complex RF waveforms (with modulation components extending down into the kilohertz region), more filtering is necessary to supplement the on-chip, low-pass filter. For this reason, the FLTR pin is provided; a capacitor attached between this pin and VPOS can extend the averaging time to very low frequencies (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section). Any external capacitor acts on a 1 kΩ resistor to yield a new corner frequency for the rms filter (see Figure 1).

Adequate filtering ensures the accuracy of the rms measurement; however, some ripple or ac residual can still be present on the dc output. To reduce this ripple, an external shunt capacitor can be used at the output to form a low-pass filter with the on-chip, 100 Ω resistance (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section).

OUTPUT BUFFER

A buffer takes the internal rms signal and amplifies it accordingly before it is output on the VRMS pin. The output stage of the rms buffer is a common source PMOS with a resistive load to provide a rail-to-rail output. The buffer has a 100 Ω on-chip series resistance on the output, allowing for easy low-pass filtering.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 34 shows the basic connections for the ADL5504. The device is powered by a single supply between 2.5 V and 3.3 V, with a quiescent current of 1.8 mA. The VPOS pin is decoupled using 100 pF and 0.1 μF capacitors.

Placing a single 75 Ω resistor at the RF input provides a broadband match of 50 Ω. More precise resistive or reactive matches can be applied for narrow frequency band use (see the RF Input Interfacing section).

The rms averaging can be augmented by placing additional capacitance at C_{FLTR}. The ac residual can be reduced further by increasing the output capacitance, C_{OUT}. The combination of the internal 100 Ω output resistance and C_{OUT} produces a low-pass filter to reduce output ripple of the VRMS output (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section for more details).

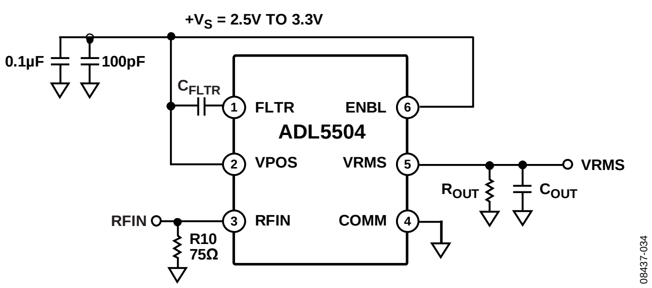

Figure 34. Basic Connections for ADL5504

RF INPUT INTERFACING

The input impedance of the ADL5504 decreases with increasing frequency in both its resistive and capacitive components (see Figure 9). The resistive component varies from 370 Ω at 900 MHz to about 240 Ω at 2600 MHz.

A number of options exist for input matching. For operation at multiple frequencies, a 75 Ω shunt to ground, as shown in Figure 35, provides the best overall match. For use at a single frequency, a resistive or a reactive match can be used. By plotting the input impedance on a Smith chart, the best value for a resistive match can be calculated. (Both input impedance and input capacitance can vary by up to ±20% around their nominal values.) Where VSWR is critical, the match can be improved with a series inductor placed before the shunt component.

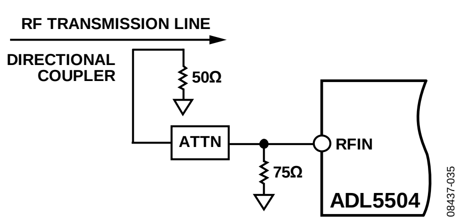

Figure 35. Input Interfacing to Directional Coupler

Resistive Tap RF Input

Figure 36 shows a technique for coupling the input signal into the ADL5504 that can be applicable when the input signal is much larger than the input range of the ADL5504. A series resistor combines with the input impedance of the ADL5504 to attenuate the input signal. Because this series resistor forms a divider with the frequency-dependent input impedance, the apparent gain changes greatly with frequency. However, this method has the advantage of very little power being tapped off in RF power transmission applications. If the resistor is large compared with the impedance of the transmission line, the VSWR of the system is relatively unaffected.

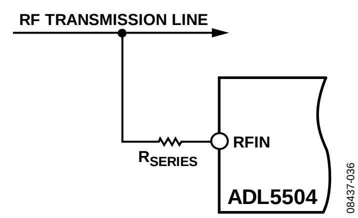

Figure 36. Attenuating the Input Signal

The resistive tap or series resistance, R_{SERIES}, can be expressed as

$$R_{SERIES} = R_{IN}\,(1 - 10^{ATTN/20})/(10^{ATTN/20}) \quad (1)$$

where:
R_{IN} is the input resistance of RFIN.
ATTN is the desired attenuation factor in decibels.

For example, if a power amplifier with a maximum output power of 28 dBm is matched to the ADL5504 input at 5 dBm, then a −23 dB attenuation factor is required. At 900 MHz, the input resistance, R_{IN}, is 370 Ω.

$$R_{SERIES} = (370\ \Omega)(1 - 10^{-23/20})/(10^{-23/20}) = 4870\ \Omega \quad (2)$$

Thus, for an attenuation of −23 dB, a series resistance of approximately 4.87 kΩ is needed.

Multiple RF Inputs

Figure 37 shows a technique for combining multiple RF input signals to the ADL5504. Some applications can share a single detector for multiple bands. Three 16.5 Ω resistors in a T network combine the three 50 Ω terminations (including the ADL5504 with the shunt 75 Ω matching component). The broadband resistive combiner ensures that each port of the T network sees a 50 Ω termination. Because there are only 6 dB of isolation from one port of the combiner to the other ports, only one band should be active at a time.

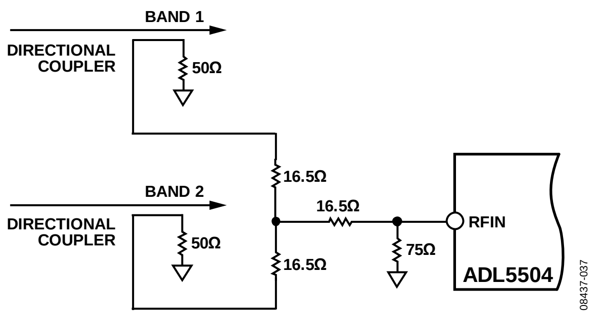

Figure 37. Combining Multiple RF Input Signals

LINEARITY

Because the ADL5504 is a linear responding device, plots of output voltage vs. input voltage result in a straight line (see Figure 4 and Figure 5) and the dynamic range in decibels (dB) is not clearly visible. It is more useful to plot the error on a logarithmic scale, as shown in Figure 7. The deviation of the plot from the ideal straight line characteristic is caused by input stage clipping at the high end and by signal offsets at the low end. However, offsets at the low end can be either positive or negative; therefore, the linearity error vs. input level plots (see Figure 7) can also trend upwards at the low end. Figure 10 to Figure 12 and Figure 16 to Figure 18 show error distributions for a large population of devices at specific frequencies over temperature.

It is also apparent in Figure 7 that the error at the lower portion of the dynamic range tends to shift up as frequency is increased. This is due to the calibration points chosen, −14 dBm and +8 dBm (see the Device Calibration and Error Calculation section).

The absolute value cell has an input impedance that varies with frequency. The result is a decrease in the actual voltage across the squaring cell as the frequency increases, reducing the conversion gain. The dynamic range is near constant over frequency, but with a decrease in conversion gain as frequency is increased.

Output Swing

At 900 MHz, the VRMS output voltage is nominally 1.87× the input rms voltage (a conversion gain of 1.87 V/V rms). The output voltage swings from near ground to 2.5 V on a 3.0 V supply.

Figure 8 shows the output swings of the ADL5504 to a CW input for various supply voltages. Only at the lowest supply voltage (2.5 V) is there a reduction in the dynamic range as the input headroom decreases.

Output Offset

The ADL5504 has a ±1 dB error detection range of about 30 dB, as shown in Figure 10 to Figure 12 and Figure 16 to Figure 18. The error is referred to the best-fit line defined in the linear region of the output response (see the Device Calibration and Error Calculation section for more details). Below an input power of −18 dBm, the response is no longer linear and begins to lose accuracy. In addition, depending on the supply voltage, saturation may limit the detection accuracy above 12 dBm. Calibration points should be chosen in the linear region, avoiding the nonlinear ranges at the high and low extremes.

Figure 38 shows a distribution of the output response vs. the input for multiple devices. The ADL5504 loses accuracy at low input powers as the output response begins to fan out. As the input power is reduced, the spread of the output response increases along with the error.

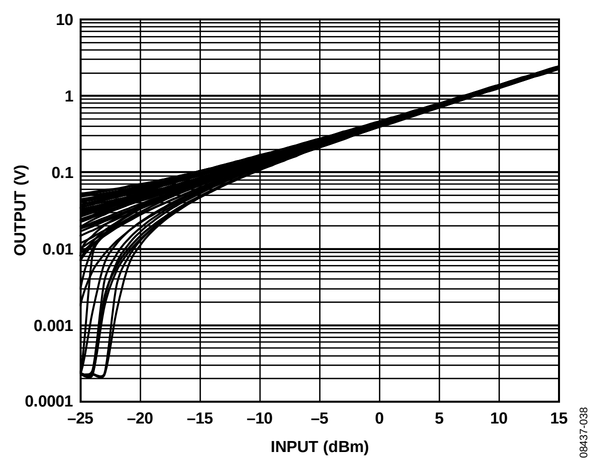

Figure 38. Output vs. Input Level Distribution of 50 Devices, 900 MHz Frequency, 3.0 V Supply

Although some devices follow the ideal linear response at very low input powers, not all devices continue the ideal linear regression to a near 0 V y-intercept. Some devices exhibit output responses that rapidly decrease and some flatten out.

With no RF signal applied, the ADL5504 has a typical output offset of 10 mV (with a maximum of 100 mV) on VRMS.

OUTPUT DRIVE CAPABILITY AND BUFFERING

The ADL5504 is capable of sourcing a VRMS output current of approximately 3 mA. The output current is sourced through the on-chip, 100 Ω series resistor; therefore, any load resistor forms a voltage divider with this on-chip resistance. It is recommended that the ADL5504 VRMS output drive high resistance loads to preserve output swing. If an application requires driving a low resistance load (as well as in cases where increasing the nominal conversion gain is desired), a buffering circuit is necessary.

SELECTING THE SQUARE-DOMAIN FILTER AND OUTPUT LOW-PASS FILTER

The internal filter capacitor of the ADL5504 provides averaging in the square domain but leaves some residual ac on the output. Signals with high peak-to-average ratios, such as W-CDMA or CDMA2000, can produce ac residual levels on the ADL5504 VRMS dc output. To reduce the effects of these low frequency components in the waveforms, some additional filtering is required.

The square-domain filter capacitance of the ADL5504 can be augmented by connecting a capacitor between Pin 1 (FLTR) and Pin 2 (VPOS). In addition, the VRMS output of the ADL5504 can be filtered directly by placing a capacitor between VRMS (Pin 5) and ground. The combination of the on-chip, 100 Ω output series resistance and the external shunt capacitor forms a low-pass filter to reduce the residual ac.

Figure 39 and Figure 40 show the effects on the residual ripple vs. the output and square-domain filter capacitor values at two communication standards with high peak-to-average ratios. Note that there is a trade-off between ac residual and response time. Large filter capacitances increase the turn-on and pulse response times (see Figure 28 to Figure 33). Figure 41 shows the effect of the two filtering options, the output filter and the square-domain filter capacitor, on the pulse response time of the ADL5504. For more information on the effects of the filter capacitances on the response, see the Power Consumption, Enable, and Power-On/Power-Off Response Time section.

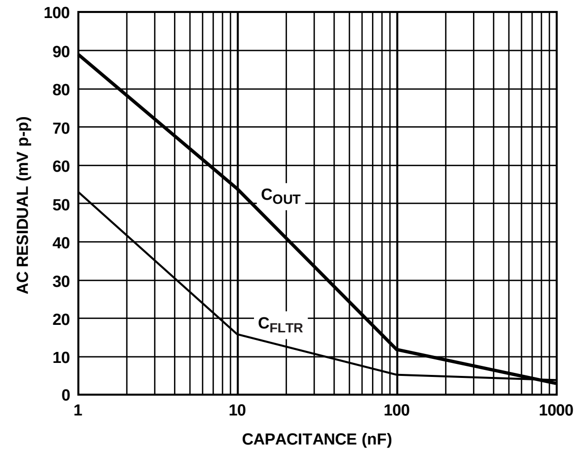

Figure 39. AC Residual vs. C_{FLTR} and C_{OUT}, W-CDMA Reverse Link (5.8 dB CF) Waveform

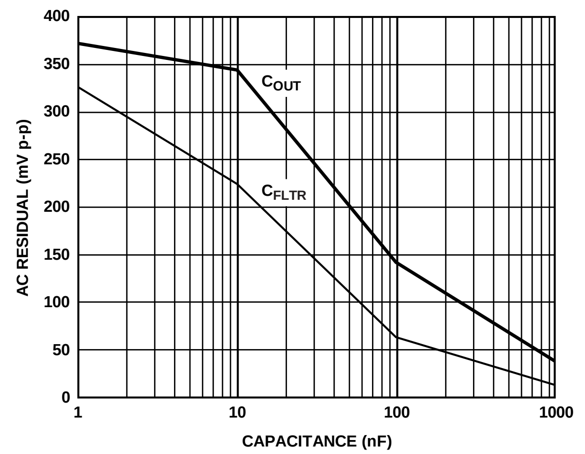

Figure 40. AC Residual vs. C_{FLTR} and C_{OUT}, W-CDMA Forward Link (11.7 dB CF) Waveform

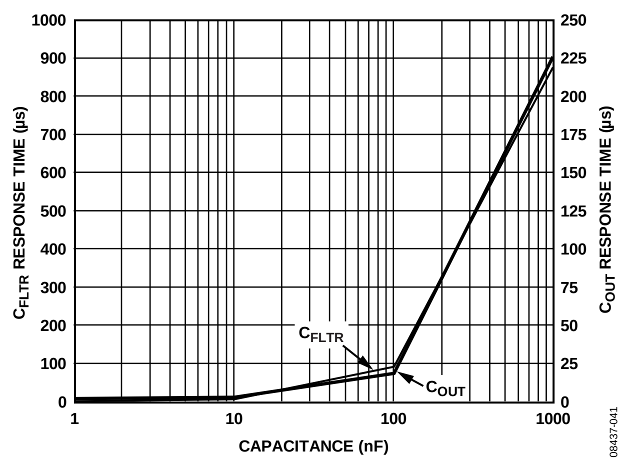

Figure 41. C_{FLTR} and C_{OUT} Response Time vs. Capacitance

POWER CONSUMPTION, ENABLE, AND POWER-ON/POWER-OFF RESPONSE TIME

The quiescent current consumption of the ADL5504 varies linearly with the size of the input signal from approximately 1.8 mA for no signal up to 9 mA at an input level of 0.7 V rms (10 dBm, referred to 50 Ω). There is little variation in supply current across power supply voltage or temperature, as shown in Figure 27.

The ADL5504 can be disabled either by pulling the ENBL (Pin 6) to COMM (Pin 4) or by removing the power supply to the device. Disabling the device via the ENBL function reduces the leakage current to less than 1 μA. When the device is disabled, the output impedance increases to approximately 5.5 kΩ on VRMS.

The turn-on time and pulse response is strongly influenced by the sizes of the square-domain filter and the output shunt capacitor. Figure 42 shows a plot of the output response to an RF pulse on the RFIN pin, with a 0.1 μF output filter capacitor and a no square-domain filter capacitor. The falling edge is particularly dependent on the output shunt capacitance, as shown in Figure 42.

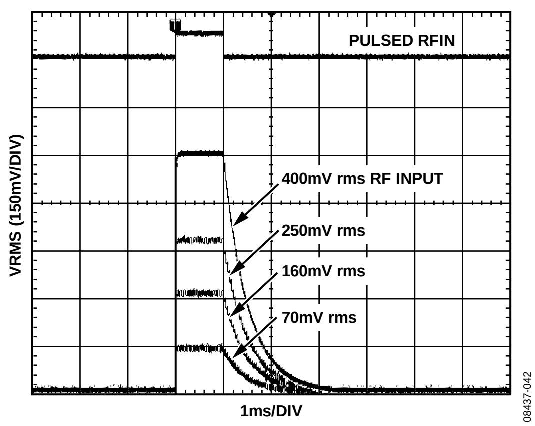

Figure 42. Output Response to Various RF Input Pulse Levels, 3 V Supply, 900 MHz Frequency, Square-Domain Filter Open, C_{OUT} = 0.1 μF

To improve the falling edge of the enable and pulse responses, a resistor can be placed in parallel with the output shunt capacitor. The added resistance helps to discharge the output filter capacitor. Although this method reduces the power-off time, the added load resistor also attenuates the output (see the Output Drive Capability and Buffering section).

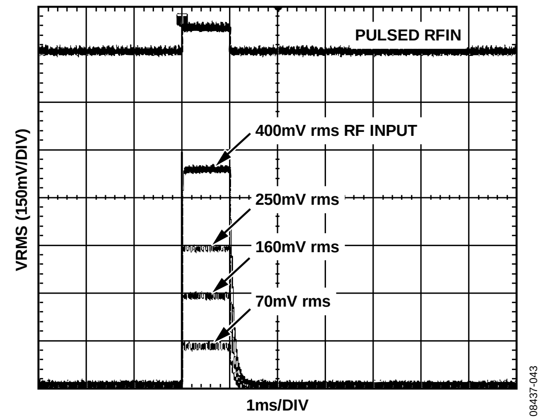

Figure 43. Output Response to Various RF Input Pulse Levels, 3 V Supply, 900 MHz Frequency, Square-Domain Filter Open, C_{OUT} = 0.1 μF with Parallel 1 kΩ

The square-domain filter improves the rms accuracy for high crest factors (see the Selecting the Square-Domain Filter and Output Low-Pass Filter section), but it can hinder the response time. For optimum response time and low ac residual, both the square-domain filter and the output filter should be used. The square-domain filter at FLTR can be reduced to improve response time, and the remaining ac residual can be decreased by using the output filter, which has a smaller time constant.

DEVICE CALIBRATION AND ERROR CALCULATION

Because slope and intercept vary from device to device, board-level calibration must be performed to achieve high accuracy. In general, calibration is performed by applying two input power levels to the ADL5504 and measuring the corresponding output voltages. The calibration points are generally chosen to be within the linear operating range of the device. The best-fit line is characterized by calculating the conversion gain (or slope) and intercept using the following equations:

$$Gain = (V_{VRMS2} - V_{VRMS1})/(V_{IN2} - V_{IN1}) \quad (3)$$

$$Intercept = V_{VRMS1} - (Gain \times V_{IN1}) \quad (4)$$

where:
V_{INx} is the rms input voltage to RFIN.
V_{VRMSx} is the voltage output at VRMS.

Once gain and intercept are calculated, an equation can be written that allows calculation of an (unknown) input power based on the measured output voltage.

$$V_{IN} = (V_{VRMS} - Intercept)/Gain \quad (5)$$

For an ideal (known) input power, the law conformance error of the measured data can be calculated as

$$ERROR\ (\text{dB}) = 20 \times \log\left[(V_{VRMS,\ MEASURED} - Intercept)/(Gain \times V_{IN,\ IDEAL})\right] \quad (6)$$

Figure 44 shows a plot of the error at 25°C, the temperature at which the ADL5504 is calibrated. Note that the error is not 0; this is because the ADL5504 does not perfectly follow the ideal linear equation, even within its operating region. The error at the calibration points is, however, equal to 0 by definition.

Figure 44 also shows error plots for the output voltage at −40°C and +85°C. These error plots are calculated using the gain and intercept at 25°C. This is consistent with calibration in a mass production environment where calibration at temperature is not practical.

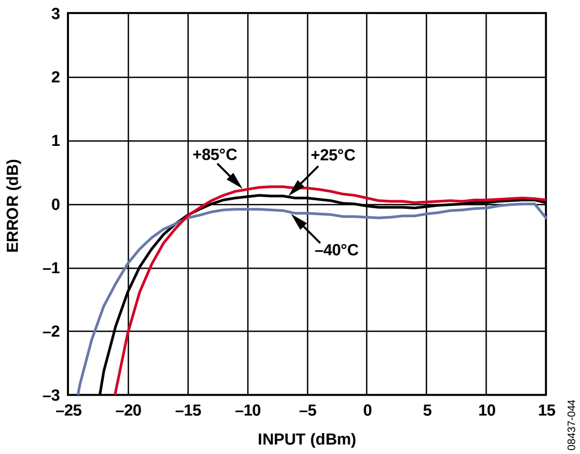

Figure 44. Error from Linear Reference vs. Input at −40°C, +25°C, and +85°C vs. +25°C Linear Reference, 1900 MHz Frequency, 3.0 V Supply

CALIBRATION FOR IMPROVED ACCURACY

Another way of presenting the error function of the ADL5504 is shown in Figure 45. In this case, the decibel (dB) error at hot and cold temperatures is calculated with respect to the transfer function at ambient temperature. This is a key difference in comparison to Figure 44, in which the error was calculated with respect to the ideal linear transfer function at ambient temperature. When this alternative technique is used, the error at ambient temperature becomes equal to 0 by definition (see Figure 45).

This plot is a useful tool for estimating temperature drift at a particular power level with respect to the (nonideal) response at ambient temperature. The linearity and dynamic range tend to be improved artificially with this type of plot because the ADL5504 does not perfectly follow the ideal linear equation (especially outside of its linear operating range). Achieving this level of accuracy in an end application requires calibration at multiple points in the operating range of the device.

In some applications, very high accuracy is required at just one power level or over a reduced input range. For example, in a wireless transmitter, the accuracy of the high power amplifier (HPA) is most critical at or close to full power. The ADL5504 offers a tight error distribution in the high input power range, as shown in Figure 45. The high accuracy range, beginning around 2 dBm at 1900 MHz, offers 12 dB of ±0.15 dB detection error over temperature. Multiple point calibration at ambient temperature in the reduced range offers precise power measurement with near 0 dB error from −40°C to +85°C.

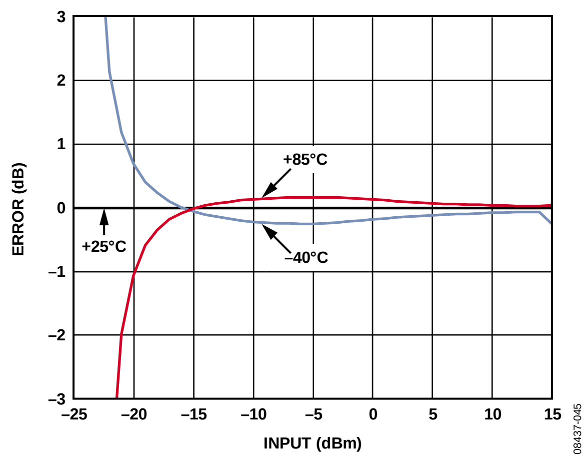

Figure 45. Error from +25°C Output Voltage at −40°C, +25°C, and +85°C After Ambient Normalization, 1900 MHz Frequency, 3.0 V Supply

Note that the high accuracy range center varies over frequency (see Figure 13 to Figure 15 and Figure 19 to Figure 21).

DRIFT OVER A REDUCED TEMPERATURE RANGE

Figure 46 shows the error over temperature for a 1900 MHz input signal. The error due to drift over temperature consistently remains within ±0.20 dB and only begins to exceed this limit when the ambient temperature rises above +55°C and drops below −30°C. For all frequencies using a reduced temperature range, higher measurement accuracy is achievable.

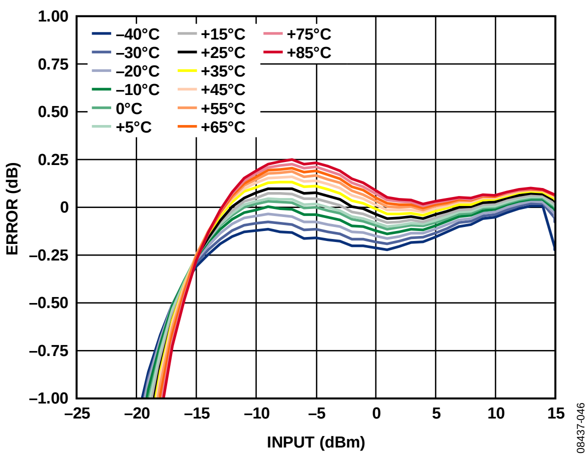

Figure 46. Typical Drift at 1900 MHz for Various Temperatures

DEVICE HANDLING

The wafer level chip scale package consists of solder bumps connected to the active side of the die. The part is Pb-free and RoHS compliant with 95.5% tin, 4.0% silver, and 0.5% copper solder bump composition. The WLCSP can be mounted on printed circuit boards using standard surface-mount assembly techniques; however, caution should be taken to avoid damaging the die. See the AN-617 Application Note, *MicroCSP Wafer Level Chip Scale Package*, for additional information. WLCSP devices are bumped die; therefore, the exposed die may be sensitive to light, which can influence specified limits. Lighting in excess of 600 lux can degrade performance.

EVALUATION BOARD

Figure 47 shows the schematic of the ADL5504 evaluation board. The board is powered by a single supply in the 2.5 V to 3.3 V range. The power supply is decoupled by 100 pF and 0.1 μF capacitors. The device must be enabled by switching SW1A to the position labeled on.

The RF input has a broadband match of 50 Ω using a single 75 Ω resistor at R7A. More precise matching at spot frequencies is possible (see the RF Input Interfacing section).

Table 4 details the various configuration options of the evaluation board. Figure 48 shows the layout of the evaluation board.

Land Pattern and Soldering Information

Pad diameters of 0.20 mm are recommended with a solder paste mask opening of 0.30 mm. For the RF input trace, a trace width of 0.30 mm is used, which corresponds to a 50 Ω characteristic impedance for the dielectric material being used (FR4). All traces going to the pads are tapered down to 0.15 mm. For the RFIN line, the length of the tapered section is 0.20 mm.

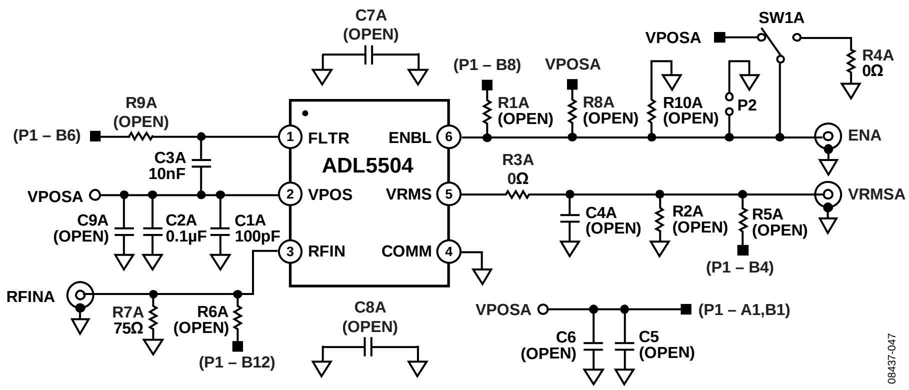

Figure 47. Evaluation Board Schematic

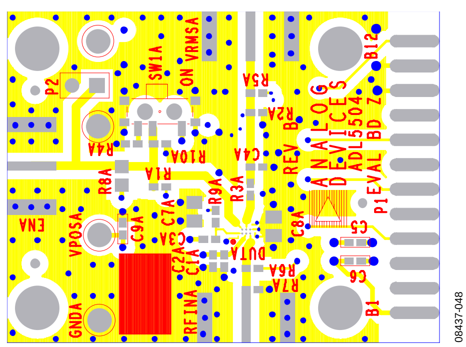

Figure 48. Layout of Evaluation Board, Component Side

Table 4. Evaluation Board Configuration Options

Component	Description	Default Condition
VPOSA, GNDA	Ground and supply vector pins.	Not applicable
C1A, C2A, C7A, C8A, C9A, C5, C6	Power supply decoupling. Nominal supply decoupling of 0.01 μF and 100 pF.	C1A = 100 pF (Size 0402) C2A = 0.1 μF (Size 0402) C7A = C8A = open (Size 0805) C9A = open (Size 0402) C5 = C6 = open (Size 0402)
C3A	Filter capacitor. The internal rms averaging capacitor can be augmented by placing additional capacitance in C3A.	C3A = 10 nF (Size 0402)
R7A	RF input interface. The 75 Ω resistor at R7A combines with the ADL5504 internal input impedance to give a broadband input impedance of around 50 Ω.	R7A = 75 Ω (Size 0402)
C4A, R2A, R3A	Output filtering. The combination of the internal 100 Ω output resistance and C4A produce a low-pass filter to reduce output ripple of the VRMS output. The output can be scaled down using the resistor divider pads, R2A and R3A.	R3A = 0 Ω (Size 0402) R2A = open (Size 0402) C4A= open (Size 0402)
SW1A, R4A, R10A, P2	Device enable. When the SW1A is set to the on position, the ENBL pin is connected to the supply and the ADL5504 is in enable mode. In the opposite switch position, the ENBL pin is grounded (through the 0 Ω resistor) putting the device in power-down mode.	R4A = 0 Ω (Size 0402) R10A = open (Size 0402) SW1A = on position P2 = not installed
P1, R1A, R5A, R6A, R8A, R9A	Alternate interface. The end connector, P1, allows access to various ADL5504 signals. These signal paths are only used during factory test and characterization.	P1 = not installed R1A = R5A = open (Size 0402) R6A = R9A = open (Size 0402) R8A = open (Size 0805)

OUTLINE DIMENSIONS

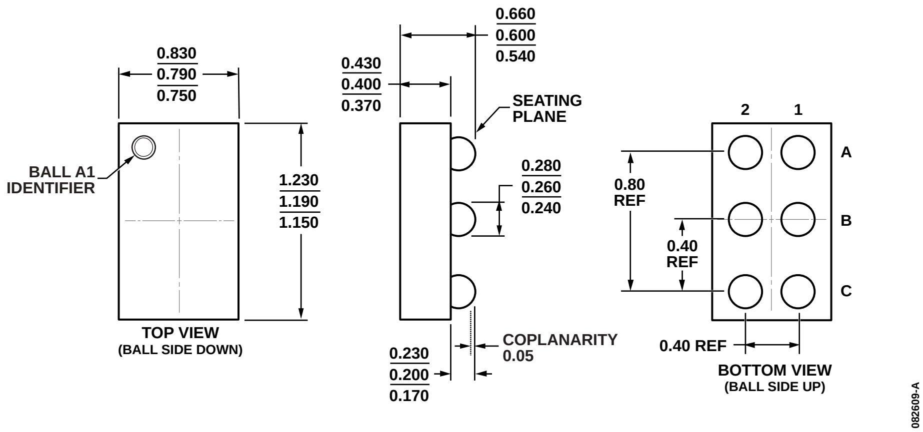

Figure 49. 6-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-6-8)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding	Ordering Quantity
ADL5504ACBZ-P7	–40°C to +85°C	6-Ball WLCSP, 7" Pocket Tape and Reel	CB-6-8	3P	3,000
ADL5504ACBZ-P2	–40°C to +85°C	6-Ball WLCSP, 7" Pocket Tape and Reel	CB-6-8	3P	250
ADL5504-EVALZ		Evaluation Board			

[1] Z = RoHS Compliant Part.

NOTES

NOTES