Programmable Timing Control Hub™ for P4™

Recommended Application:

Intel Tehema and Tehema-E Chipsets

Output Features:

- 4 Differential CPU Clock Pairs @ 3.3V
- 2 - 3V MREF clocks for memory reference seeds, (separate single ended but 180 degrees out of phase)
- 4 - 66MHz 3V66 output
- 10 - 3V 33MHz PCI clocks
- 2 - 48MHz clocks (180 degrees out of phase)
- 2 - 14.318 reference output (180 degrees out of phase)

Key Specifications:

- 3V66 Output jitter <300ps
- CPU Output Jitter <200ps
- MREF Output jitter <250ps

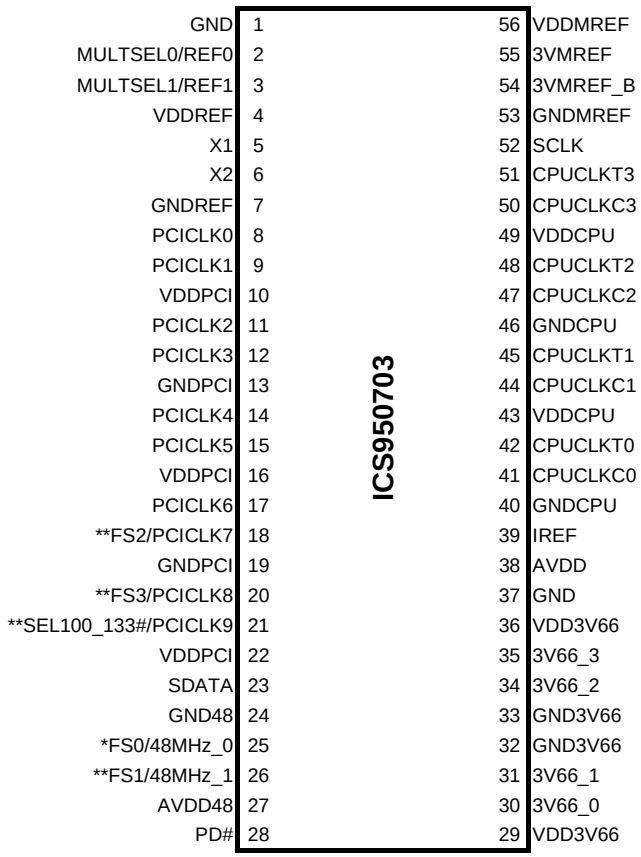
Features/Benefits:

- QuadRom™ frequency selection.
- Programmable asynchronous 3V66/PCI frequency.
- Programmable output frequency.
- Programmable output divider ratios.
- Programmable output rise/fall time.
- Programmable output skew.
- Programmable spread percentage for EMI control.
- Programmable watch dog safe frequency.
- Support I^2C Index read/write and block read/write operations.
- Uses external 14.318MHz reference input.

Frequency Table

Bit4	Bit3	Bit2	Bit1	Bit0	CPU	MREF	AGP	PCI
Sel133/100	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz
0	0	0	0	0	90.00	45.00	30.00	60.00
0	0	0	0	1	100.00	50.00	33.33	66.67
0	0	0	1	0	100.90	50.45	33.63	67.27
0	0	0	1	1	103.00	51.50	34.33	68.67
0	0	1	0	0	105.00	52.50	35.00	70.00
0	0	1	0	1	108.00	54.00	36.00	72.00
0	0	1	1	0	110.00	55.00	36.67	73.33
0	0	1	1	1	112.00	56.00	37.33	74.67
0	1	0	0	0	115.00	57.50	38.33	76.67
0	1	0	0	1	118.00	59.00	39.33	78.67
0	1	0	1	0	120.00	60.00	40.00	80.00
0	1	0	1	1	122.00	61.00	40.67	81.33
0	1	1	0	0	125.00	62.50	41.67	83.33
0	1	1	0	1	127.00	63.50	42.33	84.67
0	1	1	1	0	130.00	65.00	43.33	86.67
0	1	1	1	1	133.60	66.80	44.53	89.07
1	0	0	0	0	120.00	60.00	30.00	60.00
1	0	0	0	1	133.33	66.67	33.33	66.67
1	0	0	1	0	133.90	66.95	33.48	66.95
1	0	0	1	1	136.00	68.00	34.00	68.00
1	0	1	0	0	138.00	69.00	34.50	69.00
1	0	1	0	1	140.00	70.00	35.00	70.00
1	0	1	1	0	142.00	71.00	35.50	71.00
1	0	1	1	1	144.00	72.00	36.00	72.00
1	1	0	0	0	145.00	72.50	36.25	72.50
1	1	0	0	1	148.00	74.00	37.00	74.00
1	1	0	1	0	150.00	75.00	37.50	75.00
1	1	0	1	1	152.00	76.00	38.00	76.00
1	1	1	0	0	154.00	77.00	38.50	77.00
1	1	1	0	1	156.00	78.00	39.00	78.00
1	1	1	1	0	158.00	79.00	39.50	79.00
1	1	1	1	1	160.00	80.00	40.00	80.00

Pin Configuration



56-SSOP

* Internal Pull-Up Resistor

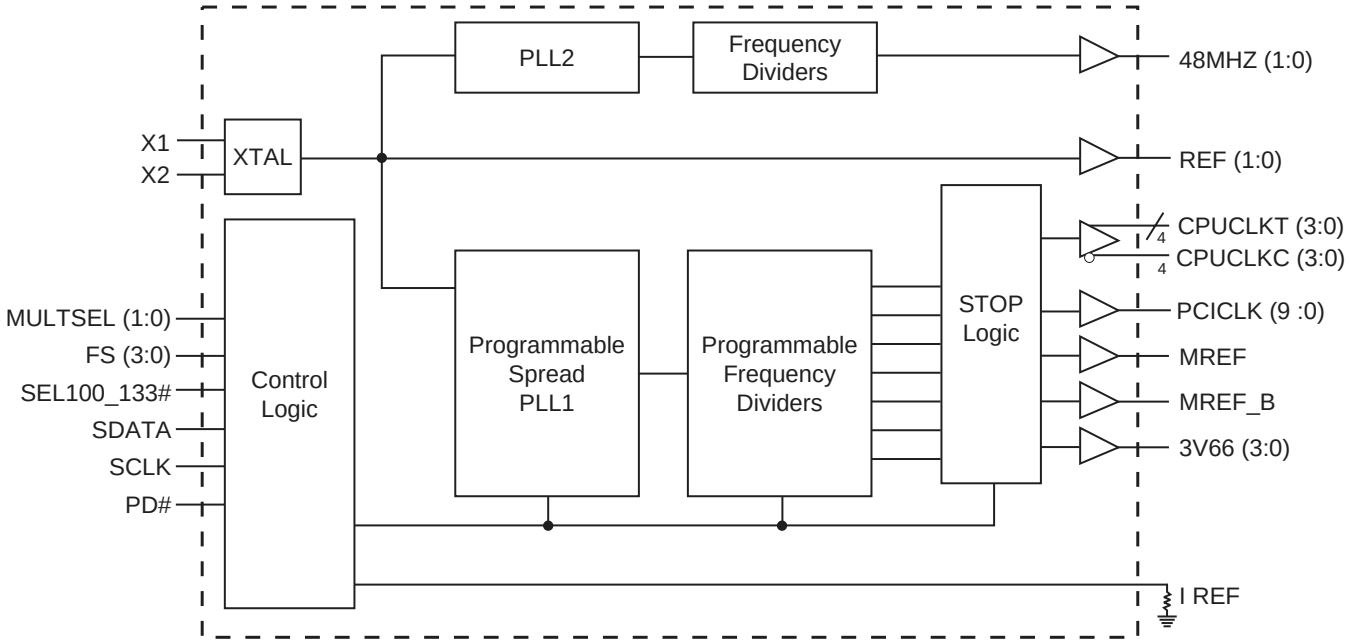
** Internal Pull-Down Resistor

General Description

The **ICS950703** is a single chip clock solution for desktop designs using the Intel Brookdale chipset with Rambus RDRAM memory. It provides all necessary clock signals for such a system.

The **ICS950703** is part of a whole new line of ICS clock generators and buffers called TCH™ (Timing Control Hub). This part incorporates ICS's newest clock technology which offers more robust features and functionality. Employing the use of a serially programmable I^2C interface, this device can adjust the output clocks by configuring the frequency setting, the output divider ratios, selecting the ideal spread percentage, the output skew, the output strength, and enabling/disabling each individual output clock. M/N control can configure output frequency with resolution up to 0.1MHz increment. This part also provides 128 frequency selections via ICS QuadROM™ technology as an alternate to M/N programming.

Block Diagram



Power Groups

Pin Number		Description
AVDD	GND	
4	7	REF output, Crystal
27	24	48MHz fixed, Fixed PLL
38	37	CPU PLL, CPU Master Clock,
VDD	GND	--
10, 16, 22	13, 19	PCI outputs
29, 36	32, 33	3V66 outputs
43, 49	40, 46	CPU Outputs, IREF, MULTSEL
56	53	MREF outputs

Pin Description

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
1	GND	PWR	Ground pin.
2	MULTSEL0/REF0	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 14.318 MHz reference clock.
3	MULTSEL1/REF1	I/O	3.3V LVTTL input for selection the current multiplier for CPU outputs / 14.318 MHz reference clock.
4	VDDREF	PWR	Ref, XTAL power supply, nominal 3.3V
5	X1	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
6	X2	I/O	Frequency select latch input pin / 3.3V PCI free running clock output.
7	GNDREF	PWR	Ground pin for the REF outputs.
8	PCICLK0	OUT	PCI clock output.
9	PCICLK1	I/O	Watchdog enable latch input/ 3.3V PCI clock output.
10	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
11	PCICLK2	OUT	PCI clock output.
12	PCICLK3	OUT	PCI clock output.
13	GNDPCI	PWR	Ground pin for the PCI outputs
14	PCICLK4	OUT	PCI clock output.
15	PCICLK5	OUT	PCI clock output.
16	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
17	PCICLK6	OUT	PCI clock output.
18	**FS2/PCICLK7	I/O	Frequency select latch input pin / 3.3V PCI clock output.
19	GNDPCI	PWR	Ground pin for the PCI outputs
20	**FS3/PCICLK8	I/O	Frequency select latch input pin / 3.3V PCI clock output.
21	**SEL100_133#/PCICLK9	I/O	Latched select input for 100 or 133.3MHz selection. 0=133MHz, 1 = 100MHz / 3.3V PCI clock output.
22	VDDPCI	PWR	Power supply for PCI clocks, nominal 3.3V
23	SDATA	I/O	Data pin for I2C circuitry 5V tolerant
24	GND48	PWR	Ground pin for the 48MHz outputs
25	*FS0/48MHz_0	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
26	**FS1/48MHz_1	I/O	Frequency select latch input pin / Fixed 48MHz clock output. 3.3V
27	AVDD48	PWR	Power for 24/48MHz outputs and fixed PLL core, nominal 3.3V
28	PD#	IN	Asynchronous active low input pin used to power down the device into a low power state. The internal clocks are disabled and the VCO and the crystal are stopped. The latency of the power down will not be greater than 1.8ms.

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ This output has 2X drive

Pin Description (Continued)

PIN #	PIN NAME	PIN TYPE	DESCRIPTION
29	VDD3V66	PWR	Power pin for the 3V66 clocks.
30	3V66_0	OUT	3.3V 66.66MHz clock output
31	3V66_1	OUT	3.3V 66.66MHz clock output
32	GND3V66	PWR	Ground pin for the AGP outputs
33	GND3V66	PWR	Ground pin for the AGP outputs
34	3V66_2	OUT	3.3V 66.66MHz clock output
35	3V66_3	OUT	3.3V 66.66MHz clock output
36	VDD3V66	PWR	Power pin for the 3V66 clocks.
37	GND	PWR	Ground pin.
38	AVDD	PWR	3.3V Analog Power pin for Core PLL
39	IREF	OUT	This pin establishes the reference current for the CPUCLK pairs. This pin requires a fixed precision resistor tied to ground in order to establish the appropriate current.
40	GNDCPU	PWR	Ground pin for the CPU outputs
41	CPUCLKC0	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
42	CPUCLKT0	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
43	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
44	CPUCLKC1	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
45	CPUCLKT1	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
46	GNDCPU	PWR	Ground pin for the CPU outputs
47	CPUCLKC2	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
48	CPUCLKT2	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
49	VDDCPU	PWR	Supply for CPU clocks, 3.3V nominal
50	CPUCLKC3	OUT	"Complementary" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
51	CPUCLKT3	OUT	"True" clocks of differential pair CPU outputs. These are current mode outputs. External resistors are required for voltage bias.
52	SCLK	IN	Clock pin of I2C circuitry 5V tolerant
53	GNDMREF	PWR	Ground pin for the 3VMREF outputs.
54	3VMREF_B	OUT	3V reference output to memory clock driver (180 degree out of phase with 3VMREF)
55	3VMREF	OUT	3V reference output to memory clock driver
56	VDDMREF	PWR	Power supply for 3VMREF clocks, nominal 3.3V

* Internal Pull-Up Resistor ** Internal Pull-Down Resistor ~ This output has 2X drive

Maximum Allowed Current

Pin Description Condition	Max 3.3V supply consumption Max discrete cap loads, Vdd = 3.465V All static inputs = Vdd or GND
Powerdown Mode (PWRDWN# = 0)	40mA
Full Active	360mA

CPUCLK Swing Select Functions

MULTSEL0	BYTE 1 BIT 3	Board Target Trace/Term Z	Reference R, Iref= Vdd/(3*Rr)	Output Current	Voh @ Z, Iref=2.32mA
0	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.56V @ 60
0	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 4*Iref	0.47V @ 50
0	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.85V /2 60
0	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 6*Iref	0.71V @ 50
1	0	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.71V @ 60
1	0	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 5*Iref	0.59V @ 50
1	1	60 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.99V @ 60
1	1	50 ohms	Rr = 475 1% Iref = 2.32mA	Ioh = 7*Iref	0.82V @ 50
0	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.75V @ 30
0	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 5*Iref	0.62V @ 20
0	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.90V @ 30
0	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 6*Iref	0.75V @ 20
1	0	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.60 @ 20
1	0	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 4*Iref	0.5V @ 20
1	1	30 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	1.05V @ 30
1	1	25 (DC equiv)	Rr = 221 1% Iref = 5mA	Ioh = 7*Iref	0.84V @ 20

General I^2C serial interface information

How to Write:

- Controller (host) sends a start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) sends the data byte count = X
- ICS clock will ***acknowledge***
- Controller (host) starts sending ***Byte N through Byte N + X -1***
  (see Note 2)
- ICS clock will ***acknowledge*** each byte ***one at a time***
- Controller (host) sends a Stop bit

How to Read:

- Controller (host) will send start bit.
- Controller (host) sends the write address $D2_{(H)}$
- ICS clock will ***acknowledge***
- Controller (host) sends the begining byte location = N
- ICS clock will ***acknowledge***
- Controller (host) will send a separate start bit.
- Controller (host) sends the read address $D3_{(H)}$
- ICS clock will ***acknowledge***
- ICS clock will send the data byte count = X
- ICS clock sends ***Byte N + X -1***
- ICS clock sends ***Byte 0 through byte X (if $X_{(H)}$ was written to byte 8)***.
- Controller (host) will need to acknowledge each byte
- Controllor (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Write Operation

Controller (Host)			ICS (Slave/Receiver)
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
	O		
	O		O
	O		O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

Index Block Read Operation

Controller (Host)		ICS (Slave/Receiver)	
T	starT bit		
Slave Address $D2_{(H)}$			
WR	WRite		
		ACK	
Beginning Byte = N			
		ACK	
RT	Repeat starT		
Slave Address $D3_{(H)}$			
RD	ReaD		
		ACK	
		Data Byte Count = X	
ACK			
		X Byte	Beginning Byte N
ACK			
			O
	O		O
	O		O
	O		
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

*See notes on the following page.

Table1: QuadRom Frequency Selection Table

Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	CPU	MREF	AGP	PCI
X	X	Sel133/100	FS3	FS2	FS1	FS0	MHz	MHz	MHz	MHz
0	0	0	0	0	0	0	90.00	45.00	30.00	60.00
0	0	0	0	0	0	1	100.00	50.00	33.33	66.67
0	0	0	0	0	1	0	100.90	50.45	33.63	67.27
0	0	0	0	0	1	1	103.00	51.50	34.33	68.67
0	0	0	0	1	0	0	105.00	52.50	35.00	70.00
0	0	0	0	1	0	1	108.00	54.00	36.00	72.00
0	0	0	0	1	1	0	110.00	55.00	36.67	73.33
0	0	0	0	1	1	1	112.00	56.00	37.33	74.67
0	0	0	1	0	0	0	115.00	57.50	38.33	76.67
0	0	0	1	0	0	1	118.00	59.00	39.33	78.67
0	0	0	1	0	1	0	120.00	60.00	40.00	80.00
0	0	0	1	0	1	1	122.00	61.00	40.67	81.33
0	0	0	1	1	0	0	125.00	62.50	41.67	83.33
0	0	0	1	1	0	1	127.00	63.50	42.33	84.67
0	0	0	1	1	1	0	130.00	65.00	43.33	86.67
0	0	0	1	1	1	1	133.60	66.80	44.53	89.07
0	0	1	0	0	0	0	120.00	60.00	30.00	60.00
0	0	1	0	0	0	1	133.33	66.67	33.33	66.67
0	0	1	0	0	1	0	133.90	66.95	33.48	66.95
0	0	1	0	0	1	1	136.00	68.00	34.00	68.00
0	0	1	0	1	0	0	138.00	69.00	34.50	69.00
0	0	1	0	1	0	1	140.00	70.00	35.00	70.00
0	0	1	0	1	1	0	142.00	71.00	35.50	71.00
0	0	1	0	1	1	1	144.00	72.00	36.00	72.00
0	0	1	1	0	0	0	145.00	72.50	36.25	72.50
0	0	1	1	0	0	1	148.00	74.00	37.00	74.00
0	0	1	1	0	1	0	150.00	75.00	37.50	75.00
0	0	1	1	0	1	1	152.00	76.00	38.00	76.00
0	0	1	1	1	0	0	154.00	77.00	38.50	77.00
0	0	1	1	1	0	1	156.00	78.00	39.00	78.00
0	0	1	1	1	1	0	158.00	79.00	39.50	79.00
0	0	1	1	1	1	1	160.00	80.00	40.00	80.00

Notes:

Table1 continues on the next three pages.

QuadRom™ Frequency Selection Table

Description										
Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VCO MHZ	CPUCLK MHz	3V66 MHz	PCICLK MHz
		Sel133/100	FS3	FS2	FS1	FS0				
0	1	0	0	0	0	0	456.00	114.00	76.00	38.00
0	1	0	0	0	0	1	460.00	115.00	76.67	38.33
0	1	0	0	0	1	0	464.00	116.00	77.33	38.67
0	1	0	0	0	1	1	468.00	117.00	78.00	39.00
0	1	0	0	1	0	0	472.00	118.00	78.67	39.33
0	1	0	0	1	0	1	476.00	119.00	79.33	39.67
0	1	0	0	1	1	0	480.00	120.00	80.00	40.00
0	1	0	0	1	1	1	484.00	121.00	80.67	40.33
0	1	0	1	0	0	0	488.00	122.00	81.33	40.67
0	1	0	1	0	0	1	492.00	123.00	82.00	41.00
0	1	0	1	0	1	0	500.00	125.00	83.33	41.67
0	1	0	1	0	1	1	508.00	127.00	84.67	42.33
0	1	0	1	1	0	0	516.00	129.00	86.00	43.00
0	1	0	1	1	0	1	524.00	131.00	87.33	43.67
0	1	0	1	1	1	0	532.00	133.00	88.67	44.33
0	1	0	1	1	1	1	540.00	135.00	90.00	45.00
0	1	1	0	0	0	0	456.00	152.00	76.00	38.00
0	1	1	0	0	0	1	459.00	153.00	76.50	38.25
0	1	1	0	0	1	0	462.00	154.00	77.00	38.50
0	1	1	0	0	1	1	465.00	155.00	77.50	38.75
0	1	1	0	1	0	0	468.00	156.00	78.00	39.00
0	1	1	0	1	0	1	471.00	157.00	78.50	39.25
0	1	1	0	1	1	0	474.00	158.00	79.00	39.50
0	1	1	0	1	1	1	477.00	159.00	79.50	39.75
0	1	1	1	0	0	0	480.00	160.00	80.00	40.00
0	1	1	1	0	0	1	483.00	161.00	80.50	40.25
0	1	1	1	0	1	0	486.00	162.00	81.00	40.50
0	1	1	1	0	1	1	489.00	163.00	81.50	40.75
0	1	1	1	1	0	0	492.00	164.00	82.00	41.00
0	1	1	1	1	0	1	495.00	165.00	82.50	41.25
0	1	1	1	1	1	0	498.00	166.00	83.00	41.50
0	1	1	1	1	1	1	501.00	167.00	83.50	41.75

Notes:

Continuation of Table1 from previous page.

QuadRom™ Frequency Selection Table

Description										
Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VCO MHZ	CPUCLK MHz	3V66 MHz	PCICLK MHz
		Sel133/100	FS3	FS2	FS1	FS0				
1	0	0	0	0	0	0	400.02	66.67	66.67	33.34
1	0	0	0	0	0	1	408.00	68.00	68.00	34.00
1	0	0	0	0	1	0	420.00	70.00	70.00	35.00
1	0	0	0	0	1	1	432.00	72.00	72.00	36.00
1	0	0	0	1	0	0	444.00	74.00	74.00	37.00
1	0	0	0	1	0	1	456.00	76.00	76.00	38.00
1	0	0	0	1	1	0	468.00	78.00	78.00	39.00
1	0	0	0	1	1	1	480.00	80.00	80.00	40.00
1	0	0	1	0	0	0	492.00	82.00	82.00	41.00
1	0	0	1	0	0	1	504.00	84.00	84.00	42.00
1	0	0	1	0	1	0	516.00	86.00	86.00	43.00
1	0	0	1	0	1	1	528.00	88.00	88.00	44.00
1	0	0	1	1	0	0	540.00	90.00	90.00	45.00
1	0	0	1	1	0	1	552.00	92.00	92.00	46.00
1	0	0	1	1	1	0	564.00	94.00	94.00	47.00
1	0	0	1	1	1	1	576.00	96.00	96.00	48.00
1	0	1	0	0	0	0	588.00	98.00	98.00	49.00
1	0	1	0	0	0	1	600.00	100.00	100.00	50.00
1	0	1	0	0	1	0	612.00	102.00	102.00	51.00
1	0	1	0	0	1	1	624.00	104.00	104.00	52.00
1	0	1	0	1	0	0	636.00	106.00	106.00	53.00
1	0	1	0	1	0	1	648.00	108.00	108.00	54.00
1	0	1	0	1	1	0	660.00	110.00	110.00	55.00
1	0	1	0	1	1	1	672.00	112.00	112.00	56.00
1	0	1	1	0	0	0	666.68	166.67	66.67	33.33
1	0	1	1	0	0	1	668.00	167.00	66.80	33.40
1	0	1	1	0	1	0	672.00	168.00	67.20	33.60
1	0	1	1	0	1	1	676.00	169.00	67.60	33.80
1	0	1	1	1	0	0	680.00	170.00	68.00	34.00
1	0	1	1	1	0	1	684.00	171.00	68.40	34.20
1	0	1	1	1	1	0	688.00	172.00	68.80	34.40
1	0	1	1	1	1	1	692.00	173.00	69.20	34.60

Notes:

Continuation of Table1 from previous page.

QuadRom™ Frequency Selection Table

Description										
Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	VCO MHZ	CPUCLK MHz	3V66 MHz	PCICLK MHz
		Sel133/100	FS3	FS2	FS1	FS0				
1	1	0	0	0	0	0	696.00	174.00	69.60	34.80
1	1	0	0	0	0	1	700.00	175.00	70.00	35.00
1	1	0	0	0	1	0	704.00	176.00	70.40	35.20
1	1	0	0	0	1	1	708.00	177.00	70.80	35.40
1	1	0	0	1	0	0	712.00	178.00	71.20	35.60
1	1	0	0	1	0	1	716.00	179.00	71.60	35.80
1	1	0	0	1	1	0	720.00	180.00	72.00	36.00
1	1	0	0	1	1	1	724.00	181.00	72.40	36.20
1	1	0	1	0	0	0	320.00	160.00	53.33	26.67
1	1	0	1	0	0	1	330.00	165.00	55.00	27.50
1	1	0	1	0	1	0	340.00	170.00	56.67	28.33
1	1	0	1	0	1	1	350.00	175.00	58.33	29.17
1	1	0	1	1	0	0	360.00	180.00	60.00	30.00
1	1	0	1	1	0	1	370.00	185.00	61.67	30.83
1	1	0	1	1	1	0	380.00	190.00	63.33	31.67
1	1	0	1	1	1	1	390.00	195.00	65.00	32.50
1	1	1	0	0	0	0	400.00	200.00	66.67	33.33
1	1	1	0	0	0	1	402.00	201.00	67.00	33.50
1	1	1	0	0	1	0	404.00	202.00	67.33	33.67
1	1	1	0	0	1	1	406.00	203.00	67.67	33.83
1	1	1	0	1	0	0	408.00	204.00	68.00	34.00
1	1	1	0	1	0	1	412.00	206.00	68.67	34.33
1	1	1	0	1	1	0	416.00	208.00	69.33	34.67
1	1	1	0	1	1	1	420.00	210.00	70.00	35.00
1	1	1	1	0	0	0	424.00	212.00	70.67	35.33
1	1	1	1	0	0	1	428.00	214.00	71.33	35.67
1	1	1	1	0	1	0	432.00	216.00	72.00	36.00
1	1	1	1	0	1	1	436.00	218.00	72.67	36.33
1	1	1	1	1	0	0	440.00	220.00	73.33	36.67
1	1	1	1	1	0	1	444.00	222.00	74.00	37.00
1	1	1	1	1	1	0	448.00	224.00	74.67	37.33
1	1	1	1	1	1	1	452.00	226.00	75.33	37.67

Notes:

Continuation of Table1 from previous page.

I²C Table: Frequency Select Register

Byte 0	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	FS Source	Frequency H/W IIC Select	RW	Latch Inputs	IIC	0
Bit 6	-	FS6	Freq Select Bit 6	RW	See Table 1: Quad Rom™ Frequency Selection Table		0
Bit 5	-	FS5	Freq Select Bit 5	RW			0
Bit 4	-	FS4	Freq Select Bit 4	RW			0
Bit 3	-	FS3	Freq Select Bit 3	RW			0
Bit 2	-	FS2	Freq Select Bit 2	RW			0
Bit 1	-	FS1	Freq Select Bit 1	RW			0
Bit 0	-	FS0	Freq Selcet Bit 0	RW			1

I²C Table: Spreading, Device Behavior and Output Control Register

Byte 1	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SS1	Spread Select 1	RW	See Table 2: Spread Spectrum Table		0
Bit 6	-	SS0	Spread Select 0	RW			0
Bit 5	-	SSEN	Spread Enable Control	RW	Disable	Enable	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	51/50	CPUT/C3	Output Control	RW	Disable	Enable	1
Bit 2	48/47	CPUT/C2	Output Control	RW	Disable	Enable	1
Bit 1	45/44	CPUT/C1	Output Control	RW	Disable	Enable	1
Bit 0	42/41	CPUT/C0	Output Control	RW	Disable	Enable	1

Table2: Spread Spectrum Select

SS1 (Byte 1 bit 7)	SS0 (Byte 1 bit 6)	Spread %	Downspread %	Note
0	0	0.35%	0.32%	Default
0	1	0.50%	0.45%	Spread 2
1	0	0.70%	0.75%	Spread 3
1	1	1.00%	1.00%	Spread 4

I²C Table: Output Control Register

Byte 2	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	18	PCICLK7	Output Control	RW	Disable	Enable	1
Bit 6	17	PCICLK6	Output Control	RW	Disable	Enable	1
Bit 5	15	PCICLK5	Output Control	RW	Disable	Enable	1
Bit 4	14	PCICLK4	Output Control	RW	Disable	Enable	1
Bit 3	12	PCICLK3	Output Control	RW	Disable	Enable	1
Bit 2	11	PCICLK2	Output Control	RW	Disable	Enable	1
Bit 1	9	PCICLK1	Output Control	RW	Disable	Enable	1
Bit 0	8	PCICLK0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 3	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	26	48MHz_1	Output Control	RW	Disable	Enable	1
Bit 6	25	48MHz_0	Output Control	RW	Disable	Enable	1
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	55	3VMREF	Output Control	RW	Disable	Enable	1
Bit 2	54	3VMREF_B	Output Control	RW	Disable	Enable	1
Bit 1	21	PCICLK_9	Output Control	RW	Disable	Enable	1
Bit 0	20	PCICLK_8	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 4	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	3	REF1	Output Control	RW	Disable	Enable	1
Bit 6	2	REF0	Output Control	RW	Disable	Enable	1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	35	3V66_3	Output Control	RW	Disable	Enable	1
Bit 3	-	Reserved	Reserved	RW	-	-	1
Bit 2	34	3V66_2	Output Control	RW	Disable	Enable	1
Bit 1	31	3V66_1	Output Control	RW	Disable	Enable	1
Bit 0	30	3V66_0	Output Control	RW	Disable	Enable	1

I²C Table: Output Control Register

Byte 5	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	PLL2EN	FIX_2 PLL Control	RW	OFF	ON	1
Bit 5	-	AEN	3V66/PCI Freq Source Select	RW	CPU_PLL Sync	FIX_PLL Async	0
Bit 4	-	AFS4	Async Rom SEL_2	RW	See Table 3: Async 3V66/PCI Frequency Selection Table		0
Bit 3	-	AFS3	Async Rom SEL_1	RW			0
Bit 2	-	AFS2	Async Rom SEL_0	RW			0
Bit 1	-	AFS1	Async Divider SEL_1	RW			0
Bit 0	-	AFS0	Async Divider SEL_0	RW			1

Table 3: Async 3V66/PCI Frequency Selection Table

Byte 5 Bit4	Byte 5 Bit3	Byte 5 Bit2	Byte 5 Bit1	Byte 5 Bit0	3V66	PCI
0	0	0	0	0	66.00	33.00
0	0	0	0	1	74.25	37.13
0	0	0	1	0	84.86	42.43
0	0	0	1	1	99.00	49.50
0	0	1	0	0	64.00	32.00
0	0	1	0	1	72.00	36.00
0	0	1	1	0	82.29	41.15
0	0	1	1	1	96.00	48.00
0	1	0	0	0	59.26	29.63
0	1	0	0	1	66.67	33.34
0	1	0	1	0	76.19	38.10
0	1	0	1	1	88.89	44.45
0	1	1	0	0	67.22	33.61
0	1	1	0	1	75.63	37.82
0	1	1	1	0	86.43	43.22
0	1	1	1	1	100.83	50.42
1	1	0	0	0	70.00	35.00
1	1	0	0	1	78.75	39.38
1	1	0	1	0	90.00	45.00
1	1	0	1	1	105.00	52.50

I^2C Table: Read Back Register

Byte 6	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WDHRB	WD Hard Alarm Status Read back	R	-	-	X
Bit 6	-	MULTSEL0	MULTSEL0 Read back	R	-	-	X
Bit 5	-	MULTSEL1	MULTISEL1 Read back	R	-	-	X
Bit 4	-	SEL100/ 133#RB	SEL100/133 # Read back	R	-	-	X
Bit 3	-	FS3RB	FS3 Read back	R	-	-	X
Bit 2	-	FS2RB	FS2 Read back	R	-	-	X
Bit 1	-	FS1RB	FS1 Read back	R	-	-	X
Bit 0	-	FS0RB	FS0 Read back	R	-	-	X

I^2C Table: Vendor & Revision ID Register

Byte 7	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	RID3	REVISION ID	R	-	-	0
Bit 6	-	RID2		R	-	-	0
Bit 5	-	RID1		R	-	-	0
Bit 4	-	RID0		R	-	-	1
Bit 3	-	VID3	VENDOR ID	R	-	-	0
Bit 2	-	VID2		R	-	-	0
Bit 1	-	VID1		R	-	-	0
Bit 0	-	VID0		R	-	-	1

I²C Table: Byte Count Register

Byte 8	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	BC7	Writing to this register will configure how many bytes will be read back, default is $0F_H$ = 15 bytes.	RW	-	-	0
Bit 6	-	BC6		RW	-	-	0
Bit 5	-	BC5		RW	-	-	0
Bit 4	-	BC4		RW	-	-	0
Bit 3	-	BC3		RW	-	-	1
Bit 2	-	BC2		RW	-	-	1
Bit 1	-	BC1		RW	-	-	1
Bit 0	-	BC0		RW	-	-	1

I²C Table: Watchdog Timer Register

Byte 9	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	WD7	These bits represent X*290ms the watchdog timer will wait before it goes to alarm mode. Default is 10*290ms = 2.9 seconds.	RW	-	-	0
Bit 6	-	WD6		RW	-	-	0
Bit 5	-	WD5		RW	-	-	0
Bit 4	-	WD4		RW	-	-	0
Bit 3	-	WD3		RW	-	-	1
Bit 2	-	WD2		RW	-	-	0
Bit 1	-	WD1		RW	-	-	1
Bit 0	-	WD0		RW	-	-	0

I²C Table: VCO Control Select Bit & WD Timer Control Register

Byte 10	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	M/NEN	M/N Programming Enable	RW	Disable	Enable	0
Bit 6	-	WD Enable	WD Enable	RW	Disable	Enable	0
Bit 5	-	WD SF Mode	WD Safe Frequency Mode	RW	Latched Inputs	B10 Bit(4:0)	0
Bit 4	-	WDSF4	Writing to these bit will configure the safe frequency as Byte 0 Bit (4:0)	RW	-	-	0
Bit 3	-	WDSF3		RW	-	-	0
Bit 2	-	WDSF2		RW	-	-	0
Bit 1	-	WDSF1		RW	-	-	0
Bit 0	-	WDSF0		RW	-	-	0

I²C Table: VCO Frequency Control Register

Byte 11	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	NDiv8	N Divider Bit 8	RW	-	-	X
Bit 6	-	MDiv6	The decimal representation of M Div (6:0) + 2 is equal to reference divider value. Default at power up = latch-in or Byte 0	RW	-	-	X
Bit 5	-	MDiv5		RW	-	-	X
Bit 4	-	MDiv4		RW	-	-	X
Bit 3	-	MDiv3		RW	-	-	X
Bit 2	-	MDiv2		RW	-	-	X
Bit 1	-	MDiv1		RW	-	-	X
Bit 0	-	MDiv0		RW	-	-	X

I²C Table: VCO Frequency Control Register

Byte 12	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	NDiv7	The decimal representation of N Div (8:0) +8 is equal to VCO divider value. Default at power up = latch-in or Byte 0 Rom table.	RW	-	-	X
Bit 6	-	NDiv6		RW	-	-	X
Bit 5	-	NDiv5		RW	-	-	X
Bit 4	-	NDiv4		RW	-	-	X
Bit 3	-	NDiv3		RW	-	-	X
Bit 2	-	NDiv2		RW	-	-	X
Bit 1	-	NDiv1		RW	-	-	X
Bit 0	-	NDiv0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 13	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	SSP7	These Spread Spectrum bits will program the spread pecentage. It is recommended to use ICS Spread % table for spread programming.	RW	-	-	X
Bit 6	-	SSP6		RW	-	-	X
Bit 5	-	SSP5		RW	-	-	X
Bit 4	-	SSP4		RW	-	-	X
Bit 3	-	SSP3		RW	-	-	X
Bit 2	-	SSP2		RW	-	-	X
Bit 1	-	SSP1		RW	-	-	X
Bit 0	-	SSP0		RW	-	-	X

I²C Table: Spread Spectrum Control Register

Byte 14	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	R	-	-	0
Bit 6	-	Reserved	Reserved	R	-	-	0
Bit 5	-	SSP13	It is recommended to use ICS Spread % table for spread programming.	R	-	-	X
Bit 4	-	SSP12		RW	-	-	X
Bit 3	-	SSP11		RW	-	-	X
Bit 2	-	SSP10		RW	-	-	X
Bit 1	-	SSP9		RW	-	-	X
Bit 0	-	SSP8		RW	-	-	X

I²C Table: Output Divider Control Register

Byte 15	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	X
Bit 6	-	Reserved	Reserved	RW	-	-	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	Reserved	Reserved	RW	-	-	X
Bit 3	-	CPUDiv3	CPU divider ratio can be configured via these 4 bits individually.	RW	See Table 4: Divider Ratio Combination Table		X
Bit 2	-	CPUDiv2		RW			X
Bit 1	-	CPUDiv1		RW			X
Bit 0	-	CPUDiv0		RW			X

Table 4: Divider Ratio Combination Table (CPU & MREF)

	Divider (3:2)								
Divider (1:0)	Bit	00		01		10		11	MSB
			1		2		4		8
	00	0000	2	0100	4	1000	8	1100	16
	01	0001	3	0101	6	1001	12	1101	24
	10	0010	5	0110	10	1010	20	1110	40
	11	0011	7	0111	14	1011	28	1111	56
	LSB	Address	Div	Address	Div	Address	Div	Address	Div

I²C Table: Output Divider Control Register

Byte 16	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIDiv3	PCI divider ratio can be configured via these 4 bits individually.	RW	See Table 4: Divider Ratio Combination Table		X
Bit 6	-	PCIBit 2		RW			X
Bit 5	-	PCIDiv4		RW			X
Bit 4	-	PCIBit 3		RW			X
Bit 3	-	3V66Div3	3V66 divider ratio can be configured via these 4 bits individually.	RW	See Table 4: Divider Ratio Combination Table		X
Bit 2	-	3V66Div2		RW			X
Bit 1	-	3V66Div1		RW			X
Bit 0	-	3V66Div0		RW			X

I²C Table: Output Divider Control Register

Byte 17	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCIINV 3V66	PCI 3V66 Phase Invert	RW	Default	Inverse	X
Bit 6	-	3V66INV	3V66 Phase Invert	RW	Default	Inverse	X
Bit 5	-	Reserved	Reserved	RW	-	-	X
Bit 4	-	CPUINV	CPU Phase Invert	RW	Default	Inverse	X
Bit 3	-	Reserved	Reserved	RW	-	-	X
Bit 2	-	Reserved	Reserved	RW	-	-	X
Bit 1	-	Reserved	Reserved	RW	-	-	X
Bit 0	-	Reserved	Reserved	RW	-	-	X

I²C Table: Group Skew Control Register

Byte 18	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	CPUSkw1	CPUC/T(2:1) to CPU C/T(3,0) Skew	RW	See Table 5: 2-bit Skew Control Table		1
Bit 6	-	CPUSkw0		RW			1
Bit 5	-	Reserved	Reserved	RW	-	-	1
Bit 4	-	Reserved	Reserved	RW	-	-	1
Bit 3	-	CPUSkw1	CPUC/T(3,0) to CPU C/T(2:1) Skew	RW	See Table 5: 2-bit Skew Control Table		1
Bit 2	-	CPUSkw0		RW			1
Bit 1	-	Reserved	Reserved	RW	-	-	1
Bit 0	-	Reserved	Reserved	RW	-	-	1

Table 5: 2 Bits Skew Programming Table

4 Step	0	1	LSB
0	0ps	250ps	-
1	500ps	750ps	-
MSB	-	-	-

I²C Table: Group Skew Control Register

Byte 19	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	MREFSkw3	CPUC/T to MREF/MREF_B Skew Cntrol	RW	See Table 6: 7-Steps Skew Control Table		0
Bit 6	-	MREFSkw2		RW			1
Bit 5	-	MREFSkw1		RW			0
Bit 4	-	MREFSkw0		RW			0
Bit 3	-	Reserved	Reserved	RW	-	-	0
Bit 2	-	Reserved	Reserved	RW	-	-	1
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Group Skew Control Register

Byte 20	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	PCISkw3	CPU to PCI(9:6) Skew Control	RW	See Table 6: 7-Steps Skew Control Table		0
Bit 6	-	PCISkw2		RW			1
Bit 5	-	PCISkw1		RW			1
Bit 4	-	PCISkw0		RW			0
Bit 3	-	PCISkw3	CPU to PCI(5:0) Skew Control	RW	See Table 6: 7-Steps Skew Control Table		0
Bit 2	-	PCISkw2		RW			1
Bit 1	-	PCISkw1		RW			1
Bit 0	-	PCISkw0		RW			0

Table 6: 7-Steps Skew Programming Table

7 Step	11	10	01	00	LSB
11	900 ps	750 ps	600 ps	450 ps	
10	N/A	N/A	N/A	300 ps	
01	N/A	N/A	N/A	150 ps	
00	N/A	N/A	N/A	0.0 ps	
MSB					

I²C Table: Group Skew Control Register

Byte 21	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	3V66Skw1	CPU to 3V66(3:2)	RW	See Table 5: 2-bit		0
Bit 6	-	3V66Skw0	Skew Control	RW	Skew Control Table		0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	3V66Skw1	CPU to 3V66(1:0)	RW	See Table 5: 2-bit		0
Bit 2	-	3V66Skw0	Skew Control	RW	Skew Control Table		0
Bit 1	-	Reserved	Reserved	RW	-	-	0
Bit 0	-	Reserved	Reserved	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 22	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	48MHzSlw1	48MHz_0 Slew	RW	-	-	1
Bit 6	-	48MHzSlw0	Rate Control	RW	-	-	0
Bit 5	-	48MHzSlw1	48MHz_1 Slew	RW	-	-	1
Bit 4	-	48MHzSlw0	Rate Control	RW	-	-	0
Bit 3	-	3V66Slw1	3V66 (0) Slew Rate	RW	-	-	1
Bit 2	-	3V66Slw0	Control	RW	-	-	0
Bit 1	-	3V66Slw1	3V66 (3:1) Slew	RW	-	-	1
Bit 0	-	3V66Slw0	Rate Control	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 23	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	1
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	PCISlw1	PCI (9:7), (5:2)	RW	-	-	1
Bit 4	-	PCISlw0	Slew Rate Control	RW	-	-	0
Bit 3	-	PCISlw1	PCI (6) Slew Rate	RW	-	-	1
Bit 2	-	PCISlw0	Control	RW	-	-	0
Bit 1	-	PCISlw1	PCI (1:0) Slew Rate	RW	-	-	1
Bit 0	-	PCISlw0	Control	RW	-	-	0

I²C Table: Slew Rate Control Register

Byte 24	Pin #	Name	Control Function	Type	0	1	PWD
Bit 7	-	Reserved	Reserved	RW	-	-	0
Bit 6	-	Reserved	Reserved	RW	-	-	0
Bit 5	-	Reserved	Reserved	RW	-	-	0
Bit 4	-	Reserved	Reserved	RW	-	-	0
Bit 3	-	REFSlw1	REF1 Slew Rate	RW	-	-	1
Bit 2	-	REFSlw0	Control	RW	-	-	0
Bit 1	-	REFSlw1	REF0 Slew Rate	RW	-	-	1
Bit 0	-	REFSlw0	Control	RW	-	-	0

Absolute Maximum Ratings

Supply Voltage . . . . . 5.5 V

Logic Inputs . . . . . GND –0.5 V to V_{DD} +0.5 V

Ambient Operating Temperature . . . . . 0°C to +70°C

Case Temperature . . . . . 115°C

Storage Temperature . . . . . –65°C to +150°C

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Electrical Characteristics - Input/Supply/Common Output Parameters

T_A = 0 - 70°C; Supply Voltage V_{DD} = 3.3 V +/-5%

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input High Voltage	V_{IH}		2		V_{DD} + 0.3	V
Input Low Voltage	V_{IL}		V_{SS} - 0.3		0.8	V
Input High Current	I_{IH}	V_{IN} = V_{DD}; Inputs with no pull-down resistors	-200		200	µA
	I_{IH}	V_{IN} = V_{DD}; Inputs with pull-down resistors			5	mA
Input Low Current	I_{IL1}	V_{IN} = 0 V; Inputs with no pull-up resistors	-200		200	µA
	I_{IL2}	V_{IN} = 0 V; Inputs with pull-up resistors	-5			mA
Operating Supply Current	$I_{DD3.3OP}$	C_L = Full load; Select @ 100 MHz	229	230	360	mA
	$I_{DD3.3OP}$	C_L =Full load; Select @ 133 MHz	220	233	360	mA
Powerdown Current	$I_{DD3.3PD}$	IREF=5 mA		35	45	mA
Input Frequency	F_i	V_{DD} = 3.3 V		14.318		MHz
Pin Inductance	L_{pin}					nH
Input Capacitance[1]	C_{IN}	Logic Inputs			5	pF
	C_{OUT}	Output pin capacitance			6	pF
	C_{INX}	X1 & X2 pins	27	36	45	pF
Clk Stabilization[1,2]	T_{STAB}	From PowerUp or deassertion of PowerDown to 1st clock.		1	3	ms
Delay[1]	t_{PZH},t_{PZL}	Output enable delay (all outputs)	1		10	ns
	t_{PHZ},t_{PLZ}	Output disable delay (all outputs)	1		10	ns

[1]Guaranteed by design, not 100% tested in production.

[2]See timing diagrams for buffered and un-buffered timing requirements.

Electrical Characteristics - CPU (0.7V Select)

T_A = 0 - 70°C; VDD=3.3V Rs=33Ω , Rp(pulldown) = 50Ω (unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Voltage High	VHigh	Statistical measurement on single ended signal using oscilloscope math function.	660	788	850	mV
Voltage Low	VLow		-150	16	150	
Max Voltage	Vovs	Measurement on single ended signal using absolute value.		818	1150	mV
Min Voltage	Vuds		-450	11		
Rise Time	t_r	V_{OL} = 0.175V, V_{OH} = 0.525V	175	306	700	ps
Fall Time	t_f	V_{OH} = 0.525V V_{OL} = 0.175V	175	330	700	ps
Duty Cycle	d_{t3}	Measurement from differential wavefrom	45	50.2	55	%
Skew	t_{sk3}	V_T = 50%		120	150	ps
Jitter, Cycle to cycle	$t_{jcyc-cyc}$ [1]	V_T = 50%		49	150	ps

[1]Guaranteed by design, not 100% tested in production.

[2] I_{OWT} can be varied and is selectable thru the MULTSEL pin.

Electrical Characteristics - MREF/MREF_B

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}					MHz
Output Impedance	R_{DSP1} [1]	$V_O = V_{DD}$*(0.5)	12		65	Ω
Output High Voltage	V_{OH} [1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL} [1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH} [1]	$V_{OH@MIN}$ = 1.0 V, Voh@MAX=3.135	-33		-33	mA
Output Low Voltage		$V_{OH@MIN}$ = 1.95 V, Voh@MAX=0.4	30		38	mA
Rise Time	t_{r1} [1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.8	2	ns
Fall Time	t_{f1} [1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.7	2	ns
Duty Cycle	d_{t1} [1]	V_T = 1.5 V	45	54	55	%
Jitter	$t_{jcyc-cyc}$ [1]	V_T = 1.5 V 3V66		138	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 3V66

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-30 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			66.66		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	12		65	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V, Voh@MAX=3.135	-33		-33	mA
Output Low Voltage		$V_{OH@MIN}$ = 1.95 V, Voh@MAX=0.4	30		38	mA
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	0.5	1.8	2	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	0.5	1.51	2	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	50	55	%
Skew	t_{sk1}[1]	V_T = 1.5 V		52	250	ps
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V 3V66		160	250	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - 48MHz

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.32		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-29		-23	
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	29		27	
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.15	4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	1.4	4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	52.5	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		184	350	ps

[1]Guaranteed by design, not 100% tested in production.

Electrical Characteristics - REF

T_A = 0 - 70°C; VDD=3.3V +/-5%; C_L = 10-20 pF (unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output Frequency	F_{O1}			14.32		MHz
Output Impedance	R_{DSP1}[1]	$V_O = V_{DD}*(0.5)$	20		60	Ω
Output High Voltage	V_{OH}[1]	I_{OH} = -1 mA	2.4			V
Output Low Voltage	V_{OL}[1]	I_{OL} = 1 mA			0.4	V
Output High Current	I_{OH}[1]	$V_{OH@MIN}$ = 1.0 V	-29		-23	
Output Low Current	I_{OL}[1]	$V_{OL@MIN}$ = 1.95 V	29		27	
Rise Time	t_{r1}[1]	V_{OL} = 0.4 V, V_{OH} = 2.4 V	1	1.1	4	ns
Fall Time	t_{f1}[1]	V_{OH} = 2.4 V, V_{OL} = 0.4 V	1	0.92	4	ns
Duty Cycle	d_{t1}[1]	V_T = 1.5 V	45	46.4	55	%
Jitter	$t_{jcyc-cyc}$[1]	V_T = 1.5 V		192	1000	ps

[1]Guaranteed by design, not 100% tested in production.

Shared Pin Operation - Input/Output Pins

The I/O pins designated by (input/output) serve as dual signal functions to the device. During initial power-up, they act as input pins. The logic level (voltage) that is present on these pins at this time is read and stored into a 5-bit internal data latch. At the end of Power-On reset, (see AC characteristics for timing values), the device changes the mode of operations for these pins to an output function. In this mode the pins produce the specified buffered clocks to external loads.

To program (load) the internal configuration register for these pins, a resistor is connected to either the VDD (logic 1) power supply or the GND (logic 0) voltage potential. A 10 Kilohm (10K) resistor is used to provide both the solid CMOS programming voltage needed during the power-up programming period and to provide an insignificant load on the output clock during the subsequent operating period.

Figure 1 shows a means of implementing this function when a switch or 2 pin header is used. With no jumper is installed the pin will be pulled high. With the jumper in place the pin will be pulled low. If programmability is not necessary, than only a single resistor is necessary. The programming resistors should be located close to the series termination resistor to minimize the current loop area. It is more important to locate the series termination resistor close to the driver than the programming resistor.

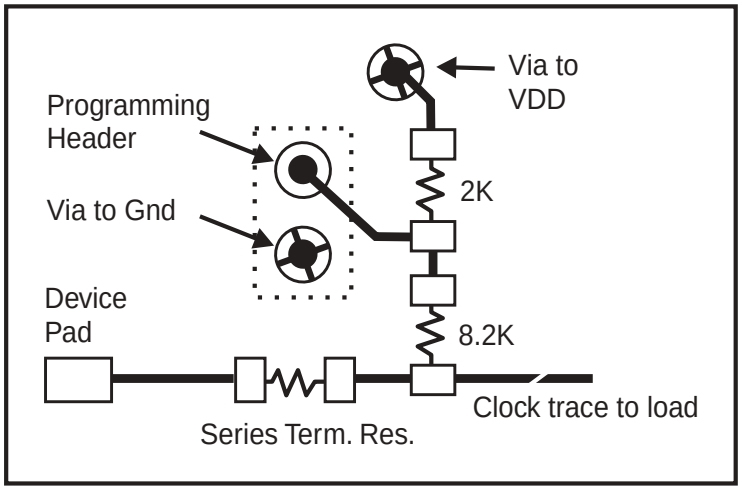
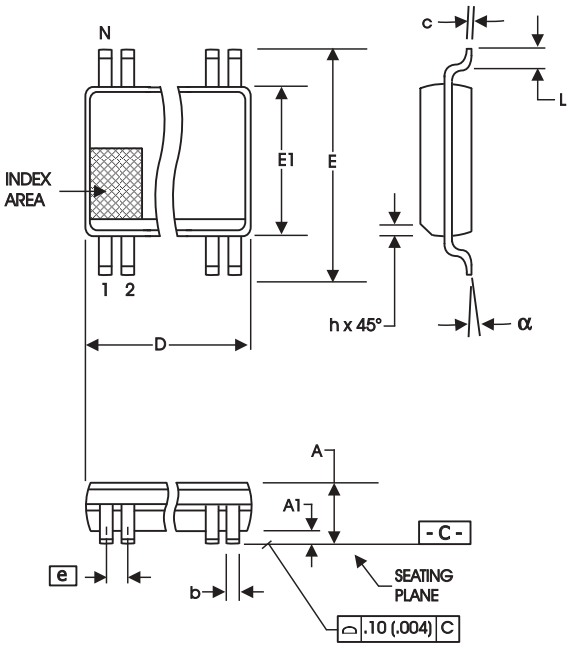


Fig. 1



300 mil SSOP Package

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	2.41	2.80	.095	.110
A1	0.20	0.40	.008	.016
b	0.20	0.34	.008	.0135
c	0.13	0.25	.005	.010
D	SEE VARIATIONS		SEE VARIATIONS	
E	10.03	10.68	.395	.420
E1	7.40	7.60	.291	.299
e	0.635 BASIC		0.025 BASIC	
h	0.38	0.64	.015	.025
L	0.50	1.02	.020	.040
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°

VARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	18.31	18.55	.720	.730

Reference Doc.: JEDEC Publication 95, MO-118

10-0034

Ordering Information

ICS950703yFT

Example:

ICS XXXXXX y F - T

- **Designation for tape and reel packaging**
- **Package Type**
  F = SSOP
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device