CMOS Low Cost 10-Bit Multiplying DAC

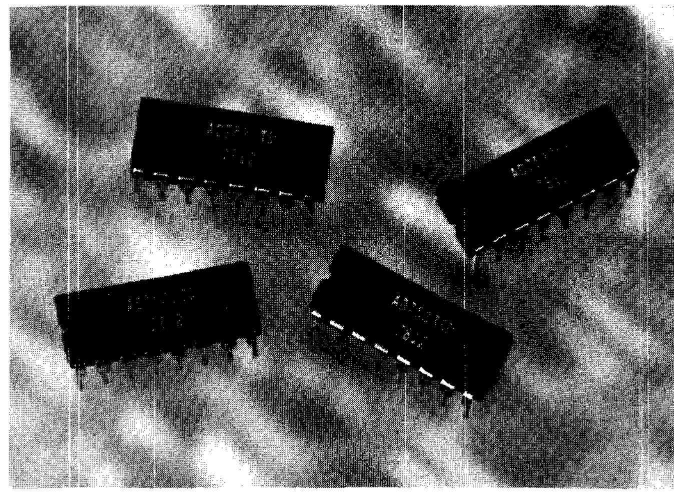
AD7533

ANALOG DEVICES

PRELIMINARY TECHNICAL DATA

FEATURES
- Lowest Cost 10-Bit DAC
- Direct AD7520 Equivalent
- Linearity: ½, 1 or 2LSB
- Low Power Dissipation
- Full Four-Quadrant Multiplying DAC
- CMOS/TTL Direct Interface

APPLICATIONS
- Digitally Controlled Attenuators
- Programmable Gain Amplifiers
- Function Generation
- Linear Automatic Gain Control



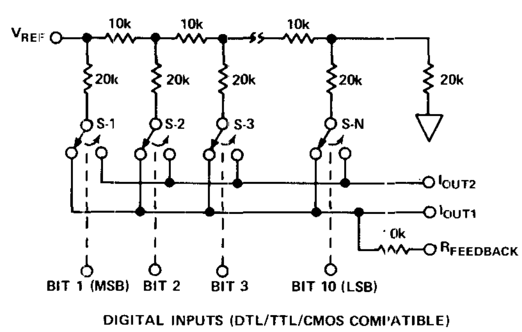
GENERAL DESCRIPTION

The AD7533 is a low cost 10-bit 4-quadrant multiplying DAC manufactured using an advanced thin-film-on-monolithic-CMOS wafer fabrication process.

Pin and function equivalent to the industry standard AD7520, the AD7533 is recommended as a lower cost alternative for old AD7520 sockets or new 10-bit DAC designs.

AD7533 application flexibility is demonstrated by its ability to interface to TTL or CMOS, operate on +5V to +15V power, and provide proper binary scaling for reference inputs of either positive or negative polarity.

FUNCTIONAL DIAGRAM

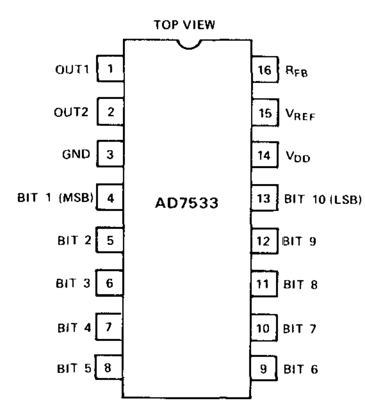


Logic: A switch is closed to $I_{OUT\ 1}$ for its digital input in a "HIGH" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range and Package		
	Commercial (Plastic) 0 to +70°C	Industrial (Ceramic) -25°C to +85°C	Military (Ceramic) -55°C to +125°C
±0.2%	AD7533JN	AD7533AD AD7533AD/883B	AD7533SD AD7533SD/883B
±0.1%	AD7533KN	AD7533BD AD7533BD/883B	AD7533TD AD7533TD/883B
±0.05%	AD7533LN	AD7533CD AD7533CD/883B	AD7533UD AD7533UD/883B

PIN CONFIGURATION



SPECIFICATIONS (V_{DD} = +15V; V_{OUT1} = V_{OUT2} = 0V; V_{REF} = +10V unless otherwise noted)

PARAMETER	T_A = 25°C	T_A = Operating Range[1]	Test Conditions
STATIC ACCURACY			
Resolution	10 Bits	10 Bits	
Nonlinearity[2]			
AD7533JN, AD, SD	±0.2% FSR max	±0.2% FSR max	
AD7533KN, BD, TD	±0.1% FSR max	±0.1% FSR max	
AD7533LN, CD, UD	±0.05% FSR max	±0.05% FSR max	
Gain Error[3]	±1.4% FS max	±1.5% FS max	Digital Inputs = V_{INH}
Supply Rejection[4]			
$\Delta Gain/\Delta V_{DD}$	0.005%/%	0.008%/%	Digital Inputs = V_{INH}; V_{DD} = +14V to +17V
Output Leakage Current			
I_{OUT1} (pin 1)	±50nA max	±200nA max	Digital Inputs = V_{INL}; V_{REF} = ±10V
I_{OUT2} (pin 2)	±50nA max	±200nA max	Digital Inputs = V_{INH}; V_{REF} = ±10V
DYNAMIC ACCURACY			
Output Current Settling Time	600ns max[5]	800ns[4]	To 0.05% FSR; R_{LOAD} = 100Ω; Digital Inputs = V_{INH} to V_{INL} or V_{INL} to V_{INH}
Feedthrough Error	±0.05% FSR max[4]	±0.1% FSR max[4]	Digital Inputs = V_{INL}; V_{REF} = ±10V, 100kHz sinewave.
REFERENCE INPUT			
Input Resistance (pin 15)	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max[6]	
ANALOG OUTPUTS			
Output Capacitance			
C_{OUT1} (pin 1)	100pF max[4]	100pF max[4]	Digital Inputs = V_{INH}
C_{OUT2} (pin 2)	35pF max[4]	35pF max[4]	Digital Inputs = V_{INH}
C_{OUT1} (pin 1)	35pF max[4]	35pF max[4]	Digital Inputs = V_{INL}
C_{OUT2} (pin 2)	100pF max[4]	100pF max[4]	Digital Inputs = V_{INL}
DIGITAL INPUTS			
Input High Voltage			
V_{INH}	2.4V min	2.4V min	
Input Low Voltage			
V_{INL}	0.8V max	0.8V max	
Input Leakage Current			
I_{IN}	±1μA max	±1μA max	V_{IN} = 0V and V_{DD}
Input Capacitance			
C_{IN}	5pF max[4]	5pF max[4]	
POWER REQUIREMENTS			
V_{DD}	+15V ±10%	+15V ±10%	Rated Accuracy
V_{DD} Range[4]	+5V to +16V	+5V to +16V	Functionality with degraded performance
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INL} or V_{INH}
I_{DD}	100μA max	150μA max	Digital Inputs = 0V or V_{DD}

NOTES:

[1] Plastic (JN, KN, LN versions): 0 to +70°C
Commercial Ceramic (AD, BD, CD versions): −25°C to +85°C
Military Ceramic (SD, TD, UD versions): −55°C to +125°C

[2] "FSR" is Full Scale Range.

[3] Full Scale (FS) = $-(V_{REF})\left(\frac{1023}{1024}\right)$

[4] Guaranteed, not tested.

[5] AC parameter, sample tested to ensure specification compliance.

[6] Absolute temperature coefficient is approximately −300ppm/°C.

[7] 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} at +25°C and +125°C (SD, TD, UD versions) or +25°C and +85°C (AD, BD, CD versions).

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

V_{DD} to GND . . . . -0.3V, +17V
R_{FB} to GND . . . . ±25V
V_{REF} to GND. . . . . ±25V
Digital Input Voltage Range . . . . -0.3V to V_{DD}
Output Voltage (pin 1, pin 2) . . . . -0.3V to V_{DD}
Power Dissipation (Package)
Plastic (Suffix N)
To +70°C. 670mW
Derates above +70°C by . . . . 8.3mW/°C
Ceramic (Suffix D)
To +75°C. 450mW
Derates above +75°C by . . . . 6mW/°C
Operating Temperature Range
Commercial (JN, KN, LN versions). . . . . 0 to +70°C
Industrial (AD, BD, CD versions) . . . . -25°C to +85°C
Military (SD, TD, UD versions) . . . . -55°C to +125°C
Storage Temperature . . . . -65°C to +150°C
Lead Temperature (Soldering, 10 seconds). . . . . +300°C

CAUTION:

1. ESD sensitive device. The digital control inputs are Zener protected; however, permanent damage may occur on unconnected devices subjected to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts.
2. Do not apply voltages lower than ground or higher the V_{DD} to any pin except V_{REF} (pin 15) and R_{FB} (pin 16).
3. The inputs of some IC amplifiers (especially wide bandwidth types) present a low impedance to V^- during power-up or power-down sequencing. To prevent the AD7533 OUT1 or OUT2 terminals from exceeding -300mV (which causes catastrophic substrate current) a Schottky diode (HP5082-2811 or equivalent) is recommended. The diode should be connected between OUT1 (OUT2) and ground as shown in Figures 5 and 6.

TERMINOLOGY

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The AD7533, a 10-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and ten CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown in Figure 1. An inverted R-2R ladder structure is used – that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines, thus maintaining a constant current in each ladder leg independent of the switch state.

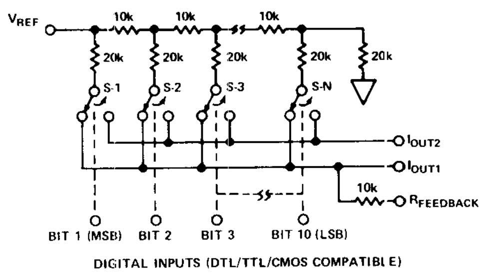


Figure 1. AD7533 Functional Diagram

One of the CMOS current switches is shown in Figure 2. The geometries of devices 1, 2 and 3 are optimized to make the digital control inputs DTL/TTL/CMOS compatible over the full military temperature range. The input stage drives two inverters (devices 4, 5, 6 and 7) which in turn drive the two output N-channels. The "ON" resistances of the switches are binarily sealed so the voltage drop across each switch is the same. For example, switch 1 of Figure 2 was designed for an "ON" resistance of 20 ohms, switch 2 or 40 ohms and so on. For a 10V reference input, the current through switch 1 is 0.5mA, the current through switch 2 is 0.25mA, and so on, thus maintaining a constant 10mV drop across each switch. It is essential that each switch voltage drop be equal if the binarily weighted current division property of the ladder is to be maintained.

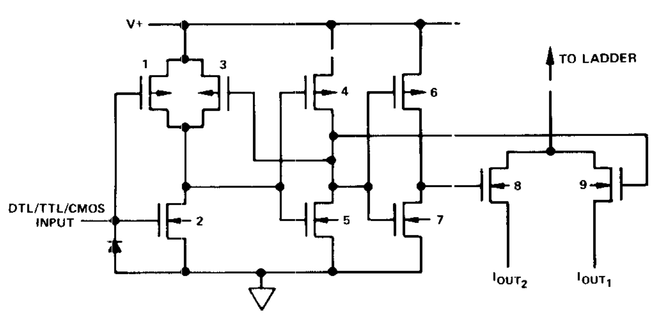


Figure 2. CMOS Switch

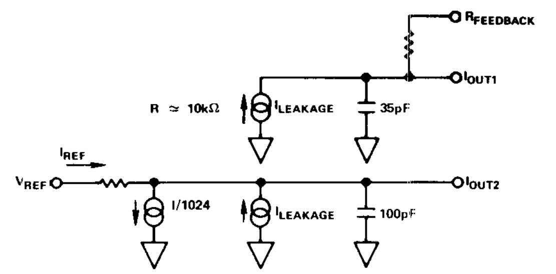


Figure 3. AD7533 Equivalent Circuit – All Digital Inputs Low

EQUIVALENT CIRCUIT ANALYSIS

The equivalent circuits for all digital inputs high and all digital inputs low are shown in Figures 3 and 4. In Figure 3 with all digital inputs low, the reference current is switched to I_{OUT2}. The current source $I_{LEAKAGE}$ is composed of surface and junction leakages to the substrate while the $\frac{I}{1024}$ current source represents a constant 1-bit current drain through the termination resistor on the R-2R ladder. The "ON" capacitance of the output N channel switch is 120pF, as shown on the I_{OUT2} terminal. The "OFF" switch capacitance is 30pF, as shown on the I_{OUT1} terminal. Analysis of the circuit for all digital inputs high, as shown in Figure 4, is similar to Figure 3; however, the "ON" switches are now on terminal I_{OUT1}, hence the 100pF at that terminal.

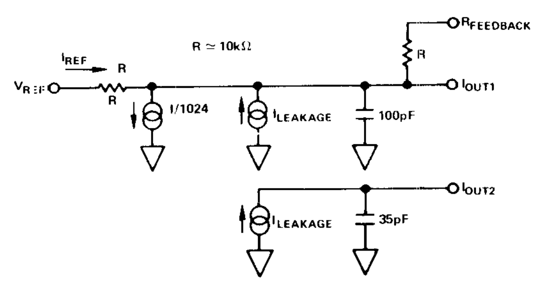
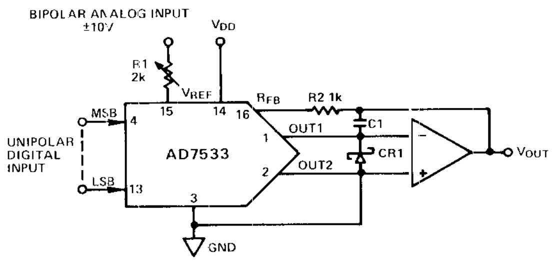


Figure 4. AD7533 Equivalent Circuit – All Digital Inputs High

OPERATION

UNIPOLAR BINARY OPERATION (2-QUADRANT MULTIPLICATION)



NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082–2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3.
3. C1 PHASE COMPENSATION (5 – 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIER.

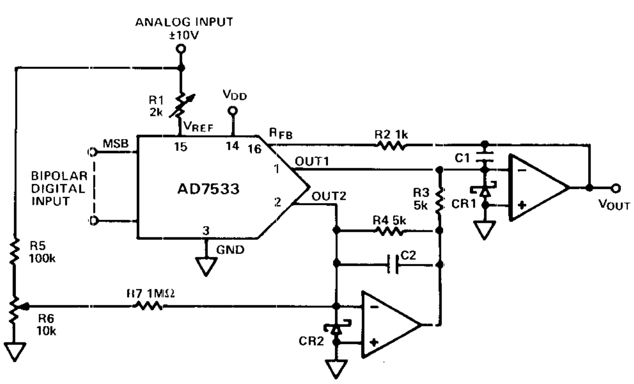
Figure 5. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 1)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:
1. Nominal Full Scale for the circuit of Figure 5 is given by FS = $-V_{REF}\left(\frac{1023}{1024}\right)$
2. Nominal LSB magnitude for the circuit of Figure 5 is given by LSB = $V_{REF}\left(\frac{1}{1024}\right)$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)



NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED
3. C1, C2 PHASE COMPENSATION (5 - 15pF) MAY BE REQUIRED WHEN USING HIGH SPEED AMPLIFIERS.
4. SCHOTTKY DIODES CR1 AND CR2 (HP5082–2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS. SEE "CAUTION" NOTE 3.

Figure 6. Bipolar Operation (4-Quadrant Multiplication)

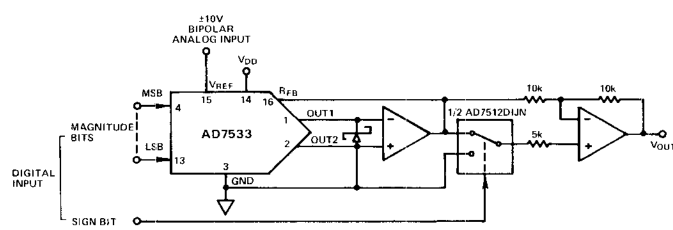
DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 2)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:
1. Nominal Full Scale Range for the circuit of Figure 6 is given by FSR = $V_{REF}\left(\frac{1023}{512}\right)$
2. Nominal LSB magnitude for the circuit of Figure 6 is given by LSB = $V_{REF}\left(\frac{1}{512}\right)$

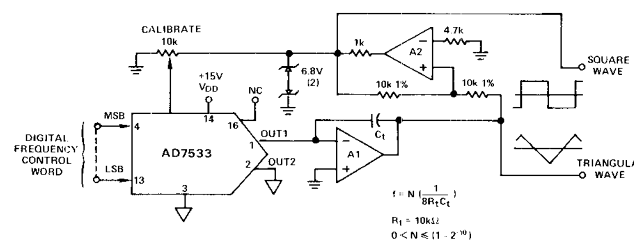
Table 2. Bipolar (Offset Binary) Code Table

APPLICATIONS

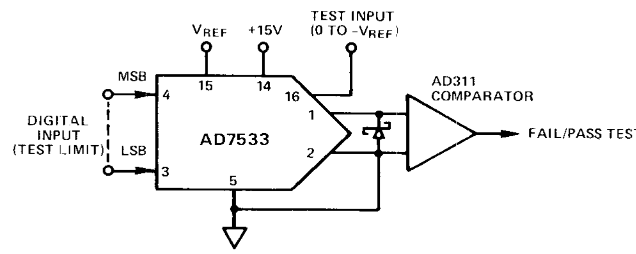
10-BIT AND SIGN MULTIPLYING DAC



PROGRAMMABLE FUNCTION GENERATOR

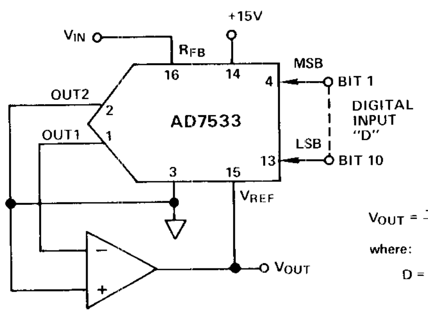


DIGITALLY PROGRAMMABLE LIMIT DETECTOR



APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)



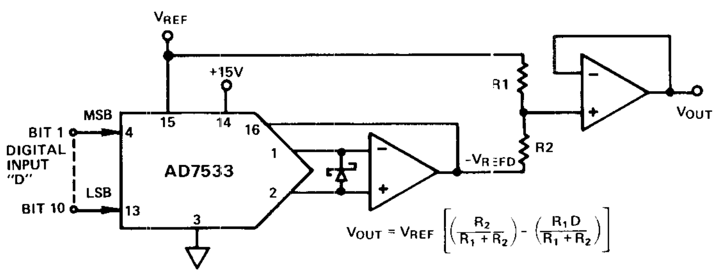
$$V_{OUT} = \frac{-V_{IN}}{D}$$

where:

$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$0 < D \leq \frac{1023}{1024}$$

MODIFIED SCALE FACTOR AND OFFSET



$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1 + R_2}\right) - \left(\frac{R_1 D}{R_1 + R_2}\right)\right]$$

where:

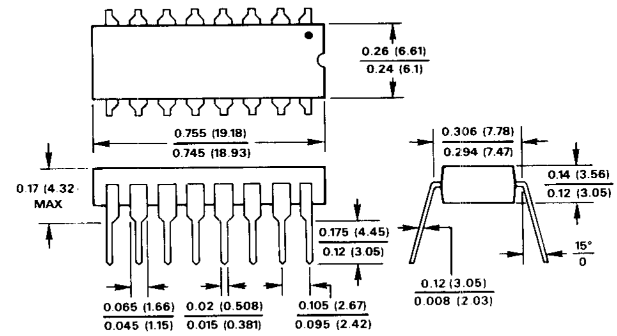
$$D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \ldots \frac{BIT\ 10}{2^{10}}$$

$$\left(0 \leq D \leq \frac{1023}{1024}\right)$$

OUTLINE DIMENSIONS

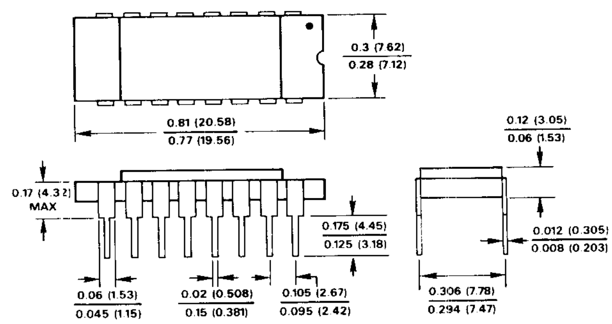
Dimensions shown in inches and (mm).

16 PIN PLASTIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE SOLDER PLATED KOVAR

16 PIN CERAMIC DIP



LEAD NO. 1 IDENTIFIED BY DOT OR NOTCH
LEADS ARE GOLD-PLATED (50 MICROINCHES MIN.) KOVAR

BONDING DIAGRAM

Dimensions shown in inches and (mm).