

## 384-OUTPUT TFT-LCD SOURCE DRIVER (COMPATIBLE WITH 64-GRAY SCALES)

### DESCRIPTION

The  $\mu$ PD16732D is a source driver for TFT-LCDs capable of dealing with displays with 64-gray scales. Data input is based on digital input configured as 6 bits by 6 dots (2 pixels), which can realize a full-color display of 260,000 colors by output of 64 values  $\gamma$ -corrected by an internal D/A converter and 5-by-2 external power modules. Because the output dynamic range is as large as  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V, level inversion operation of the LCD's common electrode is rendered unnecessary. Also, to be able to deal with dot-line inversion, n-line inversion and column line inversion when mounted on a single side, this source driver is equipped with a built-in 6-bit D/A converter circuit whose odd output pins and even output pins respectively output gray scale voltages of differing polarity. Assuring a maximum clock frequency of 65 MHz when driving at 3.0 V, 45 MHz when driving at 2.3 V, this driver is applicable to XGA-standard TFT-LCD panels and SXGA TFT-LCD panels.

### FEATURES

- CMOS level input (2.3 to 3.6 V)
- 384 outputs
- Input of 6 bits (gray-scale data) by 6 dots
- Capable of outputting 64 values by means of 5-by-2 external power modules (10 units) and a D/A converter
- Logic power supply voltage ( $V_{DD1}$ ): 2.3 to 3.6 V
- Driver power supply voltage ( $V_{DD2}$ ): 8.0 to 9.0 V
- High-speed data transfer:  $f_{CLK} = 65$  MHz (internal data transfer speed when operating at  $V_{DD1} = 3.0$  V)
- Output dynamic range:  $V_{SS2} + 0.1$  V to  $V_{DD2} - 0.1$  V
- Apply for dot-line inversion, n-line inversion and column line inversion
- Output voltage polarity inversion function (POL)
- Display data inversion function (capable of controlling by each input port) (POL21, POL22)
- Current consumption control function (LPC, Bcont)
- Succession of  $\mu$ PD16732A driver

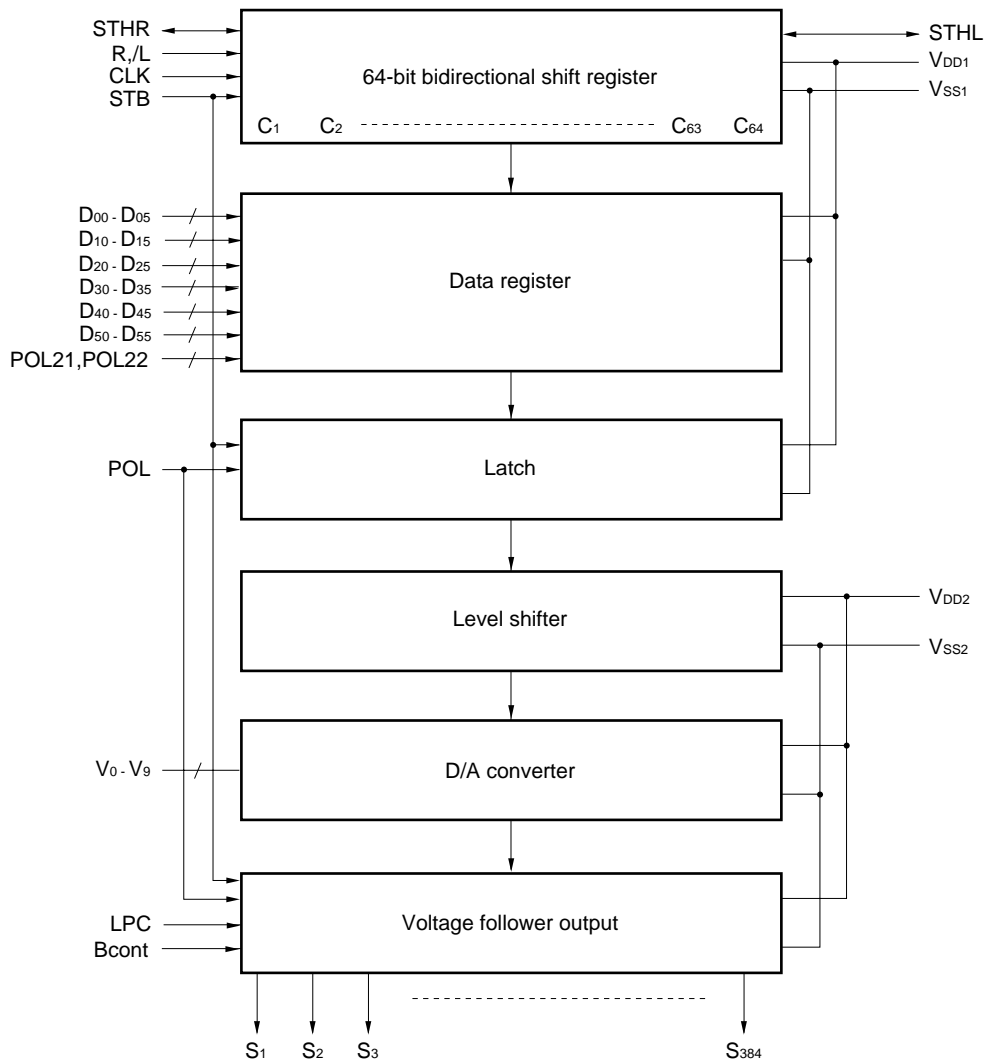
### ORDERING INFORMATION

Part Number	Package
$\mu$ PD16732DN-xxx	TCP (TAB package)

**Remark** The TCP's external shape is customized. To order the required shape, so please contact one of our sales representatives.

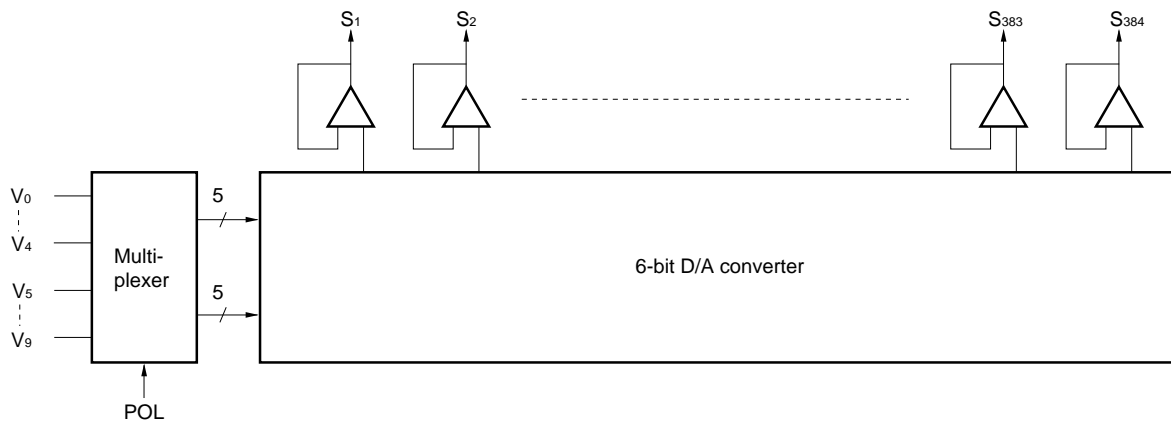
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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

1. BLOCK DIAGRAM



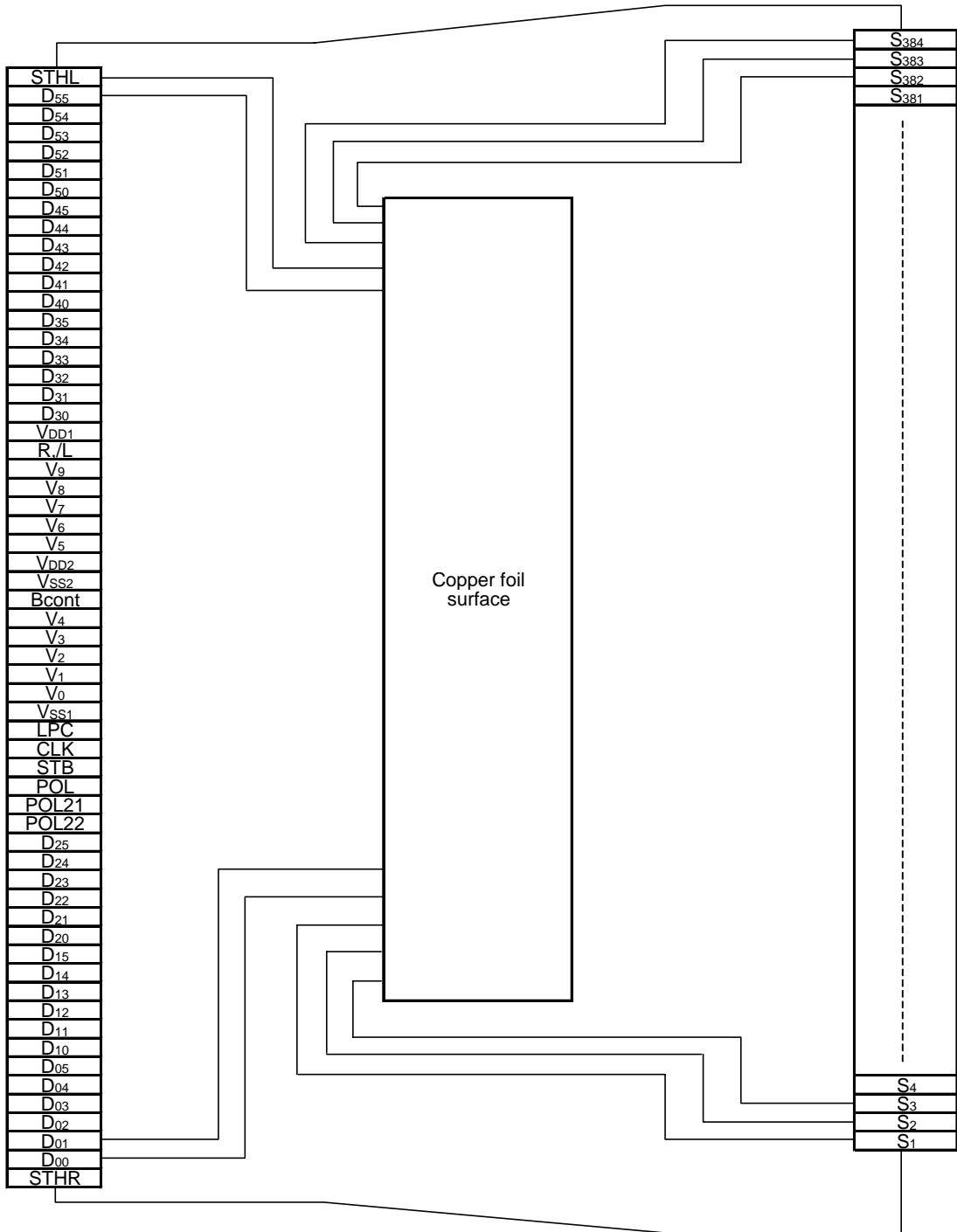
Remark /xxx indicates active low signal.

2. RELATIONSHIP BETWEEN OUTPUT CIRCUIT AND D/A CONVERTER



3. PIN CONFIGURATION (Top of copper foil surface, face-up)

μPD16732DN-xxx: TCP (TAB package)



**Remark** This figure does not specify the TCP package.

4. PIN FUNCTIONS

(1/2)

Pin Symbol	Pin Name	I/O	Description
S <sub>1</sub> to S <sub>384</sub>	Driver	Output	The D/A converted 64-gray-scale analog voltage is output.
D <sub>00</sub> to D <sub>05</sub>	Display data	Input	The display data is input with a width of 36 bits, viz., the gray scale data (6 bits) by 6 dots (2 pixels). D <sub>x0</sub> : LSB, D <sub>x5</sub> : MSB
D <sub>10</sub> to D <sub>15</sub>			
D <sub>20</sub> to D <sub>25</sub>			
D <sub>30</sub> to D <sub>35</sub>			
D <sub>40</sub> to D <sub>45</sub>			
D <sub>50</sub> to D <sub>55</sub>			
R,/L	Shift direction control	Input	The shift direction control pin of the shift register. The shift directions of the shift registers are as follows. R,/L = H (right shift): STHR (input), S <sub>1</sub> → S <sub>384</sub> , STHL (output) R,/L = L (left shift) : STHL (input), S <sub>384</sub> → S <sub>1</sub> , STHR (output)
STHR	Right shift start pulse	I/O	These refer to the start pulse I/O pins when the IC is connected in cascade. Loading of display data starts when a high level is read at the rising edge of CLK. A high level should be input as the pulse of one cycle of the clock signal.
STHL	Left shift start pulse	I/O	If the start pulse input is more than 2CLKs, the first 1CLK of the high-level input is valid. R,/L = H (right shift): STHR input, STHL output R,/L = L (left shift): STHL input, STHR output
CLK	Shift clock	Input	This pin refers to the shift clock input of the shift register. The display data is loaded into the data register at the rising edge. At the rising edge of the 64th after the start pulse input, the start pulse output reaches the high level, thus becoming the start pulse of the next-level driver. When the 66 clock pulses are input after input of the start pulse, input of display data is halted automatically. The contents of the shift register are cleared at the STB's rising edge.
STB	Latch	Input	The contents of the data register are transferred to the latch circuit at the rising edge. In addition, at the falling edge, the gray scale voltage is supplied to the driver. It is necessary to ensure input of one pulse per horizontal period.
POL	Polarity input	Input	POL = L: The S <sub>2n-1</sub> output uses V <sub>0</sub> to V <sub>4</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>5</sub> to V <sub>9</sub> as the reference supply. POL = H: The S <sub>2n-1</sub> output uses V <sub>5</sub> to V <sub>9</sub> as the reference supply. The S <sub>2n</sub> output uses V <sub>0</sub> to V <sub>4</sub> as the reference supply. S <sub>2n-1</sub> indicates the odd output: and S <sub>2n</sub> indicates the even output. Input of the POL signal is allowed the setup time (t <sub>POL-STB</sub> ) with respect to STB's rising edge.
POL21, POL22	Data inversion	Input	Select of inversion or no inversion for input data. POL21: D <sub>00</sub> -D <sub>05</sub> , D <sub>10</sub> -D <sub>15</sub> , D <sub>20</sub> -D <sub>25</sub> Data inversion or no inversion of Port1 POL22: D <sub>30</sub> -D <sub>35</sub> , D <sub>40</sub> -D <sub>45</sub> , D <sub>50</sub> -D <sub>55</sub> Data inversion or no inversion of Port2 POL21,POL22 = H: Data are inverted in the IC. POL21,POL22 = L: Data are not inverted in the IC.
LPC	Low power control	Input	The current consumption is lowered by controlling the constant current source of the output amplifier. In low power mode (LPC = L), the V <sub>DD2</sub> of static current consumption can be reduced to two thirds of the normal current consumption. This pin is pulled up to the V <sub>DD1</sub> power supply inside the IC. LPC = H or open: Normal power mode LPC = L: Low power mode
Bcont	Bias control	Input	This pin can be used to finely control the bias current inside the output amplifier. In cases when fine-control is necessary, connect this pin to the stabilized ground potential (V <sub>SS2</sub> ) via an external resistor of 10 to 100 kΩ (per IC). When this fine-control function is not required, leave this pin open. Refer to <b>9. CURRENT CONSUMPTION REDUCTION FUNCTION</b>

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(2/2)

Pin Symbol	Pin Name	I/O	Description
V <sub>0</sub> to V <sub>9</sub>	γ-corrected power supplies	–	Input the γ-corrected power supplies from outside by using operational amplifier. Make sure to maintain the following relationships. During the gray scale voltage output, be sure to keep the gray scale level power supply at a constant level. $V_{DD2} - 0.1\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5 V_{DD2}$ $0.5 V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\text{ V}$
V <sub>DD1</sub>	Logic power supply	–	2.3 to 3.6 V
V <sub>DD2</sub>	Driver power supply	–	8.0 to 9.0 V
V <sub>SS1</sub>	Logic ground	–	Grounding
V <sub>SS2</sub>	Driver ground	–	Grounding

- Cautions**
- 1. The power start sequence must be V<sub>DD1</sub>, logic input, and V<sub>DD2</sub> & V<sub>0</sub> to V<sub>9</sub> in that order. Reverse this sequence to shut down (Simultaneous power application to V<sub>DD2</sub> and V<sub>0</sub> to V<sub>9</sub> is possible.).**
  - 2. To stabilize the supply voltage, please be sure to insert a 0.1 μF bypass capacitor between V<sub>DD1</sub>-V<sub>SS1</sub> and V<sub>DD2</sub>-V<sub>SS2</sub>. Furthermore, for increased precision of the D/A converter, insertion of a bypass capacitor of about 0.01 μF is also recommended between the γ-corrected power supply terminals (V<sub>0</sub>, V<sub>1</sub>, V<sub>2</sub>,....., V<sub>9</sub>) and V<sub>SS2</sub>.**

5. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT VOLTAGE VALUE

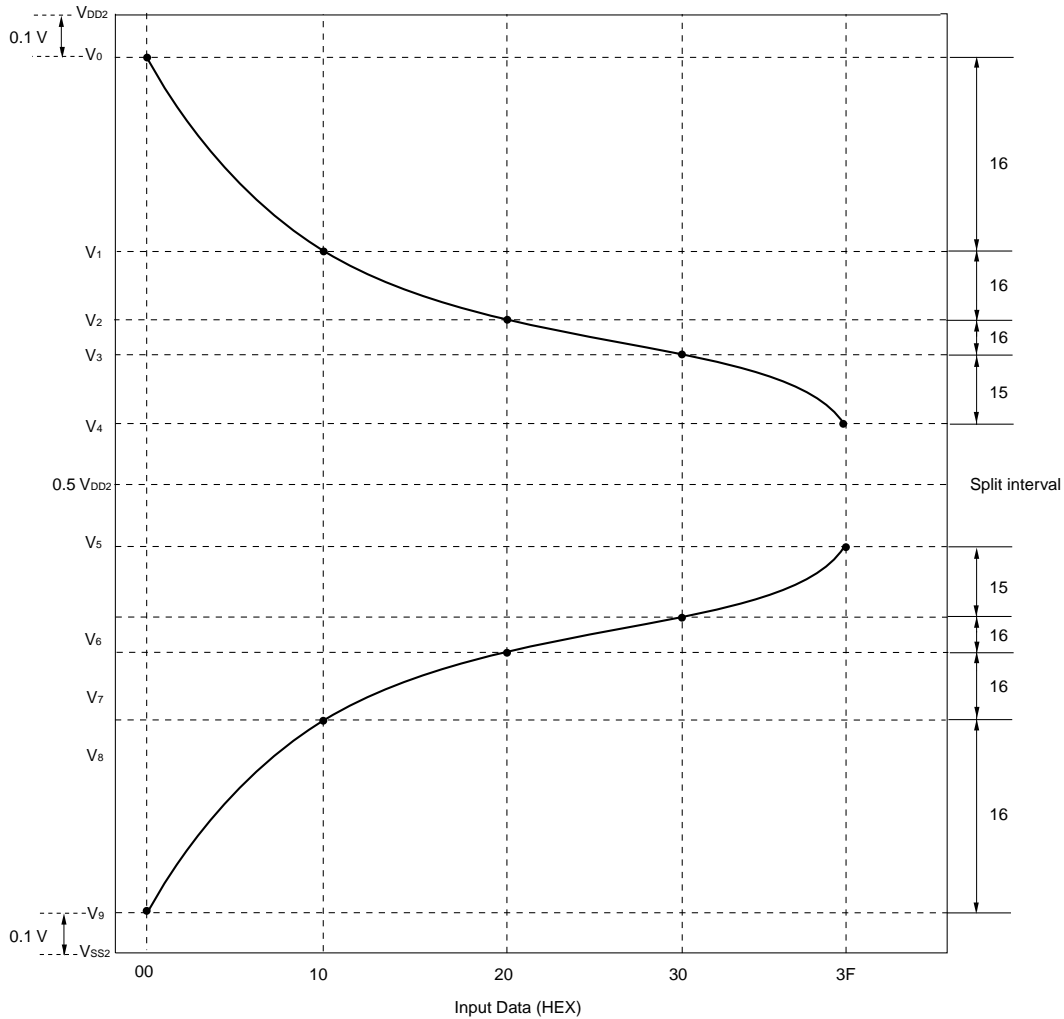
The μPD16732D incorporates a 6-bit D/A converter whose odd output pins and even output pins output respectively gray scale voltages of differing polarity with respect to the LCD's counter electrode voltage. The D/A converter consists of ladder resistors and switches. The ladder resistors ( $r_0$  to  $r_{62}$ ) are designed so that the ratio of LCD panel  $\gamma$ -compensated voltages to  $V_0'$  to  $V_{63}'$  and  $V_0''$  to  $V_{63}''$  is almost equivalent as shown in Figure 5-2. For the 2 sets of five  $\gamma$ -compensated power supplies,  $V_0$  to  $V_4$  and  $V_5$  to  $V_9$ , respectively, input gray scale voltages of the same polarity with respect to the common voltage. When fine-gray scale voltage precision is not necessary, there is no need to connect voltage follower circuit to the  $\gamma$ -corrected power supplies  $V_1$  to  $V_3$  and  $V_6$  to  $V_8$ .

Figure 5-1 shows the relationship between the driving voltages such as liquid-crystal driving voltages  $V_{DD2}$  and  $V_{SS2}$ , and  $\gamma$ -corrected voltages  $V_0$  to  $V_9$  and the input data. Be sure to maintain the voltage relationships as follows.

- ★  $V_{DD2} - 0.1\text{ V} \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5 V_{DD2}$
- $0.5 V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1\text{ V}$

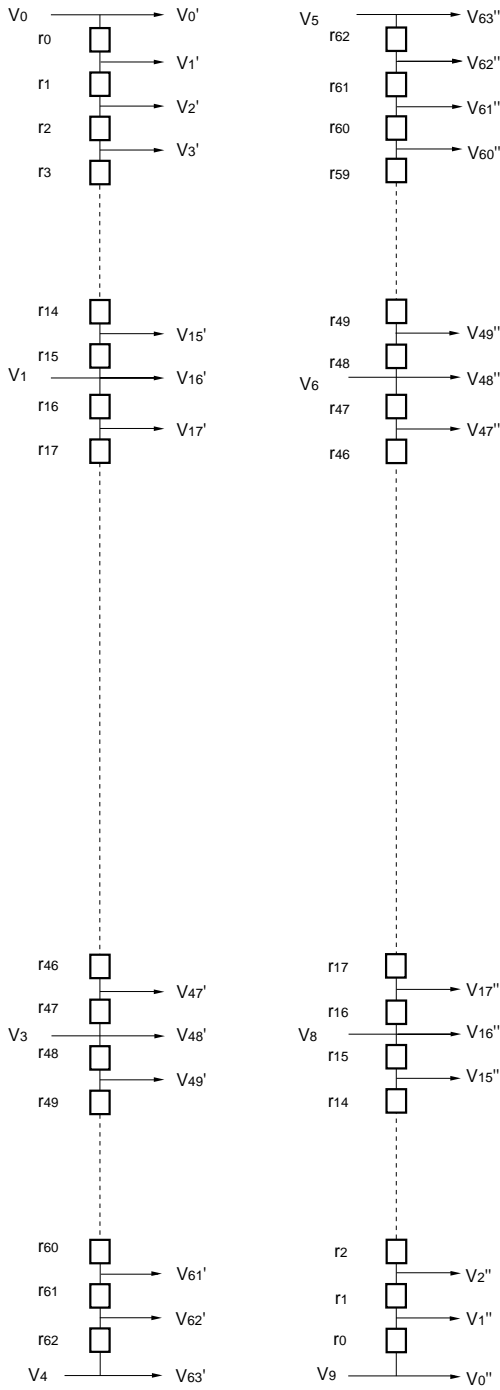
Figures 5-2 indicates  $\gamma$ -corrected voltages and ladder resistors ratio. Figures 5-3 indicates the relationship between the input data and output voltage and the resistance values of the resistor string.

Figure 5-1. Relationship between Input Data and  $\gamma$ -corrected Power Supplies



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Figure 5-2.  $\gamma$ -corrected Voltages and Ladder Resistor's Ratio



rn	Ratio1	Ratio2	Value( $\Omega$ )
r0	8.0	0.050	800
r1	7.5	0.047	750
r2	7.0	0.044	700
r3	6.5	0.041	650
r4	6.0	0.038	600
r5	5.5	0.035	550
r6	5.5	0.035	550
r7	5.0	0.032	500
r8	5.0	0.032	500
r9	4.0	0.025	400
r10	4.0	0.025	400
r11	3.5	0.022	350
r12	3.5	0.022	350
r13	3.5	0.022	350
r14	3.0	0.019	300
r15	3.0	0.019	300
r16	3.0	0.019	300
r17	2.5	0.016	250
r18	2.5	0.016	250
r19	2.5	0.016	250
r20	2.0	0.013	200
r21	2.0	0.013	200
r22	2.0	0.013	200
r23	1.5	0.009	150
r24	1.5	0.009	150
r25	1.5	0.009	150
r26	1.5	0.009	150
r27	1.0	0.006	100
r28	1.0	0.006	100
r29	1.0	0.006	100
r30	1.0	0.006	100
r31	1.0	0.006	100
r32	1.0	0.006	100
r33	1.0	0.006	100
r34	1.0	0.006	100
r35	1.0	0.006	100
r36	1.0	0.006	100
r37	1.0	0.006	100
r38	1.0	0.006	100
r39	1.0	0.006	100
r40	1.0	0.006	100
r41	1.0	0.006	100
r42	1.0	0.006	100
r43	1.0	0.006	100
r44	1.0	0.006	100
r45	1.0	0.006	100
r46	1.0	0.006	100
r47	1.0	0.006	100
r48	1.0	0.006	100
r49	1.0	0.006	100
r50	1.0	0.006	100
r51	1.0	0.006	100
r52	1.0	0.006	100
r53	1.5	0.009	150
r54	1.5	0.009	150
r55	1.5	0.009	150
r56	2.0	0.013	200
r57	2.0	0.013	200
r58	2.5	0.016	250
r59	2.5	0.016	250
r60	3.0	0.019	300
r61	5.0	0.032	500
r62	8.0	0.050	800

**Caution** There is no connection between V4 and V5 terminal in the chip.

**Remark** The resistance ratio1 is a relative ratio in the case of setting the minimum resistance value to 1.  
The resistance ratio2 is a relative ratio in the case of setting the total resistance to 1.

★ Figure 5-3. Relationship between Input Data and Output Voltage (POL21,POL22 = L)

(Output Voltage 1)  $V_{DD2} - 0.1 V \geq V_0 > V_1 > V_2 > V_3 > V_4 \geq 0.5 V_{DD2}$

(Output Voltage 2)  $0.5 V_{DD2} \geq V_5 > V_6 > V_7 > V_8 > V_9 \geq V_{SS2} + 0.1 V$

Input Data	Output Voltage1		Output Voltage2	
00H	$V_0'$	$V_0$	$V_0'$	$V_9$
01H	$V_1'$	$V_1+(V_0-V_1) \times 7250 / 8050$	$V_1'$	$V_9+(V_8-V_9) \times 800 / 8050$
02H	$V_2'$	$V_1+(V_0-V_1) \times 6500 / 8050$	$V_2'$	$V_9+(V_8-V_9) \times 1550 / 8050$
03H	$V_3'$	$V_1+(V_0-V_1) \times 5800 / 8050$	$V_3'$	$V_9+(V_8-V_9) \times 2250 / 8050$
04H	$V_4'$	$V_1+(V_0-V_1) \times 5150 / 8050$	$V_4'$	$V_9+(V_8-V_9) \times 2900 / 8050$
05H	$V_5'$	$V_1+(V_0-V_1) \times 4550 / 8050$	$V_5'$	$V_9+(V_8-V_9) \times 3500 / 8050$
06H	$V_6'$	$V_1+(V_0-V_1) \times 4000 / 8050$	$V_6'$	$V_9+(V_8-V_9) \times 4050 / 8050$
07H	$V_7'$	$V_1+(V_0-V_1) \times 3450 / 8050$	$V_7'$	$V_9+(V_8-V_9) \times 4600 / 8050$
08H	$V_8'$	$V_1+(V_0-V_1) \times 2950 / 8050$	$V_8'$	$V_9+(V_8-V_9) \times 5100 / 8050$
09H	$V_9'$	$V_1+(V_0-V_1) \times 2450 / 8050$	$V_9'$	$V_9+(V_8-V_9) \times 5600 / 8050$
0AH	$V_{10}'$	$V_1+(V_0-V_1) \times 2050 / 8050$	$V_{10}'$	$V_9+(V_8-V_9) \times 6000 / 8050$
0BH	$V_{11}'$	$V_1+(V_0-V_1) \times 1650 / 8050$	$V_{11}'$	$V_9+(V_8-V_9) \times 6400 / 8050$
0CH	$V_{12}'$	$V_1+(V_0-V_1) \times 1300 / 8050$	$V_{12}'$	$V_9+(V_8-V_9) \times 6750 / 8050$
0DH	$V_{13}'$	$V_1+(V_0-V_1) \times 950 / 8050$	$V_{13}'$	$V_9+(V_8-V_9) \times 7100 / 8050$
0EH	$V_{14}'$	$V_1+(V_0-V_1) \times 600 / 8050$	$V_{14}'$	$V_9+(V_8-V_9) \times 7450 / 8050$
0FH	$V_{15}'$	$V_1+(V_0-V_1) \times 300 / 8050$	$V_{15}'$	$V_9+(V_8-V_9) \times 7750 / 8050$
10H	$V_{16}'$	$V_1$	$V_{16}'$	$V_8$
11H	$V_{17}'$	$V_2+(V_1-V_2) \times 2450 / 2750$	$V_{17}'$	$V_8+(V_7-V_8) \times 300 / 2750$
12H	$V_{18}'$	$V_2+(V_1-V_2) \times 2200 / 2750$	$V_{18}'$	$V_8+(V_7-V_8) \times 550 / 2750$
13H	$V_{19}'$	$V_2+(V_1-V_2) \times 1950 / 2750$	$V_{19}'$	$V_8+(V_7-V_8) \times 800 / 2750$
14H	$V_{20}'$	$V_2+(V_1-V_2) \times 1700 / 2750$	$V_{20}'$	$V_8+(V_7-V_8) \times 1050 / 2750$
15H	$V_{21}'$	$V_2+(V_1-V_2) \times 1500 / 2750$	$V_{21}'$	$V_8+(V_7-V_8) \times 1250 / 2750$
16H	$V_{22}'$	$V_2+(V_1-V_2) \times 1300 / 2750$	$V_{22}'$	$V_8+(V_7-V_8) \times 1450 / 2750$
17H	$V_{23}'$	$V_2+(V_1-V_2) \times 1100 / 2750$	$V_{23}'$	$V_8+(V_7-V_8) \times 1650 / 2750$
18H	$V_{24}'$	$V_2+(V_1-V_2) \times 950 / 2750$	$V_{24}'$	$V_8+(V_7-V_8) \times 1800 / 2750$
19H	$V_{25}'$	$V_2+(V_1-V_2) \times 800 / 2750$	$V_{25}'$	$V_8+(V_7-V_8) \times 1950 / 2750$
1AH	$V_{26}'$	$V_2+(V_1-V_2) \times 650 / 2750$	$V_{26}'$	$V_8+(V_7-V_8) \times 2100 / 2750$
1BH	$V_{27}'$	$V_2+(V_1-V_2) \times 500 / 2750$	$V_{27}'$	$V_8+(V_7-V_8) \times 2250 / 2750$
1CH	$V_{28}'$	$V_2+(V_1-V_2) \times 400 / 2750$	$V_{28}'$	$V_8+(V_7-V_8) \times 2350 / 2750$
1DH	$V_{29}'$	$V_2+(V_1-V_2) \times 300 / 2750$	$V_{29}'$	$V_8+(V_7-V_8) \times 2450 / 2750$
1EH	$V_{30}'$	$V_2+(V_1-V_2) \times 200 / 2750$	$V_{30}'$	$V_8+(V_7-V_8) \times 2550 / 2750$
1FH	$V_{31}'$	$V_2+(V_1-V_2) \times 100 / 2750$	$V_{31}'$	$V_8+(V_7-V_8) \times 2650 / 2750$
20H	$V_{32}'$	$V_2$	$V_{32}'$	$V_7$
21H	$V_{33}'$	$V_3+(V_2-V_3) \times 1500 / 1600$	$V_{33}'$	$V_7+(V_6-V_7) \times 100 / 1600$
22H	$V_{34}'$	$V_3+(V_2-V_3) \times 1400 / 1600$	$V_{34}'$	$V_7+(V_6-V_7) \times 200 / 1600$
23H	$V_{35}'$	$V_3+(V_2-V_3) \times 1300 / 1600$	$V_{35}'$	$V_7+(V_6-V_7) \times 300 / 1600$
24H	$V_{36}'$	$V_3+(V_2-V_3) \times 1200 / 1600$	$V_{36}'$	$V_7+(V_6-V_7) \times 400 / 1600$
25H	$V_{37}'$	$V_3+(V_2-V_3) \times 1100 / 1600$	$V_{37}'$	$V_7+(V_6-V_7) \times 500 / 1600$
26H	$V_{38}'$	$V_3+(V_2-V_3) \times 1000 / 1600$	$V_{38}'$	$V_7+(V_6-V_7) \times 600 / 1600$
27H	$V_{39}'$	$V_3+(V_2-V_3) \times 900 / 1600$	$V_{39}'$	$V_7+(V_6-V_7) \times 700 / 1600$
28H	$V_{40}'$	$V_3+(V_2-V_3) \times 800 / 1600$	$V_{40}'$	$V_7+(V_6-V_7) \times 800 / 1600$
29H	$V_{41}'$	$V_3+(V_2-V_3) \times 700 / 1600$	$V_{41}'$	$V_7+(V_6-V_7) \times 900 / 1600$
2AH	$V_{42}'$	$V_3+(V_2-V_3) \times 600 / 1600$	$V_{42}'$	$V_7+(V_6-V_7) \times 1000 / 1600$
2BH	$V_{43}'$	$V_3+(V_2-V_3) \times 500 / 1600$	$V_{43}'$	$V_7+(V_6-V_7) \times 1100 / 1600$
2CH	$V_{44}'$	$V_3+(V_2-V_3) \times 400 / 1600$	$V_{44}'$	$V_7+(V_6-V_7) \times 1200 / 1600$
2DH	$V_{45}'$	$V_3+(V_2-V_3) \times 300 / 1600$	$V_{45}'$	$V_7+(V_6-V_7) \times 1300 / 1600$
2EH	$V_{46}'$	$V_3+(V_2-V_3) \times 200 / 1600$	$V_{46}'$	$V_7+(V_6-V_7) \times 1400 / 1600$
2FH	$V_{47}'$	$V_3+(V_2-V_3) \times 100 / 1600$	$V_{47}'$	$V_7+(V_6-V_7) \times 1500 / 1600$
30H	$V_{48}'$	$V_3$	$V_{48}'$	$V_6$
31H	$V_{49}'$	$V_4+(V_3-V_4) \times 3350 / 3450$	$V_{49}'$	$V_6+(V_5-V_6) \times 100 / 3450$
32H	$V_{50}'$	$V_4+(V_3-V_4) \times 3250 / 3450$	$V_{50}'$	$V_6+(V_5-V_6) \times 200 / 3450$
33H	$V_{51}'$	$V_4+(V_3-V_4) \times 3150 / 3450$	$V_{51}'$	$V_6+(V_5-V_6) \times 300 / 3450$
34H	$V_{52}'$	$V_4+(V_3-V_4) \times 3050 / 3450$	$V_{52}'$	$V_6+(V_5-V_6) \times 400 / 3450$
35H	$V_{53}'$	$V_4+(V_3-V_4) \times 2950 / 3450$	$V_{53}'$	$V_6+(V_5-V_6) \times 500 / 3450$
36H	$V_{54}'$	$V_4+(V_3-V_4) \times 2800 / 3450$	$V_{54}'$	$V_6+(V_5-V_6) \times 650 / 3450$
37H	$V_{55}'$	$V_4+(V_3-V_4) \times 2650 / 3450$	$V_{55}'$	$V_6+(V_5-V_6) \times 800 / 3450$
38H	$V_{56}'$	$V_4+(V_3-V_4) \times 2500 / 3450$	$V_{56}'$	$V_6+(V_5-V_6) \times 950 / 3450$
39H	$V_{57}'$	$V_4+(V_3-V_4) \times 2300 / 3450$	$V_{57}'$	$V_6+(V_5-V_6) \times 1150 / 3450$
3AH	$V_{58}'$	$V_4+(V_3-V_4) \times 2100 / 3450$	$V_{58}'$	$V_6+(V_5-V_6) \times 1350 / 3450$
3BH	$V_{59}'$	$V_4+(V_3-V_4) \times 1850 / 3450$	$V_{59}'$	$V_6+(V_5-V_6) \times 1600 / 3450$
3CH	$V_{60}'$	$V_4+(V_3-V_4) \times 1600 / 3450$	$V_{60}'$	$V_6+(V_5-V_6) \times 1850 / 3450$
3DH	$V_{61}'$	$V_4+(V_3-V_4) \times 1300 / 3450$	$V_{61}'$	$V_6+(V_5-V_6) \times 2150 / 3450$
3EH	$V_{62}'$	$V_4+(V_3-V_4) \times 800 / 3450$	$V_{62}'$	$V_6+(V_5-V_6) \times 2650 / 3450$
3FH	$V_{63}'$	$V_4$	$V_{63}'$	$V_5$

Caution There is no connection between V4 and V5 terminal in the chip.



### 6. RELATIONSHIP BETWEEN INPUT DATA AND OUTPUT PIN

Data format : 6 bits x 2 RGBs (6 dots)

Input width : 36 bits (2-pixel data)

(1) R,/L = H (Right shift)

Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	...	D <sub>40</sub> to D <sub>45</sub>	D <sub>50</sub> to D <sub>55</sub>

(2) R,/L = L (Left shift)

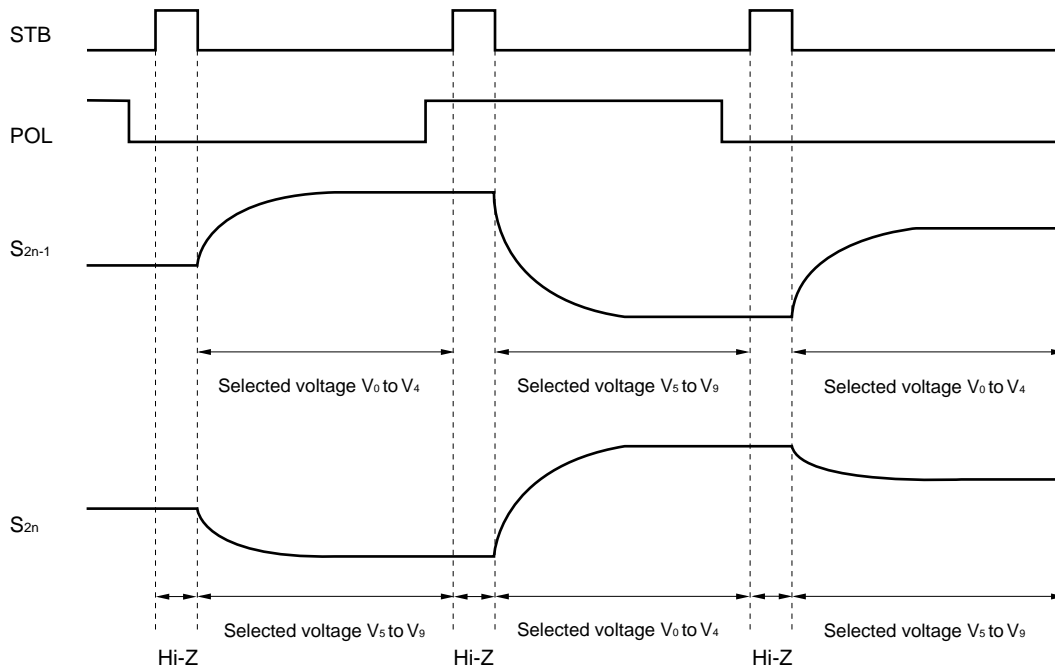
Output	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	...	S <sub>383</sub>	S <sub>384</sub>
Data	D <sub>00</sub> to D <sub>05</sub>	D <sub>10</sub> to D <sub>15</sub>	D <sub>20</sub> to D <sub>25</sub>	D <sub>30</sub> to D <sub>35</sub>	...	D <sub>40</sub> to D <sub>45</sub>	D <sub>50</sub> to D <sub>55</sub>

POL	S <sub>2n-1</sub> <small>Note</small>	S <sub>2n</sub> <small>Note</small>
L	V <sub>0</sub> to V <sub>4</sub>	V <sub>5</sub> to V <sub>9</sub>
H	V <sub>5</sub> to V <sub>9</sub>	V <sub>0</sub> to V <sub>4</sub>

**Note** S<sub>2n-1</sub> (Odd output), S<sub>2n</sub> (Even output)

### 7. RELATIONSHIP BETWEEN STB, POL AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.



8. RELATIONSHIP BETWEEN STB, CLK, AND OUTPUT WAVEFORM

The output voltage is written to the LCD panel synchronized with the STB falling edge.

Figure 8-1. Output Circuit Block Diagram

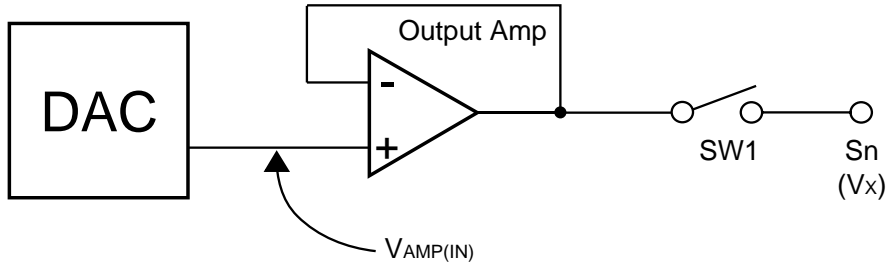
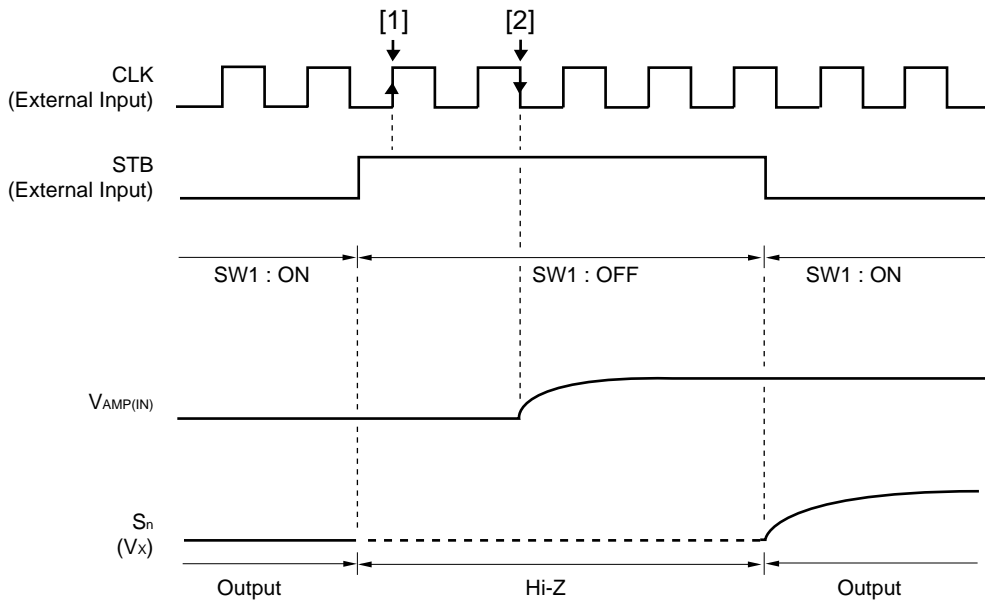


Figure 8-2. Output Circuit Block Diagram



- Remarks 1. STB = L: SW1 = ON  
STB = H: SW1 = OFF
- 2. STB = H is acknowledged at timing [1].
- 3. The display data latch is completed at timing [2] and the input voltage ( $V_{AMP(IN)}$ ): gray-scale level voltage) of the output amplifier changes.

### 9. CURRENT CONSUMPTION REDUCTION FUNCTION

The μPD16732D has a low power control function (LPC) which can switch the bias current of the output amplifier between two levels and a bias control function (Bcont) which can be used to finely control the bias current.

#### <Low power control function (LPC)>

The bias current of the output amplifier can be switched between two levels using this pin. (Bcont: open)

LPC = H or open: normal power mode

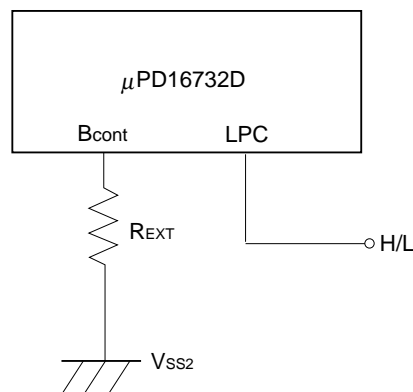
LPC = L: low power mode

The  $V_{DD2}$  of static current consumption can be reduced to two thirds of that in normal mode, input a stable DC current ( $V_{DD1}/V_{SS1}$ ) to this pin.

#### <Bias current control function (Bcont)>

It is possible to fine-control the current consumption by using the bias current control function (Bcont pin). When using this function, connect this pin to the stabilized ground potential ( $V_{SS2}$ ) via an external resistor ( $R_{EXT}$ ). When not using this function, leave this pin open.

Figure 9–1. Bias Current Control Function (Bcont)



Refer to the table below for the percentage of current regulation when using the bias current control-function.

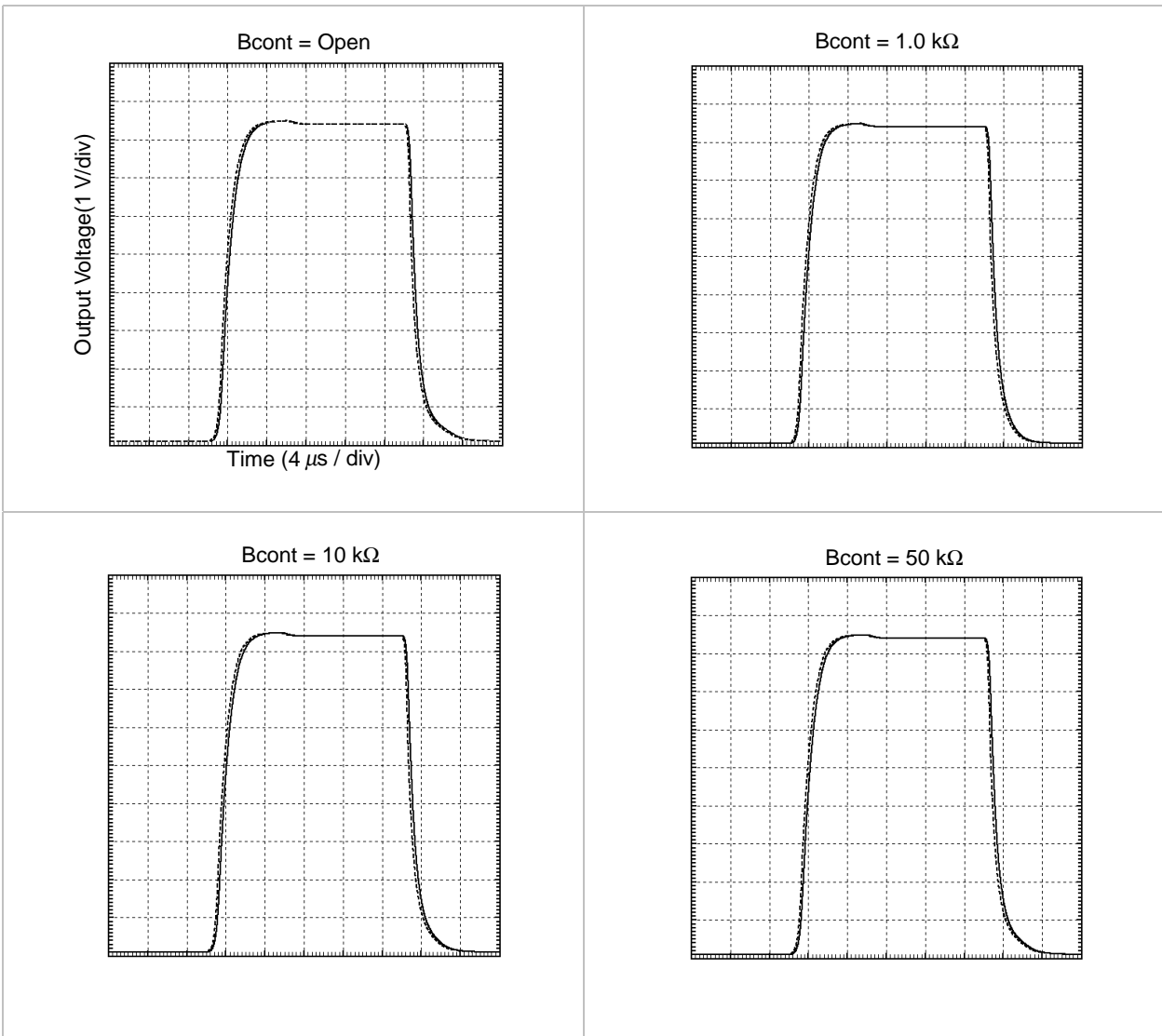
Table 9–1. Current Consumption Regulation Percentage Compared to Normal Mode  $V_{DD1} = 3.3\text{ V}$   $V_{DD2} = 8.7\text{ V}$   
LPC = 3.3 V / 0 V

$R_{EXT}$ (kΩ)	Current Consumption Regulation Percentage (%)	
	LPC = H	LPC = L
∞ (Open)	100	65
50	110	70
20	115	80
10	120	85

**Remark** The above current consumption regulation percentages are not product-characteristic guaranteed as they are based on the results of simulation.

**Caution** Because the low-power and bias-current control functions control the bias current in the output amplifier and regulate the over-all current consumption of the driver IC, when this occurs, the characteristics of the output amplifier will simultaneously change. Therefore, when using these functions, be sure to sufficiently evaluate the picture quality.

Figure9-2. Output Wave Form (LPC = L)



----- [1]  
 \_\_\_\_\_ [2]

<Test Condition>

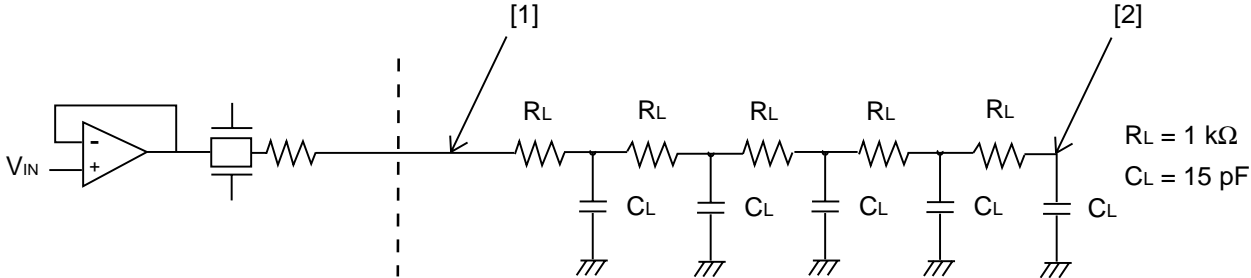
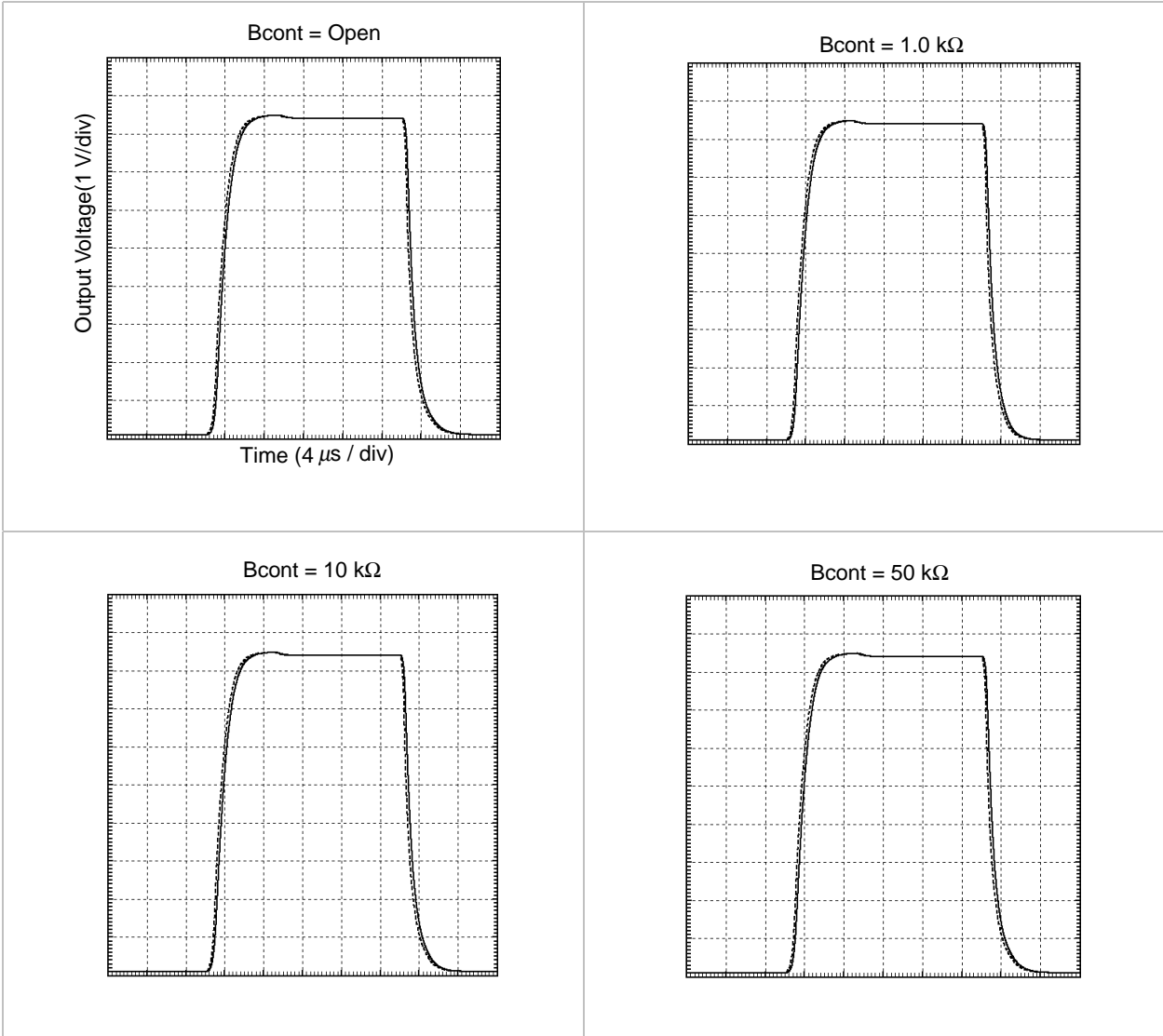


Figure9-3. Output Wave Form (LPC = H)



10. ELECTRICAL SPECIFICATIONS

**Absolute Maximum Ratings (T<sub>A</sub> = 25°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Rating	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>	-0.5 to +4.0	V
Driver Part Supply Voltage	V <sub>DD2</sub>	-0.5 to +10.0	V
Logic Part Input Voltage	V <sub>I1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Input Voltage	V <sub>I2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Logic Part Output Voltage	V <sub>O1</sub>	-0.5 to V <sub>DD1</sub> + 0.5	V
Driver Part Output Voltage	V <sub>O2</sub>	-0.5 to V <sub>DD2</sub> + 0.5	V
Operating Ambient Temperature	T <sub>A</sub>	-10 to +75	°C
Storage Temperature	T <sub>stg</sub>	-55 to +125	°C

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Recommended Operating Range (T<sub>A</sub> = -10 to +75°C, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V)**

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Logic Part Supply Voltage	V <sub>DD1</sub>		2.3		3.6	V
Driver Part Supply Voltage	V <sub>DD2</sub>		8.0	8.5	9.0	V
High-Level Input Voltage	V <sub>IH</sub>		0.7 V <sub>DD1</sub>		V <sub>DD1</sub>	V
Low-Level Input Voltage	V <sub>IL</sub>		0		0.3 V <sub>DD1</sub>	V
γ-Corrected Voltage	V <sub>0</sub> to V <sub>4</sub>		0.5 V <sub>DD2</sub>		V <sub>DD2</sub> - 0.1	V
	V <sub>5</sub> to V <sub>9</sub>		V <sub>SS2</sub> + 0.1		0.5 V <sub>DD2</sub>	V
Driver Part Output Voltage	V <sub>O</sub>		V <sub>SS2</sub> + 0.1		V <sub>DD2</sub> - 0.1	V
★ ★ Clock Frequency	f <sub>CLK</sub>	2.3 ≤ V <sub>DD1</sub> < 3.0 V			45	MHz
		3.0 V ≤ V <sub>DD1</sub> ≤ 3.6 V			65	MHz

Electrical Characteristics (T<sub>A</sub> = -10 to +75°C, V<sub>DD1</sub> = 2.3 to 3.6 V, V<sub>DD2</sub> = 8.0 to 9.0 V, V<sub>SS1</sub> = V<sub>SS2</sub> = 0 V,

Unless otherwise specified, LPC = H or open, Bcont = open)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Leak Current	I <sub>IL</sub>				±1.0	μA
High-Level Output Voltage	V <sub>OH</sub>	STHR (STHL), I <sub>OH</sub> = 0 mA	V <sub>DD1</sub> - 0.1			V
Low-Level Output Voltage	V <sub>OL</sub>	STHR (STHL), I <sub>OL</sub> = 0 mA			0.1	V
★ γ-Corrected Resistance	R <sub>γ</sub>	V <sub>0</sub> to V <sub>4</sub> = V <sub>5</sub> to V <sub>9</sub> = 4.0 V	8	16	32	kΩ
★ Driver Output Current	I <sub>VOH</sub>	V <sub>X</sub> = 7.0 V, V <sub>OUT</sub> = 6.5 V <sup>Note</sup>			-30	μA
	I <sub>VOL</sub>	V <sub>X</sub> = 1.0 V, V <sub>OUT</sub> = 1.5 V <sup>Note</sup>	30			μA
Output Voltage Deviation	ΔV <sub>O</sub>	V <sub>DD1</sub> = 3.3 V, V <sub>DD2</sub> = 8.5 V		±7	±20	mV
Output Swing Difference Deviation	ΔV <sub>P-P</sub>	V <sub>OUT</sub> = 2.0 V, 4.25 V, 6.5 V		±2	±15	mV
Output Voltage Range	V <sub>O</sub>	All input data	0.1		V <sub>DD2</sub> - 0.1	V
★ Logic Part Dynamic Current Consumption	I <sub>DD1</sub>	V <sub>DD1</sub> , with no load		1.0	6.0	mA
★ Driver Part Dynamic Current Consumption	I <sub>DD21</sub>	V <sub>DD2</sub> = 8.0 to 9.0 V, with no load, LPC =H, Bcont = open		3.0	6.0	mA
	I <sub>DD22</sub>	V <sub>DD2</sub> = 8.0 to 9.0 V, with no load, LPC =L, Bcont = open		2.0	4.0	mA

**Note** V<sub>X</sub> refers to the output voltage of analog output pins S<sub>1</sub> to S<sub>384</sub>.

V<sub>OUT</sub> refers to the voltage applied to analog output pins S<sub>1</sub> to S<sub>384</sub>.

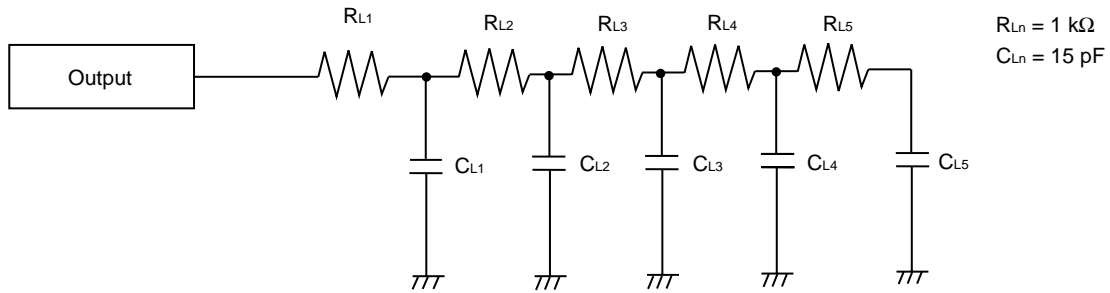
**Cautions 1. STB cycle is 20 μs, f<sub>CLK</sub> = 40 MHz**

2. The TYP. values refer to an all black or all white input pattern. The MAX. value refers to the measured values in the dot checkerboard input pattern.
3. Refers to the current consumption per driver when cascades are connected under the assumption of XGA+ single-sided mounting (8 units).

Switching Characteristics ( $T_A = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD1} = 2.3$  to  $3.6$  V,  $V_{DD2} = 8.0$  to  $9.0$  V,  $V_{SS1} = V_{SS2} = 0$  V,  
Unless otherwise specified,  $LPC = H$  or open,  $Bcont = open$ )

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Start Pulse Delay Time	$t_{PLH1}$	$C_L = 10$ pF, $2.3 \leq V_{DD1} < 3.0$ V		10	17	ns
		$C_L = 10$ pF, $3.0 \text{ V} \leq V_{DD1} \leq 3.6$ V		7	10.5	ns
★ Driver Output Delay Time	$t_{PLH2}$	$C_L = 75$ pF, $R_L = 5$ kΩ		2.5	5	μs
	$t_{PLH3}$			5	8	μs
	$t_{PHL2}$			2.5	5	μs
	$t_{PHL3}$			5	8	μs
Input Capacitance	$C_{i1}$	Exclude $STHR$ ( $STHL$ ), $T_A = 25^\circ\text{C}$		5	10	pF
	$C_{i2}$	$STHR$ ( $STHL$ ), $T_A = 25^\circ\text{C}$		8	10	pF

<Test Condition>



Timing Requirements ( $T_A = -10$  to  $+75^\circ\text{C}$ ,  $V_{DD1} = 2.3$  to  $3.6$  V,  $V_{SS1} = 0$  V,  $t_r = t_f = 8.0$  ns)

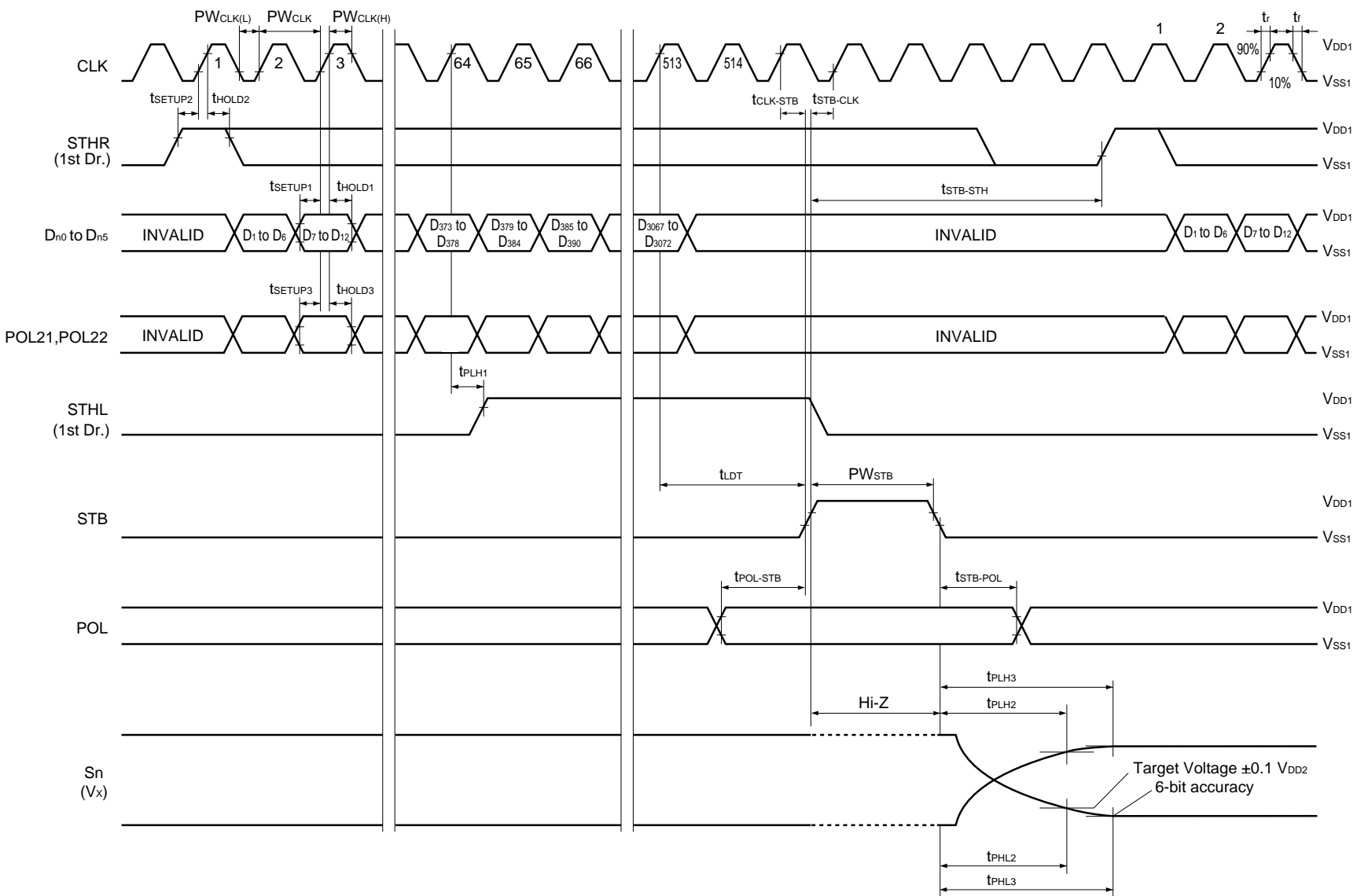
Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
★ Clock Pulse Width	$PW_{CLK}$	$2.3 \leq V_{DD1} < 3.0$ V	22			ns
		$3.0 \text{ V} \leq V_{DD1} \leq 3.6$ V	15			ns
★ Clock Pulse High Period	$PW_{CLK(H)}$		4			ns
★ Clock Pulse Low Period	$PW_{CLK(L)}$	$2.3 \leq V_{DD1} < 3.0$ V	6			ns
		$3.0 \text{ V} \leq V_{DD1} \leq 3.6$ V	4			ns
Data Setup Time	$t_{SETUP1}$		4			ns
Data Hold Time	$t_{HOLD1}$		0			ns
Start Pulse Setup Time	$t_{SETUP2}$		4			ns
Start Pulse Hold Time	$t_{HOLD2}$		0			ns
POL21,POL22 Setup Time	$t_{SETUP3}$		4			ns
POL21,POL22 Hold Time	$t_{HOLD3}$		0			ns
STB Pulse Width	$PW_{STB}$		2			CLK
Last Data Timing	$t_{LDT}$		2			CLK
CLK-STB Time	$t_{CLK-STB}$	$CLK \uparrow \rightarrow STB \uparrow$	6			ns
STB-CLK Time	$t_{STB-CLK}$	$STB \uparrow \rightarrow CLK \uparrow$ , $V_{DD1} = 2.3$ to $3.6$ V	9			ns
		$STB \uparrow \rightarrow CLK \uparrow$ , $V_{DD1} = 3.0$ to $3.6$ V	6			ns
Time Between STB and Start Pulse	$t_{STB-STH}$	$STB \uparrow \rightarrow STHR(STHL) \uparrow$	2			CLK
POL-STB Time	$t_{POL-STB}$	$POL \uparrow$ or $\downarrow \rightarrow STB \uparrow$	-5			ns
STB-POL Time	$t_{STB-POL}$	$STB \downarrow \rightarrow POL \downarrow$ or $\uparrow$	6			ns

**Remark** Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .



Switching Characteristic Waveform(R/L= H)

Unless otherwise specified, the input level is defined to be  $V_{IH} = 0.7 V_{DD1}$ ,  $V_{IL} = 0.3 V_{DD1}$ .



**11. RECOMMENDED MOUNTING CONDITIONS**

The following conditions must be met for mounting conditions of the μPD16732D.

For more details, refer to the **Semiconductor Device Mounting Technology Manual (C10535E)**.

Please consult with our sales offices in case other mounting process is used, or in case the mounting is done under different conditions.

μPD16732DN-xxx : TCP (TAB Package)

Mounting Condition	Mounting Method	Condition
Thermocompression	Soldering	Heating tool 300 to 350°C, heating for 2 to 3 seconds : pressure 100g (per solder)
	ACF (Adhesive Conductive Film)	Temporary bonding 70 to 100°C : pressure 3 to 8 kg/cm <sup>2</sup> : time 3 to 5 sec. Real bonding 165 to 180°C: pressure 25 to 45 kg/cm <sup>2</sup> : time 30 to 40 sec. (When using the anisotropy conductive film SUMIZAC1003 of Sumitomo Bakelite,Ltd).

**Caution** To find out the detailed conditions for mounting the ACF part, please contact the ACF manufacturing company. Be sure to avoid using two or more mounting methods at a time.

**NOTES FOR CMOS DEVICES****① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS**

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

**② HANDLING OF UNUSED INPUT PINS FOR CMOS**

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to  $V_{DD}$  or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

**③ STATUS BEFORE INITIALIZATION OF MOS DEVICES**

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

**Reference Documents****NEC Semiconductor Device Reliability/Quality Control System (C10983E)****Quality Grades On NEC Semiconductor Devices (C11531E)**

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