MP1048

Full Bridge CCFL Controller

The Future of Analog IC Technology

DESCRIPTION

The MP1048 is a fixed operating frequency inverter controller that controls four external N-Channel power MOSFETs in a full-bridge configuration. The inverter is designed to power up to 6 cold cathode fluorescent lamps (CCFLs) to backlight liquid crystal displays. Its full-bridge architecture converts unregulated DC input voltages to the nearly pure sine waves required to ignite and operate CCFLs.

For reliable lamp ignition, the operating frequency is set by an external resistor and during startup is temporarily swept toward the unloaded resonant frequency of the tank. Burst mode or analog mode dimming are controlled with an external analog signal. Built-in fault management features include an open lamp regulator, a transformer secondary peak current regulator and a dual-mode fault timer. The secondary over-current timeout can be shortened with external components. The MP1048 is available in TSSOP28 and SOIC28 packages.

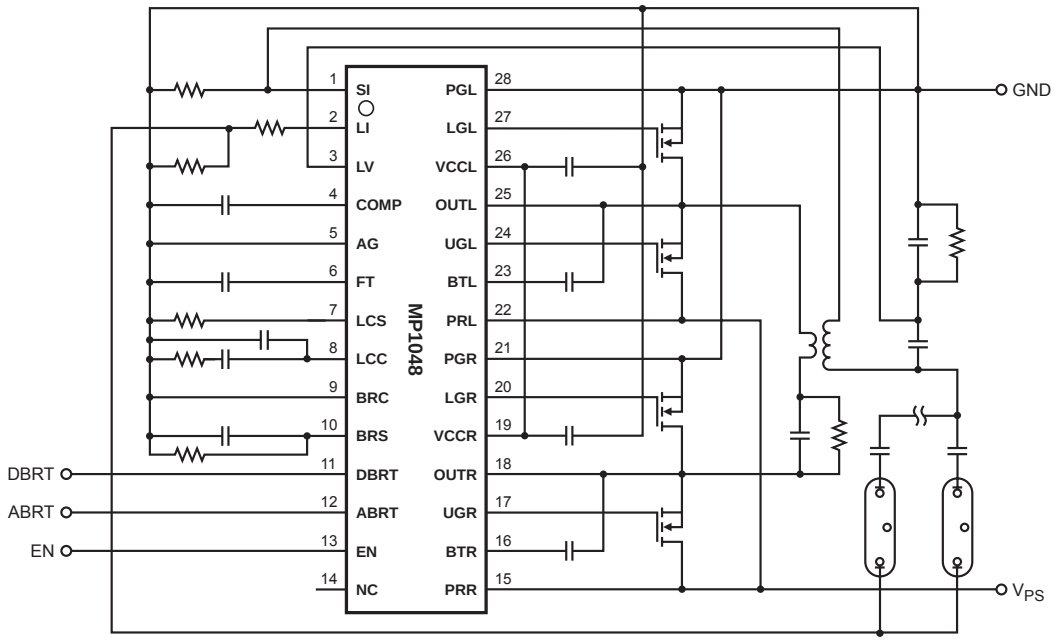
FEATURES

- Capable of Driving up to 6 Lamps
- Controls Four External, Low Cost, N-Channel MOSFETs
- Fixed Operating Frequency
- Input Voltage Range of 10V to 22V
- Lamp Current and Voltage Regulation
- Full-Wave Sense Amp
- Analog and Burst Mode Dimming Control
- Integrated Burst Mode Oscillator and Modulator
- Soft-On and Soft-Off Burst Envelope
- Open Lamp Protection
- Secondary Over-Current Protection
- Dual-Mode Fault Timer
- Available in TSSOP28 and SOIC28 Packages

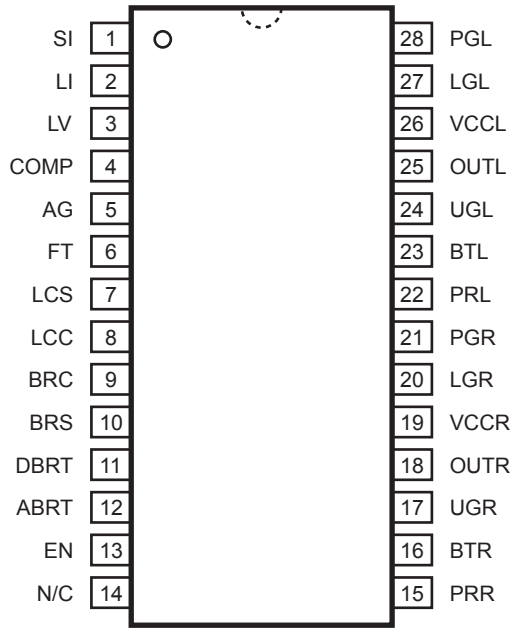
APPLICATIONS

- Desktop LCD Flat Panel Displays
- Monitors

TYPICAL APPLICATION



PACKAGE REFERENCE



Part Number*	Package	Temperature
MP1048EM	TSSOP28	–20°C to +85°C
MP1048EY	SOIC28	–20°C to +85°C

* For Tape & Reel, add suffix –Z (eg. MP1048EM–Z)
For RoHS Compliant Packaging, add suffix –LF
(eg. MP1048EM–LF–Z)

ABSOLUTE MAXIMUM RATINGS (1)

Input Voltage V_{PRR}, V_{PRL} 24V
Logic Inputs .....–0.3V to +6.5V
Inputs SI, LI, LV .....–5V to +5V
Junction Temperature.....150°C
Power Dissipation..... 0.6W
Junction Temperature.....150°C
Lead Temperature (Solder) .....260°C
Operating Frequency..... 150KHz
Storage Temperature .....–55°C to +150°C

Recommended Operating Conditions (2)

Input Voltage V_{PRR}, V_{PRL} ..... 10V to 22V
Analog Brightness Voltage V_{ABRT}..... 0V to 1.2V
Digital Brightness Voltage V_{DBRT}..... 0V to 1.2V
Enable Voltage V_{EN}..... 0V to 5.0V
Operating Frequency..... 20KHz to 100KHz
Operating Frequency (Typical) 60KHz
Operating Temperature .....–20°C to +85°C

Thermal Resistance (3)

	θ_{JA}	θ_{JC}	
TSSOP28	82	20	°C/W
SOIC28	60	30	°C/W

Notes:
1) The device is not guaranteed to function outside of its operating conditions.
2) Exceeding these ratings may damage the device.
3) Measured on approximately 1" square of 1 oz copper.

ELECTRICAL CHARACTERISTICS

V_{PRR} = V_{PRL} = 17.5V, V_{BRC} = V_{LCC} = GND, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Output						
Gate Pull-Down	R_{GD}			2.0		Ω
Gate Pull-Up	R_{GU}			20		Ω
Damper On Resistance	R_{ON}			1.2		kΩ
EN						
Threshold	V_{TH}			1.2	2.0	V
Hysteresis	V_{TH_HYS}			0.3		V
Sync Timing						
DBRT Logic Input Threshold	V_{TH}	V_{BRS} = V_{CC}	1.8	2.0	2.3	V
DBRT Logic Input Hysteresis	V_{TH_HYS}	V_{BRS} = V_{CC}		0.2		V
Burst Rate Generator						
Source Current	$I_{SRC(BRS)}$	V_{BRS} = 2V	125	150	175	µA
Lower Threshold	$V_{V(BRS)}$		2.2	2.35	2.5	V
Upper Threshold	$V_{P(BRS)}$		3.2	3.4	3.6	V

ELECTRICAL CHARACTERISTICS *(continued)*

V_{PRR} = V_{PRL} = 17.5V, V_{BRC} = V_{LCC} = GND, T_A = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply Current						
Supply Current (Enabled)	I_{PR}			2.2	3	mA
Supply Current (Disabled)	I_{PR}			3	25	µA
Operating Frequency	f_0	R3 = 100kΩ	45	49	53	KHz
Accuracy of f_0				3	8	%
Frequency Set Voltage	V_{LCS}		1.13	1.18	1.23	V
Lamp Current Feedback						
Magnitude	$\|V_{LI}\|$	V_{ABRT} > 1.2V	1.134	1.20	1.266	V
		V_{ABRT} = 0V	0.35	0.40	0.45	
Accuracy	V_{LI}			3		%
Input Resistance	R_{LI}	V_{LI} < 0V		60		kΩ
Open Lamp Voltage Feedback Threshold (Peak)	$V_{TH(LV)}$		1.15	1.20	1.25	V
Secondary Peak Current Threshold	$V_{TH(SI)}$		1.15	1.20	1.25	V
Fault Timer						
Threshold	$V_{t(FT)}$		1.15	1.20	1.25	V
Sink Current	$I_{SINK(FT)}$			–1		µA
Open Lamp Source Current	$I_{SO(FT)+}$			1		µA
Secondary Over-Current Source Current	$I_{SP(FT)+}$			65		µA
Comp						
Clamp Voltage	V_{COMP}			0.62		V
Reference Current	I_{COMP+}			20		µA
Decay Current	I_{COMP-}	End of Burst		20		µA
Output (VCCR and VCCL)						
Voltage	V_{CC}		5.7	6.0	6.3	V
Current	I_{CC}			5		mA

PIN FUNCTIONS

Pin #	Name	Description
1	SI	Secondary Current Feedback Input. Connect a current sense resistor from the cold end of the secondary winding to ground. Connect this pin to the junction of the resistor and the secondary winding. If the voltage at SI exceeds +1.2V, a pulse of current will pull down on the COMP pin in an attempt to regulate the secondary current and the Fault Timer will be started.
2	LI	Lamp Current Feedback Input. Connect this pin to the cold end of the lamp and shunt a sense resistor to ground. The sense amplifier will sink a current from the COMP pin that is proportional to the absolute value of the voltage at this pin. (In regulation the average of the absolute value of the voltage at this pin is determined by the voltage at the ABRT pin).
3	LV	Lamp Voltage Feedback Input. Connect a capacitive voltage divider from the hot end of the lamp to ground. Connect this pin to the tap on the divider and shunt a bias resistor to ground. If the voltage at LV exceeds +1.2V, a pulse of current will pull down on the COMP pin to attempt to regulate the lamp voltage and the Fault Timer will be started.
4	COMP	Feedback Compensation Node. Connect a compensation capacitor from this pin to ground.
5	AG	Analog Ground.
6	FT	Fault Timing. Connect a timing capacitor from this pin to AG to set the fault timeout period.
7	LCS	Lamp Operating Clock Set. Connect a resistor from this pin to AG. This resistor sets the operating frequency of the MP1048.
8	LCC	Lamp Clock Control. LCC provides compensation when the operating clock is swept in order to strike the lamp. Connect a resistor in series with a capacitor from LCC to AG. Connect a smaller capacitor directly from LCC to AG. Connect only a single capacitor to AG, if some sweeping of the operating clock can be tolerated during open lamp conditions. Connect LCC to AG to force the operating clock to the selected value at all times.
9	BRC	Burst Repetition Rate Control. Connect BRC to AG.
10	BRS	Burst Repetition Rate Setting. If the burst repetition rate is to be synchronized to an external clock, connect a capacitor from BRS to AG. If the burst rate generator is free-run and will not be synchronized with an external clock, connect a resistor in parallel with a capacitor from BRS to AG. If the burst is to be controlled by an external logic signal, connect BRS to VCC and apply the logic signal to the DBRT pin.
11	DBRT	Burst-Mode (Digital) Brightness Control Input. The voltage range of 0V to 1.2V at DBRT linearly sets the burst-mode duty cycle from minimum 10% to 100%. If burst dimming is not used, tie DBRT to VCC.
12	ABRT	Analog Brightness Control Input. The voltage range of 0V to 1.2V at ABRT sets the 3:1 dimming range for the lamp current. If analog dimming is not used, tie ABRT to VCC.
13	EN	Enable Input. Pull EN high to turn on the MP1048; low to turn it off.
14	NC	No Connect.
15	PRR	Input Power Rail, Right-Side. Connect PRR directly to the drain of the high-side, right-side, external power MOSFET.
16	BTR	Output Bootstrap, Right-Side. BTR provides gate bias for the right-side high-side MOSFET. Connect a capacitor from BTR to OUTR.
17	UGR	High-Side MOSFET Gate Output, Right-Side. Connect UGR to the gate of the high-side, right-side, external power MOSFET.
18	OUTR	Bridge Output, Right-Side. Connect OUTR to the source of the right-side, high-side MOSFET and the drain of the low-side, right-side MOSFET.
19	VCCR	Voltage Rail Output, Right-Side. VCCR allows bypassing the bias supply for the control circuitry. Bypass VCCR with a 0.47µF capacitor. Connect to VCCL.

PIN FUNCTIONS *(continued)*

Pin #	Name	Description
20	LGR	Low-Side MOSFET Gate Output, Right-Side. Connect LGR to the gate of the low-side, right side MOSFET.
21	PGR	Power Ground, Right-Side. Connect PGR to the source of the low-side, right-side MOSFET.
22	PRL	Input Power Rail, Left-Side. Connect PRL directly to the drain of the high-side, left-side, external power MOSFET.
23	BTL	Output Bootstrap, Left-Side. BTL provides gate bias for the left-side high-side MOSFET. Connect a capacitor from BTL to OUTL.
24	UGL	High-Side MOSFET Gate Output, Left-Side. Connect UGL to the gate of the high-side, left side, external power MOSFET.
25	OUTL	Bridge Output, Left-Side. Connect OUTL to the source of the left-side, high-side MOSFET and the drain of the left-side, low-side MOSFET.
26	VCCL	Voltage Rail Output, Left-Side. VCCL allows bypassing the bias supply for the control circuitry. Bypass VCCL with a 0.47µF capacitor. Connect to VCCR.
27	LGL	Low-Side MOSFET Gate Output, Left-Side. Connect LGL to the gate of the low-side, left side MOSFET.
28	PGL	Power Ground, Left-Side. Connect PGL to the source of the low-side, left-side MOSFET.

OPERATION

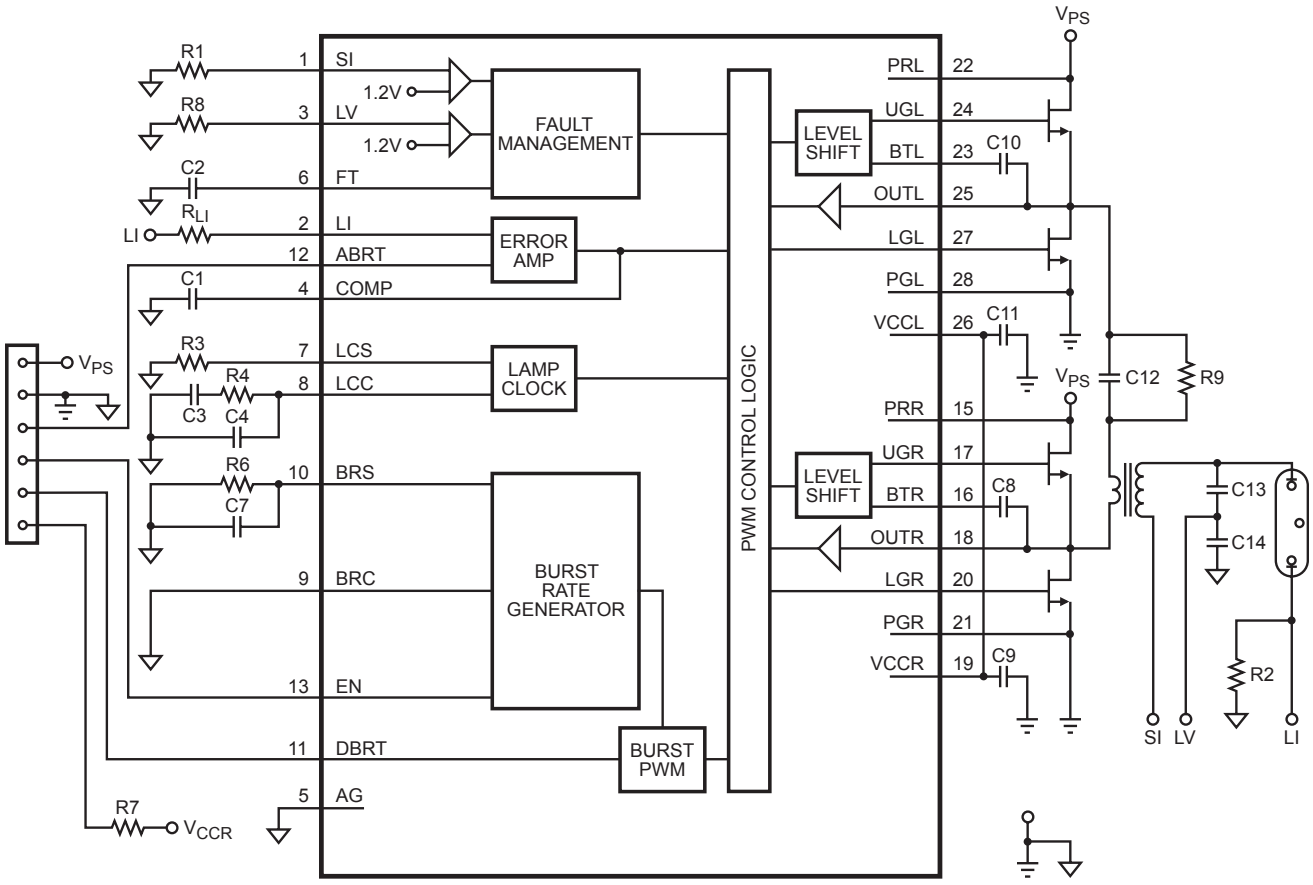


Figure 1—Functional Block Diagram

DESIGN INFORMATION

The MP1048 is a fixed operating frequency inverter controller specifically designed to drive up to 6 cold cathode fluorescent lamps (CCFLs) used as a backlight for liquid crystal displays. Designed to run off 10V to 22V input supplies, the MP1048 can drive up to 6 lamps via four (4) external N-Channel MOSFETs. Its full bridge architecture converts unregulated DC input voltages to the nearly pure sine waves required to ignite and operate CCFLs. The operating frequency is set by an external resistor to minimize the possibility of interference with the refresh rate of the display.

To ensure ignition of the lamp, the operating frequency is swept temporarily to the unloaded resonant frequency of the tank. Regulated lamp current and maximum peak transformer secondary current are set by external resistors. Regulated open lamp voltage is set by an external capacitive voltage divider. Soft startup of the lamp minimizes the peak transformer secondary voltage. The MP1048 implements burst mode dimming of the lamp and features soft-on/soft-off control of the lamp current envelope that is virtually independent of supply voltage.

Burst repetition rate and duty cycle can either be determined by driving the MP1048 with an external logic signal or by choosing an external resistor and capacitor to set the burst rate and modulating the duty cycle with a DC control voltage on D_{BRT}.

Loop gain is compensated for variations in supply voltage and the full-wave lamp current sense amplifier provides superior output pulse symmetry, loop response time and phase margin.

Careful management of limit conditions provides graceful reduction of lamp power at low supply voltages but allows the loop to recover quickly from an abrupt step in supply voltage. System fault management facilities include an on-chip open-lamp regulator, a transformer secondary peak current regulator and a dual-mode fault timer.

By regulating the peak current in the transformer secondary winding, UL1950 can be met for most systems. When the MP1048 is regulating open lamp voltage, it ignores the burst control and runs continuously to ensure either the lamp has a chance to re-ignite or the fault timer can smoothly and accurately time out. If the MP1048 detects an open lamp condition for a time that exceeds the timer interval, it will shutdown until the part is turned off and then turned on again. Similarly, the MP1048 will shutdown if it detects an over-current condition in the secondary for about 2% of the open lamp timer interval. If required, the secondary over-current timeout can be shortened with external components. On-chip current limit protects the MP1048 in case of output fault conditions.

FEATURE DESCRIPTION

All reference designators refer to the MP1048 Block Diagram, unless otherwise designated.

High Efficiency Operation

There are two major power losses in a CCFL inverter: switching loss of switches and copper loss of the transformer winding. To reduce switching loss, Zero Current Switching (ZCS as described in US patent 6,114,814) or Zero Voltage Switching (ZVS) are commonly implemented.

As shown in Figure 2, ZCS and ZVS require primary current I_{PRI} lagging primary voltage V_{PRI}. With ZVS, since D1 can only conduct at the negative phase of I_{PRI}, the beginning of A & D conduction will only happen at the negative phase of I_{PRI}.

Higher phase delay will lead to higher primary RMS current and therefore higher transformer temperature. With ZCS, A & D conduction starts at the zero crossing of I_{PRI}.

The MP1048 does not utilize ZVS or ZCS. It implements fast switching to reduce switching loss and operates at the condition that I_{PRI} and V_{PRI} are in phase to reduce primary RMS current. Therefore, higher efficiency than ZVS or ZCS is achieved.

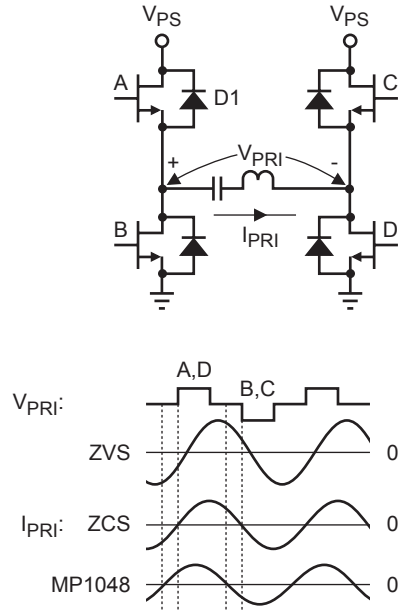


Figure 2—V_{PRI} vs. I_{PRI}

Brightness Control

The MP1048 can operate in four modes: Analog Mode, Burst Mode with a DC input, Burst Mode with an external PWM or Analog and Burst Mode. The four modes are dependent on the pin connections defined under Pin Functions.

Choosing the required burst repetition frequency can be achieved by an RC combination as defined in component selection. The MP1048 has a soft-on and soft-off feature to reduce noise when using burst mode dimming. Analog dimming and Burst dimming are independent of each other and may be used together to obtain a wider dimming range.

Table 1—Function Modes

Function	Pin Connection			
	ABRT	DBRT	BRS	Ratio
Analog Mode	0 – 1.2V	V_{CC}	V_{CC}	3:1
Burst Mode with DC Input Voltage	V_{CC}	0 – 1.2V	R6 C7	10:1
Burst Mode with External Source	V_{CC}	PWM	V_{CC}	Set by Customer
Analog and Burst Mode	0 – 1.2V	0 – 1.2V	R6 C7	30:1
Analog and Burst Mode with External Source	0 – 1.2V	PWM	V_{CC}	Set by Customer

Brightness Polarity
Burst: 100% duty cycle is at 1.2V
Analog: 1.2V is for maximum brightness

Fault Protection

Open Lamp: The LV pin (#3) is used to detect whether an open lamp condition has occurred. If the voltage at LV exceeds +1.2V, a pulse of current will pull down on the COMP pin to regulate the lamp voltage. The Fault Timer will be started with a 1μA current source injecting into C2 at the FT pin, while the fault condition persists. If the voltage at the FT pin exceeds 1.2V, then the chip will shutdown.

Excessive Secondary Current (Shorted Lamp): The SI pin (#1) is used to detect whether excessive secondary current has occurred. If a fault condition occurs that increases the secondary current, then the voltage at SI will be greater than 1.2V. A pulse of current will pull down on the COMP pin to regulate the secondary current. The Fault Timer will be started with a 65μA current source injecting into C2 at the FT pin while the fault condition persists.

If the voltage at the FT pin exceeds 1.2V, then the chip will shutdown and need to be enabled again.

Fault Timer: The timing for the fault timer will depend on the sourcing current as described above and the capacitor C2 on the FT pin. The user can program the time for the voltage to rise after the chip detects a “real” fault. When a fault is triggered, the internal voltage (V_{CC}) will collapse from 6V to 0V. If no fault is detected a 1μA current sink will keep FT to 0V.

Startup

For reliable ignition of the lamp, the operating frequency is swept temporarily toward the unloaded resonant frequency of the tank during startup. This guarantees the strike voltage of the lamp at any temperature due to a resonant topology for switching the outputs and eliminates the need for external ramp timing circuits to ensure startup. Once the strike voltage is achieved, the switching frequency is gradually adjusted to the preset fixed value. The operating frequency before the lamp strikes can be swept as much as 160% of the preset frequency value.

Chip Enable

The chip has an ON/OFF function, which is controlled by the EN pin (#13). The enable signal goes directly to a Schmitt trigger. The chip will turn ON with an EN = High and OFF with an EN = Low.

APPLICATION INFORMATION

Pin 1 (SI), R1:

Secondary Short Protection: R1 is used for feedback to the SI pin to detect excessive secondary current. The value for R1 is calculated as 1.2V divided by the secondary peak current.

Pin 2 (LV): C13, C14 and R8:

Open Lamp protection: The regulated open lamp voltage is proportional to the C14 and C13 ratio. C13 has to be rated at 3kV and is typically between 5pF to 22pF. The value of C14 is set by the customer to achieve the required open lamp voltage detection value.

$$C14 = C13 \times 1.18 \times V_{(MAX)}\text{rms}$$

The value of bias resistor R8 is typically 100kΩ (not critical).

Pin 2 (LI), R2:

Lamp Current Regulation: R2 is used for feedback to the LI pin to regulate the lamp current. The value for R2 is calculated as 1.33V divided by the lamp rms current (assuming V_{ABRT} is greater than 1.2V). For a RMS 6mA lamp current, the R2 value is 220Ω.

Pin 6 (FT), C2:

C2 is used to set the fault timer. This capacitor will determine when the chip will reach the fault threshold value.

Open Lamp Time Out:

$$C2\,(nF) = \frac{t_{OPEN\,LAMP} \times 1\mu A}{1.2V}$$

For C2 = 820nF, then the timeout for open lamp will be 0.98 sec.

Secondary Over Current Timeout: When the MP1048 is regulating secondary over current (SI feedback), the source current in the Fault Timer (FT) cap is approximately 65µA. This causes the SI timeout to be about 1/65 of the Open Lamp (LV) timeout. To reduce the SI timeout further, modify the network at the FT pin as shown in Figure 3.

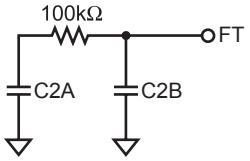


Figure 3—Timeout Adjustment

For a C2B = 10nF, then the time out for secondary short will be 0.2ms.

Note: The open lamp time out will remain the same value as defined by C2A.

Pin 7 (LCS), R3:

R3 is used to set the lamp operating clock. The value for R3 is calculated by

$$R3 = \frac{5e^9}{fo}$$

For R3 = 100kΩ, operating clock will be 50KHz.

Pin 8 (LCC):

This is the lamp clock control compensation pin and needs a lag lead lag capacitor/resistor network.

Pin 4 (COMP), C1:

C1 is the feedback compensation capacitor that connects between COMP and AG. A 1.5nF or 2.2nF cap is recommended. This cap should be X7R ceramic. The value of C1 affects the soft-on rise time and soft-off fall time.

Pin 18 (OUTR), Pin 25 (OUTL), C12, R9:

The OUTR and OUTL pins are used to sense the voltage at the output of the full bridge. They are also the point of access for the output dampers. OUTR and OUTL should make a Kelvin connection to the sources of the high-side MOSFETs and the drains of the low-side MOSFETs in the output bridge.

The primary transformer current flows through capacitor C12. Its value is typically 2.2µF. This capacitor should be ceramic and has a ripple current rating greater than the primary current. It is more optimal to use two parallel 1µF ceramic caps for minimal ESR losses. R9 is used to ensure that the bridge outputs are at 0V prior to startup. Typically R9 = 300Ω to 3kΩ.

Pin 16 (BTR), Pin 23 (BTL), C8, C10:
BTR and BTL are the bias supplies for the level shift of the upper MOSFETs. C8 and C10 should be 22nF and made of X7R ceramic material.

Pin 19 (VCCR), Pin 26 (VCCL), C9, C11:
These capacitors bypass the gate supply for the low-side switches. They also supply power to the MP1048. These pins should be bypassed with a 0.47µF ceramic X7R capacitor.

IMPORTANT–For all applications, VCCR and VCCL must be connected together.

Pin 11 (DBRT):
This pin is used for burst brightness control. The DC voltage on this pin will control the burst percentage on the output. The signal is filtered for optimal operation. A voltage ranging from 0V to 1.2V on DBRT will correspond to a Burst Duty Cycle of the minimum to 100% respectively.

For direct Pulse Width Modulation of the burst signal, connect BRS to VCC and connect DBRT with a logic level PWM signal. A logic High is Burst On and a logic Low is Burst Off.

Pin 10 (BRS): C7, R6:
BRS is used to set the Burst Repetition Rate. C7 and R6 will set the burst repetition rate and the minimum burst time: $t_{MIN.}$ Set t_{MIN} to achieve the minimum required system brightness. Ensure that t_{MIN} is long enough that the lamp does not extinguish.

These values are determined as follows:

Select a Minimum Duty Cycle, D_{MIN}, where:

$$D_{MIN} = t_{MIN} \times f_{Burst}$$

$$D_{MIN} = \frac{t_{FALL}}{(t_{FALL} + t_{RISE})}$$

If operating in Free-Running mode:

$$R6 = \frac{\frac{\left(\frac{1}{D_{MIN}} - 1\right)Vbg}{\xi} + \frac{V_P + V_V}{2}}{I_b}$$

$$R6 \sim 21.16k\left(\frac{1}{D_{MIN}} - 1\right) + 21.43k$$

For D_{MIN}=0.1 and R6=212kΩ

$$C7 = \frac{1 - D_{MIN}}{f_b \times R6 \times \gamma}$$

For D_{MIN}=0.1, R6=212k, f_b=200Hz, then C7=52nf:

Where D_{MIN}=Minimum Burst Duty Cycle, $Vbg=V_P - V_V$ (~1.2V), V_P=peak BRS voltage (~3.6V), V_V = valley BRS voltage (~2.4V) and f_b=burst repetition rate.

$$\gamma = \ln\left(\frac{3.6}{2.4}\right) \approx 0.405$$

ESD Resistor
It is recommended that a resistor (R_{LI} = 1kΩ) be added in series with the lamp current feedback as shown in Figure 4.

The addition of this resistor helps minimize the possibility of ESD damage in case of mishandling of the IC during board level assembly and test.

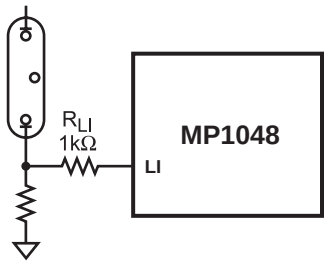
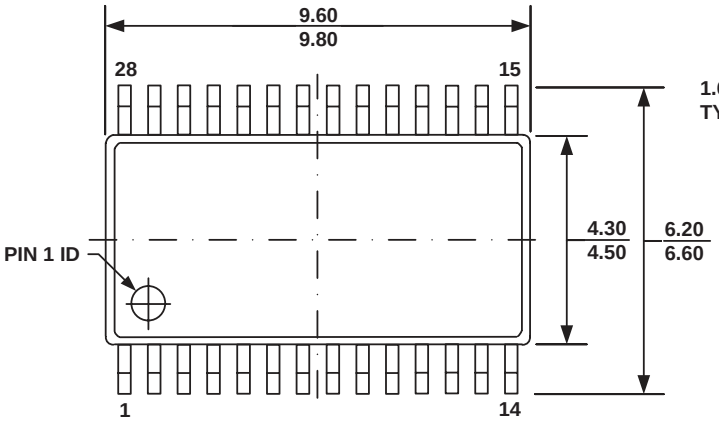


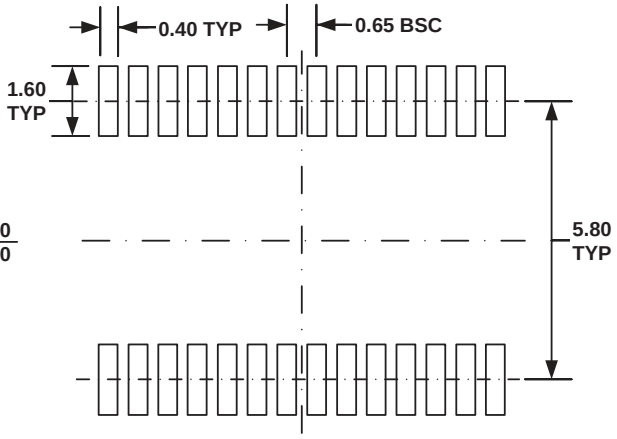
Figure 4—ESD Resistor

PACKAGE INFORMATION

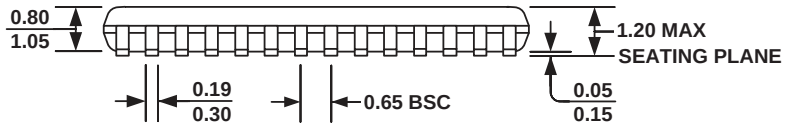
TSSOP28



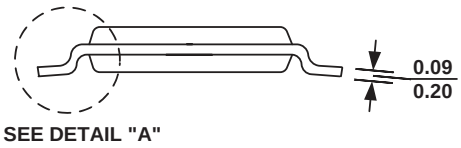
TOP VIEW



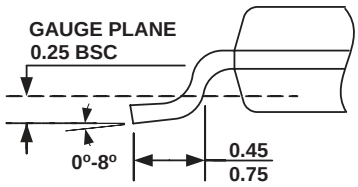
RECOMMENDED LAND PATTERN



FRONT VIEW



SIDE VIEW

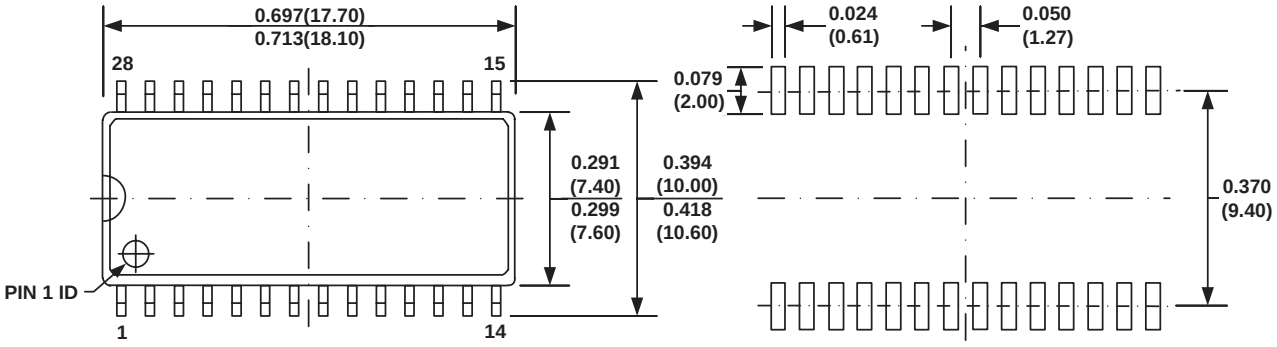


DETAIL A

NOTE:

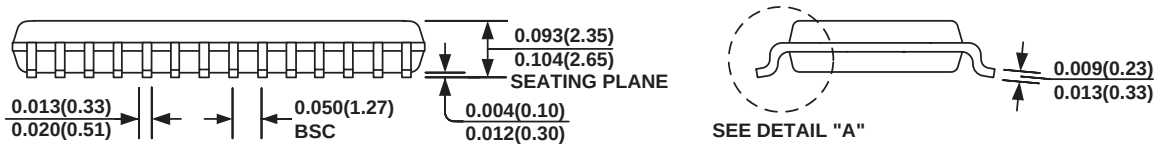
1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AE.
6) DRAWING IS NOT TO SCALE.

SOIC28



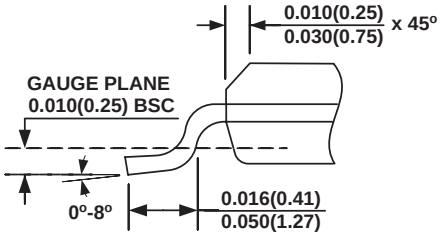
TOP VIEW

RECOMMENDED LAND PATTERN



FRONT VIEW

SIDE VIEW



DETAIL "A"

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX.
5) DRAWING CONFORMS TO JEDEC MS-013, VARIATION AE.
6) DRAWING IS NOT TO SCALE.