PLEASE NOTE: The SMB118 has entered End-of-Life.

SMB118/218

Six-Channel Programmable DC-DC Power Managers with Battery Charger

FEATURES & APPLICATIONS

- **Digital programming of all major parameters via I²C interface and non-volatile memory**
  - **Output voltage setpoint/margining**
  - **Sequencing & digital soft start**
  - **Enable/Disable outputs independently**
  - **Input/Output UV/OV voltage thresholds**
  - **PWM/PFM mode**
- **Six programmable regulator channels with 1.5% accuracy**
  - **Three synchronous step-down (Buck) with internal PFETs**
  - **One configurable step-up (Boost) or synchronous step-down (Buck)**
  - **One step-up (Boost)**
  - **One adjustable output voltage LDO**
- **Programmable Linear Li-Ion Battery Charger**
  - **Precharge/fast charge/termination current**
  - **Fast Charge voltage threshold**
  - **Float Voltage**
- **+2.7V to +6.0V Input Range (Higher system voltages supported)**
- **Built-in current limiting, UV/OV, and thermal protection**
- **Highly accurate reference and output voltage**
- **1MHz PWM frequency and power-saving automatic PFM mode**
- **96 bytes of user configurable nonvolatile memory**

Applications

- **Portable Media Players**
- **Digital camcorders/still cameras**
- **Smart PDA/Camera phones**
- **Handheld GPS/PDA's**
- **TFT-LCD Displays/Monitors/TVs**

INTRODUCTION

The SMB118 and SMB218 are highly integrated and flexible six-channel power managers designed for use in a wide range of portable applications. The built-in digital programmability allows system designers to custom tailor the device to suit almost any multi-channel power supply application from digital camcorders to mobile phones.

The SMB118 and SMB218 integrate all the essential blocks required to implement a complete seven-channel power subsystem including three synchronous step-down "Buck" converters, one configurable step-up "Boost" or step-down synchronous "Buck" converter, one step-up "Boost" converter, one linear regulator (LDO) and a fully programmable Li-Ion battery charger. Additionally sophisticated power control/monitoring functions required by complex systems are built-in. These include digitally programmable output voltage setpoint, power-up/down sequencing, enable/disable, margining and UV/OV input/output monitoring on all channels.

The integration of features and built-in flexibility of the SMB118 and SMB218 allows the system designer to create a "platform solution" that can be easily modified via software without major hardware changes. Combined with the re-programmability of the SMB118 and SMB218, this facilitates rapid design cycles and proliferation from a base design to futures generations of product.

The SMB118 and SMB218 are suited to battery-powered applications with an input range of +2.7V to +6.0V and provide a very accurate voltage regulation. Communication is accomplished via the industry standard I²C bus. All user-programmed settings are stored in non-volatile EEPROM of which 96 bytes may be used for general-purpose memory applications. The commercial operating temperature range is 0C to +70C, the industrial operating range is –40C to +85C, and the available package is a 48-pad 7mm x 7mm QFN.

SIMPLIFIED APPLICATIONS DRAWING

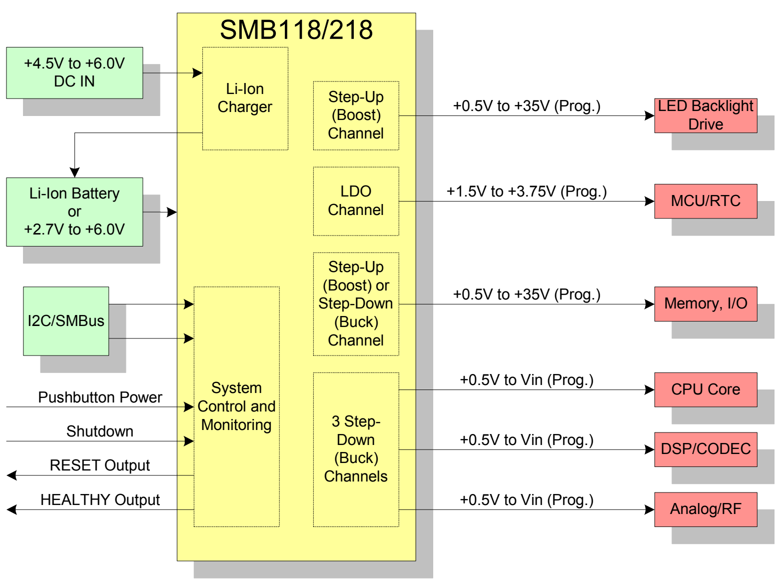


Figure 1 – Applications block diagram featuring the SMB118/218 six-channel, programmable DC/DC converters. These integrated power supply and battery managers provide precision regulation, monitoring, cascade sequencing, output margining and battery charging.

GENERAL DESCRIPTION

The SMB118 and SMB218 are fully programmable power supply and battery managers that regulate, sequence, monitor, and margin, an entire power subsystem while controlling the charging of a lithium-ion battery pack. They feature 6 voltage outputs, consisting of: three synchronous PWM “Buck” step-down converters, one configurable PWM “Boost or Buck” converter, one PWM “Boost” step-up converter, one Low Dropout (LDO) linear regulator, and a fully programmable Li-Ion battery charger.

The SMB118 and SMB218 regulate each of the six output channels to an accuracy of ±1.5% (typical). The output is individually programmed and can be reprogrammed via the I^2C interface. In addition, several sophisticated power management functions are built-in. The SMB118 and SMB218 are capable of power-on/off cascade sequencing where each channel can be assigned one of six sequence positions. Supplies may also be individually powered on/off through an I^2C command or by assertion of the enable pin. Cascade sequencing, unlike time based sequencing, uses feedback to ensure that each output is valid before the next channel is enabled.

Each output voltage and the battery are monitored for under-voltage and over-voltage conditions, using a comparator based scheme. In the event of a fault, all supplies may be sequenced down or immediately disabled. Multiple output status pins are provided to notify host processors or other supervisory circuits of system faults.

The SMB118 and SMB218 feature an Under-voltage Lockout (UVLO) circuit to ensure the IC will not power up until the battery voltage has reached a safe operating voltage. The UVLO function exhibits hysteresis, ensuring that noise on the supply rail does not inadvertently cause faults on the internally regulated supply.

In the event of a system fault, all monitored supplies may trigger fault actions such as power-off, or force-shutdown operations. Each output on the SMB118 and SMB218 may also be turned off individually at any point through an I^2C command or by a programmable enable pin.

When used in portable applications, the devices are powered from the main system battery. This input is continuously monitored for under-voltage conditions.

There are two under-voltage settings for this supply; both are user programmable and have a corresponding status pin. When the first threshold level is reached, the POWER_FAIL pin is asserted and latched. When the second threshold level is reached on the main supply, the nBATT_FAULT pin is asserted.

The SMB118 and SMB218 are equipped with three synchronous Buck outputs and one “Buck-or-Boost” output that use a 1MHz oscillator frequency. The feedback circuitry on each step-down channel is simplified by an internal programmable resistor divider (Buck-or-Boost uses external resistor divider).

The SMB118 and SMB218 are equipped with one Boost output that uses a 1MHz oscillator, and an asynchronous topology reducing the necessity for an additional external MOSFET driver. This Boost output also uses an external p-channel sequencing MOSFET to isolate load from the battery when not needed.

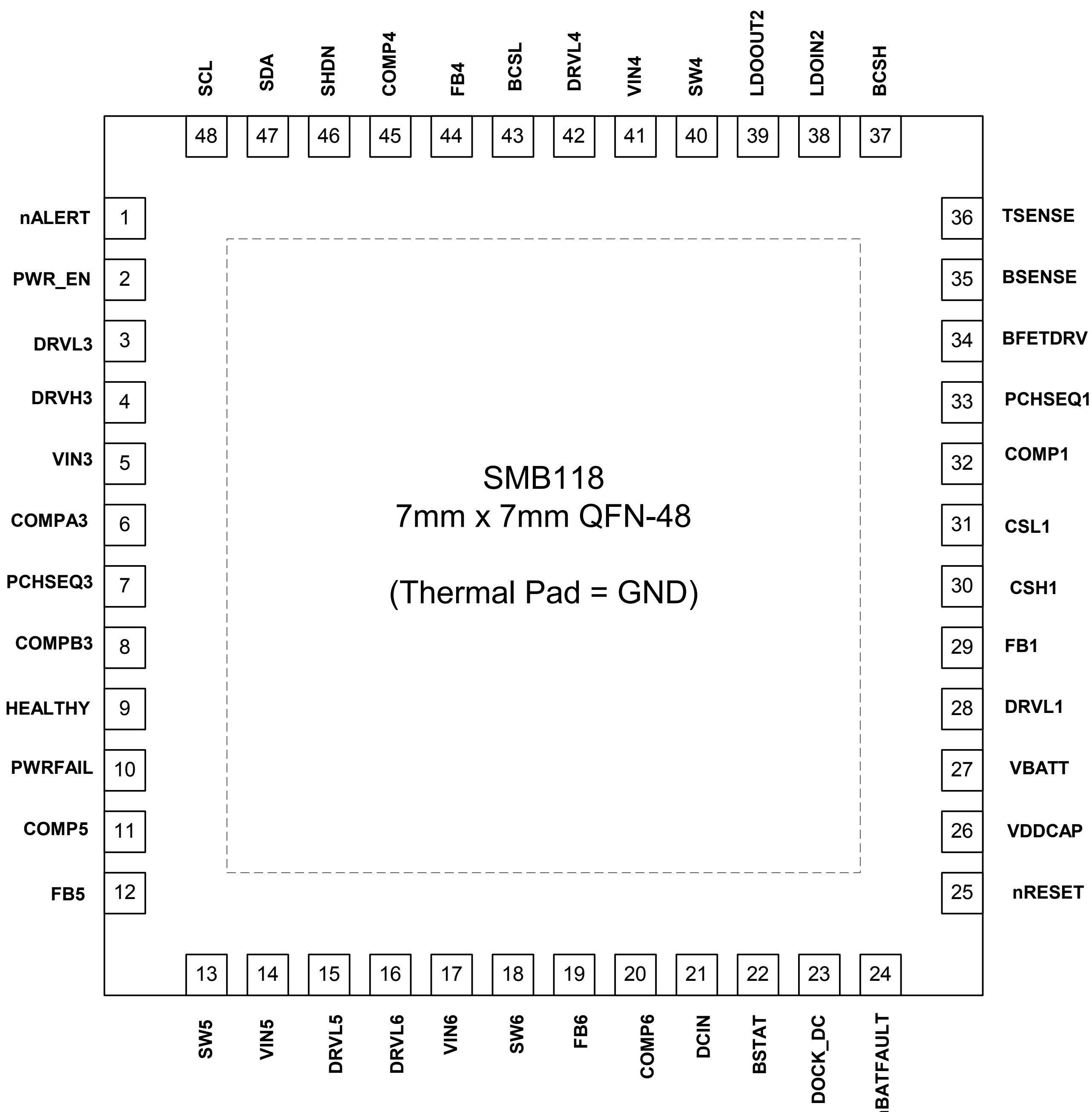
A Low Dropout (LDO) linear regulator with an adjustable 1.5V to 3.75V output provides a small dropout voltage and ripple free supply that is optimal for “always on” microcontrollers. The LDO has a separate input supply pin.

The SMB118 and SMB218 provide margining control over all of its output voltages. Through an I^2C command, all outputs can be margined by up to ±10% of the nominal output voltage. 7-level dynamic voltage management is also available for one of the channels. In addition, each output is slew rate limited by soft-start circuitry that is user programmable and requires no external capacitors.

All programmable settings on the SMB118 and SMB218 are stored in non-volatile registers and are easily accessed and modified over an industry standard I^2C serial bus. For fastest possible production times Summit offers an evaluation card and a Graphical User Interface (GUI).

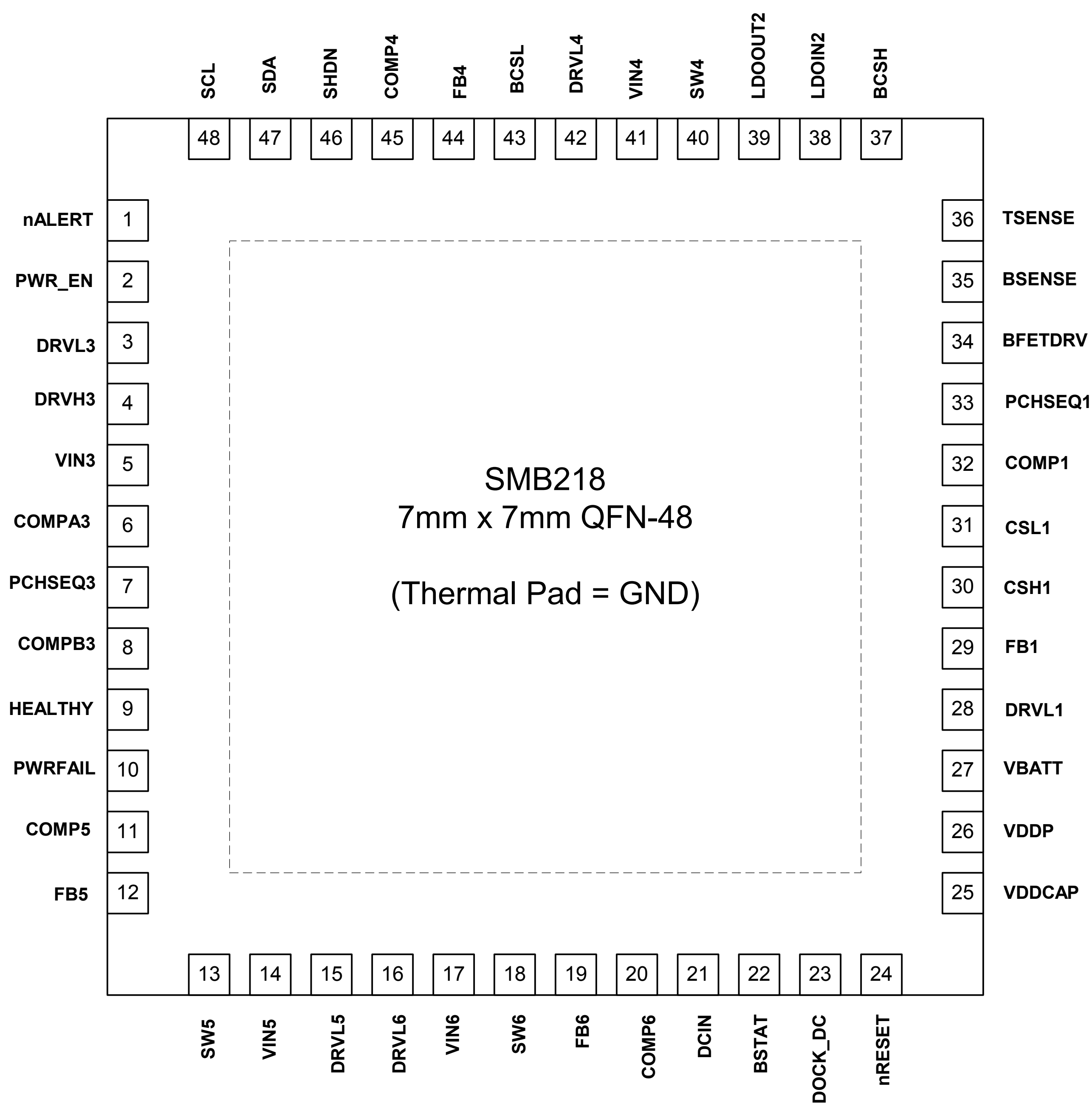
SMB118 PACKAGE AND PIN DESCRIPTION

SMB118
48-pad QFN
Top view



SMB218 PACKAGE AND PIN DESCRIPTION

SMB218
48-pad QFN
Top view



SMB118 TYPICAL APPLICATION

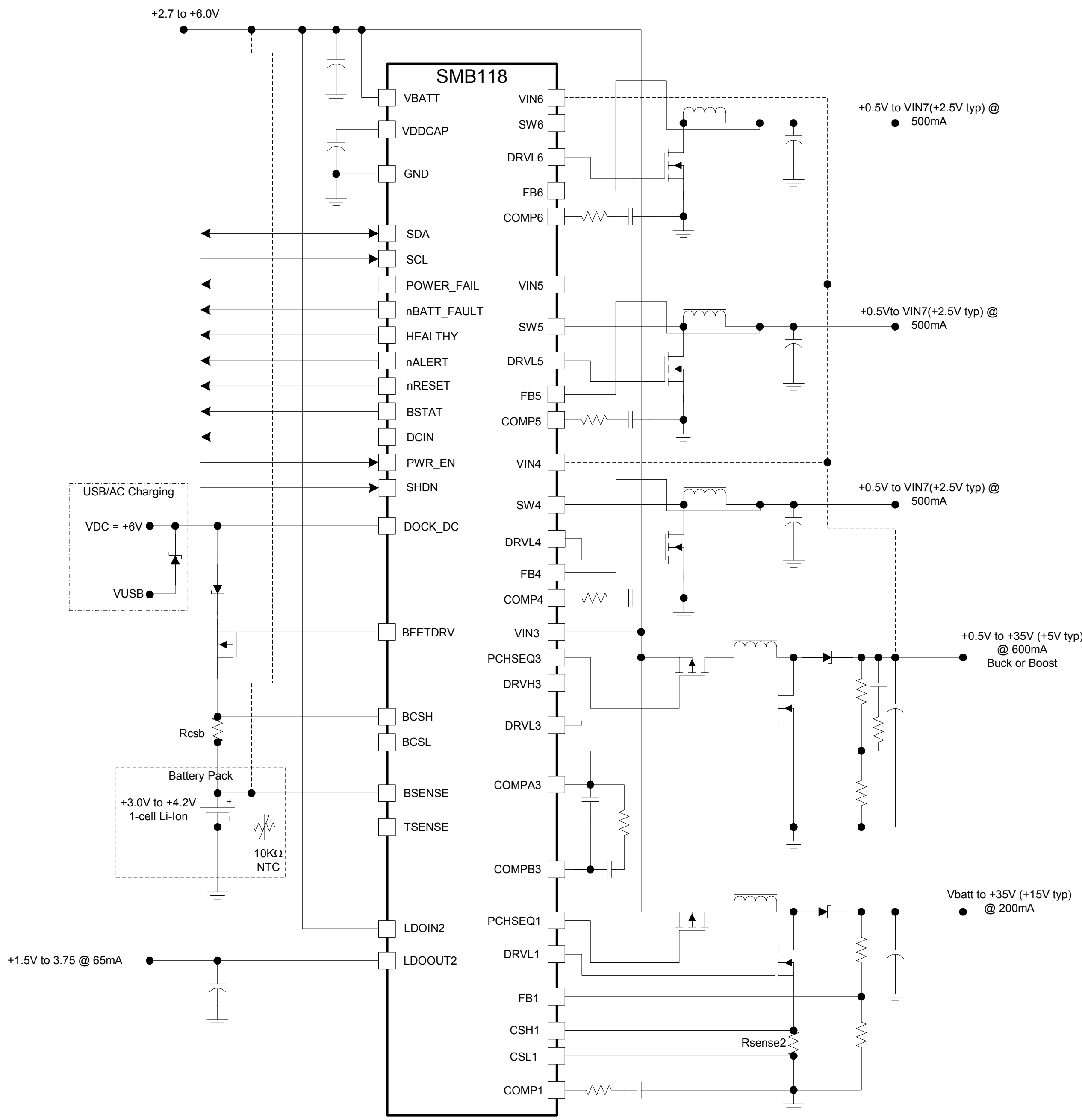


Figure 2a – Typical application schematic of the SMB118 (QFN-48) showing external circuitry necessary to configure the output channels as: step-up, LDO, step-down outputs and battery charger.

SMB218 TYPICAL APPLICATION

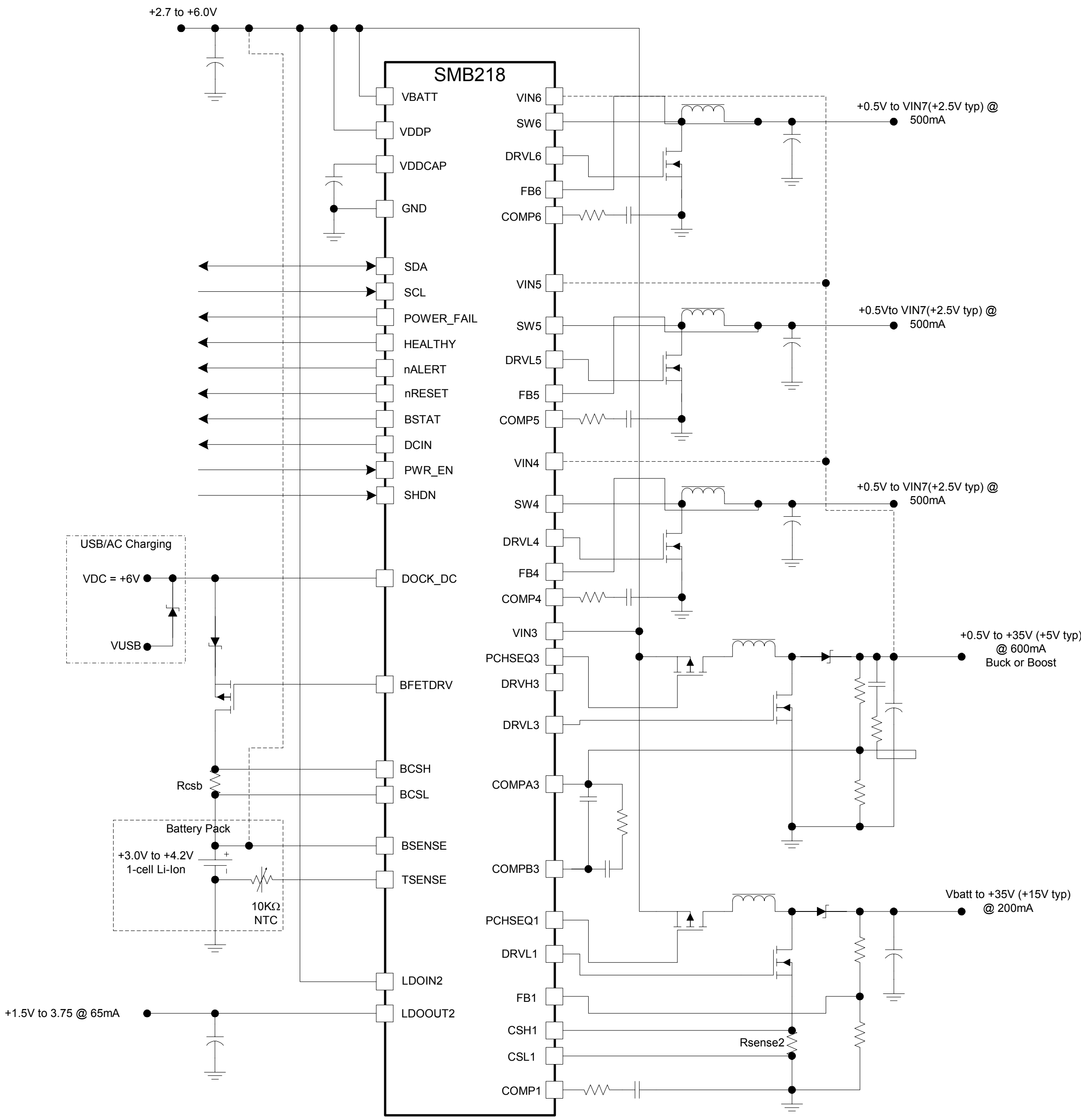


Figure 2a – Typical application schematic of the SMB218 (QFN-48) showing external circuitry necessary to configure the output channels as: step-up, LDO, step-down outputs and battery charger.

PIN DESCRIPTIONS

Pin #	Pin Name	Pin Type	Pin Description
1	nALERT	Output	Fault Interrupt – Latched, open-drain active low output. Flag for all fault conditions (multiplexed)
2	PWR_EN	Input	Enable input. PWR_EN is programmable to activate one or more channels. This pin can be programmed to latch and act as a debounced, manual push button input. Active high when level triggered, active low when used as a push- button input. A Software power-off command overrides this pin.
3	DRVL3	Output	Buck or Boost converter low-side drive – connect to NFET gate
4	DRVH3	Output	Buck converter high-side drive – connect to PFET gate (for Buck only)
5	VIN3	Power	Channel 3 controller power – Connect to +2.7V to +6.0V to supply internal FET drivers
6	COMPA3	Input	Buck or Boost Primary Compensation – Connect to R/C compensation network
7	PCHSEQ3	Output	Boost converter 3 sequence – connect to PFET gate for Boost channel on/off and sequencing. Must be tied to ground when unused.
8	COMPB3	Input	Buck or Boost Secondary Compensation – Connect to R/C compensation network
9	HEALTHY	Output	Output Monitor – Open drain active-high output asserts when all output channels are within UV/OV limits (ignoring disabled outputs)
10	POWER_FAIL	Output	Battery/Input Monitor. Detects low input voltage. Latched open-drain active high output. Associated threshold must be set higher than nBATT_FAULT threshold.
11	COMP5	Input	Buck converter 5 compensation pin – Connect to R/C compensation network
12	FB5	Input	Buck converter 5 feedback pin – Connect directly to output
13	SW5	Input/Output	Buck converter 5 switch pin – Connect to drains of NFET
14	VIN5	Power	Buck Converter 5 Power – Connect to +2.7V to +6.0V to supply internal PFET
15	DRVL5	Output	Buck converter 5 low-side drive – Connect to NFET gate
16	DRVL6	Output	Buck converter 6 low-side drive – Connect to NFET gate
17	VIN6	Power	Buck Converter 6 Power – Connect to +2.7V to +6.0V to supply internal PFET
18	SW6	Input/ Output	Buck converter 6 switch pin – Connect to drains of NFET
19	FB6	Input	Buck converter 6 feedback pin – Connect directly to output
20	COMP6	Input	Buck converter 6 compensation pin – Connect to R/C compensation network
21	DCIN	Output	DC Input Valid – Active high open drain indicates presence of DC input voltage (docking) with programmable threshold
22	BSTAT	Output	Battery Charger Status Output – Open Drain output asserts low when battery is charging and releases when charging is terminated/interrupted. Can be configured to blink while charging. When configured to blink, it will blink once every second while pre-charging and twice per second while fast and taper charging.
23	DOCK_DC	Power	Docking Connector Detector. DOCK_DC detects presence of external DC input and asserts DCIN pin. Provides power to the chip when greater than VBATT. Voltage on this pin must be greater than DOCK_DC trip point (programmable) for battery charging to be initiated. When voltage is present on DOCK_DC pin the SHDN pin is bypassed.
24	SMB118: nBATT_FAULT	Output	SMB118: Battery/Input Monitor. nBATT_FAULT detects low input voltage. Open-drain active low output. Associated threshold must be set lower than POWER_FAIL threshold.
	SMB218: nRESET	Output	SMB218: Reset Output. Releases with programmable delay after all selected outputs are valid (see UV/OV trip points). Open-drain active low output.

PIN DESCRIPTIONS (CONT.)

Pin Number	Pin Name	Pin Type	Pin Description
25	SMB118: nRESET	Output	SMB118: Reset Output. Releases with programmable delay after all selected outputs are valid (see UV/OV trip points). Open-drain active low output.
	SMB218: VDD_CAP	Power	SMB218: VDD Bypass – Connect to VDD bypass capacitor with 10uF capacitor.
26	SMB118: VDD_CAP	Power	SMB118: VDD Bypass – Connect to VDD bypass capacitor with 10uF capacitor.
	SMB218: VDDP	Power	SMB218: Power Input for the Boost Converter. Connect to +2.7V to +6.0V voltage source. Must be at same voltage as source of PFET for the Boost converter.
27	VBATT	Power	Power Input for Controller. Connect to +2.7V to +6.0V voltage source Bypass with a 0.1uF ceramic capacitor close to the pin
28	DRVL1	Output	Boost converter 1 low-side drive – Connect to NFET gate
29	FB1	Input	Boost converter 1 feedback pin – Connect to external resistor divider
30	CSH1	Input	Boost converter 1 current sense high – Connect to high side of sense resistor. This input is used to Kelvin sense the voltage across the current sense resistor.
31	CSL1	Input	Boost converter 1 current sense low – Connect to low side of sense resistor. This input is used to Kelvin sense the voltage across the current sense resistor.
32	COMP1	Input	Boost converter 1 compensation pin – Connect to R/C compensation network
33	PCHSEQ1	Output	P-Channel MOSFET sequencing pin. Connect to PFET gate for Boost channel on/off and sequencing. Internally connected to a 100uA current sink to pull PFET gate resistor from VDD to GND to enable sequencing. Tie to GND when unused.
34	BFETDRV	Output	Battery Charger FET Drive – Connects to gate of a PFET to control battery charging current
35	BSENSE	Input	Battery Voltage Sense – Connect directly to positive terminal of battery
36	TSENSE	Input	Battery Temperature Sense – Connect to “Temp” terminal of battery pack. This pin injects a programmable current into the NTC thermistor internal to the battery pack and measures the resulting current to detect temperatures. Place a 24.9K resistor, for 10K NTC, from this node to ground.
37	BCSH	Input	Charge Current Sense – Connect to high-side of charge current sense resistor. This input is used to Kelvin sense the voltage across the current sense resistor.
38	LDOIN2	Power	LDO Power Input – Connect to +2.7V to +6.0V to supply internal LDO
39	LDOOUT2	Input/ Output	LDO Output/Feedback
40	SW4	Input/ Output	Buck converter 4 switch pin – Connect to drains of NFET
41	VIN4	Power	Buck Converter 4 Power – Connect to +2.7V to +6.0V to supply internal PFET
42	DRVL4	Output	Buck converter 4 low-side drive – Connect to NFET gate
43	BCSL	Input	Charge Current Sense resistor. Connect to low side of charge current sense resistor. Do not attach to battery node at any other point.
44	FB4	Input	Buck converter 4 feedback pin – Connect directly to output
45	COMP4	Input	Buck converter 4 compensation pin – Connect to R/C compensation network
46	SHDN	Input	Shutdown – When high this input disables all functions of the SMB118 for low power operation. When voltage is present on the DOCK_DC input the part will exit the shutdown state, regardless of the state of the shutdown input.
47	SDA	Input/ Output	I^2C Data
48	SCL	Input	I^2C Clock
PAD (49)	DRVGND	Ground	Power Ground – Internally connect to under package pad. Connect to isolated PCB ground plane/flood

ABSOLUTE MAXIMUM RATINGS

Temperature Under Bias……………….-55°C to 125°C
Storage Temperature........................... -65°C to 150°C
Terminal Voltage with Respect to GND:
VBATT... -0.3V to +6.5V
VIN[7:5], LDOIN3........................... -0.3V to +6.5V
All Others .... -0.3V to +6.5V
Output Short Circuit Current 100mA
Lead Solder Temperature (10 s)......................... 300°C
Junction Temperature...150°C
ESD Rating per JEDEC……………………...……..2000V
Latch-Up testing per JEDEC………..…....……±100mA

RECOMMENDED OPERATING CONDITIONS

Commercial Temperature Range ....0°C to +70°C
Industrial Temperature Range .... -40°C to +85°C
VBATT..+2.7V to +6.0V
VIN[6:3], LDOIN2 ....+2.7V to +6.0V
DOCK_DC...+4.5V to +6.0V
48-lead 7x7 QFN Package Thermal Resistance (θ_{JA})
Die paddle not attached to PCB.......................... 53°C/W
Die paddle attached to PCB............................. 22.9°C/W
Moisture Classification Level 3 (MSL 3) per J-STD- 020

RELIABILITY CHARACTERISTICS

Data Retention .... 100 Years
Endurance ....100,000 Cycles

Note - The device is not guaranteed to function outside its operating rating. Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions outside those listed in the operational sections of the specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability. Devices are ESD sensitive. Handling precautions are recommended.

DC OPERATING CHARACTERISTICS

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
General						
V_{BATT}	Input supply voltage		+2.7		+6.0	V
VIN[6:3], LDOIN2	Regulator power supply voltage		+2.7		+6.0	V
V_{UVLO}	Under-voltage lockout voltage	V_{BATT} rising		2.3	2.4	V
		V_{BATT} falling		2.1		V
$I_{DD-ACTIVE}$	Active supply current	All regulators and monitors enabled – no load, V_{BATT} = 4.2V		3.3	4.5	mA
$I_{DD-STANDBY}$	Standby supply current	All regulators disabled, monitors active, V_{BATT} = 4.2V		135	300	µA
$I_{DD-SHUTDOWN}$	Shutdown supply current	All regulators and monitors disabled		0.6	5	µA
T_{SHDN}	Thermal shutdown temp			160		°C
T_{HYST}	Thermal shutdown temp hysteresis			20		°C
VDD_CAP	Voltage on VDD_CAP pin	All logic derived from this voltage, no load	2.4	2.5	2.6	V
f_{OSC}	Oscillator frequency (Note 1)	T = 0°C to +70°C	900	1000	1100	kHz
		T = -40°C to +85°C	850	1000	1150	

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Channel 1 – Step-up BOOST						
V_{OUT}	Voltage (nominal set point)	V_{BATT} = 4.2V, I_{LOAD} = 0A	VIN		+35	V
V_{FB}	Feedback Voltage Reference	Programmable in 4mV steps	0		1	V
ΔV_{FB}	Feedback Voltage Accuracy at FB[2:1] Pin (Note 2)	V_{FB}=0.836V	-3	±1	+3	%
g_m	Error amp transconductance			145		umho
I_{EA}	Error amp output drive			±20		µA
R_{CS}	CS amplifier transresistance	R_{SENSE} = 0.1Ω, R_{LOAD}=350mA		0.8		Ω
				1.6		
$I_{OL\text{-}SEQ}$	PCHSEQ pull down current	$V_{OL\text{-}SEQ}$ = 1V	60	100		µA
R_{DRVL}	LS Gate drive impedance	Output High		6.0		Ω
		Output Low		2.5		Ω
V_{cl}	Clamp threshold voltage	Programmable 1.0, 1.1, 1.2, 1.5V	1.0		1.5	V
V_{cl_acc}	Clamp threshold voltage Accuracy	Clamp threshold 1.0 and 1.5V		±5		%
D.C.	Duty Cycle	Maximum (clamp on)	85	90	98	%
		Minimum, PWM mode		16	30	%
Channel 2 – LDO						
V_{OUT}	Voltage (nominal set point)	LDOIN2=4.2V, I_{LOAD}=0A	+1.5		+3.75	V
ΔV_{OUT}	Voltage accuracy	LDOIN3=4.2V, I_{LOAD}=0A, V_{OUT}=2.5V	-2.5	±0.5	+2.5	%
ΔV_{LINE}	Line regulation	LDOIN2=4.2V, I_{LOAD}=0A		1		mV/V
ΔV_{LOAD}	Load regulation	Vo=2.5, Vin = 4.2V		1		mV/ mA
ΔV_{TRANS}	Load Transient Regulation	Step Load: 5mA to 50mA C_{OUT} = 10uF		50		mV
PSRR	Input Ripple Rejection	LDOIN2=3.8V, V_{OUT}=3.3V I_{LOAD}=50mA, $V_{P\text{-}P}$=200mV, F=1kHz		45		dB
I_{OUTMAX}	Maximum output Current	LDOIN2=3.2V, V_{OUT} = 2.5V	50	75		mA
V_{DO}	Dropout voltage	I_{LOAD}=50mA		150		mV

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Channel [6:4] – Step-down BUCK

V_{OUT}	Voltage (nominal set point)	VIN[6:4] 4.2V, I_{LOAD}=0A	+0.5		VIN	V
ΔV_{OUT}	Voltage accuracy	Note 2, V_{OUT} = 2.5V, T = -40°C to +85°C	-2	±1	+2	%
		Note 2, V_{OUT} = 1.2V, T = 0°C to +70°C	-2	±1	+2	%
V_{FB}	Feedback voltage reference range	Programmable in 4mV steps	0		1	V
g_m	Error amp transconductance			160		umho
I_{EA}	Error amp output drive			±20		µA
R_{CS}	CS amplifier transresistance	I_{LOAD} = 500mA		1.2		Ω
R_{HS}	HS Switch Resistance	I_{LOAD} = 500mA		320		mΩ
R_{DRVL}	LS Gate drive impedance	Output High		5.5		Ω
		Output Low		2.7		Ω
V_{cl}	Clamp threshold voltage	Programmable 1.0, 1.1, 1.2, 1.5V	1.0		1.5	V
V_{cl_acc}	Clamp threshold voltage Accuracy	Clamp threshold 1.0 and 1.5V		±5		%
D.C.	Duty Cycle	Maximum, V_{BATT} = 4.2V		100		%
		Minimum, PWM mode, V_{BATT} = 4.2V		15	30	%

DC OPERATING CHARACTERISTICS (CONTINUED)						
(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)						
Channel 3 – Step-down BUCK or Step-up BOOST						
V_{OUT}	Voltage (nominal set point, Buck)	V_{BATT}=4.2V, I_{LOAD}=0A	+0.5		+VIN	V
V_{OUT}	Voltage (nominal set point, Boost)	V_{BATT}=4.2V, I_{LOAD}=0A	+VIN		+35	V
V_{FB}	Feedback Voltage Reference range	Programmable in 4mV steps	0		1	V
ΔV_{FB}	Feedback Voltage Reference	FB3 Pin, V_{FB} = 0.656V, Note 2	-2		+2	%
A_{VOL}	Error amp open loop gain			60		dB
I_{EA}	Error amp output drive			±20		µA
I_{EAB}	Error amp input bias current			9	10	nA
R_{DRVH}	HS Gate drive impedance (Buck only)	Output High		15		Ω
		Output Low		15		Ω
R_{DRVL}	LS Gate drive impedance	Output High		15		Ω
		Output Low		15		Ω
D.C. (Boost)	Duty Cycle	Maximum, V_{BATT} = 4.2V	80	90	98	%
		Minimum, PWM mode, V_{BATT} = 4.2V		6	10	%
D.C. (Buck)	Duty Cycle	Maximum, V_{BATT} = 4.2V		100		%
		Minimum, PWM mode, V_{BATT} = 4.2V		7	11	%

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Battery Charger (Note 3), DOCK_DC=5V						
V_{Dockdc}	Input Voltage	VBATT=3.6V		5.0		V
V_{PRECHG}	Precharge voltage threshold range	Programmable: 100mV steps	2.500		3.200	V
V_{PRECHG_ACC}	Precharge voltage threshold accuracy	VBATT rising, V_{PRECHG}= 2.5V and 3.2V		±20		mV
I_{PRECHG}	Nominal precharge current range	R_{CSB}=0.1Ω , 15mA steps	25		250	mA
ΔI_{PRECHG}	Precharge current tolerance	I_{PRECHG} = 100mA	70	100	130	mA
I_{CHG}	Nominal Fast charge current	R_{CSB}=0.1Ω , 60mA steps	100		1000	mA
ΔI_{CHG}	Fast charge current tolerance	I_{CHG} = 520mA	485	520	565	mA
V_{FLT}	Float voltage range	20mV steps	4.000		4.620	V
ΔV_{FLT}	Float voltage tolerance	V_{FLT} = 4.2V	-1.2	±0.5	+1.2	%
V_{FLT_HYST}	Float voltage hysteresis (recharge threshold)	VBATT falling, V_{FLT} - V_{FLT_HYST}		100		mV
I_{TERM}	Charge termination current range	R_{CSB}=0.1Ω, 15mA steps	100		145	mA
ΔI_{TERM}	Termination current tolerance	I_{TERM} = 100mA	50	100	170	mA
T_{HI}	Charge cutoff temp (high)	5°C steps	+30		+65	°C
T_{LO}	Charge cutoff temp (low)	5°C steps	-20		+15	°C
T_{TSENSE}	THERM bias current		80	100	130	µA
$T_{precharge}$	Precharge timer duration	Adjustable (3 setpoints)		2621		s
T_{charge}	Charge timer duration	Adjustable (3 setpoints)		20972		s
V_{PDDCTH}	Programmable DOCK_DC threshold range	Programmable in 200 mV increments	3.4		4.8	V
$V_{PDDCTHACC}$	DOCK_DC threshold accuracy	V_{PDDCTH} = 4.6V	-4		+4	%

DC OPERATING CHARACTERISTICS (CONTINUED)

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
V_{IH}	Input high voltage			0.7 x VDD_CAP		V
V_{IL}	Input low voltage			0.3 x VDD_CAP		V
V_{PBFTH}	Programmable nBATT_FAULT threshold range	Programmable in 150 mV increments	2.55		3.60	V
ΔV_{PBFTH}	nBATT_FAULT accuracy	V_{PBFTH}=3.15V	-3		+4	%
V_{PPFTH}	Programmable POWER_FAIL threshold range	Programmable in 150 mV increments	2.55		3.60	V
ΔV_{PPFTH}	POWER_FAIL accuracy	V_{PPFTH}=3.3V	-3		+4	%
P_{UVTH}	Programmable under voltage threshold	Relative to nominal operating voltage. CH1 to CH7. Note 3.		-5		%
				-10		
				-15		
			-15	-20	-25	
P_{OVTH}	Programmable over voltage threshold	Relative to nominal operating voltage. CH1 to CH7. Note 4.		5		%
				10		
				15		
			15	20	25	

Note 1: Contact Summit factory for other frequency settings.

Note 2: Voltage, current and frequency accuracies are only guaranteed for factory-programmed settings. Changing any of these parameters from the values reflected in the customer specific CSIR code will result in inaccuracies exceeding those specified above.

Note 3: The SMB118 and SMB218 devices are not intended to function as a battery pack protector. Battery packs used in conjunction with these devices need to provide adequate internal protection and to comply with the corresponding battery pack specifications.

Note 4: Guaranteed by Design and Characterization – not 100% tested in Production.

AC OPERATING CHARACTERISTICS (CONTINUED)

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{PPTO}	Programmable power-On sequence timeout period.	Programmable power-On sequence position to sequence position delay.		1.5		ms
				12.5		
				25		
				50		
t_{DPOFF}	Programmable power-off sequence timeout period.	Programmable power-off sequence position to sequence position delay.		1.5		ms
				12.5		
				25		
				50		
t_{PRTO}	Programmable reset time-out delay	Programmable time following assertion of last supply before nRESET pin is released high.		25		ms
				50		
				100		
				200		
t_{PST}	Programmable sequence termination period	Time between active enable in which corresponding outputs must exceed there programmed under voltage threshold. If exceeded, a force shutdown will be initiated.		OFF		ms
				50		
				100		
				200		
t_{PDB}	PWR_EN de-bounce period	When PWR_EN is programmed as power on pin.		0		ms
				25		
				100		
				400		
t_{PFTO}	POWER_FAIL timeout period	Timeout begins after latch is cleared.		3		ms
t_{BFTO}	nBATT_FAULT timeout period	Timeout begins after fault conditions cleared.		3		ms
t_{PGF}	Programmable glitch filter	Period for which fault must persist before fault triggered actions are taken. Present on all Buck, Boost, and inverting supplies.		3		µs

AC OPERATING CHARACTERISTICS (CONTINUED)						
(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)						
Symbol	**Parameter**	**Notes**	**Min**	**Typ**	**Max**	**Unit**
SR_{REF}	Programmable slew rate reference	Adjustable slew rate factor proportional to output slew rate.		400		V/s
				200		
				100		
				66.7		
				50		
				33.3		
				25		
				20		

I²C-2 WIRE SERIAL INTERFACE AC OPERATING CHARACTERISTICS –100 kHz

(Over commercial operating conditions, unless otherwise noted. All voltages are relative to GND.)

Symbol	Description	Conditions	100kHz			
			Min	Typ	Max	Units
f_{SCL}	SCL clock frequency		0		100	KHz
T_{LOW}	Clock low period		4.7			µs
T_{HIGH}	Clock high period		4.0			µs
t_{BUF}	Bus free time	Before new transmission - Note 5	4.7			µs
$t_{SU:STA}$	Start condition setup time		4.7			µs
$t_{HD:STA}$	Start condition hold time		4.0			µs
$t_{SU:STO}$	Stop condition setup time		4.7			µs
t_{AA}	Clock edge to data valid	SCL low to valid SDA (cycle n)	0.2		3.5	µs
t_{DH}	Data output hold time	SCL low (cycle n+1) to SDA change	0.2			µs
t_R	SCL and SDA rise time	Note 5			1000	ns
t_F	SCL and SDA fall time	Note 5			300	ns
$t_{SU:DAT}$	Data in setup time		250			ns
$t_{HD:DAT}$	Data in hold time		0			ns
TI	Noise filter SCL and SDA	Noise suppression		100		ns
t_{WR_CONFIG}	Write cycle time config	Configuration registers			10	ms
t_{WR_EE}	Write cycle time EE	Memory array			5	ms

Note 5: Guaranteed by Design

I²C TIMING DIAGRAMS

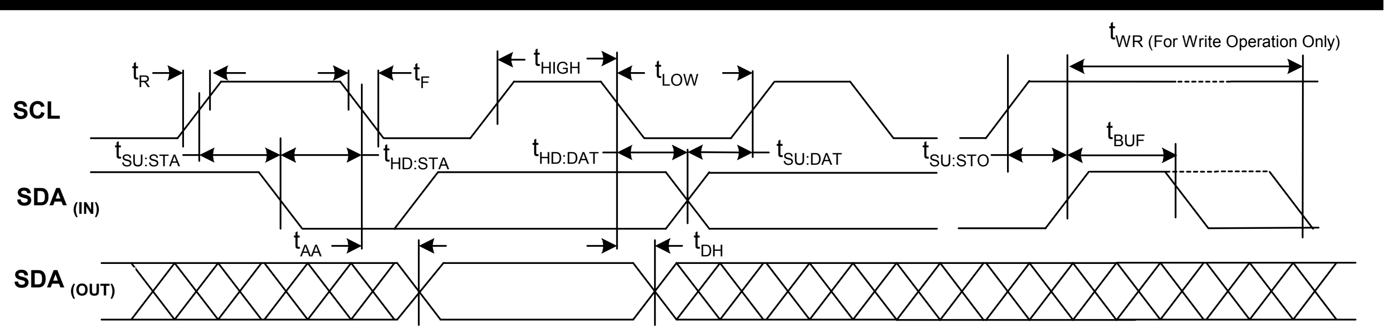


Figure 3 – I²C timing diagram

APPLICATIONS INFORMATION

DEVICE OPERATION

POWER SUPPLY

The SMB118 and SMB218 can be powered from an input voltage between +2.7 and +6 volts applied between the VBATT pin and ground. The input voltage applied to the VBATT pin is filtered by an external filter capacitor attached between the VDD_CAP pin and ground; this filtered voltage is then used as an internal VDD supply. The VDD_CAP node is monitored by an Under-Voltage Lockout (UVLO) circuit, which prevents the outputs from turning on when the voltage at this node is less than the UVLO threshold.

When the voltage on the DOCK_DC input exceeds that on the VBATT input the VBATT pin goes into a high impedance state and no longer powers the devices, and the DOCK_DC pin becomes the new power input.

SHUTDOWN

The SMB118 and SMB218 are equipped with a shutdown pin that disconnects power from the devices and reduces the current consumption to 0.6µA when asserted. When the SHDN pin is pulled high, all outputs will be disabled and the SMB118 and SMB218 will not respond to I^2C commands.

To exit the shutdown mode the SHDN pin can be pulled high, or voltage can be applied to the DOCK_DC input. When voltage is present on the DOCK_DC input the device will exit the shutdown mode and operate normally.

POWER-ON/OFF CONTROL

Sequencing can be initiated: automatically, by a volatile I^2C Power on command, or by asserting the PWREN pin. When the PWREN pin is programmed to initiate sequencing, it can be level or edge triggered. The PWREN input has a programmable de-bounce time of 100, 50, or 25ms. The de-bounce time can also be disabled.

When configured as a push-button enable, the PWREN must be low longer than the debounce time before sequencing can commence, and pulled low for the same period to disable the channels.
When a software power off command is written to the volatile memory the system will be powered off regardless of the state of the PWREN pin.

ENABLE

Each output can be enabled and disable by an enable signal. The enable signal is can be provided from either the PWREN pin or by the contents of the enable register.

When enabling a channel from the enable register, the register contents default state must be set so that the output will be enabled or disabled following a POR (power on reset). The default state is programmable.

CASCADE SEQUENCING

Each channel on the SMB118 and SMB218 may be placed in any one of 6 unique sequence positions, as assigned by the configurable non-volatile register contents. The SMB118 and SMB218 navigate between each sequence position using a feedback-based cascade-sequencing circuit. Cascade sequencing is the process in which each channel is continually compared against a programmable reference voltage until the voltage on the monitored channel exceeds the reference voltage, at which point an internal sequence position counter is incremented and the next sequence position is entered. In the event that a channels enable input is not asserted when the channel is to be sequenced on, that sequence position will be skipped and the channel in the next sequence position will be enabled.

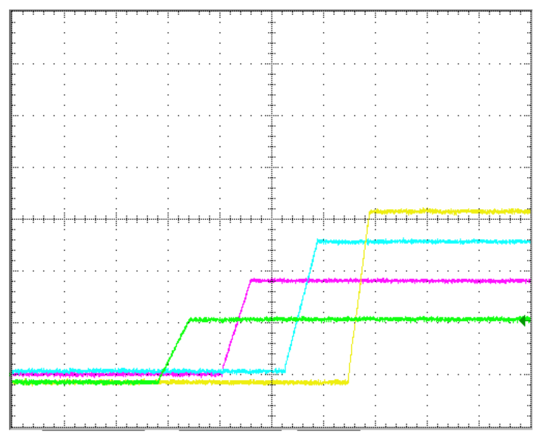


Figure 4 – Power on sequencing waveforms.
Time = 4ms/devision, Scale = 1V/devision
Ch 1 = 3.3V output (Yellow trace)
Ch 2 = 2.5V output (Blue trace)
Ch 3 = 1.8V output (Purple trace)
Ch 4 = 1.2V output (Green trace)

POWER ON/OFF DELAY

There is a programmable delay between when channels in subsequent sequence positions are enabled. The delay is programmable at 50, 25, 12.5 and 1.5ms intervals. This delay is programmable for each of the four sequence positions.

MANUAL MODE

The SMB118 and SMB218 provide a manual power-on mode in which each channel may be enabled

APPLICATIONS INFORMATION (CONTINUED)

individually irrespective of the state of other channels. In this mode, the enable signal has complete control over the channel, and all sequencing is ignored. In Manual mode, channels will not be disabled in the event of a UV/OV fault on any output or the VBATT pin.

FORCE-SHUTDOWN

When a battery fault occurs, a UV/OV is detected on any output, or an I^2C force-shutdown command is issued, all channels will be immediately disabled, ignoring sequence positions or power off delay times.

SEQUENCE TERMINATION TIMER

At the beginning of each sequence position, an internal programmable timer will begin to time out. When this timer has expired, the SMB118 and SMB218 will automatically perform a force-shutdown operation. This timer is user programmable with a programmable sequence termination period (t_{PST}) of 50, 100, 200 ms; this function can also be disabled.

POWER OFF SEQUENCING

The SMB118 and SMB218 have a power-off sequencing operation. During a power off operation, the supplies will be powered off in the reverse order they where powered on in. During the power off sequencing, all enables are ignored.

When a power-off command is issued the devices will set the sequence position counter to the last sequence position and disable that channel without soft-start control; once off, the power off delay for the channel(s) in the next to last sequence position will begin to timeout, after which that channel(s) will be disabled. This process will continue until all channels have been disabled and are off. The programmable

If a channel fails to turn off within the sequence termination period, the sequence termination timer will initiate a force shutdown, if enabled.

INPUT AND OUTPUT VOLTAGE MONITORING

The SMB118 and SMB218 monitor all outputs for under-voltage (UV) and over-voltage (OV) faults. The monitored levels are user programmable, and may be set at 5, 10, 15, and 20 percent of the nominal output voltage.

The VBATT pin is monitored for two user programmable UV settings. The VBATT UV settings are programmable from 2.55V to 3.45V in 150mV increments.

Once the UV/OV voltage set points have been violated, the SMB118 and SMB218 can be programmed to sequence off the supplies (POWER OFF), turn off all supplies simultaneously (FORCE SHUTDOWN), assert the nRESET/HEALTHY pin, or take no action.

SOFT START

The SMB118 and SMB218 provide a programmable soft-start function for all PWM outputs. The soft-start control limits the slew rate that each output is allowed to ramp up without the need for an external capacitor. The soft start slew rate is proportional to the product of the output voltage and a slew rate reference. This global reference is programmable and may be set to 400, 200, 100, 67, 50, 33, 25, and 20 Volts per second. The slew rate control can also be disabled on any channel not requiring the feature.

DYNAMIC VOLTAGE MANAGEMENT

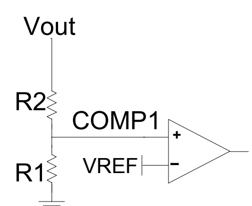
The SMB118 and SMB218 have two additional voltage set points, dynamic voltage control high and low settings. Together with the nominal voltage setting, three pre-determined voltage levels can be used. The three voltage levels are ideal for situations where a core voltage needs to be reduced for power conservation.

The dynamic voltage control high and low settings have the same voltage range as the controllers' nominal output voltage. These settings are stored in the non-volatile configuration registers and can be set by a write to volatile configuration registers. The dynamic voltage control command registers contain two bits for each channel that adjust the output voltages to the high, low or nominal set point after a volatile I2C write command.

A seven level dynamic voltage control option is available for channel 3. When enabled, seven level dynamic voltage control allows channel 3 to be dynamically modified to one of seven pre-determined voltage levels. This transition is made by means of a volatile I^2C write command.

When all channels are at their voltage setting, a bit is set in the dynamic voltage control status registers.

Note: Configuration writes or reads of registers should not be performed while dynamic voltage management.



Soft-Start Slew Rate=SRref* (1 + R2/R1)
Vout= Vref* (1 + R2/R1)

Figure 5 – The output voltage is set by the voltage divider. The VREF voltage is programmable from 0 to 1.0 volt in 4mV increments via the I^2C interface

APPLICATIONS INFORMATION (CONTINUED)

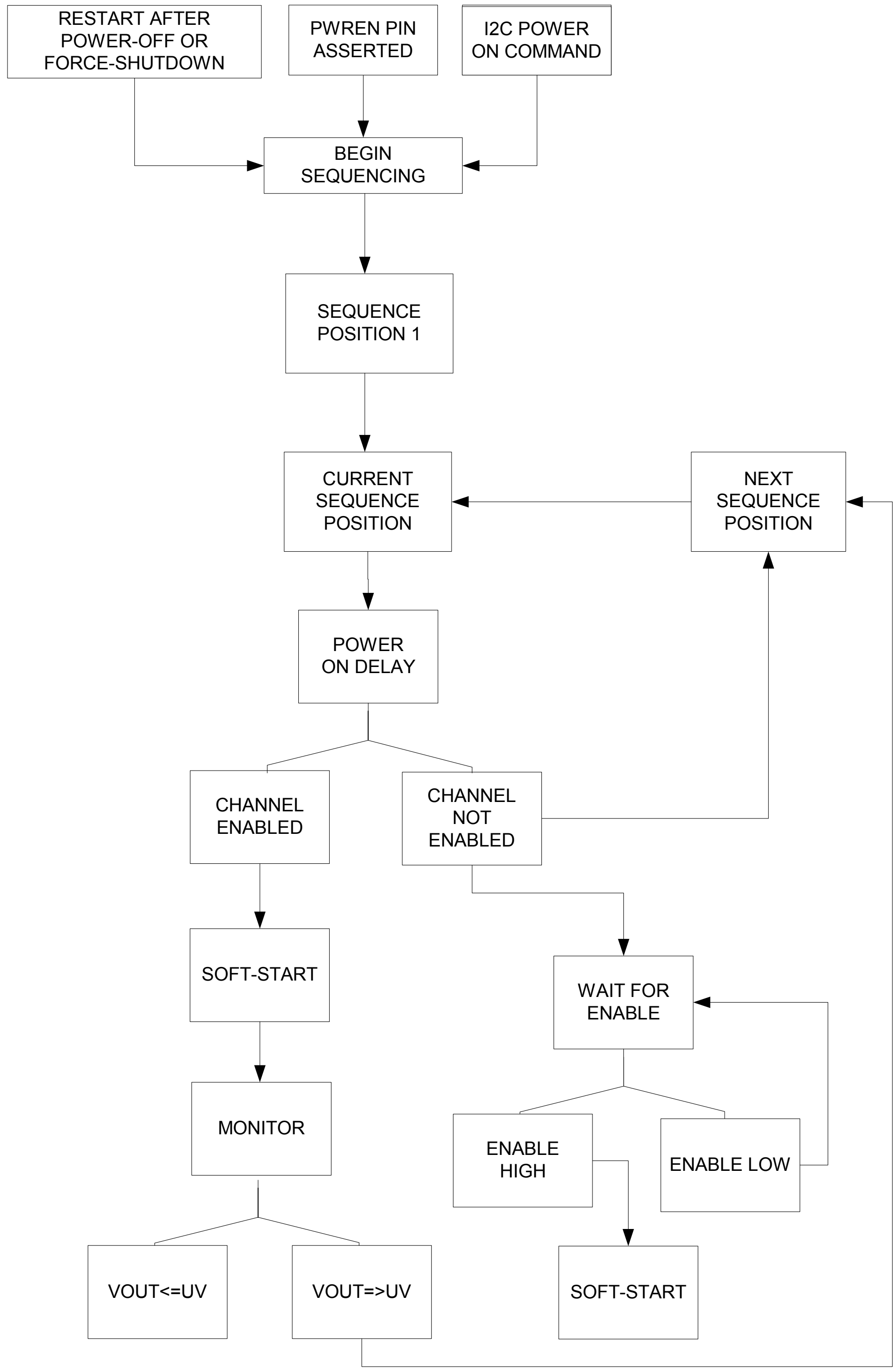


Figure 6 – Power-on sequencing flow chart.

APPLICATIONS INFORMATION (CONTINUED)

BATTERY MONITORING

The battery voltage is monitored for two user-programmable UV settings via the VBATT pin. In addition, the battery charging input, DOCK_DC, is provided to monitor for the presence of a battery charging docking station, or AC wall adaptor.

Monitoring is accomplished by a comparator-based approach, in which a programmable voltage reference is compared against the monitored signal. Each channel possesses a dedicated reference voltage generated by a programmable level shifting digital to analog converter.

The SMB118 and SMB218 contain three user programmable voltage-monitoring levels, each of which triggers a corresponding status pin when exceeded. Battery voltage, like all monitored voltages, is compared against a user programmable voltage set internally by a digital to analog converter.

The DOCK_DC pin is a power input pin that can be used to power the SMB118 and SMB218, and also to indicate the presence, and level, of a supplemental input like that supplied by a docking station or AC wall adaptor. It has a user programmable threshold from 3.4-4.8 volts at 200mV increments. When the user programmable voltage level for this pin is exceeded, continuously, for a de-bounced period in excess of 100 ms the DC_IN pin will be asserted.

When asserted, the POWER_FAIL pin is latched and will not be released as long as the voltage on the battery is below the POWER_FAIL level. Once the voltage on the battery has risen above the POWER_FAIL level one of three conditions may clear the latch and allow the POWER_FAIL pin to be released: if the nBATT_FAULT output pin is asserted and released, if the DC_IN output pin is asserted, and finally if an I^2C *POWER FAIL CLEAR* command is issued. Once one of these conditions has been met, the POWER_FAIL pin will be released after a power-fail timeout period (t_{PFTO}) of 3.0-4.5ms. The POWER_FAIL level is user programmable from 2.55-3.6V in 150 mV increments.

When the voltage at the VBATT pin falls below the second user programmable level (available for SMB118 only), the active low nBATT_FAULT pin will be asserted. This pin is not latched and is used to indicate the impending loss of power to the SMB118. After the nBATT_FAULT pin has been asserted, a battery fault timeout period (t_{BFTO}) of 3.0-4.5ms must pass in which the battery voltage exceeds the nBATT_FAULT threshold before it will be released. The nBATT_FAULT threshold is user programmable from 2.55-3.6.0V at 150 mV increments.

Normally Dock DC, Power fail, and battery fault thresholds are set in descending order respectively.

Upon assertion of either the nBATT_FAULT or POWER_FAIL pin the SMB118 and SMB218 can be programmed to respond in one of three ways, they may perform: a power-off operation, a force-shutdown operation, or take no action. When programmed to perform a power-off or force-shutdown operation the devices can optionally be programmed to latch the outputs off until the power on pin is toggled or an I^2C power-on command is issued.

LDO STANDBY VOLTAGE

The LDO has a programmable output voltage from 1.5V to 3.75V. It is capable of supplying up to 75mA (typical) and has UV and OV monitoring levels with corresponding fault responses. The channel 2 LDO can be sequenced on in any of the six sequence positions, and can be enabled and disabled at any time.

OUTPUT VOLTAGE

The PWM output voltages are set by a resistive voltage divider from the output to the COMPA or FB node; see Figure 4. For the Buck channels (Ch[6:4]), the voltage divider is internal to the part and programmable. The resistive divider may be set by adjusting a 100kΩ resistor string with 8 taps from R1 = 20-90kΩ. For the Boost output (Ch[1]), the resistive divider is external and any appropriate value of R1 an R2 can be chosen. The reference voltage that sets the output is user programmable, and may be set anywhere from 0-1.000 volt at 4mV increments.

BATTERY CHARGER

The SMB118 and SMB218 are equipped with a fully programmable lithium ion battery charger. The programmable feature set includes fast and pre-charge option, each with a programmable charge current level, a charge termination timeout period, an over and under temperature limit, multiple allowable recharge events, fault logging that can be accessed via the I^2C interface and a general purpose output used to indicate the current status of the battery.

APPLICATIONS INFORMATION (CONTINUED)

Battery charging is initiated by the detection a DC voltage on the DOCK_DC input. When the voltage on DOCK_DC exceeds the programmed minimum threshold voltage, the DC_IN pin will be asserted indicating the successful connection of a charging input.

Once the charging voltage exceeds the DOCK_DC threshold voltage, the SMB118 will be powered from the DOCK_DC pin. Once the voltage on DOCK_DC is above the programmed setting, battery charging will automatically commence. However, a programmable option allows the user to prevent battery charging until an I^2C command has been issued. The SHDN pin is bypassed once voltage is sensed on the DOCK_DC pin.

TRICKLE CHARGE

Once all pre-qualification conditions are met, the devices check the BSENSE voltage to decide if trickle charging is required. If the battery voltage is below approximately 2.0V, a charging current of 2mA (typical) is applied on the battery cell. This allows the SMB118 and SMB218 to reset the protection circuit in the battery pack and bring the battery voltage to a higher level without compromising safety.

PRE-CHARGE MODE

Once the battery voltage crosses the 2.0V level, the SMB118 and SMB218 will begin to pre-charge the battery to safely charge the deeply discharged cells. The device stays in this mode until the voltage on BSENSE input is above the programmed pre-charge threshold voltage. The pre-charge threshold voltage is programmable from 2.5V to 3.2V in 100mV increments. The pre-charge current is programmable from 25 to 250mA, in 15mA increments.

FAST-CHARGE MODE

After the pre-charge threshold voltage has been exceeded, the battery charging current will be increased from the pre-charge current to the fast-charge current. The fast-charge current is programmable from 100mA to 1A, in 60mA increments. The battery will be charged with the fast-charge current until the battery voltage exceeds the final float voltage.

TAPER CHARGE MODE

Once the final float voltage has been reached, the battery charger will enter a constant voltage taper charging mode, in which the battery voltage is held at the final float voltage. The taper charging mode will continue until the charge current drops below the termination current threshold. The termination current threshold is programmable at 100mA, 115mA, 130mA and 145mA, assuming a 100mΩ sense resistor. A programmable option allows the Taper Charge mode to be bypassed and the battery charging to be completed once the final float voltage has been reached.

CURRENT SCALING

All charging currents are determined by measuring the voltage across the battery current sense resistor. All programmable currents are based on the use of a 100mΩ sense resistor. Currents can be increased or decreased by scaling the current sense resistor. For example, a 50mΩ sense resistor will scale the charging current by a factor of two, while using a 200mΩ resistor will scale the charging current by one half.

TEMPERATURE MONITORING

To inhibit charging when the battery temperature is outside normal operating range a temperature sensing input is provided.

The battery temperature is measured by sensing the voltage between the TSENSE pin and ground. The voltage is created by injecting a current into the parallel combination of Negative Temperature Coefficient (NTC) thermistor and a resistor. As the temperature changes, the resistance of the thermistor changes creating a voltage proportional to temperature. This voltage is then compared to two predetermined voltages representing the maximum and minimum temperature settings of the battery. The purpose of the resistor in parallel to the NTC thermistor is to linearize the resistance of the thermistor. Table 1, shows the 1% resistor that should be placed in parallel with the corresponding thermistor.

The temperature coefficient or Beta (B) of the thermistor must be as close to 4400 as possible to achieve the maximum temperature accuracy.

NTC THERMISTOR	RESISTANCE
10K	24.9K
25K	61.9K
100K	249K

Table 1: NTC values and associated parallel resistances.

If the temperature limits are exceeded, battery charging will be suspend until the battery voltage has fallen within the safe operating range.. The over temperature limit is programmable from 30°C to 65°C in 5°C

APPLICATIONS INFORMATION (CONTINUED)

increments. The under temperature limit is programmable from –20°C to 15°C in 5°C increments.

CHARGE TERMINATION TIMERS

There are two timers on the SMB118 and SMB218 used to disable battery charging. The first timer is used to limit the allowable pre-charge duration. This timer begins when trickle charging is completed and ends when fast charging begins. It can be programmed to one of three settings: 44 minutes, 1 hour 27 minutes, and 2 hours 55 minutes.

The second timer limits the fast-charge and taper charge duration. This timer begins when pre-charge mode is completed and ends when taper charging has been terminated. It is programmable in three settings, 5 hours 48 minutes, 11 hours 36 minutes, and 23 hours. Each timer can be independently disabled.

PROGRAMMABLE SWITCHING FREQUENCY

The SMB118 and SMB218 have a 1MHz switching frequency. If a different frequency is desirable, please contact the Summit factory.

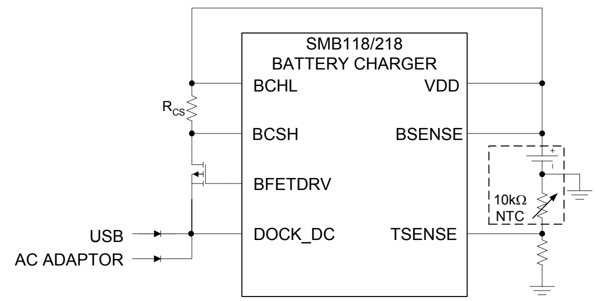


Figure 7 – Battery charging circuit

BATTERY CHARGING ALGORITHM

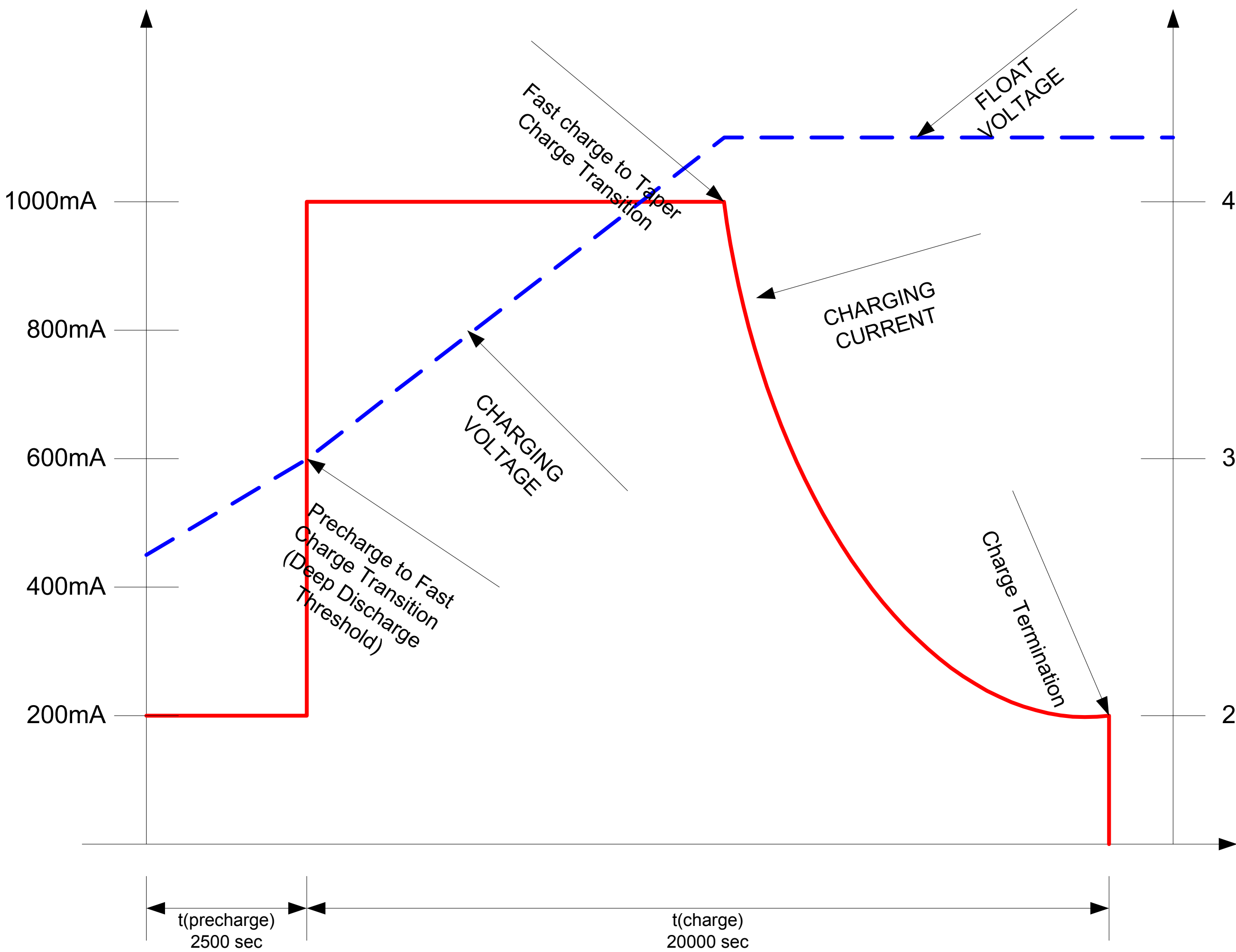


Figure 8 – Battery charging algorithm.

BATTERY CHARGING FLOWCHART

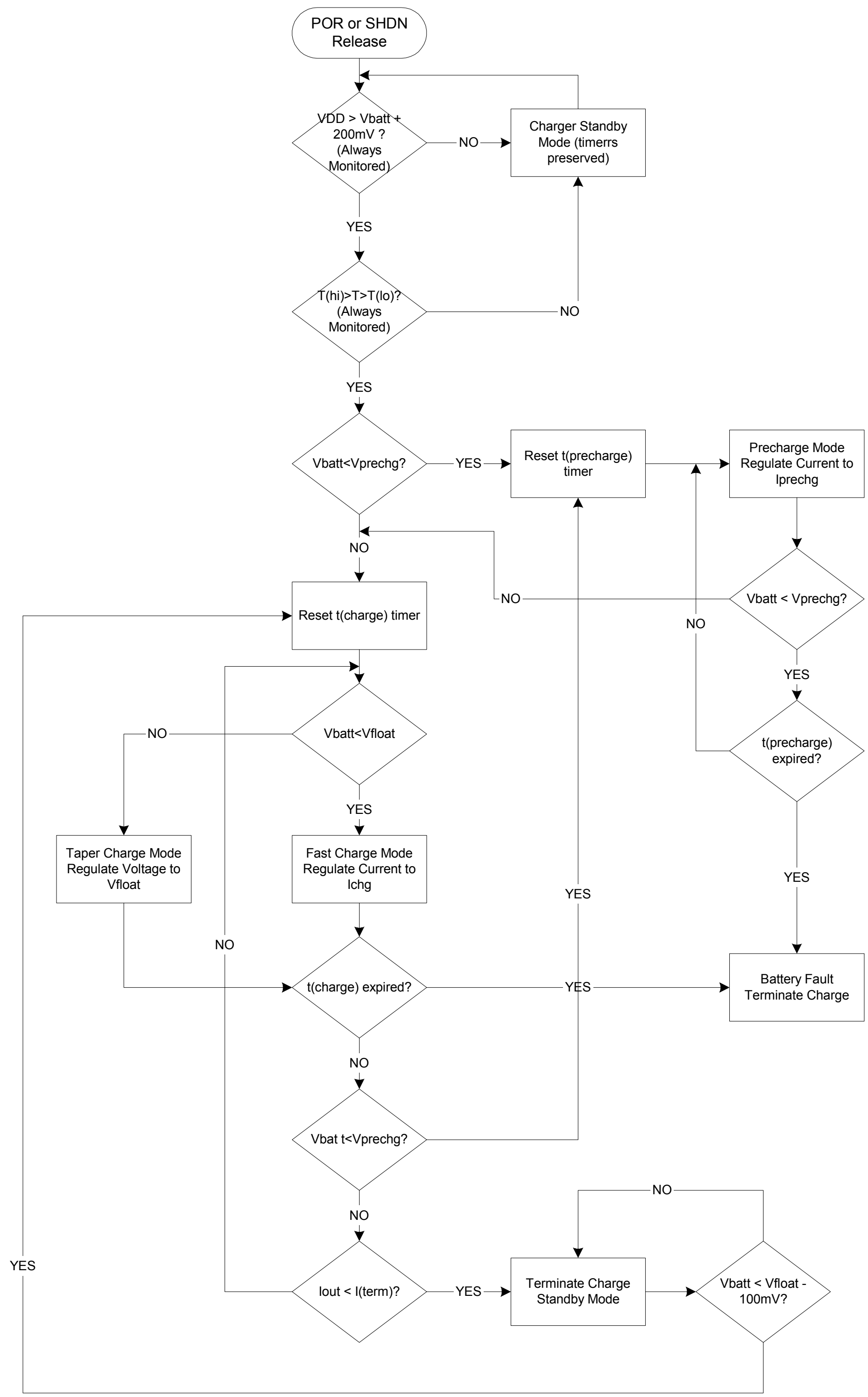


Figure 9 – Battery charging flowchart.

APPLICATIONS INFORMATION (CONTINUED)

BUCK CONVERTERS

The SMB118 and SMB218 have three synchronous buck converters with integrated p-channel MOSFETS and a driver for an external NFET, see Figure 10. Each channel has an output voltage range from the input supply to approximately 0.5V.

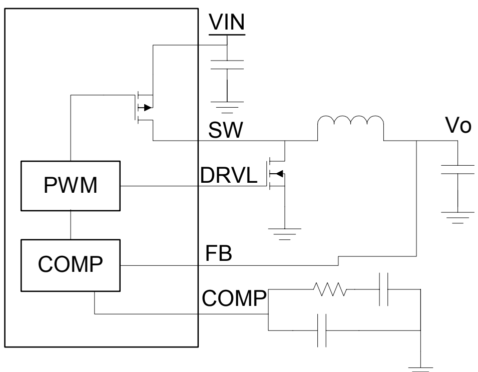


Figure 10 – Buck channel with internal PFET.

Buck Channel Asynchronous Operation

The buck converters use either a constant frequency or variable frequency current mode control technique.

During the fixed frequency PWM mode of operation, the converter switches at a fixed frequency and modulates the duty cycle to attain the correct output voltage. This can lead to “charge shuttling” under light load conditions were the charge delivered to the output capacitor during the on time of the PFET is discharged to ground during the on time of the NFET. This mode of operation is desirable in situations requiring low voltage ripple, the ability to sink current, or a known switching frequency for all loads.

During the PFM mode of operation the converter operates asynchronously where the FET is held off and the body diode of the FET is used as a “catch” diode; preventing the voltage on the switch node from falling below ground by more than a diode drop. It is desirable to operate asynchronously under light load so that charge shuttling does not occur. The asynchronous operation allows the converter to only switch when the voltage falls below the error amplifier reference voltage. While it is advantageous to operate asynchronously for light load currents, it is less efficient for moderate loads where the power loss across the forward voltage drop of the diode leads to decreased efficiency. To increase the efficiency for these moderate load conditions an external schottky diode can be placed in parallel with the body diode of the FET.

To maximize the converter efficiency for both light and heavy loads the buck converters automatically switch from PFM to PWM mode for higher loads. The PWM to PFM crossover is accomplished by observing the voltage on the COMP pin, the voltage on the COMP pin is directly proportional to the load current. When the voltage on the COMP pin falls below a programmable reference, the converter operates in PFM. The drivers will stay in this state until the voltage on the COMP pins rise above the programmable PFM to PWM crossover voltage.

Each channel has an over current protection mechanism. When a channel reaches its current limit, the output voltage will be reduced as the load rises. This is accomplished by clamping the COMP node to one of four programmable settings. The over-current level can be programmed to four different levels by clamping the error amplifier's output voltage to a programmable voltage.

All current limits and PFM to PWM crossover currents are calculated by the GUI interface.

The output of all buck converters is determined by the portion of the switching period for which the inductor voltage is at the converter supply voltage, this percentage is referred to as the duty cycle. For a buck channel operating synchronously duty cycle and the output voltage are related by equation 1 below:

Equation 1: $Vo = D * Vin$

Each buck converter can operate up to 100% duty cycle allowing the output to equal the input. The minimum voltage is determined by the minimum duty cycle listed in the electrical specifications section. For a buck converter operating in PFM mode the duty cycle is essentially 0% implying that the output can go to ground.

Each converter has a separate VIN input used to power the converter. This supply attaches to the source of the integrated PFET. It is important to connect an input (or Bulk) as close to the VIN pin as possible. For information on the type of capacitor to use, refer to the component selection section.

Boost Controller

The SMB118 and SMB218 have one asynchronous current mode Boost converter with over-current protection and either a PWM or PFM mode of operation.

As a current mode boost controller a sense resistor must be added, externally, in series with the source of the N-channel MOSFET, see Figure 11. The over-

APPLICATIONS INFORMATION (CONTINUED)

current circuitry is identical to that descried for the buck converter, the current limit is displayed in the GUI.

The PWM to PFM crossover current is identical to the circuitry used for the buck converter, we monitor the voltage on the COMP node and when the voltage is below a programmable reference the NFET is held off.

The boost converter has a fixed PWM option, when enabled the boost channel will switch every cycle keeping the ripple voltage low. Care must be taken in selecting the PWM option on the boost channel, as this converter does not have the ability to shuttle charge. As a result, the load must be sufficient to deplete the deposited charge every cycle or else the output voltage will rise above the output set point.

All boost controller drivers are powered from the VBATT supply pin. Therefore, without voltage on the VBATT input the boost converters will not function.

The output of all boost controllers are determined by the portion of the switching period for which the inductor voltage is at ground, this percentage is referred to as the duty cycle. For a boost controller where the inductor current does not go to 0A during the cycle (CCM) the relation between the duty cycle and the output voltage is determined by equation 2 below:

Equation 2: $$Vo = \left(\frac{1}{1-D}\right) * Vin$$

The maximum duty cycle the boost converter can achieve is determined by the max duty cycle specified in the electrical specification section of the datasheet.

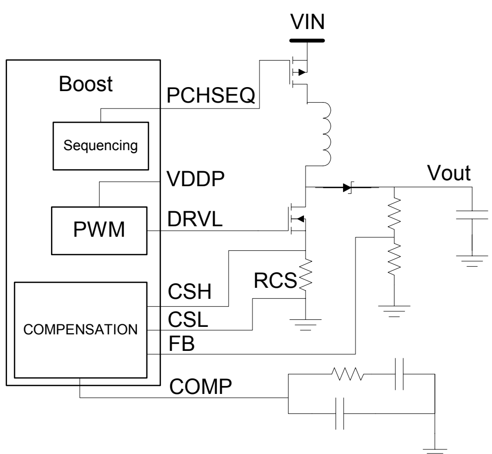


Figure 11: Boost Channel

BOOST OR BUCK CONTROLLER

The SMB118 and SMB218 have one voltage mode output that can be configured as either a boost or a buck controller; see Figures 12 and 13.

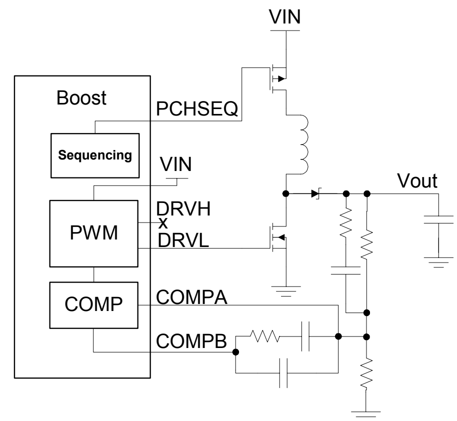


Figure 12 –Buck or boost channel configured as boost.

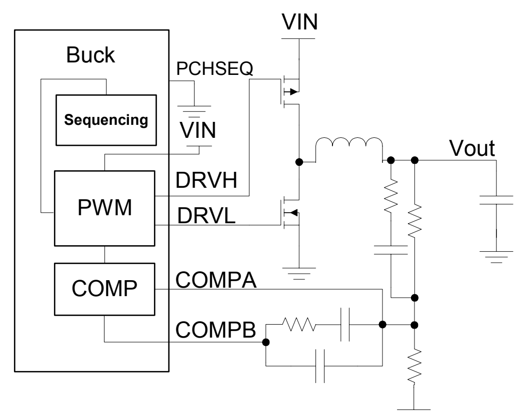


Figure 13 – Buck or boost channel configured as buck.

A type three-compensation network is used for this voltage mode controller to provide optimal transient response. Both configurations can operate in PWM or PFM mode. In addition, when configured a buck the output is allowed to reach a 100% duty cycle and operate in a low dropout mode.

This is not to be confused with a Buck-Boost converter that can act as a buck if the output is below the input or a Boost if the output is below the input.

APPLICATIONS INFORMATION (CONTINUED)

COMPONENT SELECTION

Buck Outputs:

Inductor:

The starting point design of any and DC/DC converter is the selection of the appropriate inductor for the application. The optimal inductor value will set the inductor current at 30% of the maximum expected load current. The inductors current for Buck and Boost converters are as follows:

Buck: Equation 3: $L = \frac{Vo(V_{IN} - Vo)}{Vin * 0.3 * I_{MAX} * f}$

Boost: Equation 4: $L = \frac{V_{IN}(V_O - V_{IN})}{V_O * 0.3 * I_{MAX} * f}$

Where Vo is the output voltage, VIN is the input voltage, f is the frequency, and I_{MAX} is the max load current.

For example: For a 1.2V output and a 3.6V input with a 500mA max load, and a 1MHz switching frequency the optimal inductor value is:

$$L = \frac{1.2(3.6 - 1.2)}{3.6 * 0.3 * 0.5 \quad * 1E6} = 5.3uH$$

Choosing the nearest standard inductor value we select a 5.6uH inductor. It is important that the inductor has a saturation current level greater than 1.2 times the max load current.

Other parameters of interest when selecting an inductor are the DCR (DC winding resistance). This has a direct impact on the efficiency of the converter. In general, the smaller the size of the inductor is the larger the resistance. As the DCR goes up the power loss increases according to the I^2R relation. As a result choosing a correct inductor is often a trade off between size and efficiency.

Input Capacitor

Each converter should have a high value low impedance input (or bulk) capacitor to act as a current reservoir for the converter stage. This capacitor should be either a X5R or X7R MLCC (multi-layer-ceramic capacitor). The value of this capacitor is normally chosen to reflect the ratio of the input and output voltage with respect to the output capacitor. Typical values range from 2.2uF to 10uF.

For Buck converters, the input capacitor supplies square wave current to the inductor and thus it is critical to place this capacitor as close to the PFET as possible in order to minimize trace inductance that would otherwise limit the rate of change of the current. While the placement of this inductor for Boost channels is not as critical as with the Buck channels, each Boost must still have its own reservoir capacitor.

Output capacitor

Each converter should have a high value low impedance output capacitor to act as a current reservoir for current transients and to. This capacitor should be either a X5R or X7R MLCC.

For a Buck converter, the value of this capacitance is determined by the maximum expected transient current. Since the converter has a finite response time, during a load transient the current is provided by the output capacitor. Since the voltage across the capacitor drops proportionally to the capacitance, a higher output capacitor reduces the voltage drop until the feedback loop can react to increase the voltage to equilibrium.

For the Boost converters, the output is disconnected from the inductor while the diode is reverse biased. This means that the entire load current is being taken from the output capacitance for this portion of the duty cycle. For this reason it is necessary to choose the output capacitor such that the cycle-to-cycle voltage droop is minimized to be within system limits.

The voltage drop can be calculated according to:

Equation 5: $V = \frac{I * T}{C}$

Where I is the load or transient current, T is the time the output capacitor is supporting the output and C is the output capacitance. Typical values range from 10uF to 44uF.

Other important capacitor parameters include the Equivalent Series Resistance (E.S.R) of the capacitor. The ESR in conjunction with the ripple current determines the ripple voltage on the output, for typical values of MLCC the ESR ranges from 2-10mΩ. In addition, carful attention must be paid to the voltage rating of the capacitor the voltage rating of a capacitor must never be exceeded. In addition, the DC bias voltage rating can reduce the measured capacitance by as much as 50% when the voltage is at half of the max rating, make sure to look at the DC bias de-rating curves when selecting a capacitor.

APPLICATIONS INFORMATION (CONTINUED)

MOSFETS

When selecting the appropriate FET to use attention must be paid to the gate to source rating, input capacitance, and maximum power dissipation.

Most FETs are specified by an on resistance (RDS_{ON}) for a given gate to source voltage (V_{GS}). It is essential to ensure that the FETs used will always have a V_{GS} voltage grater then the minimum value shown on the datasheet. It is worth noting that the specified V_{GS} voltage must not be confused with the threshold voltage of the FET.

The input capacitance must be chosen such that the rise and fall times specified in the datasheet do not exceed ~5% of the switching period.

To ensure the maximum load current will not exceed the power rating of the FET, the power dissipation of each FET must be determined. It is important to look at each FET individually and then add the power dissipation of complementary FETs after the power dissipation over one cycle has been determined. The Power dissipation can be approximated as follows:

Equation 6: $P \sim R_{DSON} * I_L{}^2 * T_{ON}$

Where T_{ON} is the on time of the primary switch. T_{ON} can be calculated as follows:

Equations 7, 8, 9:

$$Buck - NFET : (1 - \frac{V_O}{V_{IN}}) * T$$

$$Buck - PFET : \frac{V_O}{V_{IN}} * T$$

$$Boost : (\frac{V_O - V_{IN}}{V_O}) * T$$

Compensation:

Summit provides a design tool to called Summit Power Designer" that will automatically calculate the compensation values for a design or allow the system to be customized for a particular application. The power designer software can be found at http://www.summitmicro.com/prod_select/xls/SummitPowerDesigner_Install.zip.

DEVELOPMENT HARDWARE & SOFTWARE

The end user can obtain the Summit SMX3200 parallel port programming system or the I^2C2USB (SMX3201) USB programming system for device prototype development. The SMX3200(1) system consist of a programming Dongle, cable and Windows™ GUI software. It can be ordered on the website or from a local representative. The latest revisions of all software and an application brief describing the SMX3200 and SMX3201 are available from the website (**http://www.summitmicro.com**).

The SMX3200 programming Dongle/cable interfaces directly between a PC's parallel port and the target application; while the SMX3201 interfaces directly to the PC's USB port and the target application. The device is then configured on-screen via an intuitive graphical user interface employing drop-down menus.

The Windows GUI software will generate the data and send it in I^2C serial bus format so that it can be directly downloaded to the SMB118 and SMB218 via the programming Dongle and cable. An example of the connection interface is shown in Figure 14.

When design prototyping is complete, the software can generate a HEX data file that should be transmitted to Summit for approval. Summit will then assign a unique customer ID to the HEX code and program production devices before the final electrical test operations. This will ensure proper device operation in the end application.

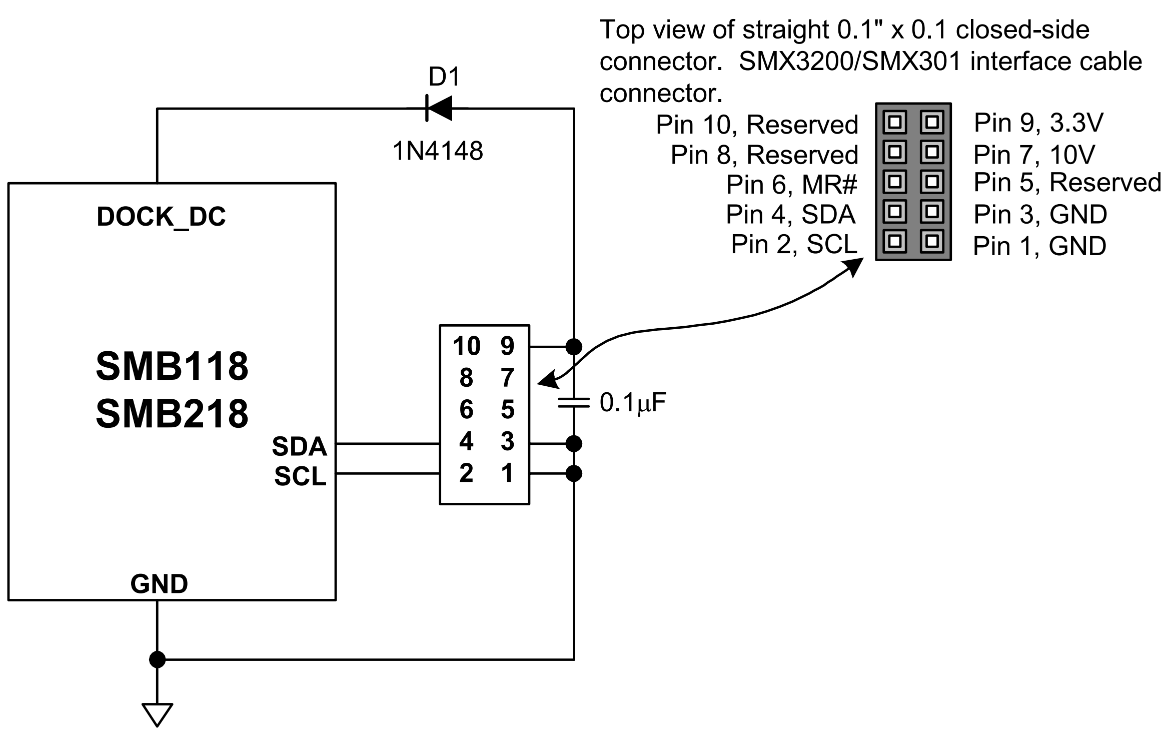


Figure 14 – SMX3200-3.3 Programmer I^2C serial bus connections to program the SMB118 or SMB218.

I²C PROGRAMMING INFORMATION

SERIAL INTERFACE

Access to the configuration registers, general-purpose memory and command and status registers is carried out over an industry standard 2-wire serial interface (I^2C). SDA is a bi-directional data line and SCL is a clock input. Data is clocked in on the rising edge of SCL and clocked out on the falling edge of SCL. All data transfers begin with the MSB. During data transfers, SDA must remain stable while SCL is high. Data is transferred in 8-bit packets with an intervening clock period in which an Acknowledge is provided by the device receiving data. The SCL high period (t_{HIGH}) is used for generating Start and Stop conditions that precede and end most transactions on the serial bus. A high-to-low transition of SDA while SCL is high is considered a Start condition while a low-to-high transition of SDA while SCL is high is considered a Stop condition.

The interface protocol allows operation of multiple devices and types of devices on a single bus through unique device addressing. The address byte is comprised of a 7-bit device type identifier (slave address). The remaining bit indicates either a read or a write operation. Refer to Table 1 for a description of the address bytes used by the SMB118 and SMB218.

The device type identifier for the memory array, the configuration registers and the command and status registers are accessible with the same slave address. The slave address can be can be programmed to any seven bit number 0000000_{BIN} through 1111111_{BIN}.

WRITE

Writing to the memory or a configuration register is illustrated in Figures 15, 16, 18, and 19. A Start condition followed by the slave address byte is provided by the host; the SMB118 responds with an Acknowledge; the host then responds by sending the memory address pointer or configuration register address pointer; the SMB118 and SMB218 respond with an acknowledge; the host then clocks in one byte of data. For memory and configuration register writes, up to 15 additional bytes of data can be clocked in by the host to write to consecutive addresses within the same page.

After the last byte is clocked in and the host receives an Acknowledge, a Stop condition must be issued to initiate the nonvolatile write operation.

READ

The address pointer for the non-volatile configuration registers and memory registers as well as the volatile command and status registers must be set before data can be read from the SMB118 and SMB218. This is accomplished by issuing a dummy write command, which is a write command that is not followed by a Stop condition. A dummy write command sets the address from which data is read. After the dummy write command is issued, a Start command followed by the address byte is sent from the host. The host then waits for an Acknowledge and then begins clocking data out of the slave device. The first byte read is data from the address pointer set during the dummy write command. Additional bytes can be clocked out of consecutive addresses with the host providing an Acknowledge after each byte. After the data is read from the desired registers, the read operation is terminated by the host holding SDA high during the Acknowledge clock cycle and then issuing a Stop condition. Refer to Figures 17 and 20 for an illustration of the read sequence.

CONFIGURATION REGISTERS

The configuration registers are grouped with the general-purpose memory. Writing and reading the configuration registers is shown in Figures 15, 16 and 17.

GENERAL-PURPOSE MEMORY

The 96-byte general-purpose memory block is segmented into two continuous independently lockable blocks. The first 48-byte memory block begins at register address pointer $A0_{HEX}$ and the second memory block begins at the register address pointer $C0_{HEX}$; see Table 1. Each memory block can be locked individually by writing to a dedicated register in the configuration memory space. Memory writes and reads are shown in Figures 18, 19 and 20.

I²C PROGRAMMING INFORMATION

GRAPHICAL USER INTERFACE (GUI)

Device configuration utilizing the Windows based SMB118 graphical user interface (GUI) is highly recommended. The software is available from the Summit website (www.summitmicro.com). Using the GUI in conjunction with this datasheet, simplifies the process of device prototyping and the interaction of the various functional blocks. A programming Dongle (SMX3201) is available from Summit to communicate with the SMB118 and SMB218. The Dongle connects directly to the USB port of a PC and programs the device through a cable using the I²C bus protocol. See Figure 14 and the SMX3201 Data Sheet.

Slave Address	Register Type
ANY	Configuration Registers are located in 00_{HEX} thru $9F_{HEX}$
	General-Purpose Memory Block 0 is located in $A0_{HEX}$ thru BF_{HEX}
	General-Purpose Memory Block 1 is located in $C0_{HEX}$ thru FF_{HEX}

Table 2 - Address bytes used by the SMB118 and SMB218.

I²C PROGRAMMING INFORMATION (Continued)

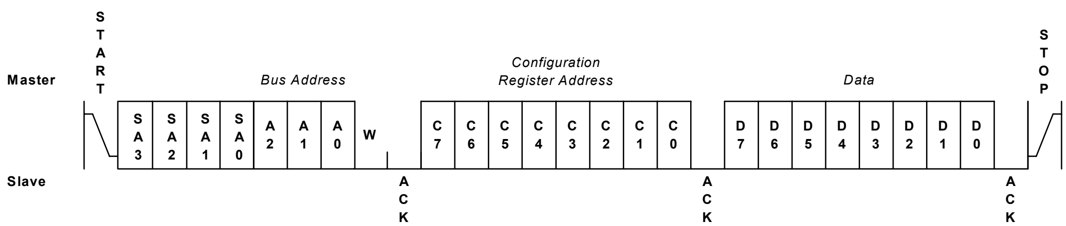


Figure 15 – Configuration Register Byte Write

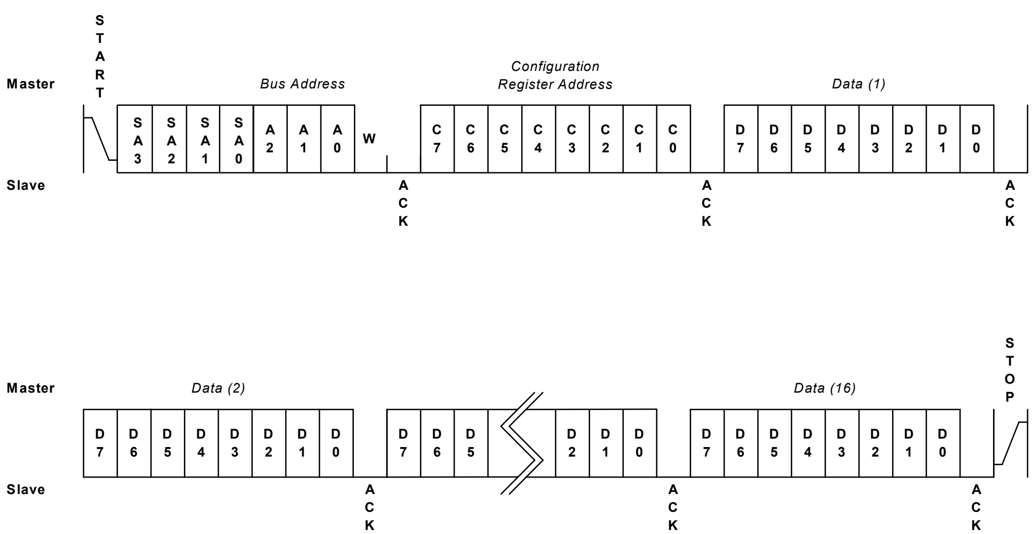


Figure 16 – Configuration Register Page Write

I²C PROGRAMMING INFORMATION (Continued)

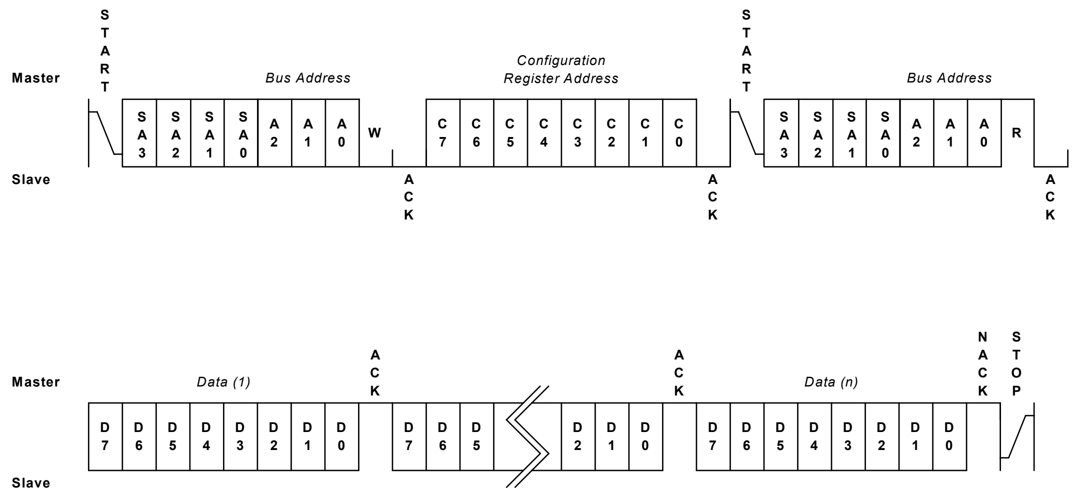


Figure 17 - Configuration Register Read

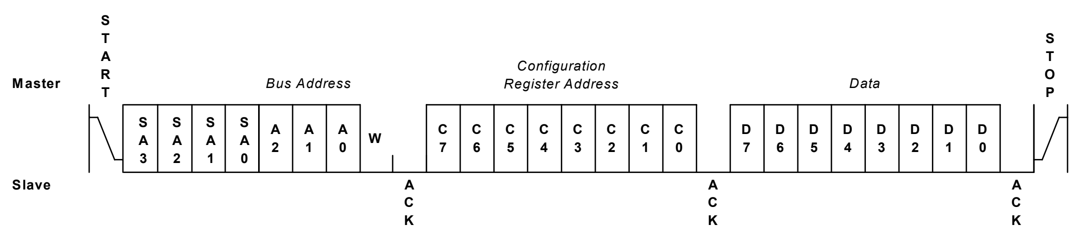


Figure 18– General Purpose Memory Byte Write

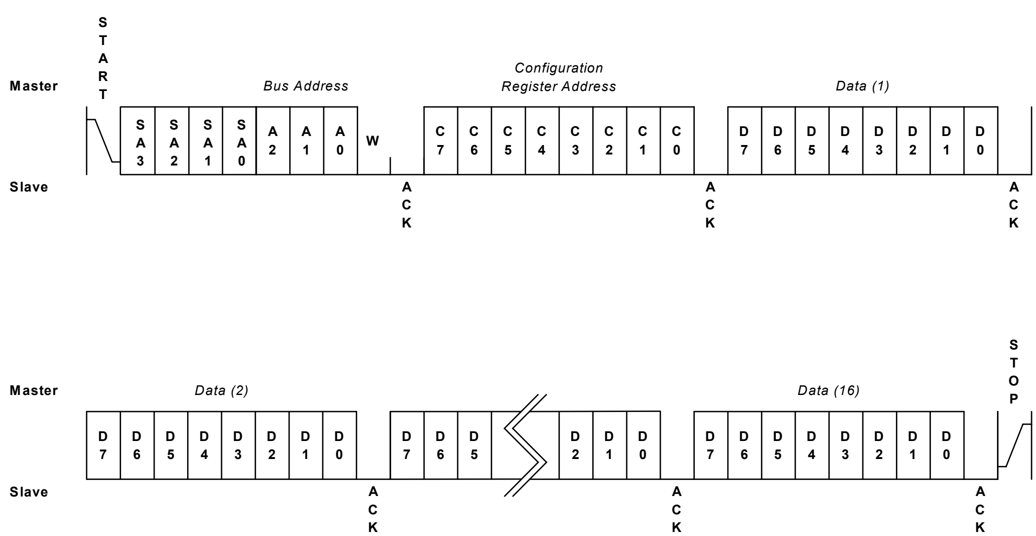


Figure 19 - General Purpose Memory Page Write

I²C PROGRAMMING INFORMATION (Continued)

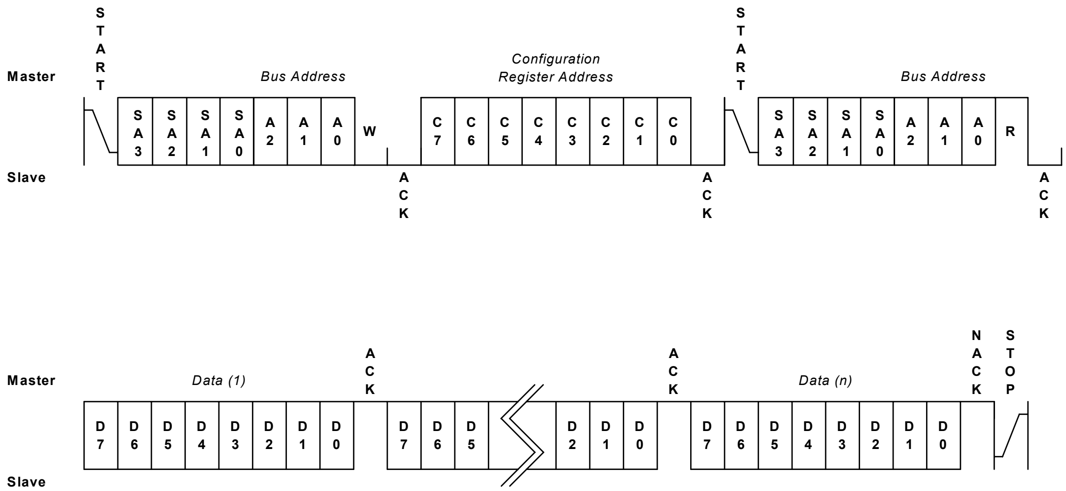
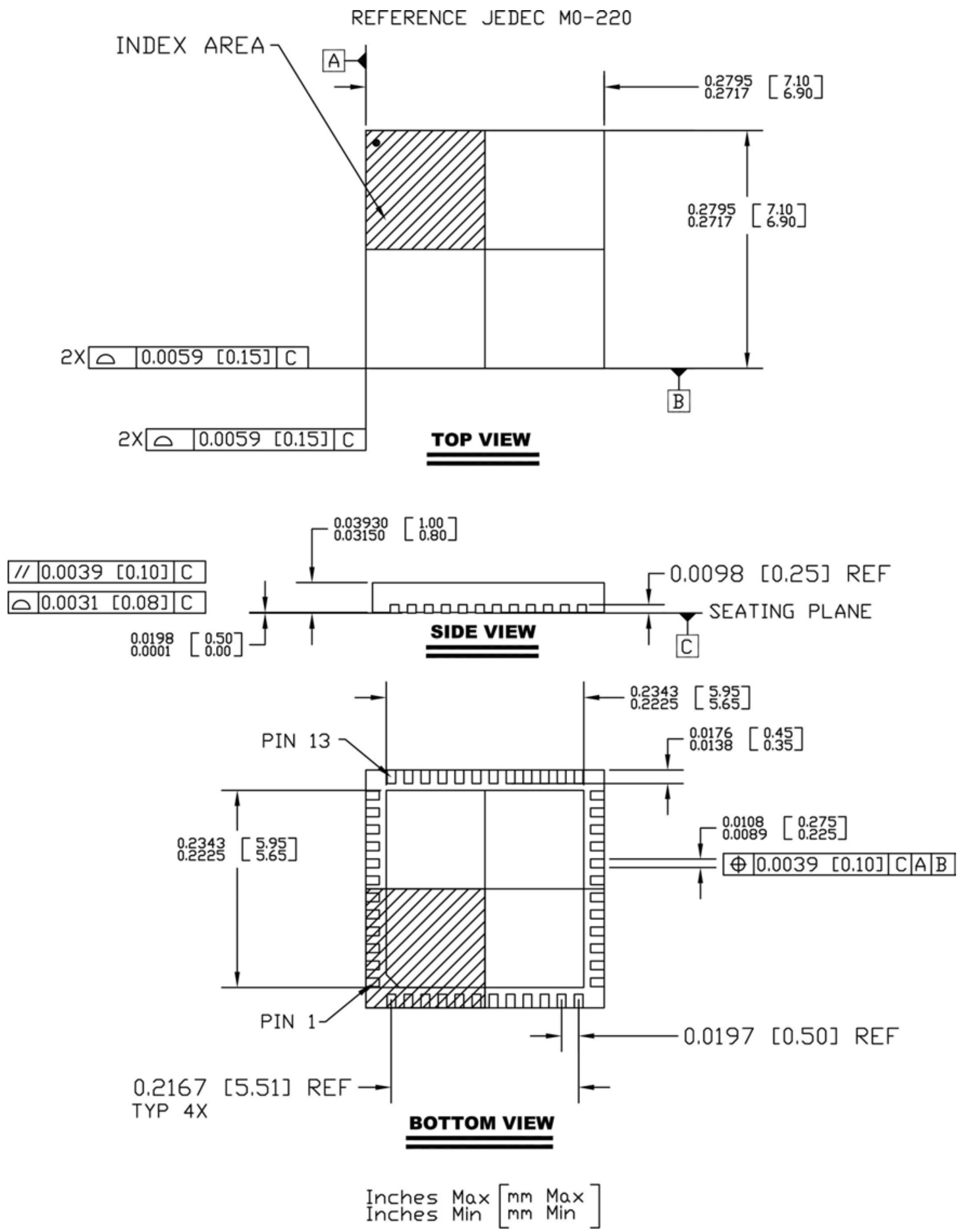


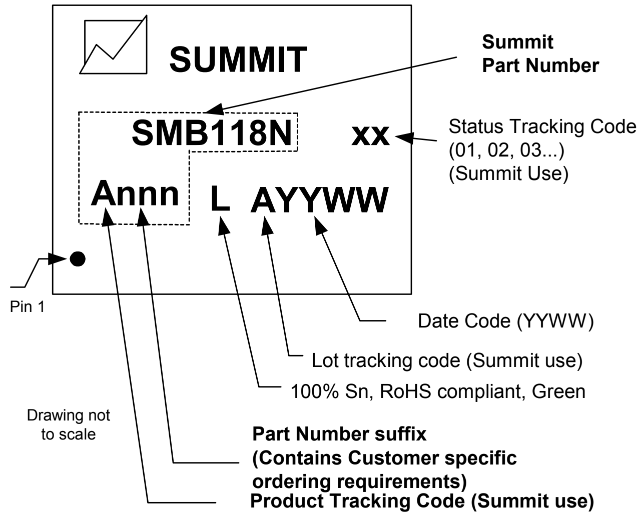
Figure 20 - General Purpose Memory Read

PACKAGE

48 Pad QFN – 7X7



PART MARKING



ORDERING INFORMATION

SMB118 N C nnn L

Summit Part Number
SMB118 or SMB218

Package
N = 48-Pad QFN

Temperature Range
C = Commercial
BLANK = Industrial

Part Number Suffix
Specific requirements are contained in the suffix

Environmental Attribute
L = 100% Sn, RoHS compliant

NOTICE

NOTE 1 - This is a ***Final*** data sheet that describes a Summit product currently in production.

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