REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 03. Update boilerplate. Editorial corrections throughout.	96-08-09	Ray Monnin

REV																				
SHEET																				
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SHEET																				

REV STATUS OF SHEETS															
REV	A	A	A	A	A	A	A	A	A	A	A	A	A		
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
Rick Officer

CHECKED BY
Ray Monnin

APPROVED BY
Michael A. Frye

DRAWING APPROVAL DATE
2 SEPTEMBER 1988

REVISION LEVEL
A

DEFENSE ELECTRONICS SUPPLY CENTER
DAYTON, OHIO 45444

MICROCIRCUIT, DIGITAL, 4K X 1 CMOS SRAM, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-88587**

SHEET 1 OF 13

DESC FORM 193
JUL 94

5962-E500-96

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

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1. SCOPE

1.1 Scope. This drawing describes device requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A.

1.2 Part or Identifying Number (PIN). The complete PIN is as shown in the following example:

5962-88587	01	V	X
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function	Access time
01	See 6.4	4096 X 1 CMOS static RAM	45 ns
02	See 6.4	4096 X 1 CMOS static RAM	35 ns
03	See 6.4	4096 X 1 CMOS static RAM	35 ns

1.2.2 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
V	GDIP1-T18 or CDIP2-T18	18	Dual-in-line
X	See figure 1	18	Flat pack
Y	CQCC4-N18	18	Rectangular leadless chip carrier

1.2.3 Lead finish. The lead finish is as specified in MIL-PRF-38535, appendix A.

1.3 Absolute maximum ratings.

Supply voltage to ground potential ..... -0.5 V dc to +7.0 V dc
DC voltage applied to outputs in high impedance state .... -0.5 V dc to +7.0 V dc
DC input voltage ..... -3.0 V dc to +7.0 V dc
DC output current ..... 20 mA
Storage temperature range ..... -65°C to +150°C
Maximum power dissipation (P_D) 1/ ..... 1.0 W 1/
Lead temperature (soldering, 10 seconds) ..... +300°C
Thermal resistance, junction-to-case (O_{JC}):
  Cases V and Y ..... See MIL-STD-1835
  Case X ..... +55°C/W 2/
Junction temperature (T_J) ..... +175°C 3/

1.4 Recommended operating conditions.

Supply voltage range (V_{CC}) ..... 4.5 V dc minimum to 5.5 V dc maximum
High level input voltage range (V_{IH}) ..... 2.0 V dc to 6.0 V dc
Low level input voltage range (V_{IL}) ..... -3.0 V dc to +0.8 V dc
Case operating temperature range (T_C) ..... -55°C to +125°C

1/ Must withstand the added P_D due to short circuit test (e.g., I_{OS}).
2/ When the thermal resistance for this case is specified in MIL-STD-1835, that value shall supercede the value indicated herein.
3/ Maximum junction temperature may be increased to +175°C during burn-in and steady state life.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein. Product built to this drawing that is produced by a Qualified Manufacturer Listing (QML) certified and qualified manufacturer or a manufacturer who has been granted transitional certification to MIL-PRF-38535 may be processed as QML product in accordance with the manufacturers approved program plan and qualifying activity approval in accordance with MIL-PRF-38535. This QML flow as documented in the Quality Management (QM) plan may make modifications to the requirements herein. These modifications shall not affect form, fit, or function of the device. These modifications shall not affect the PIN as described herein. A "Q" or "QML" certification mark in accordance with MIL-PRF-38535 is required to identify when the QML flow option is used.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535, appendix A and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.2 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full (case or ambient) operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are described in table I.

3.5 Marking. Marking shall be in accordance with MIL-PRF-38535, appendix A. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103 (see 6.6 herein). For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device.

3.6 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6 herein). The certificate of compliance submitted to DESC-EC prior to listing as an approved source of supply shall affirm that the manufacturer's product meets the requirements of MIL-PRF-38535, appendix A and the requirements herein.

3.7 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change. Notification of change to DESC-EC shall be required in accordance with MIL-PRF-38535, appendix A.

3.9 Verification and review. DESC, DESC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

4.3 Quality conformance inspection. Quality conformance inspection shall be in accordance with method 5005 of MIL-STD-883 including groups A, B, C, and D inspections. The following additional criteria shall apply.

4.3.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurement) shall be measured only for the initial test and after process or design changes which may affect input capacitance.

d. Subgroups 7 and 8 shall include verification of the truth table.

TABLE I. Electrical performance characteristics.

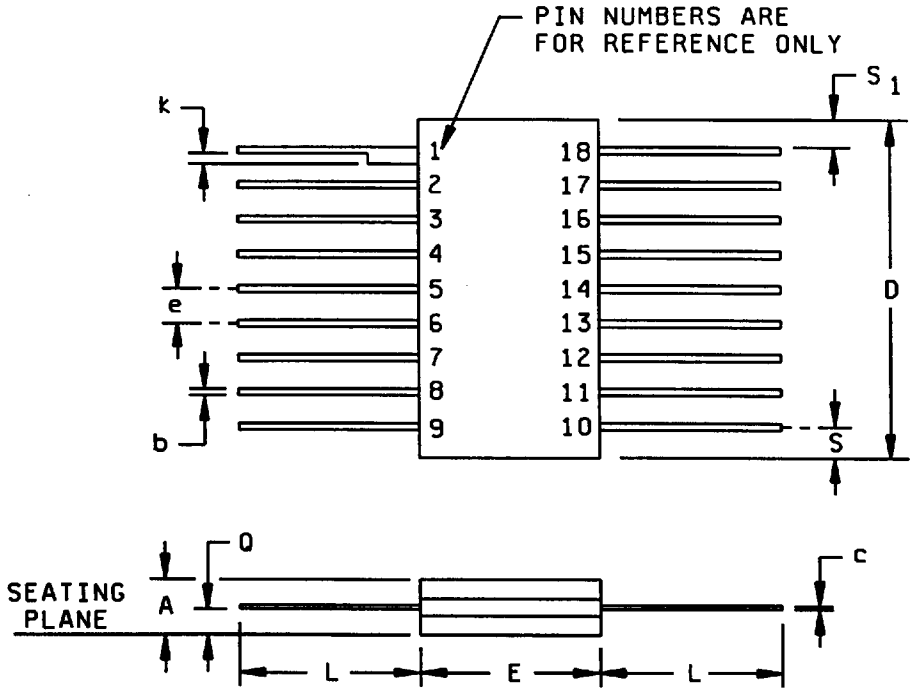
Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Output high voltage	V_{OH}	V_{CC} = 4.5 V, I_{OH} = -4.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All	2.4		V
Output low voltage	V_{OL}	V_{CC} = 4.5 V, I_{OH} = 12.0 mA, V_{IL} = 0.8 V, V_{IH} = 2.0 V	1, 2, 3	All		0.4	V
Input load current	I_I	0 V $\le V_{IN} \le$ 5.5 V	1	All	-10	10	µA
Output current, high impedance	I_{OZ}	GND $\le V_{OUT} = V_{CC}$, output disabled	1, 2, 3	All	- 50	50	µA
Output short-circuit output current 1/ 2/	I_{OS}	V_{CC} = 5.5 V, V_{OUT} = 0 V	1, 2, 3	All		-350	mA
Power supply current	I_{CC}	$\overline{CE} = \overline{WE} = V_{IL}$ = 5.0 V, f = 0 Hz, V_{CC} = 5.5 V, I_{OUT} = 0 mA, $A_0 - A_{11} = V_{IL}$ and V_{IH}	1, 2, 3	01,02		110	mA
				03		120	
Automatic $\overline{CE}$ power down current	I_{SB}	V_{CC} = 5.5 V, $\overline{CE} \ge V_{IH}$ 3/	1, 2, 3	All		10	mA
Input capacitance	C_{IN}	V_{CC} = 5.5 V, f = 1.0 Mhz, T_A =+25° C, see 4.3.1c	4	01,02		5.0	pF
				03		7.0	
Output capacitance	C_{OUT}		4	01,02		6.0	
				03		9.0	
Functional tests		See 4.3.1d	7, 8A, 8B	All			
Read cycle time	t_{RC}	See figures 4 and 5 4/	9, 10, 11	01	45		ns
				02,03	35		
Address valid to data valid	t_{AA}		9, 10, 11	01		45	
				02,03		35	
Data hold from address change	t_{OHA}		9, 10, 11	01,02	5.0		
				03	3.0		
Chip enable low to data valid	t_{ACE}		9, 10,11	01		45	
				02,03		35	
Chip enable low to low Z	t_{LZCE}	See figures 4 and 5 2/ 4/ 6/	9, 10, 11	01,02	5.0		
				03	2.0		
Chip enable high to high Z	t_{HZCE}	See figures 4 and 5 2/ 5/ 6/	9, 10, 11	All		30	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - continued.

Test	Symbol	Conditions $-55°C \le T_C \le +125°C$ unless otherwise specified	Group A subgroups	Device Type	Limits		Unit
					Min	Max	
Chip enable low to power up	t_{PU}	See figures 4 and 5 2/ 4/	9, 10, 11	All	0		ns
Chip enable high to power down	t_{PD}		9, 10, 11	All		20	
Write cycle time	t_{WC}	See figures 4 and 6 4/	9, 10, 11	01	45		
				02,03	35		
Chip enable low to write end	t_{SCE}		9, 10, 11	01	45		
				02,03	35		
Address set-up to write end	t_{AW}		9, 10, 11	01	45		
				02,03	35		
Address hold from write end	t_{HA}		9, 10, 11	All	0		
Address set-up to write start	t_{SA}		9, 10, 11	All	0		
Write enable pulse width	t_{PWE}		9, 10, 11	01	25		
				02,03	20		
Data set-up to write end	t_{SD}		9, 10, 11	01	25		
				02,03	20		
Data hold from write end	t_{HD}		9, 10, 11	All	10		
Write enable high to low Z	t_{LZWE}	See figures 4 and 6 2/ 4/ 6/	9, 10,11	All	0		
Write enable low to high Z	t_{HZWE}	See figures 4 and 6 2/ 5/ 6/	9, 10,11	01		25	
				02,03		20	

1/ Not more than one output should be shorted at a time, and duration of short circuit shall not exceed 30 seconds.
2/ If not tested, shall be guaranteed to limits specified in table I.
3/ A pull-up resistor to V_{CC} on the $\overline{CE}$ input is required to keep the device deselected during V_{CC} power-up, otherwise I_{SB} will exceed value given.
4/ Test conditions assume signal transition times of 5.0 ns or less. Timing is referenced at input and output levels of 1.5 V and input pulse levels of 0 to 3.0 V. Output loading is equivalent to the specified I_{OL}/I_{OH} with a load capacitance of 30 pF.
5/ Test conditions assume signal transition times of 5.0 ns or less. Transition is measured at steady state high level of -500 mV or steady state low level of +500 mV on the output from 1.5 V level on the input with a load capacitance of 5.0 pF.
6/ At any given temperature and voltage condition, t_{HZ} is less than t_{LZ} for any given device.



Symbol	Inches		Millimeters	
	Min	Max	Min	Max
A	.045	.090	1.14	2.29
b	.015	.019	0.38	0.48
c	.004	.009	0.10	0.23
D	.480	.520	12.19	13.21
e	.045	.055	1.14	1.40
E	.250	.300	6.35	7.62
k	.005	.015	0.13	0.38
L	.250	.350	6.35	8.89
Q	.026	.040	0.66	1.02
S	---	.085	---	2.16
S1	.005	---	0.13	---

NOTE: Metric equivalents are given for general information only.

FIGURE 1. Case outline X.

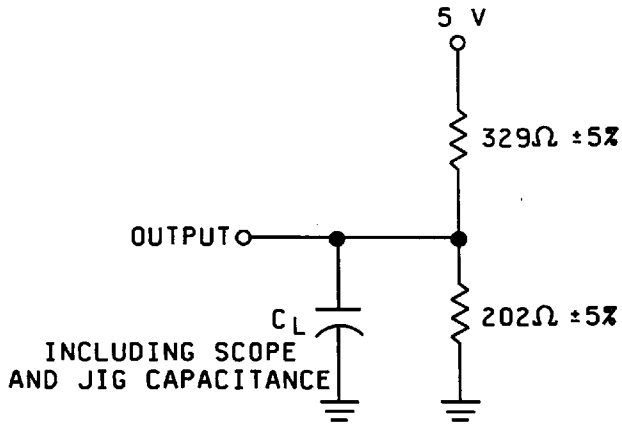
Device types	All
Case outlines	V, X, and Y
Terminal number	Terminal symbol
1	A_0
2	A_1
3	A_2
4	A_3
5	A_4
6	A_5
7	D_0
8	$\overline{WE}$
9	GND
10	$\overline{CE}$
11	D_I
12	A_{11}
13	A_{10}
14	A_9
15	A_8
16	A_7
17	A_6
18	V_{CC}

FIGURE 2. Terminal connections.

$\overline{CE}$	$\overline{WE}$	Mode	Output	Power
H	X	Not selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	D_{OUT}	Active

H = Logic 1 state
L = Logic 0 state
X = Don't care
High Z = High impedance state

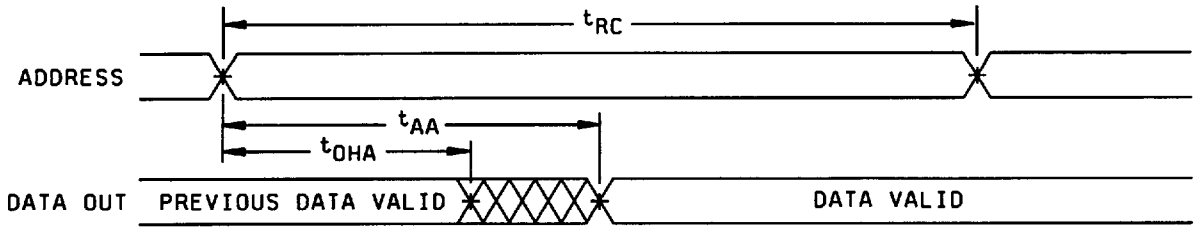
FIGURE 3. Truth table.



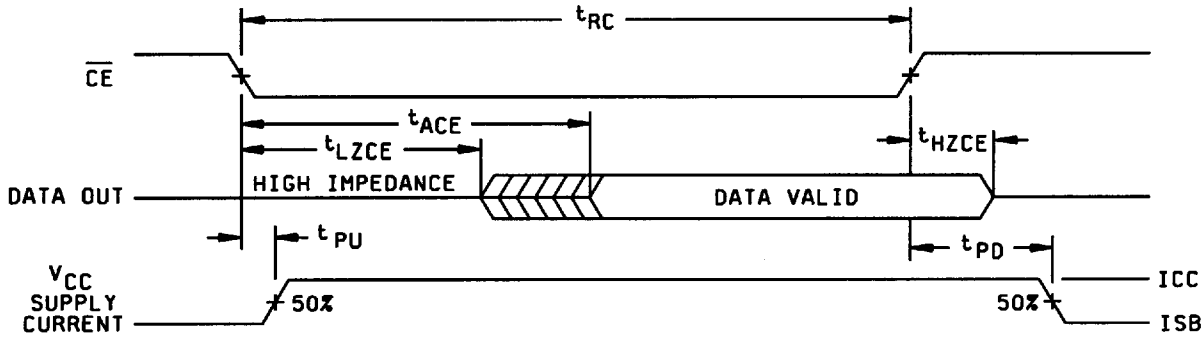
Measurement	C_L including scope and jig capacitance (minimum)
t_{HZCE} and t_{HZWE}	C_L = 5.0 pF
All others	C_L = 30 pF

FIGURE 4. Output load circuit.

Read cycle 1 (See notes 1 and 2)



Read cycle 2 (See notes 1 and 3)

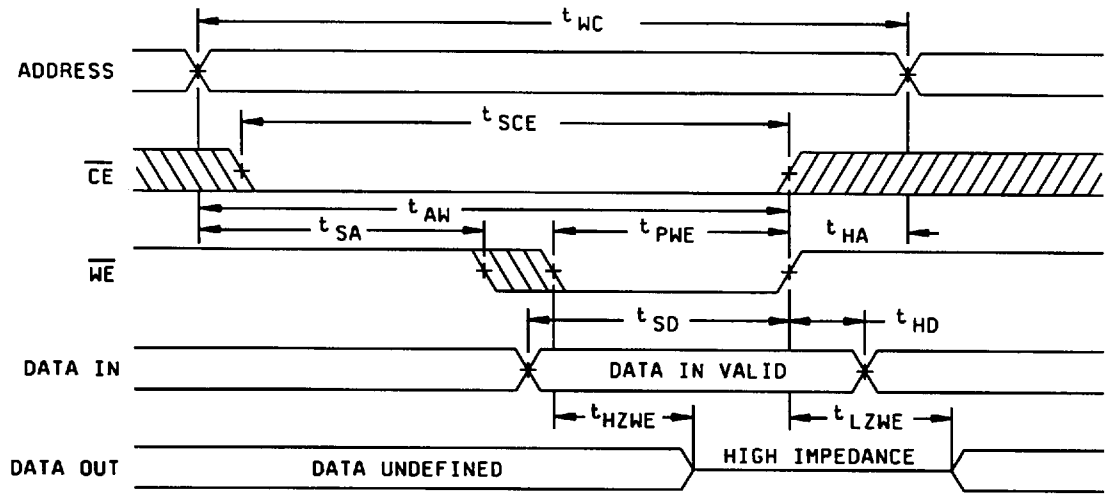


NOTES:

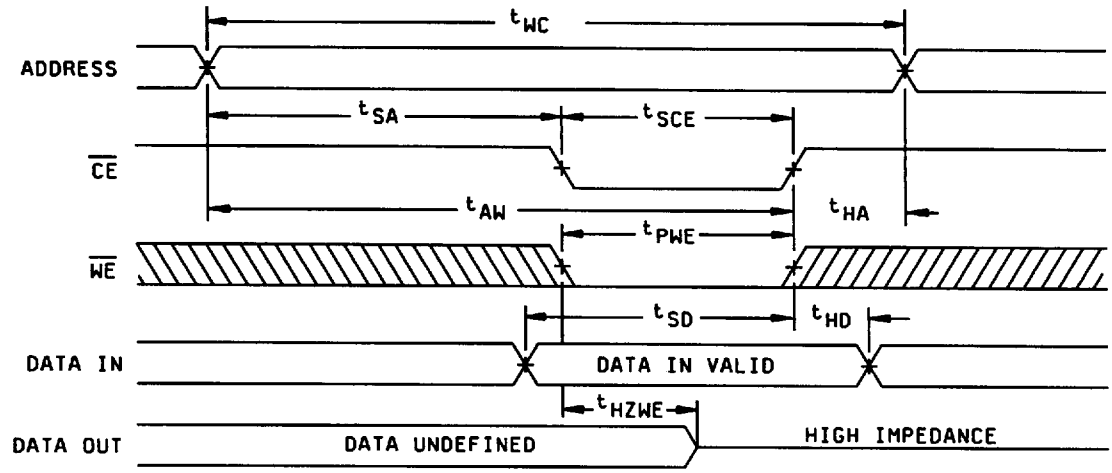
1. $\overline{WE}$ is HIGH for read cycle.
2. Device is continuously selected, $\overline{CE}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

FIGURE 5. Read cycle timing diagram.

Write cycle 1 - $\overline{WE}$ controlled (See note 1)



Write cycle 2 - $\overline{CE}$ controlled (See notes 1 and 2)



NOTES:
1. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
2. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high impedence state.

FIGURE 6. Write cycle timing diagram.

TABLE II. Electrical test requirements.

MIL-STD-883 test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)
Interim electrical parameters (method 5004)	
Final electrical test parameters (method 5004)	1*, 2, 3, 7*, 8A, 8B, 9, 10, 11
Group A test requirements (method 5005)	1, 2, 3, 4**, 7, 8A, 8B, 9, 10, 11
Groups C and D end-point electrical parameters (method 5005)	2, 3, 7, 8A, 8B

* PDA applies to subgroup 1 and 7.
**See 4.3.1c.

4.3.2 Groups C and D inspections.

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test conditions, method 1005 of MIL-STD-883.

(1) Test condition C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A = +125°C, minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535, appendix A.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Electronics Supply Center when a system application requires configuration control and the applicable SMD. DESC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronics devices (FSC 5962) should contact DESC-EC, telephone (513) 296-6047.

6.5 Comments. Comments on this drawing should be directed to DESC-EC, Dayton, Ohio 45444-5270, or telephone (513) 296-5377.

6.6 Approved sources of supply. Approved sources of supply are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DESC-EC.