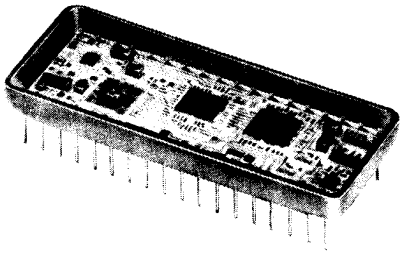
IDC-14542 AND IDC-14544®*

ILC DATA DEVICE CORPORATION



12 AND 14 BIT INDUCTOSYN TO DIGITAL CONVERTER

DESCRIPTION

The IDC-14542 and IDC-14544 are high quality, Inductosyn or resolver to digital converters. Their custom monolithic chip design enables them to be packaged in a 36 pin, hermetically sealed DDIP, which significantly reduces size and weight. These converters are available in 12 or 14 bit resolutions with tracking rates of 100 and 25 rps, and accuracies of ±8.5 and ±5.3 minutes respectively.

The signal and reference frequency range is 600 Hz to 11 kHz for 14 bit units and 360 Hz to 22 kHz for 12 bit units. The 2V line to line input is transient protected voltage follower buffer, resolver format (sine and cosine).

Digital outputs include Count (CB), which is useful for turns counting applications. An Inhibit (INH) input provides a means for freezing parallel data in the transparent latch (figure 1), while the converter continues to track the input. Parallel data, which is

3-state natural binary angle is available in two bytes for interfacing with an 8 bit microprocessor bus. Other control logic inputs include MSB and LSB byte, which control the 3-state operation of two output buffers which may be enabled simultaneously or independently (logic "0"), according to the application.

A unique control transformer algorithm enables the IDC-14542 and IDC-14544 to output highly accurate jitter free data, while the internal type II servo tracking loop permits a DC analog velocity output which exhibits no lag up to the specified tracking rate.

APPLICATIONS

These converters are particularly suited for multi-axis machine tool applications, where accurate and repeatable positioning is required. The IDC-14542 and IDC-14544 will resolve an Inductosyn pitch of 0.1 inch to 24.4 and 6.1 microinches respectively.

Inductosyns have been widely used in high accuracy military applications such as fire control systems and satellite tracking systems.

FEATURES

- *MIL-STD-883B OPTIONAL*
- *100 RPS TRACKING (12 BITS)*
- *12 OR 14 BITS*
- *3-STATE LATCHED OUTPUTS*
- *LOW POWER*
- *OPERATES AT UP TO 20 KHz*

*Patented

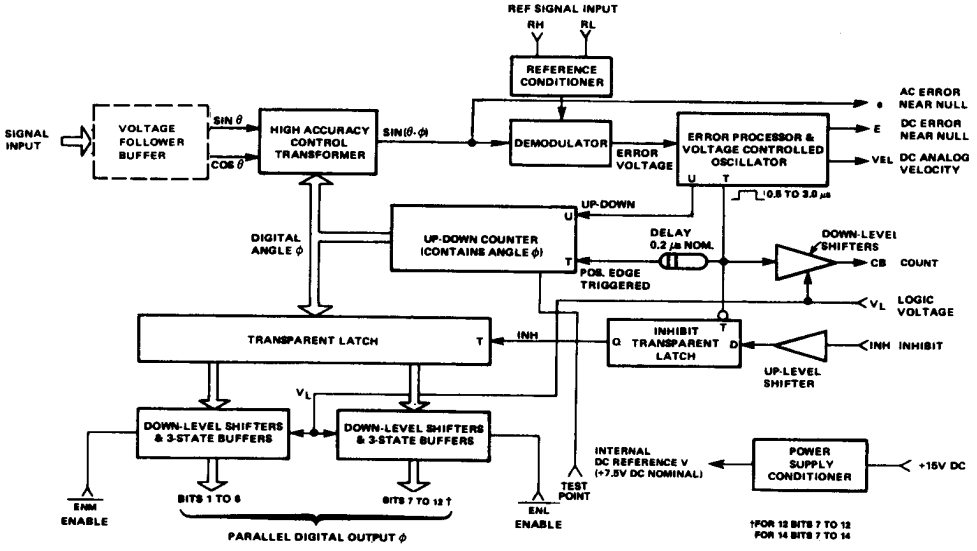


FIGURE 1. BLOCK DIAGRAM

SPECIFICATIONS

Apply over temperature range, power supply range, reference frequency and amplitude range, ±10% signal amplitude variation, and up to 10% harmonic distortion in the reference.

PARAMETER	UNITS	VALUE	
		IDC-14542	IDC-14544
CONVERTER			
RESOLUTION	bits	12	14
ACCURACY	min	±8.5	±5.3
DYNAMIC CHARACTERISTICS			
Input Rate	rps	100	25
Acceleration Constant		K_a=460,000	K_a=370,000
Settling Time (179° step to 1 LSB)	ms	60	90
Velocity Constant		K_v=∞ (No limitation with type II servo loop)	
REFERENCE INPUT			
Carrier Frequency	Hz	360 to 22k	600 to 11k
Voltage Range	V_{rms}	4 to 50 (26 nom)	
Input Impedance			
Single Ended	Ω	50k min	
Differential	Ω	100k min	
Common Mode Range			
(DC Common mode plus recurrent AC peak)	V	60 max	
SIGNAL INPUT CHARACTERISTICS			
Input Signal Type		Sin and cos resolver signals referenced to internal DC reference V	
Voltage Level	V	2 nom, 2.3 max	
Maximum voltage without damage	V	15 rms continuous; 100 peak transient	
Input Impedance	Ω	Z_{in} 20M (transient protected voltage follower)	
DIGITAL INPUT/OUTPUT			
Logic		TTL/CMOS compatible, depending on logic supply voltage	
Inputs			
Inhibit (INH)		Logic "0" inhibits	
Enable Bits 1-6 $\overline{ENM}$		$\overline{ENM}$ and $\overline{ENL}$ [logic "0" Enables, logic "1" high impedance	
Enable Bits 7-12 $\overline{ENL}$			
Enable Bits 7-14 $\overline{ENL}$			
OUTPUTS			
Parallel Data	bits	12 or 14 parallel lines, natural binary angle, positive logic	
Count (CB)		0.7 to 2.0 μsec positive pulse; leading edge initiates counter update	
Drive Capability	TTL	1 std load, 1.6 mA at 0.4 V max (logic "0")	
	TTL	10 std loads, 0.4 mA at 2.8 V min (logic "1")	
	μA	10 max (high impedance)	
ANALOG OUTPUTS			
Internal DC Reference (V)		+15 VDC/2 ~ 7 V nom	
AC Error (e)		10 mV rms per LSB of error (14 bits) 12.5 mV rms per LSB of error (12 bits)	
Filtered DC Error Voltage (E)		−1 VDC per +LSB of error (±3 LSB range), 14 bits −1.25 VDC per +LSB of error (±3 LSB range), 12 bits	
POWER SUPPLY CHARACTERISTICS		+15V Supply	Logic Supply
Nominal Voltage	V	+11 to +16.5	+4.5 to +15
Voltage Range	V	+18	+18
Maximum Voltage Without Damage		25 mA max	Z_{in}=5kΩ min
Current or Impedance			
TEMPERATURE RANGES			
Operating			
−3XX	°C	0 to +70	
−1XX	°C	−55 to +125	
Storage	°C	−55 to +135	
PHYSICAL CHARACTERISTICS			
Package		36 pin DDIP	
Size	in	0.78 x 1.9 x 0.21 (19.7 x 48 x 5.3 mm)	
Weight	oz	1.0 (28 gm)	

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TECHNICAL INFORMATION

DIRECT INPUT

The input of the IDC-14542 and IDC-14544 requires that an external signal conditioner be provided to establish a 2.0 V rms input signal referenced to the converter's internal DC reference (V). Figure 4 suggests a method for amplifying the output of an Inductosyn to meet the required signal input level. The use of this circuit will sufficiently condition the input so resistors R3 and R4 are not needed for most applications.

Trimming should be done by measuring the differential voltage at the input of the op amp closest to the Inductosyn slider (+sin). The output voltage is then measured to determine the gain. The same procedure is performed on the +cos amplifier. A high accuracy digital voltmeter is recommended for the final output readings. Capacitors C1 and C2 are used to create a DC voltage block.

LOGIC INPUT/OUTPUT

Logic outputs consist of 12 or 14 parallel data bits and count (CB). All logic outputs are short-circuit proof to ground and to positive voltages as high as V_L. The CB output is a positive 0.7-2.0μs pulse and data changes about 0.2μs after the leading edge of the pulse, because of an internal delay (figure 1). Data is valid 0.5μs after the leading edge of a CB. Angle is determined by adding bits in the "1" state.

The parallel digital outputs are gated to provide 6 or 8 bit bytes when the MSB byte is enabled ($\overline{ENM}$). The 8 bit byte is reserved for the 14 bit resolution converter only. The LSB byte ($\overline{ENL}$) is gated to provide a 6 bit byte. When the Enables for the gates are at logic "0" the gate outputs are at normal logic "1" or "0", depending on the bit state. When the Enables are at logic "1" the gate outputs are high impedance and the subsystem sees an essentially open line. Outputs are valid 0.5μs after an Enable is driven to logic "0". For 12 and 14 bit parallel output operation, when the 3-state feature is not used, the Enable lines should be tied to logic "0".

The Inhibit (INH) logic input locks the transparent latch so that the bits will remain stable while data is being transferred (see Figure 1). The output is stable 0.5μs after the Inhibit is driven to logic "0". A logic "0" at the T input locks the latch, and a logic "1" allows the bits to change. The purpose of the INH transparent latch is to prevent the transmission of invalid data when there is an overlap between the CB and INH. While the counter is not being updated the CB is at logic "0" and the INH latch is transparent. When the CB goes to logic "1" the INH latch is locked. If a CB occurs after an INH has been applied, the latch will remain locked and its data cannot change until the CB returns to logic "0". If an INH is applied during a CB pulse, the latch will not lock until the CB pulse is over. The purpose of the 0.2μs delay is to prevent a race condition between the CB and the INH in which the up-down counter begins to change just as an INH is applied.

Since the IDC-14542 and IDC-14544 converters contain a CMOS device, standard CMOS handling procedures should be followed.

TIMING

Figure 2 shows the timing waveforms of the converter. Whenever an input angle change occurs, the converter changes the digital angle in 1 LSB steps and generates a converter busy pulse. The output data change is initiated by the leading edge of the CB pulse, delayed by the 0.2μs (nominal) delay. The output becomes stable in less than 0.5μs even though the CB pulse may last longer. Data transfer can be made synchronous with the leading edge of CB, delayed by 0.5μs. (See Timing Diagram.)

An Inhibit input, regardless of its duration, does not affect converter update. A simple method of interfacing to a computer, asynchronous to CB pulse, is to (a) apply the inhibit, (b) wait 1.5 μs min., (c) transfer the data and (d) release the inhibit.

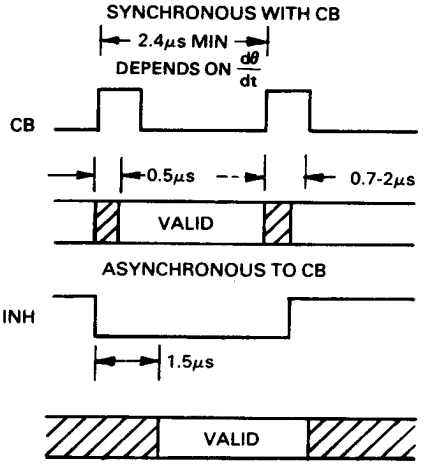
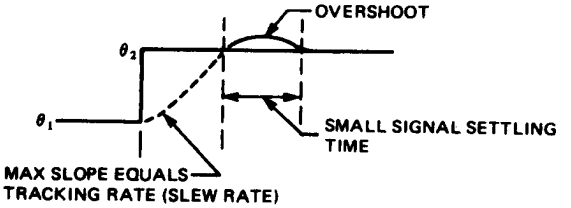


FIGURE 2. TIMING DIAGRAM

DYNAMIC PERFORMANCE

A Type II servo loop ($K_V=\infty$) and very high acceleration constants give these converters superior dynamic performance, as listed in the specifications. If the power supply voltage is not the +15VDC nominal value, the specified input rates for full accuracy will increase or decrease in proportion to the fractional change in voltage.

As long as the maximum tracking rate is not exceeded, there will be no lag in the converter output. If a step input occurs, as is likely when the power is initially turned on, the response will be critically damped. The figure shows the response to a step input. After initial slewing at the maximum tracking rate of the converter, there is one overshoot which is inherent to a Type II servo. The overshoot settling to a final value is a function of the small signal settling time.



RESPONSE TO A STEP INPUT

ANALOG OUTPUTS

The analog outputs are V, e, E and VEL. V is an internal DC reference, ±7 VDC nominal. The outputs e, E and VEL ride on the internal DC reference voltage V, and should be measured with respect to V. Outputs can swing ±5V when the voltage level of the +15V power supply is +15V. The output swing changes proportionally if the level is not a +15V.

AC error (e) is proportional to the error $(\theta-\phi)$ with 10 mV/LSB nominal for the 14 bit unit and 12.5 mV/LSB nominal for the 12 bit units.

E is a filtered DC voltage proportional to the error $(\theta-\phi)$ near the null point, with −1 VDC/+LSB of error for the 14 bit unit and −1.25 VDC/+LSB of error for the 12 bit units.

Velocity output (VEL) is a DC voltage proportional to angular velocity $d\theta/dt=d\phi/dt$. The output is positive for an increasing angle.

Maximum loading for each analog output is 1.0 mA. Outputs e, E, and VEL are not required for normal operation of the converter; V is used as internal DC reference.

The outputs e, E and VEL are not closely controlled or characterized. Consult factory for further information.

$$G=\frac{680^2\left(\frac{S}{300}+1\right)}{S^2\left(\frac{S}{3000}+1\right)} \qquad G=\frac{610^2\left(\frac{S}{300}+1\right)}{S^2\left(\frac{S}{3000}+1\right)}$$

12 BIT **14 BIT**

CONVERTER LOOP DYNAMICS

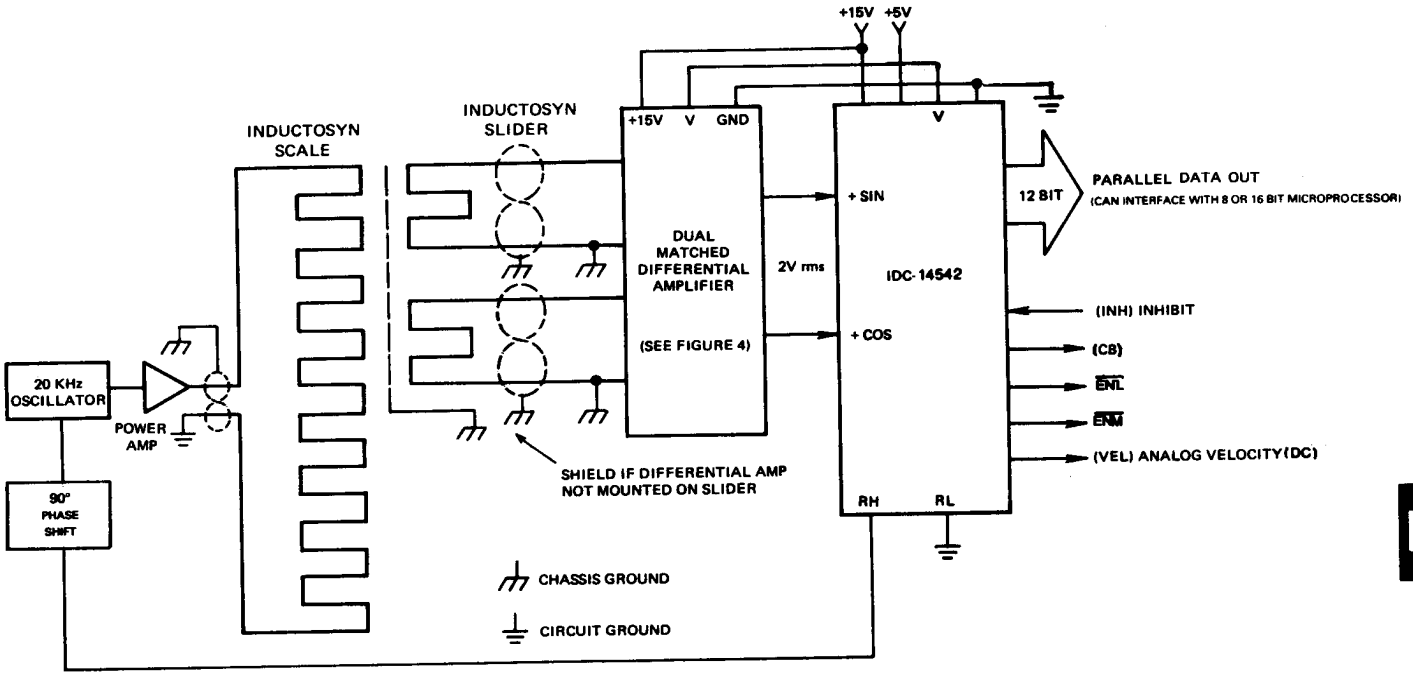


FIGURE 3. INDUCTOSYN CONNECTION DIAGRAM

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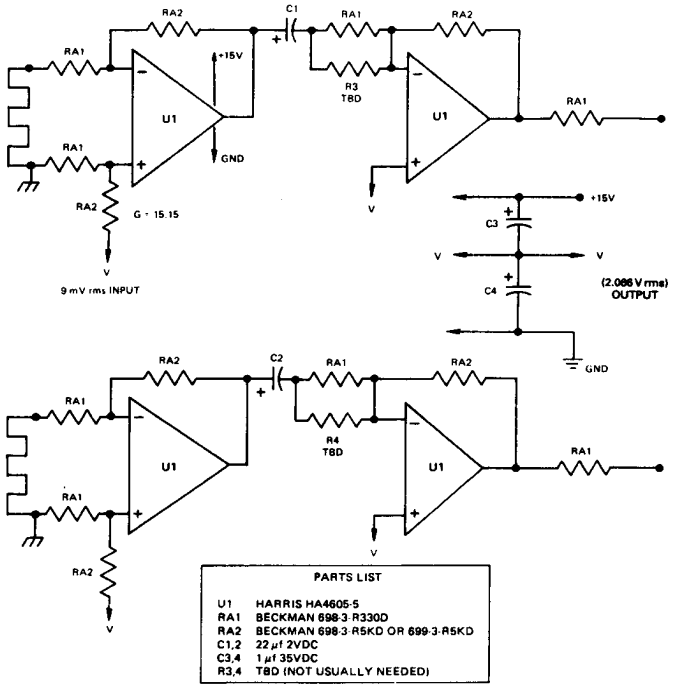

PARTS LIST	
U1	HARRIS HA4605-5
RA1	BECKMAN 698-3-R330D
RA2	BECKMAN 698-3-R5KD OR 699-3-R5KD
C1,2	22 μf 2VDC
C3,4	1 μf 35VDC
R3,4	TBD (NOT USUALLY NEEDED)

NOTES. 1. For other input levels select RA1 and RA2 as required. Standard values are: 100, 200, 330, 470, 500, 1K, 2K, 2.2K, 4.7K, 5K, 10K, 15K, and 20KΩ.
2. For lower input levels use Harris HA-4625-5

FIGURE 4. DUAL PREAMPLIFIER DIAGRAM

PIN CONNECTION TABLE

PIN	FUNCTION	PIN	FUNCTION
	Voltage Follower Buffer	18	Bit 14
		19	RH (Ref High)
1	NC	20	RL (Ref Low)
2	COS	21	N.C.
3	SIN	22	E (Filtered DC Error Out)
4	NC	23	θ (Analog Velocity Out)
5	Bit 1 MSB	24	CB (Converter Busy)
6	Bit 2	25	ENL (Enable, Bits 7 to 14)*
7	Bit 3	26	ENM (Enable, Bits 1 to 6)
8	Bit 4	27	e (AC Error Out)
9	Bit 5	28	V_L (Logic Voltage Input
10	Bit 6	29	GND
11	Bit 7	30	T.P.
12	Bit 8	31	N.C.
13	Bit 9	32	+15V (Power Supply In)
14	Bit 10	33	INH (Inhibit)
15	Bit 11	34	V (Internal DC Ref)
16	Bit 12	35	BC (Buffered Cos)
17	Bit 13	36	BS (Buffered Sin)

NOTES:
BS and BC pins are used in other applications.
*Enable 7 to 12 (IDC-14542)

IN GENERAL

For applications where a square wave is more convenient than the conventional sine wave, the IDC-14542 and IDC-14544 are capable of operating with square waves.

For users who desire a built-in test (BIT) function to detect position error between the input and output, a simple detection circuit can be implemented with the AC error signal provided by the IDC-14542 and IDC-14544 converter. The schematic diagram for the BIT circuit is available from DDC.

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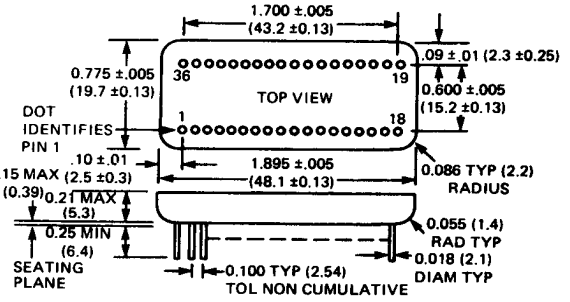
RELIABILITY

MTBF values are very high because the use of custom monolithics greatly decreases the number of active components, because thin film resistor networks are used, and because of careful thermal design. Summaries of MTBF calculations are available on request.

All DDC hybrids are built in accordance with requirements of MIL-STD-883B.

MECHANICAL OUTLINE
36 PIN DOUBLE DIP



NOTES
1. Dimensions shown are in inches. (millimeters)
2. Lead identification numbers are for reference only.
3. Lead cluster shall be centered within ±0.10 of outline dimensions. Lead spacing dimensions apply only at seating plane.
4. Pin material meets solderability requirements of MIL-STD-202E, Method 208C.
5. Package is Kovar with electroless nickel plating.
6. Case is electrically floating.

ORDERING INFORMATION

IDC-1454 X-X X X

- Family Code
- Resolution
  - 2=12 bits
  - 4=14 bits
- Temperature (operating)
  - 1=−55°C to +125°C (Case)
  - 3=0°C to +70°C (Case)
- Reliability Grade:
  - 0 = Screened to MIL-STD-883 but without pre burn-in testing, burn-in, and QCI testing.
  - 1 = Fully compliant with MIL-STD-883.
  - 2 = Screened to MIL-STD-883 but without QCI testing.
- Accuracy:
  - 2=±8.5′ (12 bit only)
  - 3=±5.3′ (14 bit only)