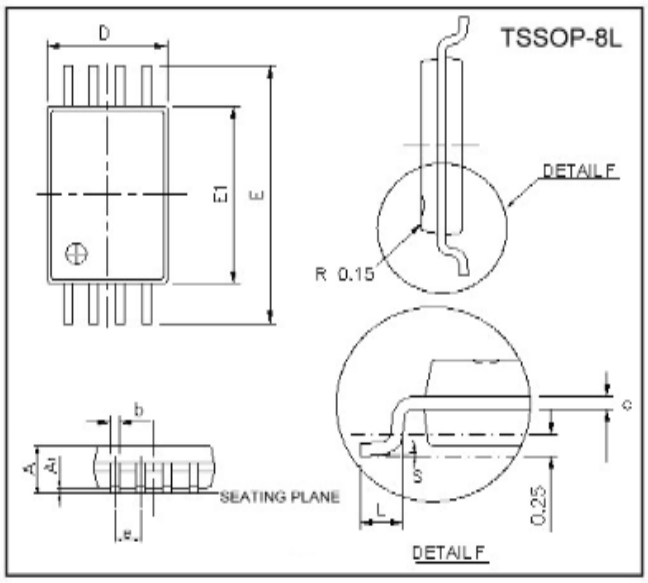
20V Dual N-Channel Enhancement Mode MOSFET

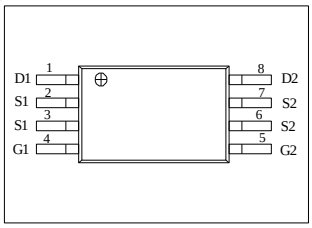
VDS= 20V
RDS(ON), Vgs@1.8V, Ids@2A = 50mΩ
RDS(ON), Vgs@2.5V, Ids@5.5A = 32mΩ
RDS(ON), Vgs@4.5V, Ids@6.6A = 24mΩ

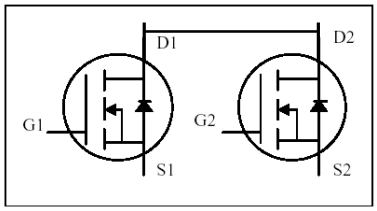
Features

Advanced trench process technology
High Density Cell Design For Ultra Low On-Resistance

Ideal for Li ion battery pack applications
Package Dimensions







REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	1.10 MAX.		L	0.45 REF.	
A1	0	0.10	L1	0.60 REF.	
A2	0.70	1.00	θ	0°	10°
c	0.12 REF.		b	0.30	0.50
D	2.70	3.10	e	0.95 REF.	
E	2.60	3.00	e1	1.90 REF.	
E1	1.40	1.80			

Maximum Ratings and Thermal Characteristics (TA = 25oC unless otherwise noted) 25 °C

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	± 12	
Continuous Drain Current		I_D	7	A
Pulsed Drain Current		I_{DM}	25	
Maximum Power Dissipation	TA = 25°C	P_D	2	W
	TA = 75°C		1.2	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to 150	°C
Junction-to-Ambient Thermal Resistance (PCB mounted)		$R_{\theta JA}$	62.5	°C/W

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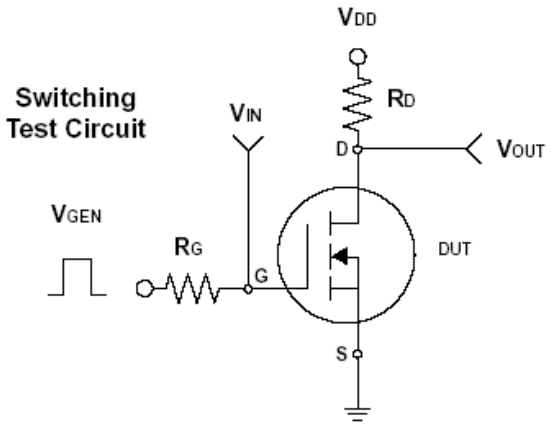
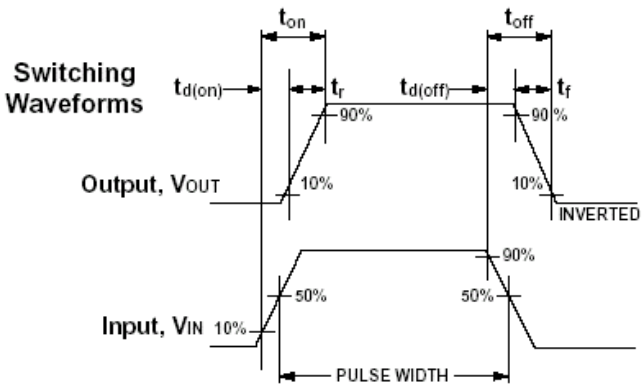
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 250uA	20			V
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 1.8V, I_D = 2A		36.0	50.0	mΩ
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 2.5V, I_D = 5.5A		25.0	32.0	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 4.5V, I_D = 6.6A		19.0	24.0	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} =V_{GS}, I_D = 250uA	0.4		1	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20V, V_{GS} = 0V			1	uA
Gate Body Leakage	I_{GSS}	V_{GS} = ± 12V, V_{DS} = 0V			±100	nA
Forward Transconductance	g_{fs}	V_{DS} = 5V, I_D = 7A		17.7	__	S
Dynamic						
Total Gate Charge	Q_g	V_{DS} = 10V, I_D = 7A V_{GS} = 4.5V		8.19	10	nC
Gate-Source Charge	Q_{gs}			1		
Gate-Drain Charge	Q_{gd}			1.93		
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 10V, I_D = 1A, V_{GEN} = 4.5V R_G = 6Ω		10.87		ns
Turn-On Rise Time	t_r			6.03		
Turn-Off Delay Time	$t_{d(off)}$			28.07		
Turn-Off Fall Time	t_f			4.33		
Input Capacitance	C_{iss}	V_{DS} = 10V, V_{GS} = 0V f = 1.0 MHz		836.88		pF
Output Capacitance	C_{oss}			126.53		
Reverse Transfer Capacitance	C_{rss}			92.78		
Source-Drain Diode						
Max. Diode Forward Current	I_S				2.5	A
Diode Forward Voltage	V_{SD}	I_S = 1A, V_{GS} = 0V			1.2	V

Note: Pulse test: pulse width <= 300us, duty cycle<= 2%





20V Dual N-Channel Enhancement Mode MOSFET

Characteristics Curve

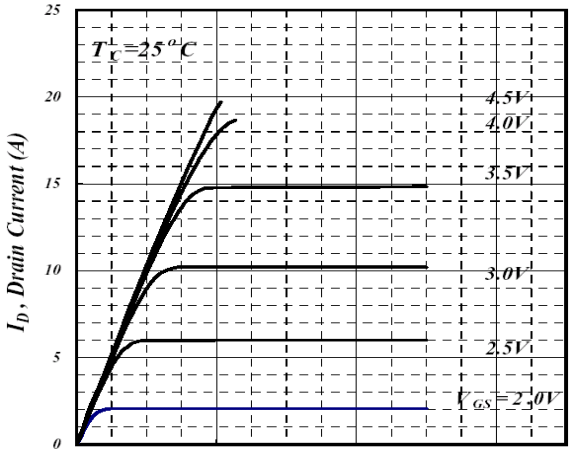


Fig 1. Typical Output Characteristics

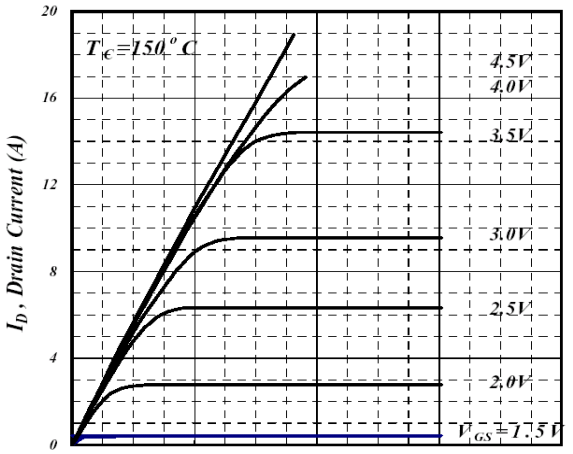


Fig 2. Typical Output Characteristics

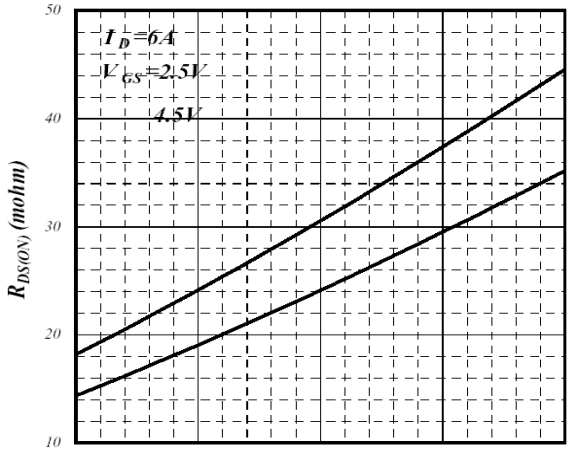


Fig 3. R_{DSON} v.s. Junction Temperature

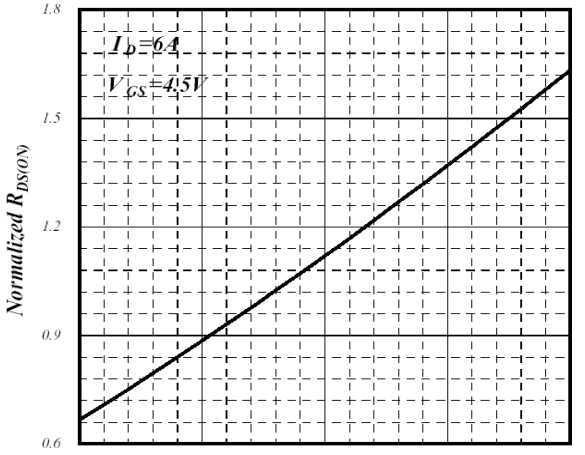


Fig 4. Normalized On-Resistance v.s. Junction Temperature

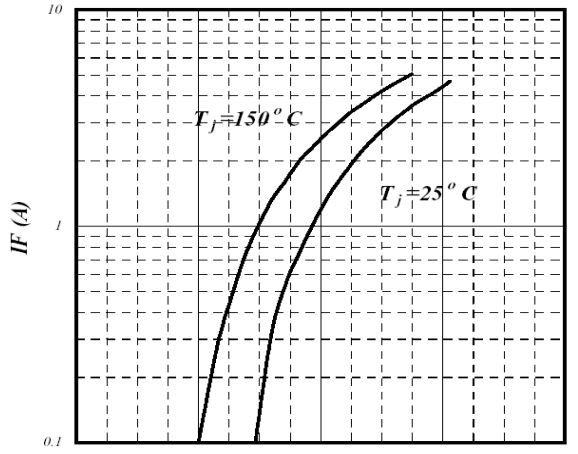


Fig 5. Forward Characteristics of Reverse Diode

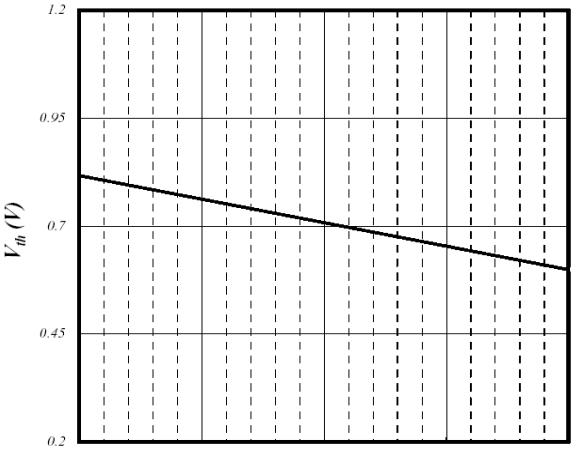


Fig 6. Gate Threshold Voltage v.s. Junction Temperature