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SYM53C040 **Data Sheet**

Symbios SYM53C040
Enclosure Services Processor

Overview

The SYM53C040 is a highly integrated single-chip enclosure services processor, with the flexibility to implement SCSI drive enclosure management functions such as SAF-TE (SCSI Accessed Fault-Tolerant Enclosure) or SES (SCSI-3 Enclosure Services). The industry standard SAF-TE and SES protocols are used to detect drive presence, conditioning a slot for drive insertion/removal, fan speed control, power supply voltage monitoring, door lock status and usage statistics.

Hardware Features

- A flexible single-chip processor solution capable of implementing SAF-TE or SES protocols AND working in either parallel SCSI or serial Fibre Channel environments

- Integrated LVDlink™ transceivers for direct attach to either low voltage differential (LVD) or single-ended (SE) SCSI busses

- Supports the SFF-8067 environment interface for Fibre Channel enclosures

- Programmable multi-purpose I/O pins (MPIO) and multi-purpose LED pins (MPLED) for OEM specific monitoring
  - 28 MPIO for enclosure sensory inputs
  - 24 MPLED with programmable blink rates for displaying status events

- Two multi-master 2 wire serial interfaces for chip configuration, firmware downloading, and access to external 2 wire peripherals

- Recommended for use with SYM53C120 and/or SYM53C141 SCSI bus expanders

- Integrated MCS® 51 micro controller

- Internal SYM53C80 SCSI protocol controller

- Ability to set SCSI ID in upper byte lane

- IEEE 1149.1 JTAG compliant

- Packaged in a 160 PQFP or 169 PBGA

Applications

- Server clustering environments

- JBOD or RAID storage enclosures

- Fibre Channel or SCSI enclosures

Figure 1 on page two, is an example of a SCSI storage enclosure implementing the SYM53C040, the SYM53C141/120 SCSI bus expanders, and the SYM8951U/22910 PCI-Ultra2 SCSI host adapters. By way of the MPIO pins, the SYM53C040 monitors the environment within the enclosure, such as temperature, power supply status, disk slot status, etc. Then, during regular intervals, the status information is sent to the host controller via the SCSI bus. Likewise, in response to commands sent by the host controller, the SYM53C040 uses the MPIO and MPLED pins to enable or disable enclosure elements, such as disk slots, enclosure key lock, individual drive key locks, indicator displays, SCSI bus expanders, etc.
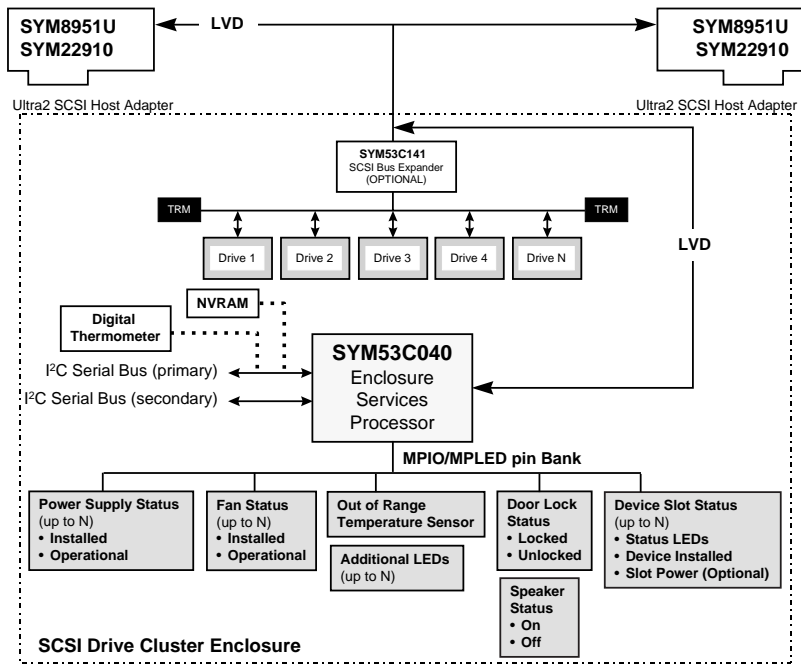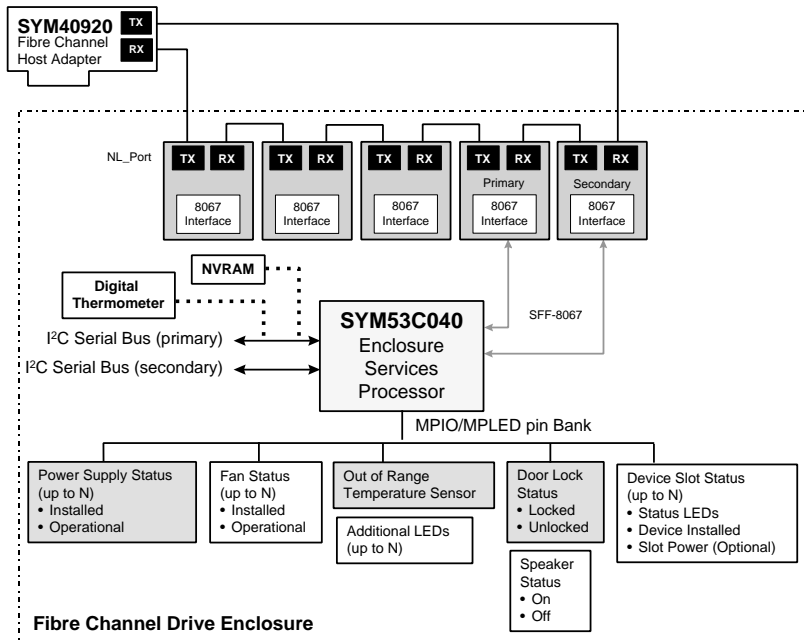
Figure 1: SCSI storage enclosure

Figure 2: Fibre Channel storage enclosure

Figure 2 is an example of a Fibre Channel storage enclosure implementing the SYM53C040. As in Figure 1, the SYM53C040 is collecting sensory inputs and reporting this information back to the host system. However, in this configuration, it communicates this information via the SFF-8067 interface. The drive acts as a conduit in passing commands and data between the host and enclosure.
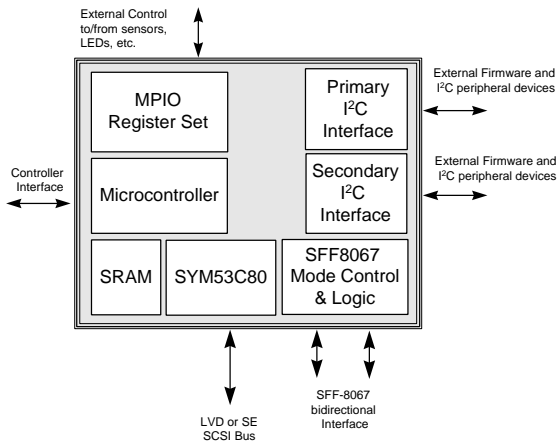
Figure 3: SYM53C040 block diagram

Figure 3 shows the functional block diagram for the SYM53C040. In order to achieve functionality and flexibility, the SYM53C040 incorporates an integrated SYM53C80 SCSI protocol controller, a MCS-51 family compatible micro controller, internal Static RAM, two 2 wire serial interfaces and multi-purpose I/O registers connected to the MPIO and MPLED pins. Below is a brief description of each element.

SYM53C80:

The SYM53C80 is an 8-bit asynchronous SCSI core which supports ultra SCSI speeds. The core contains support for a DMA interface and additional support for micro controller interrupts. The SYM53C040 uses the dedicated DMA interface and MCS® 51 micro controller for memory accesses to/from the SCSI core.

Micro Controller:

The micro controller is an 8-bit Intel MCS® 51 compatible device. The micro controller is operated with a 20 MHz CPU clock in the SYM53C040 derived from the 40 MHz ESP system clock. This micro controller uses a shared address/data bus and can address either 64K of shared program and data memory or 64 K each of separate program and data memory spaces.

2 Wire Serial Interfaces:

The SYM53C040 has two 2 wire Serial Interface blocks. Access to external serial EEPROM storage and any other user-defined 2 wire peripheral devices is provided by the 2 wire Serial Interface blocks. As a default, the SYM53C040 will attempt to download from an external serial configuration ROM through one 2 wire interface at power-on or after a reset.

MPIO Banks:

The SYM53C040 provides up to 28 separate multi-purpose I/O (MPIO) signal pins and 24 multi-purpose LED (MPLED) pins. For design flexibility, the MPLED pins can, if desired, be used as additional multi-purpose

I/O pins. The I/O pins are firmware programmable to configure the SYM53C040 to meet many possible monitoring combinations. As a result, numerous configurations of drives, fans, and power supplies can be supported given the total number of MPIO and MPLED pins.

SFF-8067 Mode Control & Logic Interface:

This mode is a configuration option determined at power on. In operation, the SFF-8067 interface is used instead of the SCSI interface. A transfer sequence is initiated upon assertion of Parallel_ESI by the drive. The host initiates all read and write operations. The drive does not initiate any activity, but does control the bi-directional interface. The back plane uses SEL_N to specify the loop identifier for the drive.
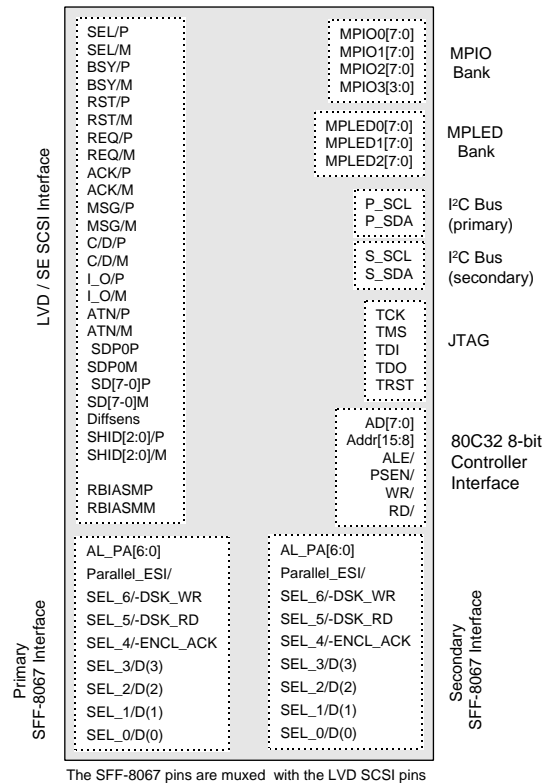

The SFF-8067 pins are muxed with the LVD SCSI pins

Figure 4: Functional signal grouping

Technical Information

Firmware protocol:	SAF-TE, SES
Monitoring capability:	28 programmable MPIO pins 24 programmable MPLED pins
Input clock:	40 MHz
Package:	160 Plastic Quad Flat Pack (PQFP) 169 Plastic Ball Grid Array (PBGA)
Complementary products:	SYM53C120 (SE to SE or SE to HVD) SYM53C141 (SE to SE or SE to LVD) For electrical and logical isolation of SCSI Bus segments

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