MSM62705/62720

CMOS SINGLE-CHIP MICROCOMPUTER FOR IC CARD

GENERAL DESCRIPTION

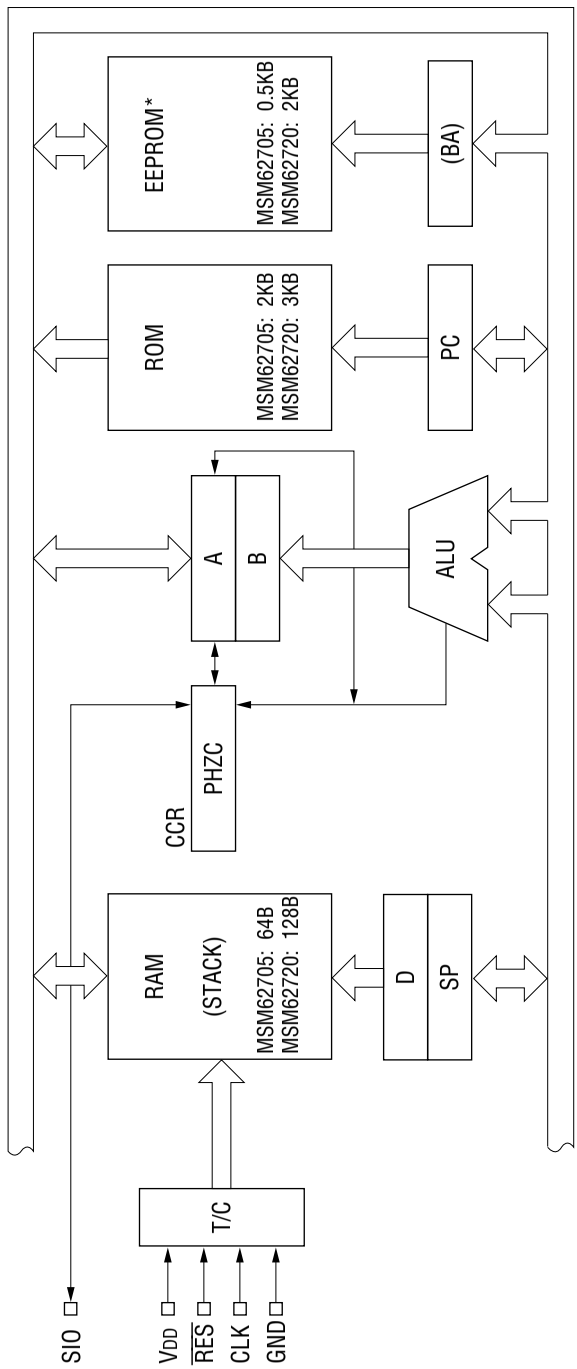
The MSM62705/62720 is CMOS 8-bit single-chip microcomputer developed for IC cards. MSM62705 is the smallest die size in the Oki IC card MCU series.

FEATURES

- ROM : MSM62705: 2048 bytes, MSM62720: 3072 bytes
- EEPROM : MSM62705: 512 bytes, MSM62720: 2048 bytes
- RAM : MSM62705: 64 bytes, MSM62720: 128 bytes
- Clock frequency : 5.0 MHz maximum
- Instruction execution time : 800 ns minimum at 5.0 MHz
- Number of instructions : 100
- Power supply voltage : 5 V±10% (single power supply)
- Number of pins : 5
- Operating temperature range : 0°C to 70°C

1) CMOS original single-chip microcomputer
2) Simple architecture allowing easy programming
3) Instruction sets allowing a high ROM usage efficiency, SIN, SOUT, DLY, bit manipulation, index addressing, 1-byte call, auto increment, auto decrement, and 16-bit operation instruction
4) Error correction circuit (ECC)

BLOCK DIAGRAM



* The contents of EEPROM cannot be executed as instructions.

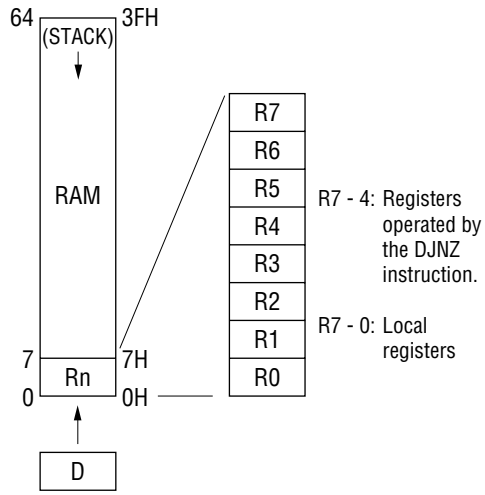
A	: Accumulator	P	: Parity flag
ALU	: Arithmetic and logic unit	PC	: Program counter
B	: B register (auxiliary)	RAM	: Random access memory (data memory)
(BA)	: Paired register of A and B	$\overline{\text{RES}}$	: Reset pin
C	: Carry flag	ROM	: Read-only memory (program memory)
CCR	: Condition code register	SIO	: Serial input/output pin
CLK	: Clock input pin	SP	: Stack pointer
D	: D register (data pointer)	(STACK)	: Stack memory
EEPROM	: Electrically erasable and programmable ROM (nonvolatile data memory)	T/C	: Timing and control circuit
		V_{DD}	: Power pin (5V)
GND	: Power pin (0V)	Z	: Zero flag
H	: Half carry flag		

PIN DESCRIPTION

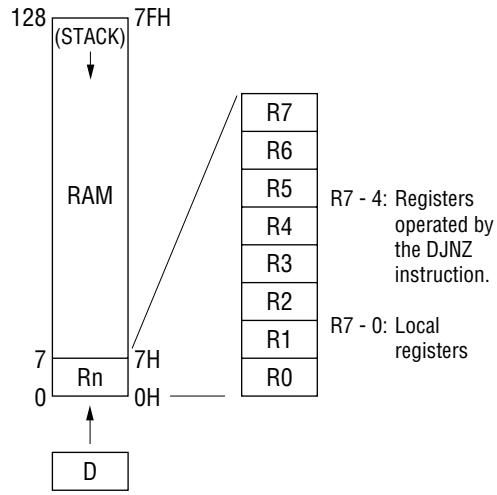
Description	Input/Output	Function
SIO	Input/Output	Serial data input/output port. Pseudo bidirectional I/O port. Set "1" level after "Reset". (Pulled up to V_{DD} by an Internal approx. 10kΩ resistor.)
V_{DD}	—	Main power source
GND	—	Circuit GND
$\overline{RES}$	Input	Reset input pin. (Pulled down to GND by an internal approx. 1.5 MΩ resistor.)
CLK	Input	Clock input pin. (Pulled down to GND by an internal approx. 1.5 MΩ resistor).

RAM CONFIGURATION

MSM62705

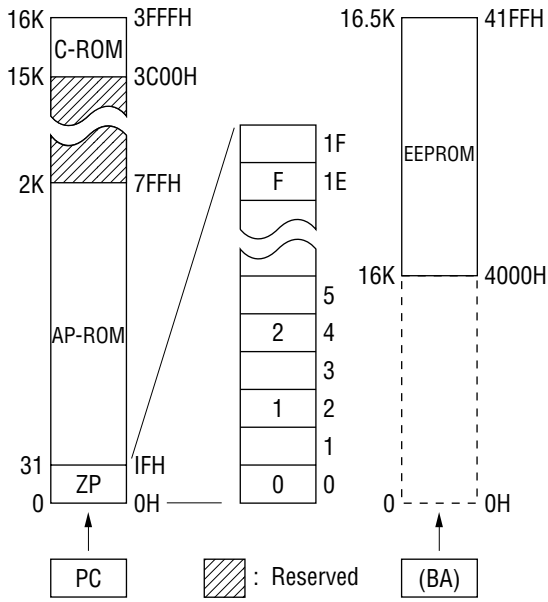


MSM62720



CONFIGURATIONS OF ROM AND EEPROM

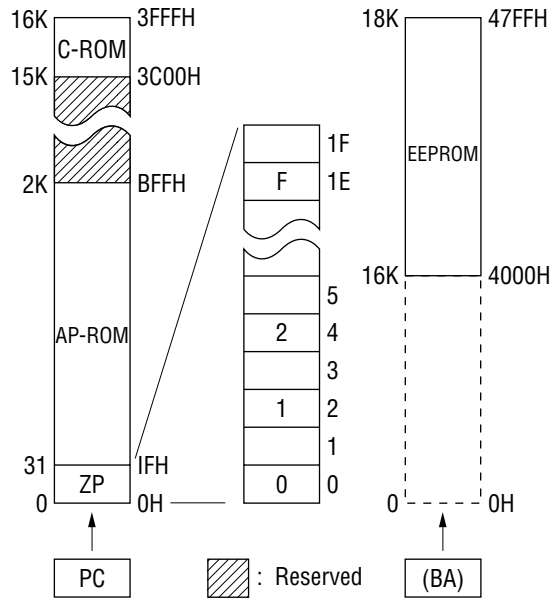
MSM62705



ZP: Zero page address called by the CZP instruction.
C-ROM: Control ROM area
AP-ROM: Application ROM area

(a) ROM (b) EEPROM

MSM62720



ZP: Zero page address called by the CZP instruction.
C-ROM: Control ROM area
AP-ROM: Application ROM area

(a) ROM (b) EEPROM

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Supply Voltage	V_{DD}	Ta=25°C	–0.5 to +7	V
Input Voltage	V_{IN}		–0.5 to V_{DD}+0.5	
Output Voltage	V_{OUT}		–0.5 to V_{DD}+0.5	
Storage Temperature	T_{STG}	—	–55 to +150	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Condition	Range	Unit
Supply Voltage	V_{DD}	—	4.5 to 5.5	V
Operating Temperature	T_{op}		0 to +70	°C
EEPROM Data Hold Temperature	T_{EEH}			

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD}=5 V±10%, Ta=0 to +70°C)

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Current		I_{DD}	f_{CLK}=5 MHz	—	6.0	10	mA
"L" Input Voltage	CLK	V_{IL}	—	–0.3	—	0.5	V
	$\overline{RES}$			–0.3	—	0.6	
	SIO			–0.3	—	0.8	
"H" Input Voltage	CLK	V_{IH}	—	2.4	—	V_{DD}+0.3	V
	$\overline{RES}$			4	—	V_{DD}+0.3	
	SIO			2.0	—	V_{DD}+0.3	
"L" Output Voltage		V_{OL}	I_{OL} max=1.6 mA	0	—	0.4	V
"H" Output Voltage		V_{OH}	I_{OH} max=–100 µA	2.4	—	V_{DD}	V
Input Current (CLK, $\overline{RES}$)		I_{IH1}	V_{DD}=V_I=5.5 V	—	—	10	µA
		I_{IL1}	V_{DD}=5.5 V, V_I=0.0 V	—	—	–10	µA
Input Current (SIO)		I_{IH2}	V_{DD}=V_I=5.5 V	—	—	10	µA
		I_{IL2}	V_{DD}=5.5 V, V_I=0.0 V	—	—	–1	mA
Input Capacitance		C_I	f=1 MHz, Ta=25°C	—	—	20	pF
Output Capacitance		C_O	f=1 MHz, Ta=25°C	—	—	20	pF

Note: CLK, $\overline{RES}$ has pull-down resistor, and SIO has pull-up resistor.

AC Characteristics

(V_{DD}=5 V±10%, Ta=0 to +70°C)

Parameter	Symbol	Min.	Typ.	Max.	Unit
CLK Cycle Time	t_{CYC}	200	—	—	ns
CLK Low Level Time	t_{CL}	0.4*t_{CYC}	—	0.6*t_{CYC}	
CLK High Level Time	t_{CH}	0.4*t_{CYC}	—	0.6*t_{CYC}	
CLK Rise Time	t_{CR}	—	—	1.0	
CLK Fall Time	t_{CF}	—	—	1.0	
$\overline{RES}$ Pulse Width	t_{RW}	8*t_{CYC}	—	—	
SIO Rise Time (Input)	t_{SIR}	—	—	1.0	
SIO Fall Time (Input)	t_{SIF}	—	—	1.0	
SIO Rise Time (Output)	t_{SOR}	—	—	1.0	
SIO Fall Time (Output)	t_{SOF}	—	—	1.0	

Note: At output load capacitance Co=30 pF

TIMING CHARTS