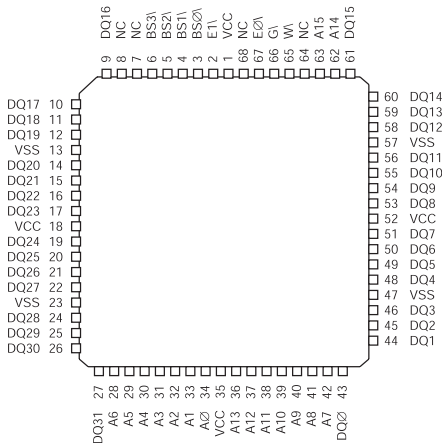




FEATURES

- 128Kx32 bit CMOS Static
- Analog SHARC™ External Memory Solution
 - ADSP-21060L
 - ADSP-21062L
- Random Access Memory Array
 - Fast Access Times: 12,15 and 20ns
 - User Configurable Organization with Minimal Additional Logic
 - Master Output Enable and Write Control
 - TTL Compatible Inputs and Outputs
 - Fully Static, No Clocks
- Surface Mount Package
 - 68 Lead PLCC, No. 99 (JEDEC MO-47AE)
 - Small Footprint, 0.990 Sq. In.
 - Multiple Ground Pins for Maximum Noise Immunity
- Single 3.3V (±5%) Supply Operation

PIN CONFIGURATIONS AND BLOCK DIAGRAM



Note: Pin 2 & 67 on the 64Kx32 (EDI8L3265C) and the 256Kx32 (EDI8L32256C) are word select pins.

128KX32 CMOS HIGH SPEED STATIC RAM

The EDI8L32128V is a high speed, 3.3 volt, four megabit density Static RAM. The device is available with access times of 12, 15 and 20ns, allowing the device to support 60MHz DSPs with no wait states. The high speed, 3.3V supply voltage and byte configurability make the device ideal for interfacing with Analog Devices ADSP-21062L or ADSP-21060L SHARC DSPs.

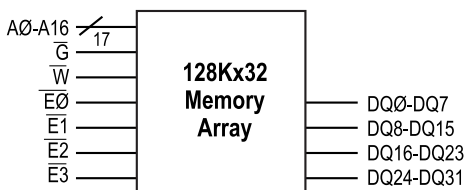
The device can be configured as a 128Kx32 and used to create a single chip external data memory solution for the SHARC (figure 1). Providing a 51% space savings when compared to four 128Kx8, 400mil wide plastic SOJs. the EDI8L32128V has a 10pf load on the data lines vs. 24pf for four plastic SOJs. Memory upgrades in the same footprint can be accomplished with the EDI8L32256V (256Kx32) or the EDI8L32512V (512KX32). This is covered in detail in the application report "The EDI's x32 MCM-L SRAM Family: Integrated Memory Solution for the Analog SHARC DSP"

Alternatively the device's chip enables can configure it as a 256Kx16. A 256Kx48 program memory array for the SHARC is created using three devices (figure 2). If this memory is too deep, two 128Kx24's (EDI8L24128V) can be used to create a 128Kx48 memory array.

Note: Solder Reflow temperature should not exceed 260°C for 10 seconds

PIN NAMES

- A0-A16 Address Inputs
- E0-E3 Chip Enables (One per Byte)
- W Master Write Enable
- OE Master Output Enable
- DQ0-DQ31 Common Data Input/Output
- VCC Power (+3.3V±10%)
- VSS Ground
- NC No Connection





ABSOLUTE MAXIMUM RATINGS*

| | |
|------------------------------------|-----------------|
| Voltage on any pin relative to VSS | -0.5V to 4.6V |
| Operating Temperature TA (Ambient) | |
| Commercial | 0°C to + 70°C |
| Industrial | -40°C to +85°C |
| Storage Temperature | -55°C to +125°C |
| Power Dissipation | 3 Watts |
| Output Current. | 20 mA |
| Junction Temperature, TJ | 175°C |

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

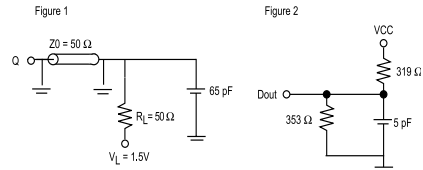
RECOMMENDED DC OPERATING CONDITIONS

| Parameter | Sym | Min | Typ | Max | Units |
|--------------------|-------|-------|-----|---------|-------|
| Supply Voltage | VCC3. | 1.35V | 3.3 | 3.465V | V |
| Supply Voltage | VSS | 0 | 0 | 0 | V |
| Input High Voltage | VIH | 2.2 | -- | VCC+0.3 | V |
| Input Low Voltage | VIL | -0.3 | -- | 0.8 | V |

AC TEST CONDITIONS

| | |
|--------------------------------|-------------|
| Input Pulse Levels | VSS to 3.0V |
| Input Rise and Fall Times | 5ns |
| Input and Output Timing Levels | 1.5V |
| Output Load | Figure 1 |

(note: For TEHQZ, TGHQZ and TWLQZ, CL = 5pF) (see figure 2)



DC ELECTRICAL CHARACTERISTICS

| Parameter | Sym | Conditions | Min | Max | | | Units |
|----------------------------------|------|-------------------------------------------------------------------------------|-----|----------|-----|-----|---------|
| | | | | 12 | 15 | 20 | |
| Operating Power Supply Current | ICC1 | $\overline{W} = VIL, I/O = 0mA,$ Min Cycle | | 680 | 660 | 620 | mA |
| Standby (TTL) Supply Current | ICC2 | $\overline{E} \geq VIH, VIN \leq VIL$ or $VIN \geq VIH, f = \emptyset MHz$ | | 120 | 120 | 120 | mA |
| Full Standby CMOS Supply Current | ICC3 | $\overline{E} \geq VCC-0.2V$ $VIN \geq VCC-0.2V$ or $VIN \leq 0.2V$ | | 40 | 40 | 40 | mA |
| Input Leakage Current | ILI | $VIN = 0V$ to VCC | | ± 10 | | | μA |
| Output Leakage Current | ILO | $V I/O = 0V$ to VCC | | ± 10 | | | μA |
| Output High Voltage | VOH | $IOH = -4.0mA$ | 2.4 | | | | V |
| Output Low Voltage | VOL | $IOL = 8.0mA$ | | 0.4 | | | V |

Typical: TA=25°C, VCC=3.3V

TRUTH TABLE

| \overline{G} | \overline{E} | \overline{W} | Mode | Output | Power |
|----------------|----------------|----------------|-----------------|--------|------------|
| X | H | X | Standby | High Z | ICC2, ICC3 |
| H | L | H | Output Deselect | High Z | ICC1 |
| L | L | H | Read | DOUT | ICC1 |
| X | L | L | Write | DIN | ICC1 |

CAPACITANCE

(f=1.0MHz, VIN=VCC or VSS)

| Parameter | Sym | Max | Unit |
|-----------------------------|-------------------------------|-----|------|
| Address Lines | CA | 40 | pF |
| Data Lines | CD/Q | 10 | pF |
| Write & Output Enable Lines | $\overline{W}, \overline{G}$ | 40 | pF |
| Chip Enable Lines | $\overline{E0}-\overline{E3}$ | 8 | pF |

These parameters are sampled, not 100% tested.

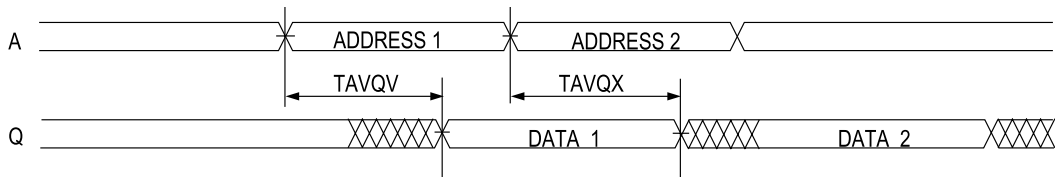


AC CHARACTERISTICS READ CYCLE

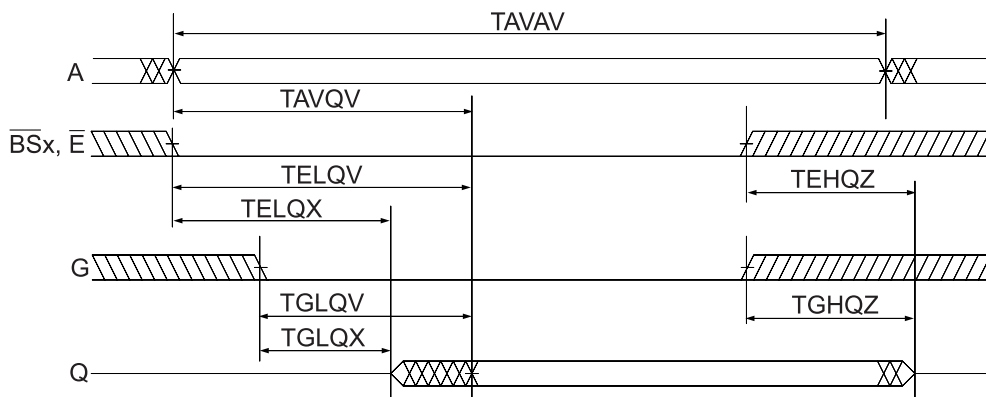
| Parameter | Symbol | | 12ns | | 15ns | | 20ns | | Units |
|---------------------------------------|--------|------|------|-----|------|-----|------|-----|-------|
| | JEDEC | Alt. | Min | Max | Min | Max | Min | Max | |
| Read Cycle Time | TAVAV | TRC | 12 | | 15 | | 20 | | ns |
| Address Access Time | TAVQV | TAA | | 12 | | 15 | | 20 | ns |
| Chip Enable Access Time | TELQV | TACS | | 8 | | 10 | | 20 | ns |
| Chip Enable to Output in Low Z (1) | TELQX | TCLZ | 2 | | 3 | | 3 | | ns |
| Chip Disable to Output in High Z (1) | TEHQZ | TCHZ | | 7 | | 8 | | 10 | ns |
| Output Hold from Address Change | TAVQX | TOH | 3 | | 3 | | 3 | | ns |
| Output Enable to Output Valid | TGLQV | TOE | | 5 | | 6 | | 8 | ns |
| Output Enable to Output in Low Z (1) | TGLQX | TOLZ | 2 | | 2 | | 2 | | ns |
| Output Disable to Output in High Z(1) | TGHQZ | TOHZ | | 4 | | 5 | | 8 | ns |

Note 1: Parameter guaranteed, but not tested.

READ CYCLE 1 - \overline{W} HIGH, \overline{G} , \overline{E} LOW



READ CYCLE 2 - \overline{W} HIGH



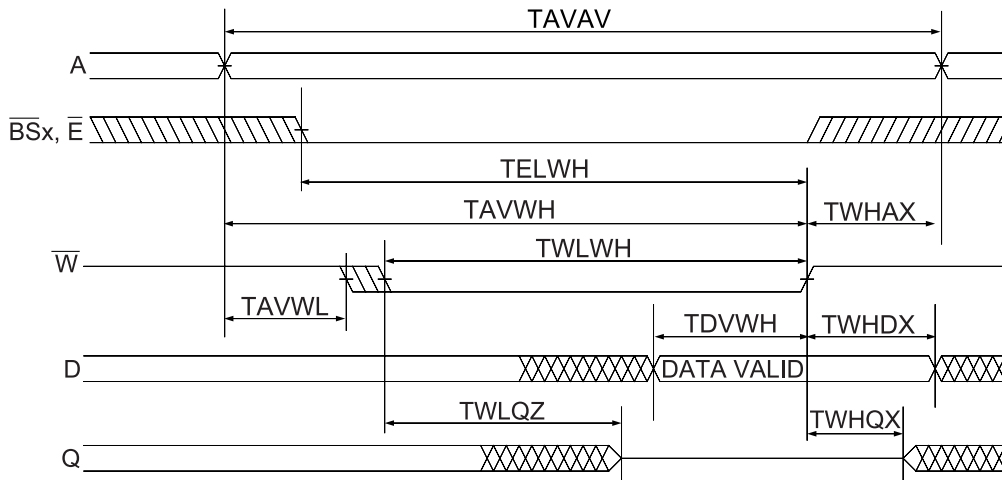


AC CHARACTERISTICS WRITE CYCLE

| Parameter | Symbol | | 12ns | | 15ns | | 20ns | | Units |
|-------------------------------------|--------|------|------|-----|------|-----|------|-----|-------|
| | JEDEC | Alt. | Min | Max | Min | Max | Min | Max | |
| Write Cycle Time | TAVAV | TWC | 12 | | 15 | | 20 | | ns |
| Chip Enable to End of Write | TELWH | TCW | 8 | | 9 | | 15 | | ns |
| | TELEH | TCW | 8 | | 9 | | 15 | | ns |
| Address Setup Time | TAVWL | TAS | 0 | | 0 | | 0 | | ns |
| | TAVEL | TAS | 0 | | 0 | | 0 | | ns |
| Address Valid to End of Write | TAVWH | TAW | 9 | | 10 | | 15 | | ns |
| | TAVEH | TAW | 9 | | 10 | | 15 | | ns |
| Write Pulse Width | TWLWH | TWP | 9 | | 10 | | 15 | | ns |
| | TWLEH | TWP | 9 | | 10 | | 15 | | ns |
| Write Recovery Time | TWHAX | TWR | 0 | | 0 | | 0 | | ns |
| | TEHAX | TWR | 0 | | 0 | | 0 | | ns |
| Data Hold Time | TWHDX | TDH | 0 | | 0 | | 0 | | ns |
| | TEHDX | TDH | 0 | | 0 | | 0 | | ns |
| Write to Output in High Z (1) | TWLQZ | TWHZ | 0 | 5 | 0 | 6 | 0 | 7 | ns |
| Data to Write Time | TDVWH | TDW | 5 | | 6 | | 8 | | ns |
| | TDVEH | TDW | 5 | | 6 | | 8 | | ns |
| Output Active from End of Write (1) | TWHQX | TWLZ | 2 | | 2 | | 2 | | ns |

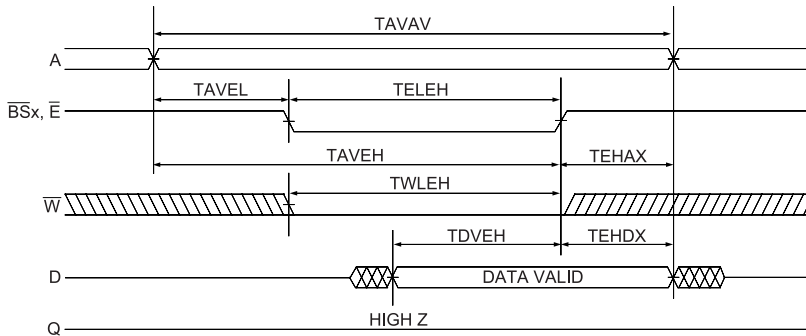
Note 1: Parameter guaranteed, but not tested.

WRITE CYCLE 1 - \overline{W} CONTROLLED





WRITE CYCLE 2 - E CONTROLLED



ORDERING INFORMATION

Commercial (0°C to 70°C)

Industrial (-40°C to +85°C)

Table with 3 columns: Part Number, Speed (ns), Package No. for Commercial versions.

Table with 3 columns: Part Number, Speed (ns), Package No. for Industrial versions.

PACKAGE DESCRIPTION

Package No. 99
68 Lead PLCC
JEDEC MO-47AE

THETA JA=40°C/W
THETA Jc=15°C/W
WEIGHT =4.2G

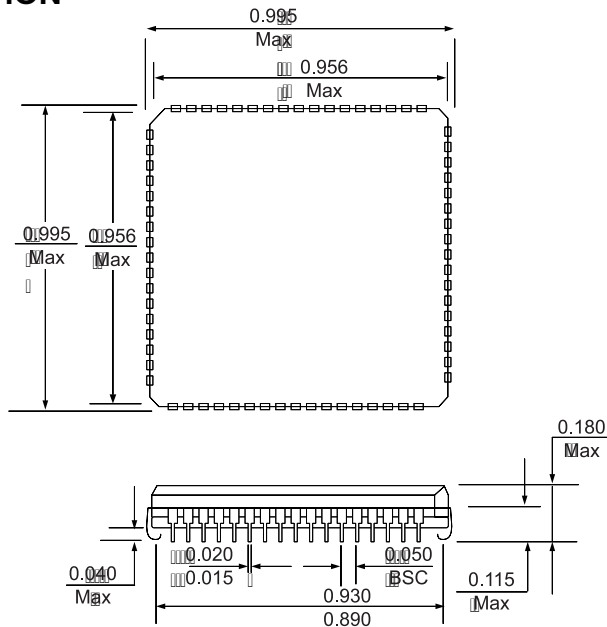




Figure 1

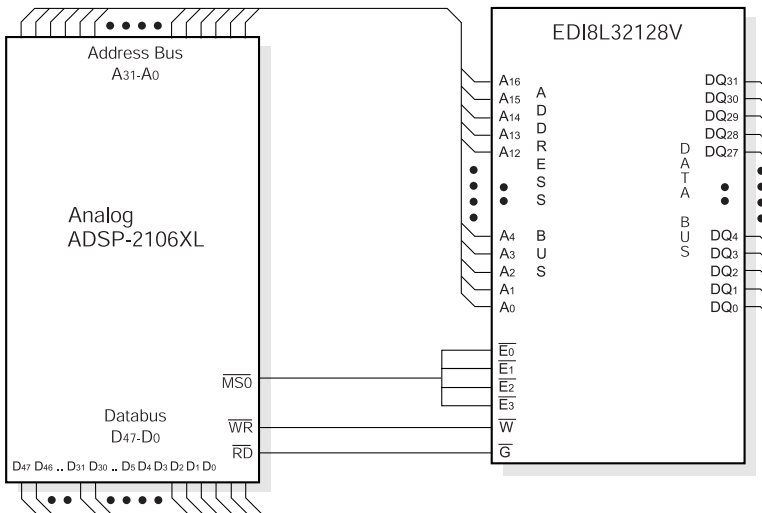


Figure 2

