T-46-13-27

CATALYST SEMICONDUCTOR
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CAT28C256
32K x 8 BIT CMOS E²PROM

DESCRIPTION

The CAT28C256 is a fast, low power, 5V-only CMOS E²PROM organized as 32,768 words by 8 bits. It requires a simple interface for in-system programming. On-chip address and data latches, self-timed write cycle with auto-clear and Vcc power up/down write protection eliminate additional timing and protection hardware. Data Polling and Toggle status bits signal the start and end of the self-timed write cycle. Additionally, the CAT28C256 features hardware and software write protection as well as an internal Error Correction Code (ECC) for extremely high reliability.

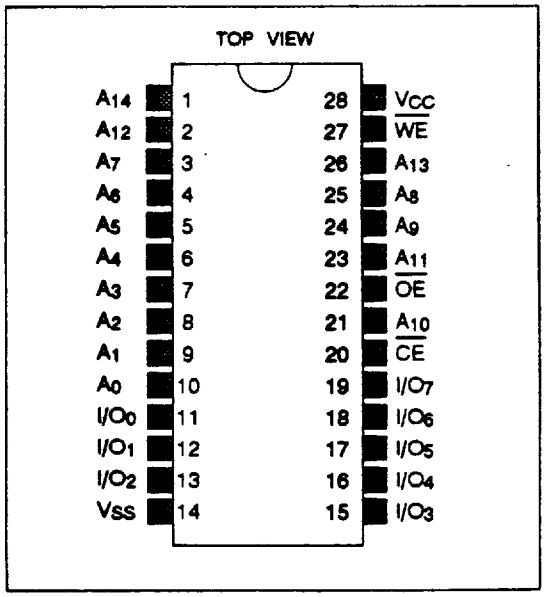
Manufactured using Catalyst's Advanced CMOS floating gate technology, the device can endure 10,000 erase/write cycles and has a data retention of 100 years. The CAT28C256 is assembled in either a 28-pin PDIP or CERDIP, or a 32-pin PLCC or LCC package.

FEATURES

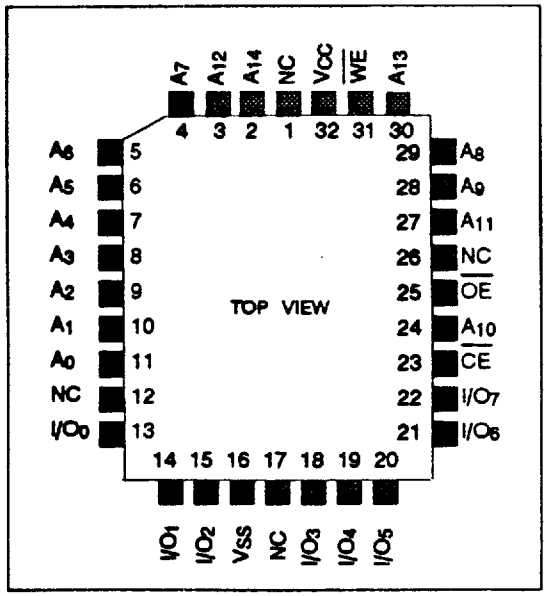
- Fast Read Access Times: 200/250/300 ns
- Low CMOS Power Dissipation:
  - Active: 30mA max
  - Standby: 150µA max
- Simple Write Operation:
  - -On-Chip Address and Data Latches
  - -Self-Timed Write Cycle with Auto-Clear
- Fast Nonvolatile Write Cycle:
  - -10ms max (5ms available)
- Automatic Page Write Operation:
  - -1 to 64 Bytes in 10ms
  - -Page Load Timer
- Hardware and Software Write Protection
- End of Write Detection:
  - -Toggle Bit
  - -Data Polling
- CMOS and TTL Compatible I/O
- JEDEC Approved PDIP, CERDIP, PLCC and LCC packages
- 10,000 Rewrites/byte
- 100 Year Data Retention

PIN CONFIGURATION

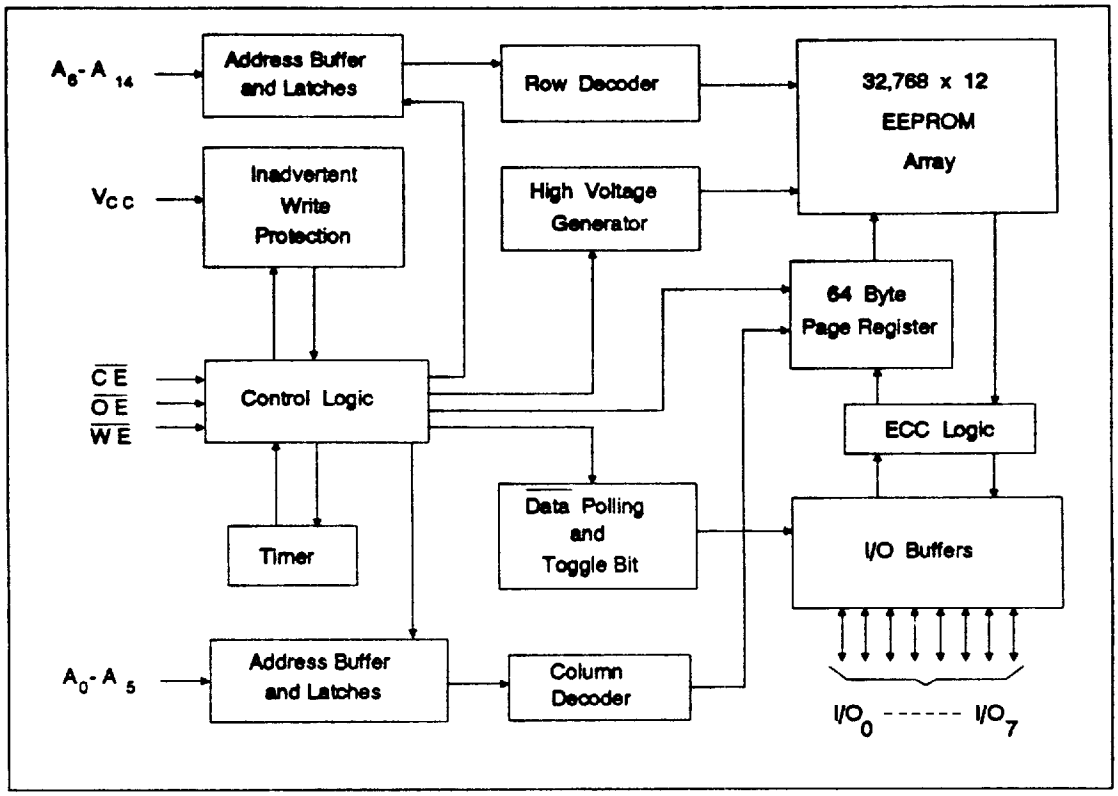
28-Pin PDIP and CERDIP



32-Pin PLCC and LCC



BLOCK DIAGRAM



PIN NAMES

A_0 - A_{14}	Address Inputs
I/O_0 - I/O_7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS *

Temperature under bias	-10°C to +85°C
Storage temperature	-65°C to +150°C
Voltage on any input pin relative to V_{SS}	-0.3 to V_{CC} +0.3V
Voltage on any output pin relative to V_{SS}	-0.3 to V_{CC} +0.3V

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	Conditions	Limits Min.	Limits Max.	Unit
I_{CC}	V_{CC} Current (operating, TTL)	$\overline{CE}$=$\overline{OE}$=V_{IL}, f= 5MHz, all I/O's open		30	mA
I_{SB}	V_{CC} Current (standby, TTL)	$\overline{CE}$ = V_{IH} all I/O's open		1	mA
I_{SBC}	V_{CC} Current (standby, CMOS)	$\overline{CE}$ = V_{IHC}** all I/O's open		150	µA
I_{LI}	Input Leakage Current	V_{IN} = GND to V_{CC}	-1	1	µA
I_{LO}	Output Leakage Current	V_{OUT} = GND to V_{CC}, $\overline{CE}$ = V_{IH}	-10	10	µA
V_{IH}	High Level Input Voltage		2.0	V_{CC} +0.3	V
V_{IL}	Low Level Input Voltage		-0.3	0.8	V
V_{OH}	High Level Output Voltage	I_{OH} = -400µA	2.4		V
V_{OL}	Low Level Output Voltage	I_{OL} = 2.1mA		0.4	V
V_{WI}	Write Inhibit Voltage		3.5	4.0	V

NOTE:

* V_{ILC} = -0.3V to +0.3V

** V_{IHC} = V_{CC} - 0.3V to V_{CC} + 0.3V

CAPACITANCE

(T_A = 25°C, f = 1.0 MHz, V_{CC} = 5V)

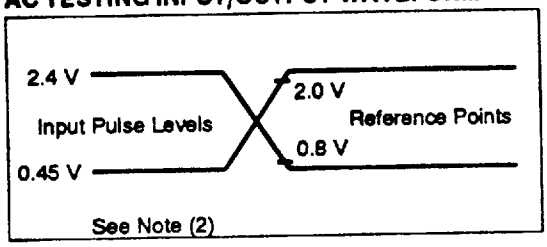
Symbol	Parameter	Conditions	Limits Max.	Unit
$C_{I/O}$ (1)	Input/Output capacitance	$V_{I/O}$ = 0V	10	pF
C_{IN} (1)	Input capacitance	V_{IN} = 0V	10	pF

NOTE: (1) These parameters are tested initially or after a change that affects the parameter.

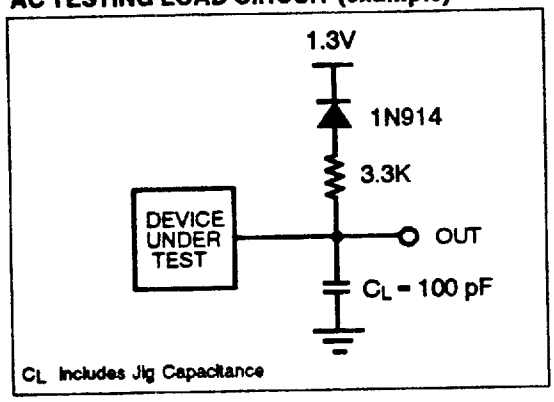
MODE SELECTION

Mode	$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	I/O	Power
Read	L	H	L	D_{OUT}	ACTIVE
Byte write ($\overline{WE}$ controlled)	L	⎍	H	D_{IN}	ACTIVE
Byte write ($\overline{CE}$ controlled)	⎍	L	H	D_{IN}	ACTIVE
Standby, and Write inhibit	H	X	X	HIGH-Z	STANDBY
Read and Write inhibit	X	H	H	HIGH-Z	ACTIVE

AC TESTING INPUT/OUTPUT WAVEFORM



AC TESTING LOAD CIRCUIT (example)



AC CHARACTERISTICS <Read Cycle>

(V_{CC} = +5V ±10%, T_A = 0°C to +70°C)

Symbol	Parameter	28C256-20 min	28C256-20 max	28C256-25 min	28C256-25 max	28C256-30 min	28C256-30 max	Units
t_{RC}	Read Cycle Time	200		250		300		ns
t_{CE}	$\overline{CE}$ Access Time		200		250		300	ns
t_{AA}	Address Access Time		200		250		300	ns
t_{OE}	$\overline{OE}$ Access Time		80		100		110	ns
t_{LZ}	$\overline{CE}$ Low to Active Output [1]	0		0		0		ns
t_{OLZ}	$\overline{OE}$ Low to Active Output [1]	0		0		0		ns
t_{HZ}	$\overline{CE}$ High to High-Z Output [1],[3]		50		50		55	ns
t_{OHZ}	$\overline{OE}$ High to High-Z Output [1],[3]		50		50		55	ns
t_{OH}	Output Hold from Address Change [1]	0		0		0		ns

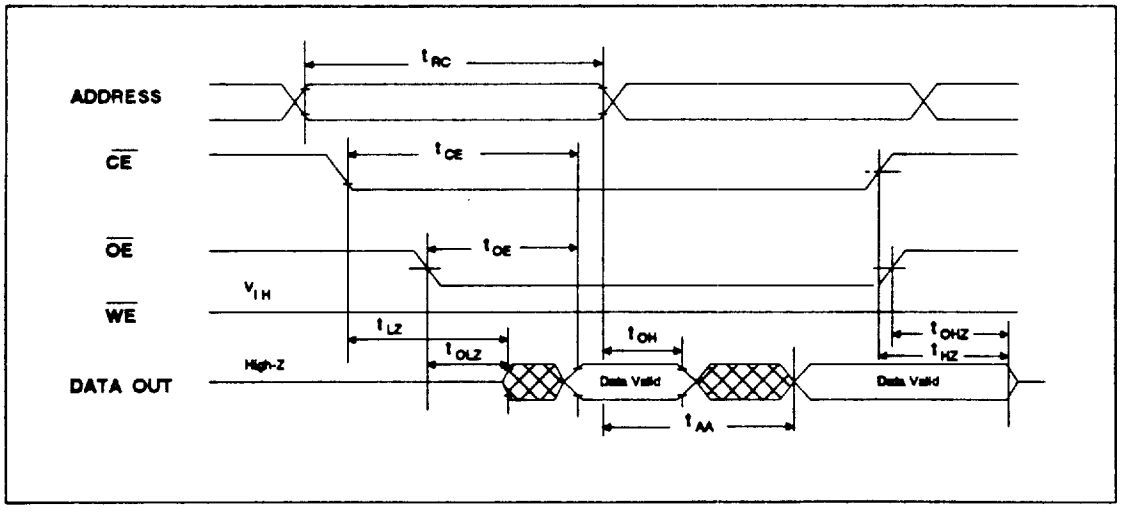
NOTES: (1) These parameters are tested initially and after a change that affects the parameter.
(2) Input rise and fall times (10% and 90%) < 10ns
(3) Output floating (High-Z) is defined as the state when the external data line is no longer driven by the output buffer.

AC CHARACTERISTICS <Write Cycle>

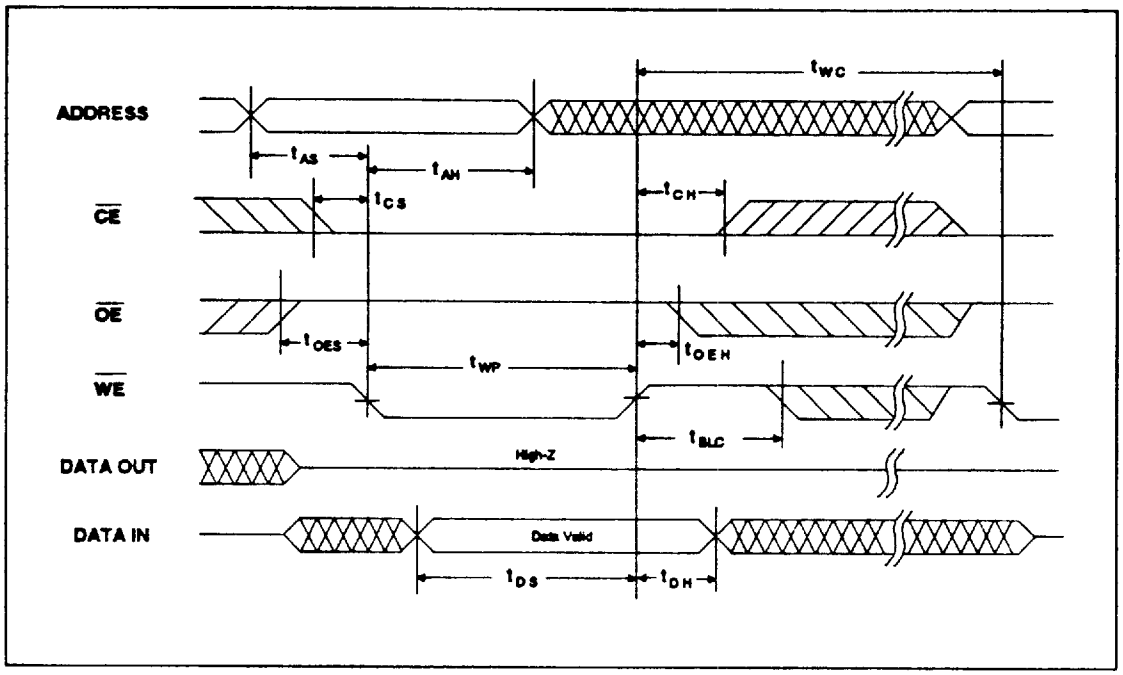
Symbol	Parameter	28C256-20 min	28C256-20 max	28C256-25 min	28C256-25 max	28C256-30 min	28C256-30 max	Units
t_{WC}	Write Cycle Time		10		10		10	ms
t_{AS}	Address Setup Time	0		0		0		ns
t_{AH}	Address Hold Time	100		100		120		ns
t_{CS}	Write Setup Time	0		0		0		ns
t_{CH}	Write Hold Time	0		0		0		ns
t_{CW} (1)	$\overline{CE}$ Pulse Time	100		100		120		ns
t_{OES}	$\overline{OE}$ Setup Time	10		10		10		ns
t_{OEH}	$\overline{OE}$ Hold Time	10		10		10		ns
t_{WP} (1)	$\overline{WE}$ Pulse Width	100		100		120		ns
t_{DS}	Data Setup Time	50		50		50		ns
t_{DH}	Data Hold Time	10		10		20		ns
t_{INIT} (3)	Write Inhibit Period After Power-up	5	10	5	10	5	10	ms
t_{BLC} (2),(3)	Byte Load Cycle Time	.1	100	.1	100	.12	100	µs

NOTES: (1) A write pulse of less than 20ns duration will not initiate a write cycle.
(2) A timer of duration t_{BLC} max begins with every LOW to HIGH transition of WE. If allowed to time out, a page or byte write will begin; however a transition from HIGH to LOW within t_{BLC} max stops the timer.
(3) These parameters are tested initially and after a change that affects the parameter.

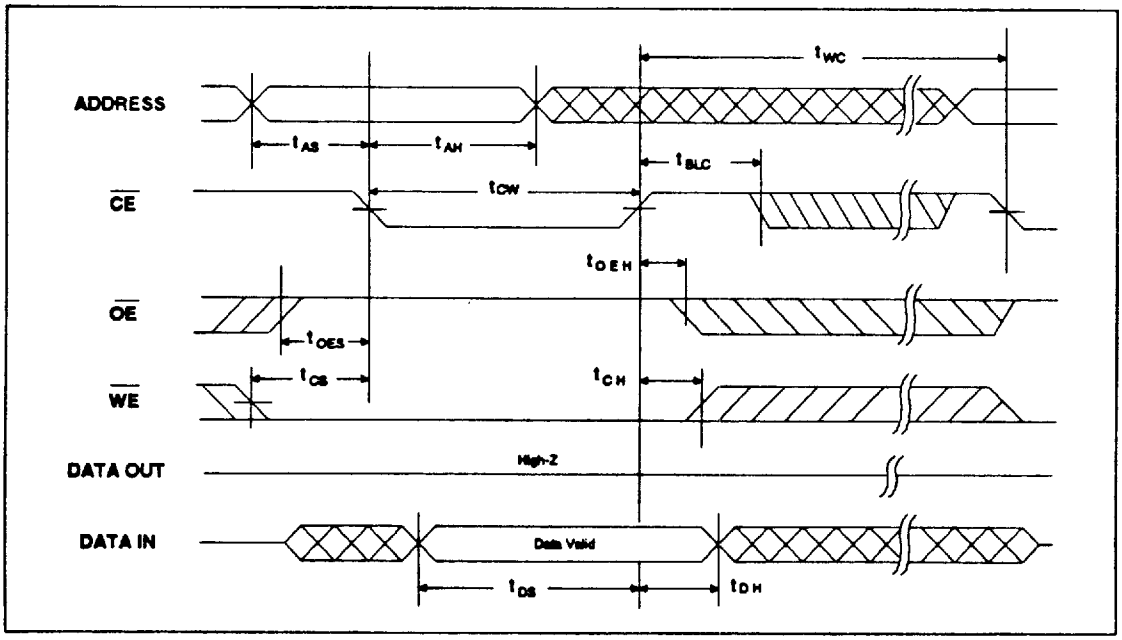
Read Cycle



Byte Write Cycle [$\overline{WE}$ controlled]



Byte Write Cycle [$\overline{CE}$ controlled]



DEVICE OPERATION

READ

Data stored in the CAT28C256 is transferred to the data bus when $\overline{WE}$ is held high, and both $\overline{OE}$ and $\overline{CE}$ are held low. The data bus is set in a high impedance state when either $\overline{CE}$ or $\overline{OE}$ go high. This 2-line control architecture can be used to eliminate bus contention in a system environment.

BYTE WRITE

A write cycle is initiated when both $\overline{CE}$ and $\overline{WE}$ are low, and $\overline{OE}$ is high. Write cycles can be executed using either $\overline{WE}$ or $\overline{CE}$, with the address input being latched on the falling edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs last. Data, conversely, is latched on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Once initiated, a byte write cycle automatically erases the addressed byte and the new data is written within 10ms.

PAGE WRITE

The page write mode of the CAT28C256 (essentially an extended BYTE WRITE mode) allows from 1 to 64 bytes of data to be programmed within a single E^2PROM write cycle. This effectively reduces the byte-write time by a factor of 64.

Following an initial WRITE operation ($\overline{WE}$ pulsed low, for t_{WP}, and then high) the page write mode can begin by issuing sequential $\overline{WE}$ pulses, which load the address and data bytes into a 64 byte temporary buffer. The page address where data is to be written, specified by bits A_6 to A_{14}, is latched on the last falling edge of $\overline{WE}$. Each byte within the page is defined by address bits A_0 to A_5 (which can be loaded in any order) during the first and subsequent write cycles. Each successive byte load cycle must begin within t_{BLC} max of the rising edge of the preceeding $\overline{WE}$ pulse. There is no page write window limitation as long as $\overline{WE}$ is maintained low within t_{BLC} max.

Upon completion of the page write sequence, $\overline{WE}$ must stay high a minimum of t_{BLC} max for the internal automatic program cycle to commence. This programming cycle consists of an erase cycle, which clears any data that existed in each addressed cell, and a write cycle, which writes new data back into the cell. A page write will only write data to the locations that were addressed and will not rewrite the entire page.

DATA POLLING

$\overline{Data}$ polling is provided to indicate the completion of a write cycle. Once a write cycle is initiated, attempting to read the last byte written will output the complement of that data on I/O_7 (I/O_0-I/O_6 are indeterminate) until the programming cycle is complete. Upon completion of the self-timed write cycle all I/O's will output true data during a read cycle.

TOGGLE BIT

In addition to the Data Polling feature of the CAT28C256 the device offers an additional method for determining the completion of a write cycle. While a write cycle is in progress, successively reading data from the device will result in I/O_6 toggling between one and zero. However, once the write is complete, I/O_6 stops toggling and valid data can be read from the device.

HARDWARE DATA PROTECTION

The following lists the hardware data protection features that are incorporated into the CAT28C256.

(1) V_{CC} sense provides for write protection when V_{CC} falls below 3.8 V (typ).

(2) A power on delay mechanism, t_{INIT} (see AC characteristics), provides a 5 to 10 ms delay before a write sequence, after V_{CC} has reached 3.8 V.

(3) Write inhibit is activated by holding any one of $\overline{OE}$ low, $\overline{CE}$ high or $\overline{WE}$ high.

(4) Noise pulses of less than 20 ns on the $\overline{WE}$ or $\overline{CE}$ inputs will not result in a write cycle.

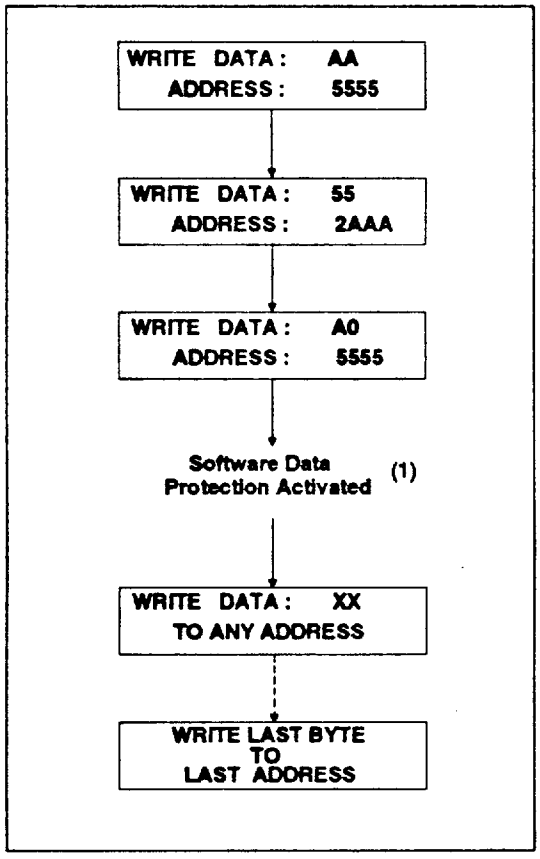
SOFTWARE DATA PROTECTION:

The CAT28C256 features a software controlled data protection scheme which, once activated, requires a data algorithm to be issued to the device before a write can be performed. The device is shipped from Catalyst with the software protection NOT ENABLED (the CAT28C256 is in the standard operating mode).

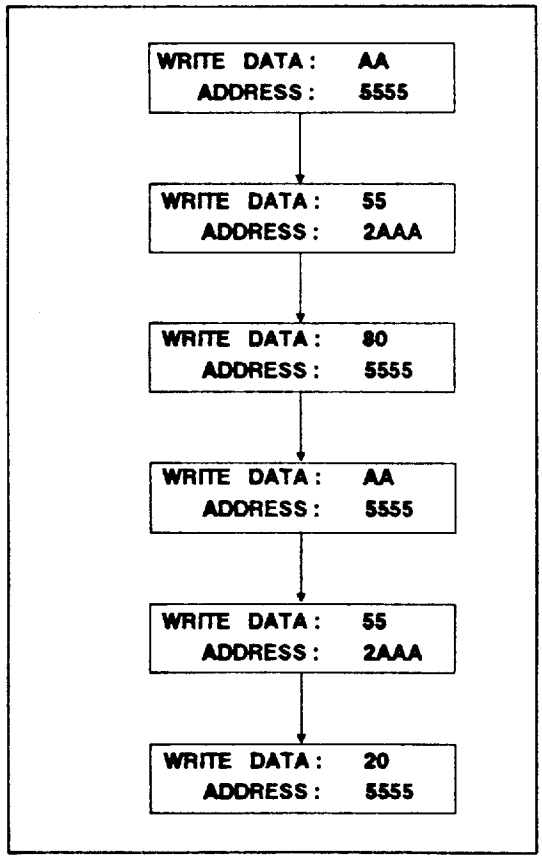
To activate the software data protection the device must be sent three write commands to specific addresses with specific data, as shown below. This sequence of commands (along with subsequent writes) must adhere to the page write timing specifications. Once this is done, all subsequent writes to the device must be preceded by this same set of write commands. The data protection mechanism is activated until a deactivate sequence is issued regardless of power on/off transitions. This gives the user added inadvertent write protection on power-up in addition to the hardware protection provided.

To allow the user the ability to program the part with an EEprom programmer (or for testing purposes) there is a software command sequence for deactivating the data protection. The six step algorithm (shown below) will reset the internal protection circuitry and the device will return to standard operating mode. After the sixth byte of this reset sequence has been issued, standard byte or page writing can commence.

Write Sequence for Activating Software Data Protection



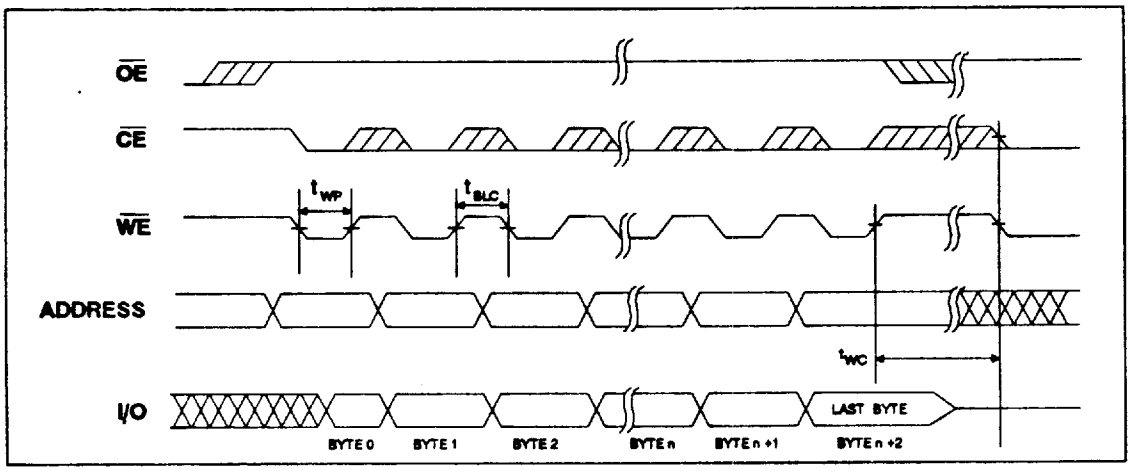
Write Sequence to Deactivate Software Data Protection



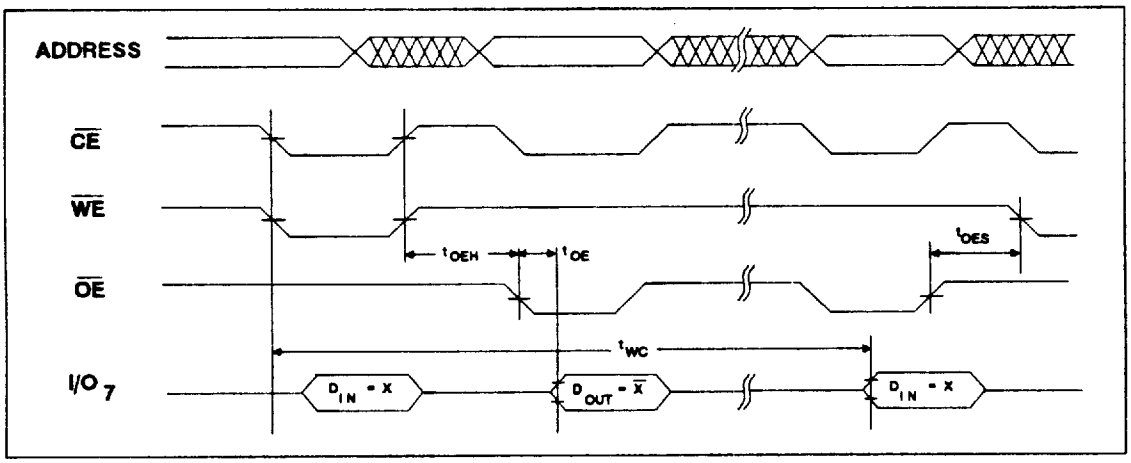
Note: (1) Write protection is activated at this point whether or not any more writes are completed. Writing to addresses must occur within t_{BLC} Max, after SDP activation.

Preliminary

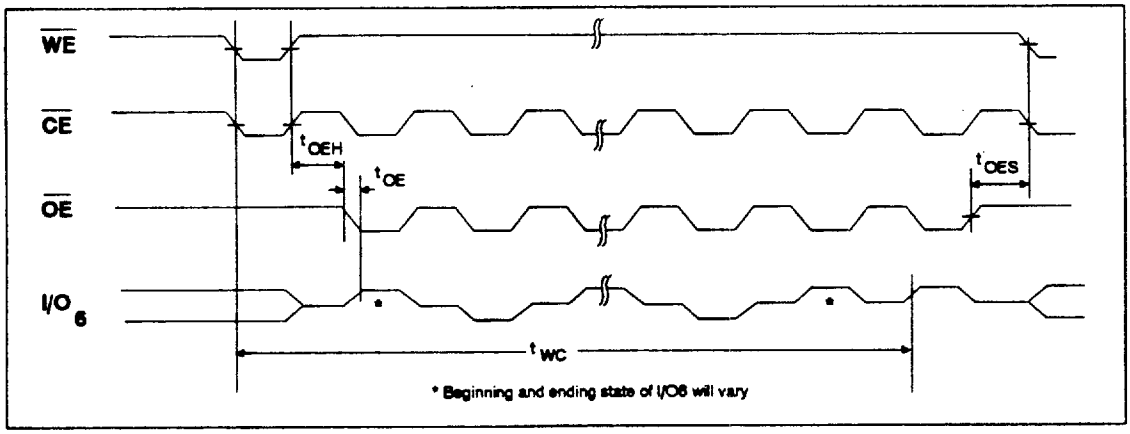
PAGE MODE WRITE CYCLE



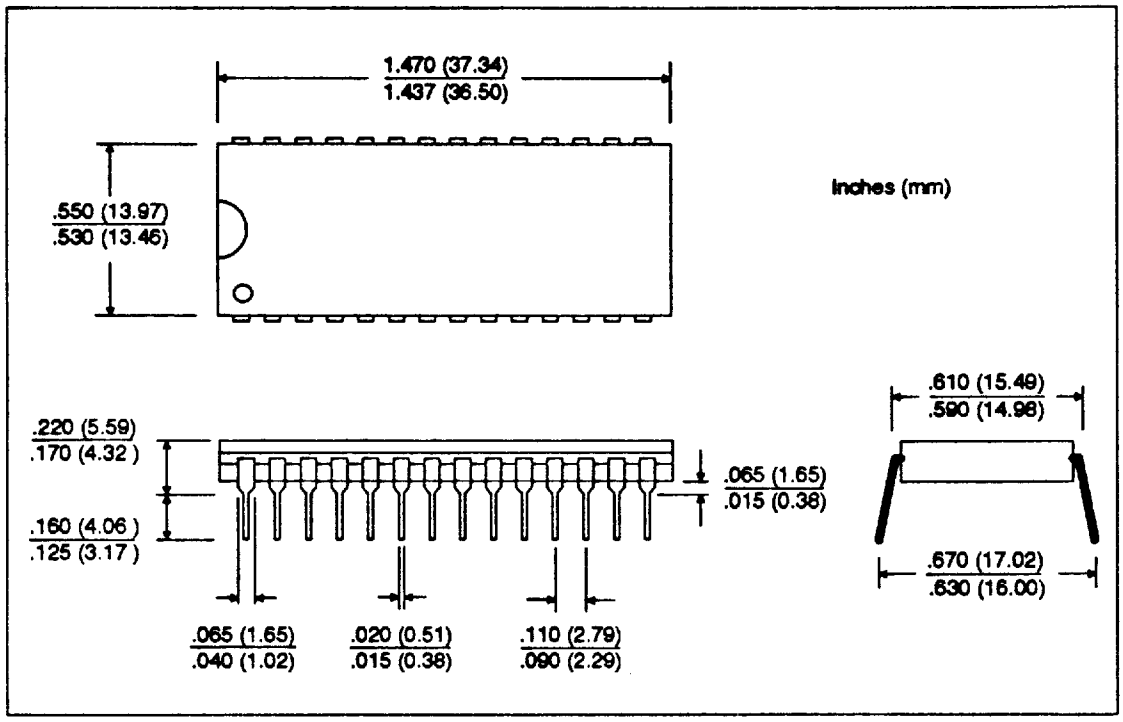
DATA POLLING



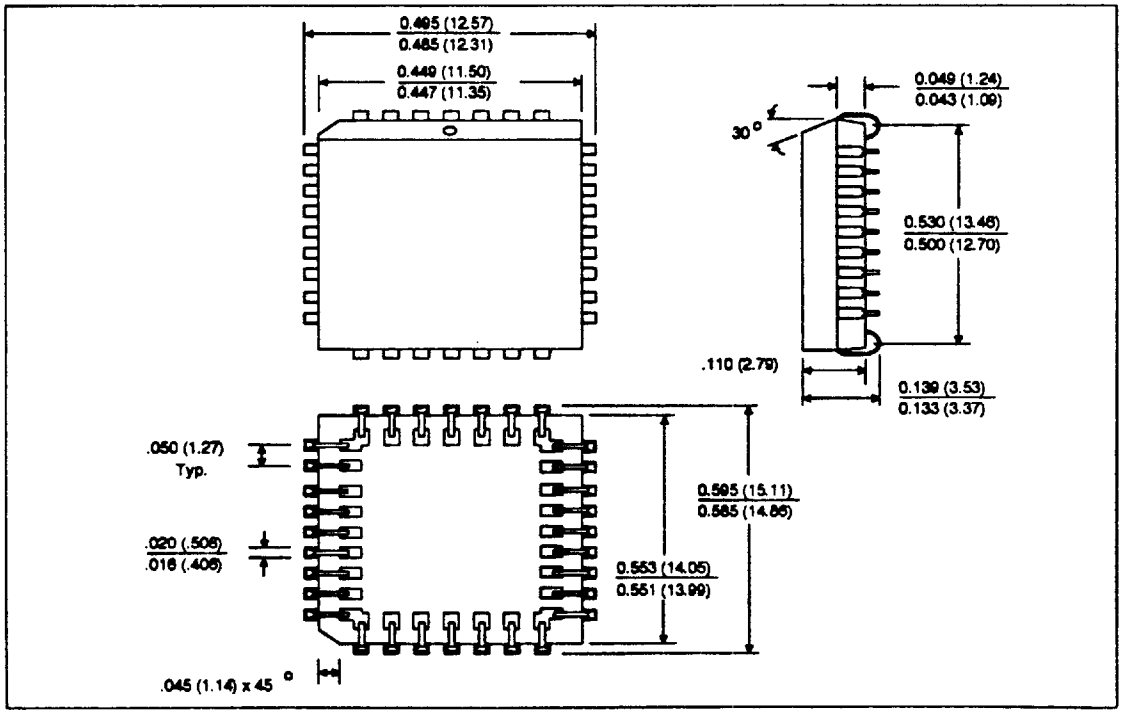
TOGGLE BIT



28-Pin PDIP



32-Pin PLCC



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