

# TrenchMOS™ transistor Standard level FET

BUK7608-55

## GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

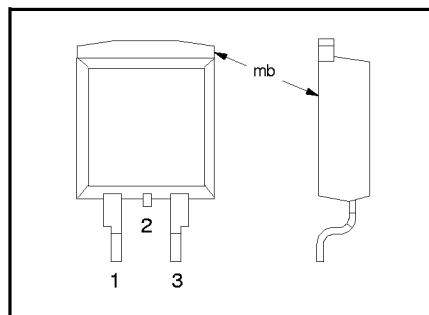
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
$V_{DS}$	Drain-source voltage	55	V
$I_D$	Drain current (DC)	75	A
$P_{tot}$	Total power dissipation	187	W
$T_j$	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	8	mΩ

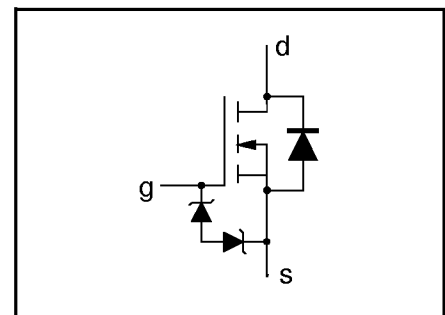
## PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

## PIN CONFIGURATION



## SYMBOL



## LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{DS}$	Drain-source voltage	-	-	55	V
$V_{DGR}$	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	16	V
$I_D$	Drain current (DC)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	75	A
$I_D$	Drain current (DC)	$T_{mb} = 100\text{ }^\circ\text{C}$	-	65	A
$I_{DM}$	Drain current (pulse peak value)	$T_{mb} = 25\text{ }^\circ\text{C}$	-	240	A
$P_{tot}$	Total power dissipation	$T_{mb} = 25\text{ }^\circ\text{C}$	-	187	W
$T_{stg}, T_j$	Storage & operating temperature	-	-55	175	°C

## ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_C$	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

## THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	0.8	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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### STATIC CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	V <sub>GS</sub> = 0 V; I <sub>D</sub> = 0.25 mA; T <sub>j</sub> = -55°C	55 50	- -	- -	V V
V <sub>GS(TO)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> ; I <sub>D</sub> = 1 mA T <sub>j</sub> = 175°C T <sub>j</sub> = -55°C	2 1 -	3.0 - -	4.0 - 4.4	V V V
I <sub>DSS</sub>	Zero gate voltage drain current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 175°C	-	0.05	10	μA
I <sub>GSS</sub>	Gate source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V T <sub>j</sub> = 175°C	-	0.02	500	μA
±V <sub>(BR)GSS</sub>	Gate-source breakdown voltage	I <sub>G</sub> = ±1 mA; T <sub>j</sub> = 175°C	16	-	20	μA V
R <sub>DS(ON)</sub>	Drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A T <sub>j</sub> = 175°C	- -	6.5 -	8 17	mΩ mΩ

### DYNAMIC CHARACTERISTICS

T<sub>mb</sub> = 25°C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g <sub>fs</sub>	Forward transconductance	V <sub>DS</sub> = 25 V; I <sub>D</sub> = 25 A	10	45	-	S
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz	-	3600	4500	pF
C <sub>oss</sub>	Output capacitance		-	830	1000	pF
C <sub>rss</sub>	Feedback capacitance		-	320	440	pF
t <sub>d on</sub>	Turn-on delay time	V <sub>DD</sub> = 30 V; I <sub>D</sub> = 25 A; V <sub>GS</sub> = 10 V; R <sub>G</sub> = 10 Ω Resistive load	-	27	40	ns
t <sub>r</sub>	Turn-on rise time		-	70	105	ns
t <sub>d off</sub>	Turn-off delay time		-	100	140	ns
t <sub>f</sub>	Turn-off fall time		-	50	70	ns
L <sub>d</sub>	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L <sub>s</sub>	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

### REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T<sub>j</sub> = 25°C unless otherwise specified

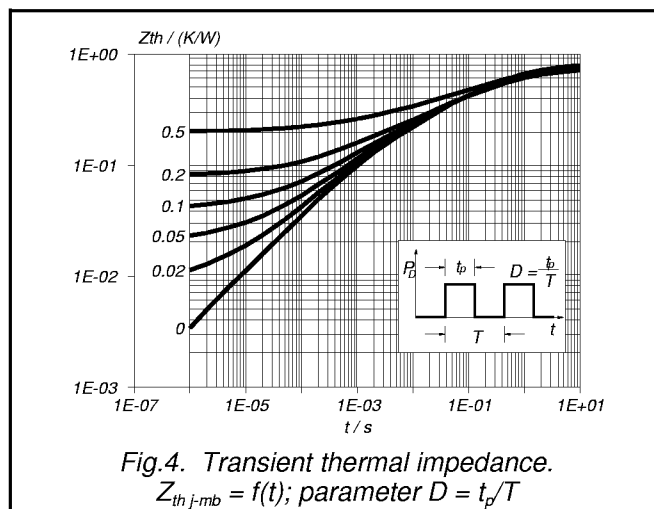
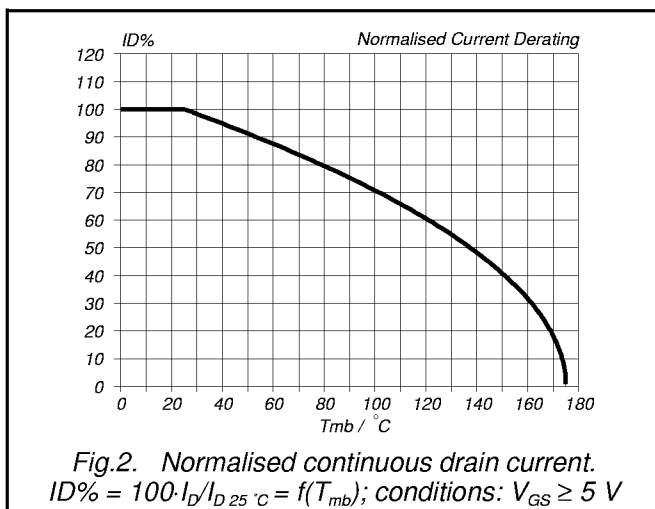
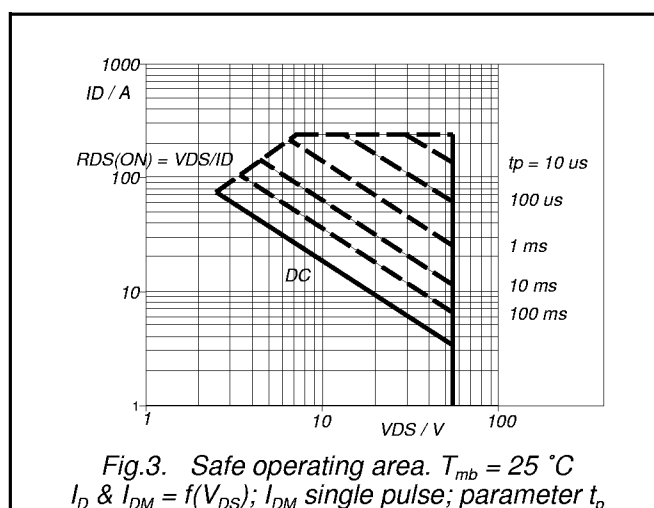
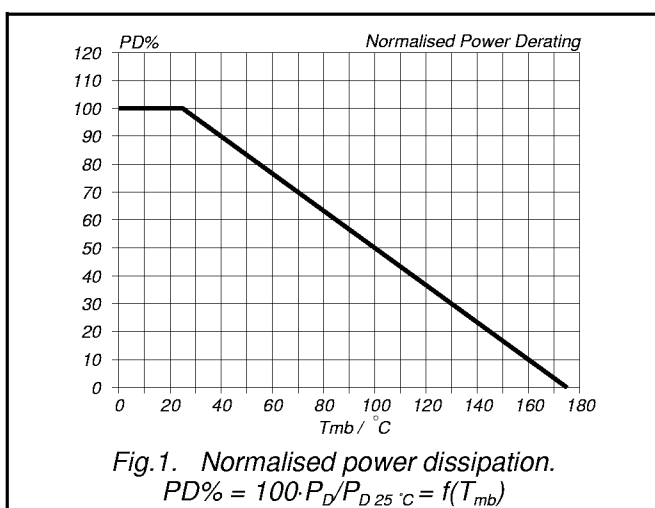
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I <sub>DR</sub>	Continuous reverse drain current		-	-	75	A
I <sub>DRM</sub>	Pulsed reverse drain current		-	-	240	A
V <sub>SD</sub>	Diode forward voltage	I <sub>F</sub> = 25 A; V <sub>GS</sub> = 0 V	-	0.85	1.2	V
		I <sub>F</sub> = 75 A; V <sub>GS</sub> = 0 V	-	1.0	-	V
t <sub>rr</sub>	Reverse recovery time	I <sub>F</sub> = 75 A; -di <sub>F</sub> /dt = 100 A/μs;	-	65	-	ns
Q <sub>rr</sub>	Reverse recovery charge	V <sub>GS</sub> = -10 V; V <sub>R</sub> = 30 V	-	0.18	-	μC

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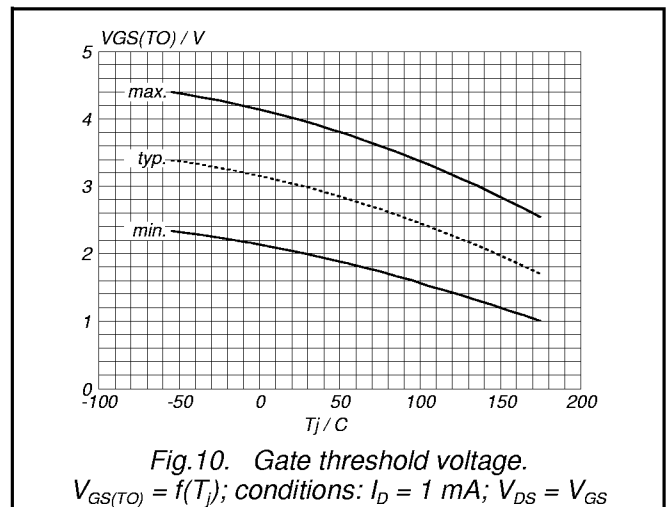
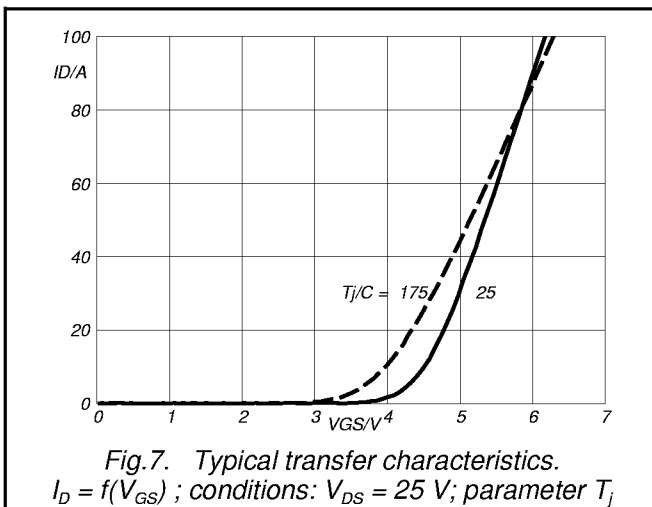
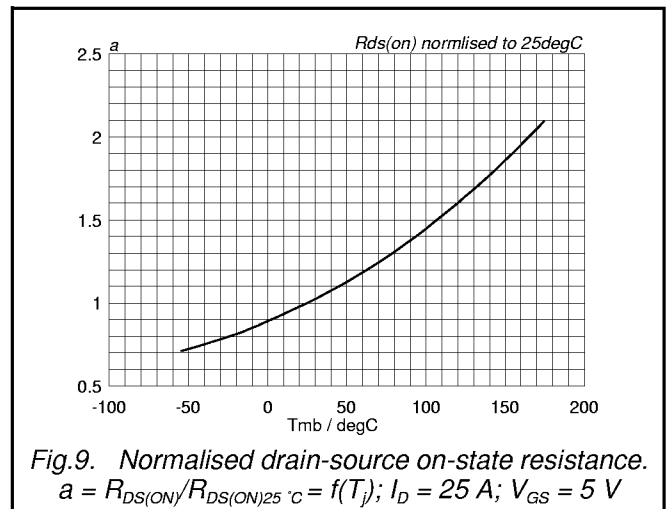
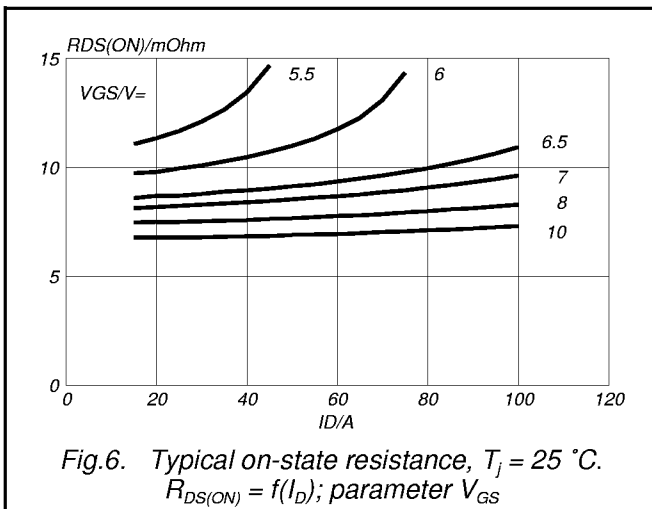
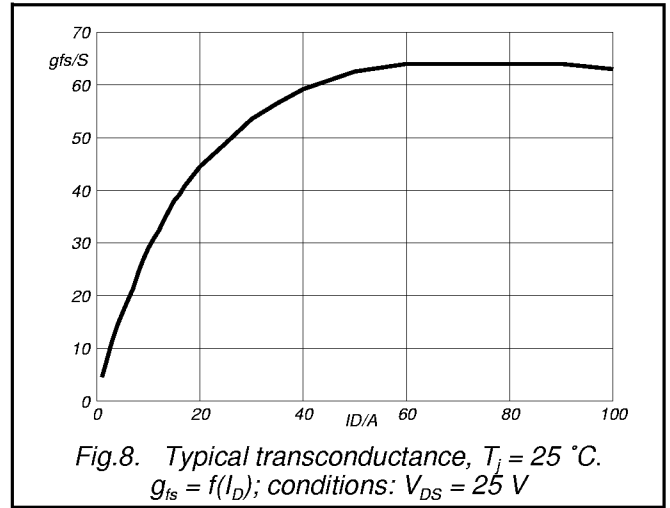
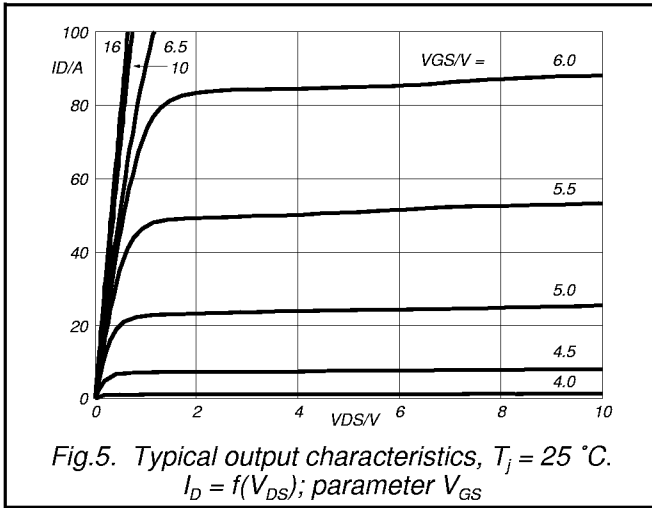
**AVALANCHE LIMITING VALUE**

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$W_{DSS}$	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 75 \text{ A}; V_{DD} \leq 25 \text{ V}; V_{GS} = 10 \text{ V}; R_{GS} = 50 \Omega; T_{mb} = 25 \text{ }^\circ\text{C}$	-	-	500	mJ



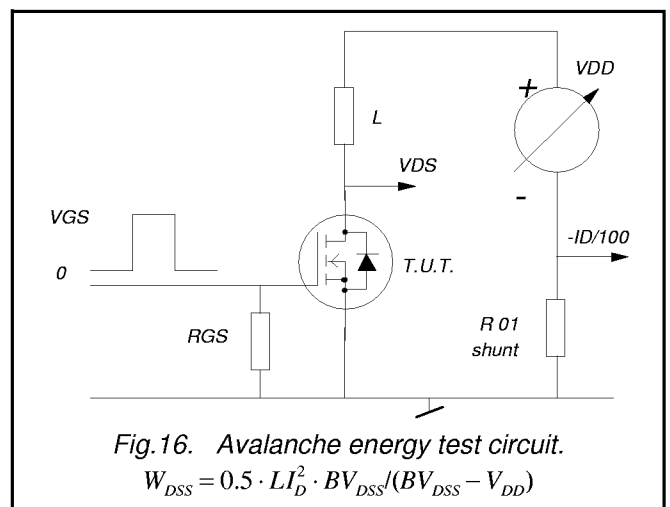
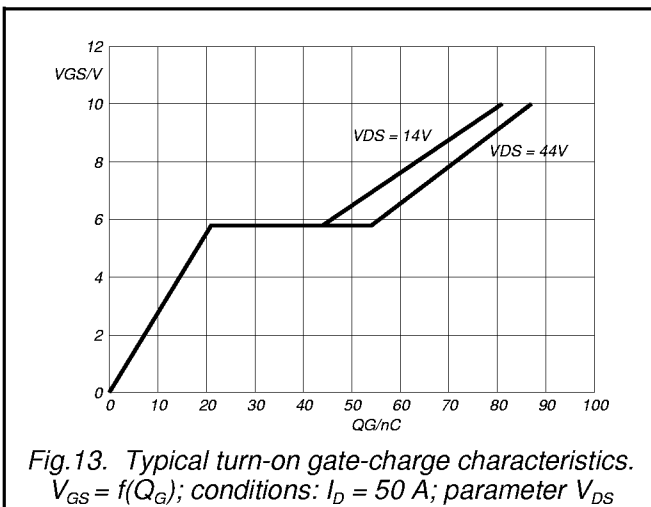
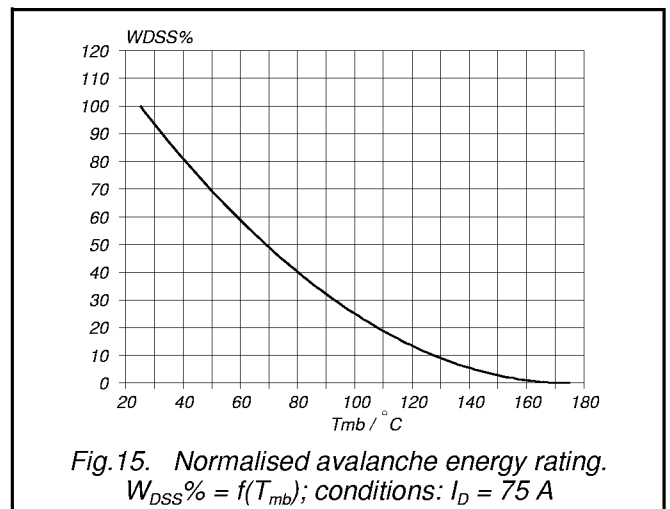
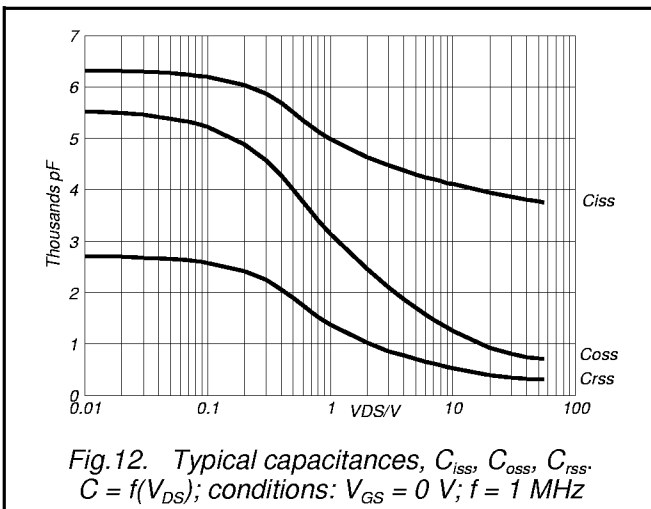
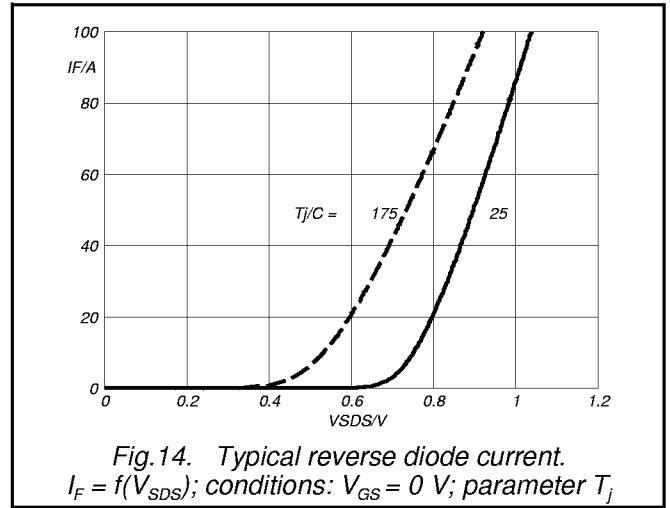
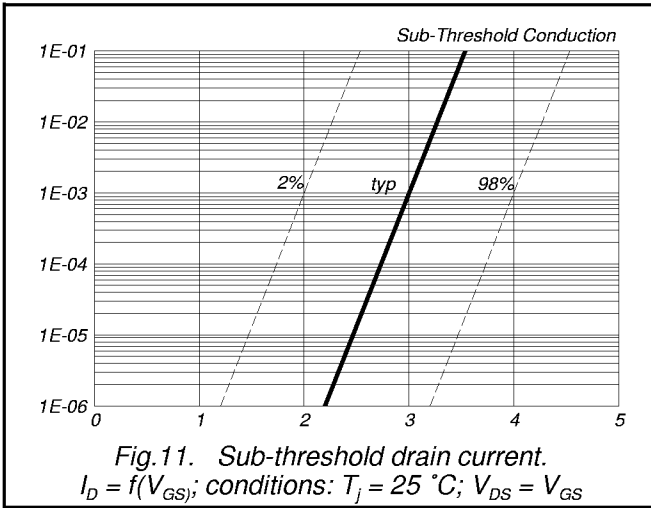
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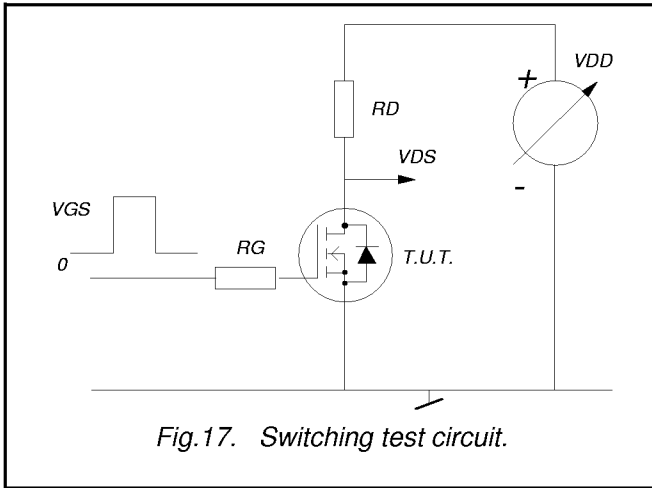
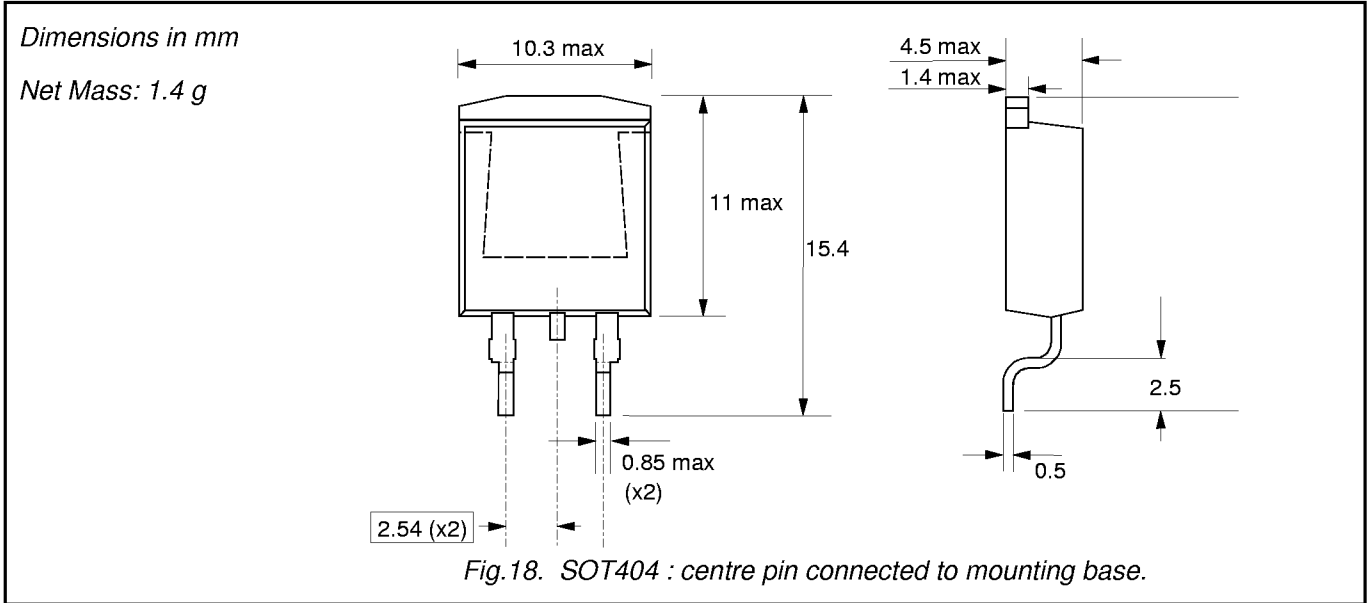


Fig.17. Switching test circuit.

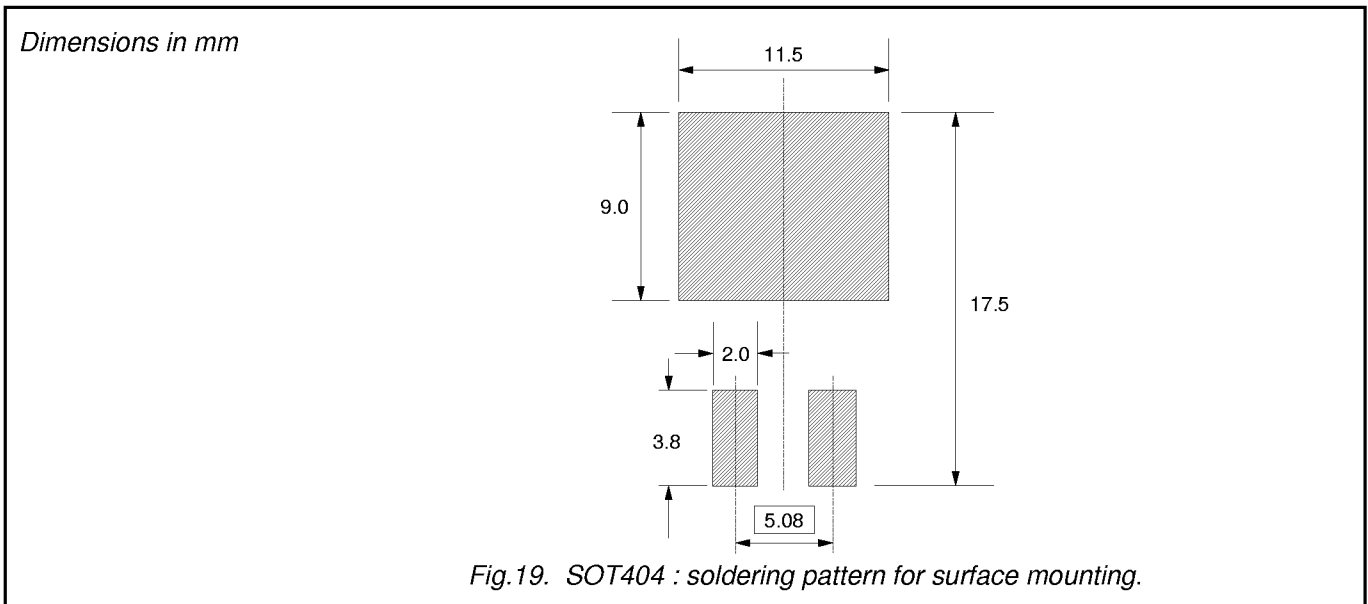
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**MECHANICAL DATA**



**MOUNTING INSTRUCTIONS**



**Notes**

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".