National Semiconductor

July 1983

TP3022/TP3023 Monolithic CODECs

General Description

The TP3022 and TP3023 are monolithic PCM CODECs implemented with double-poly CMOS technology. The TP3022 is intended for A-law applications. The TP3023 is intended for μ-law applications.

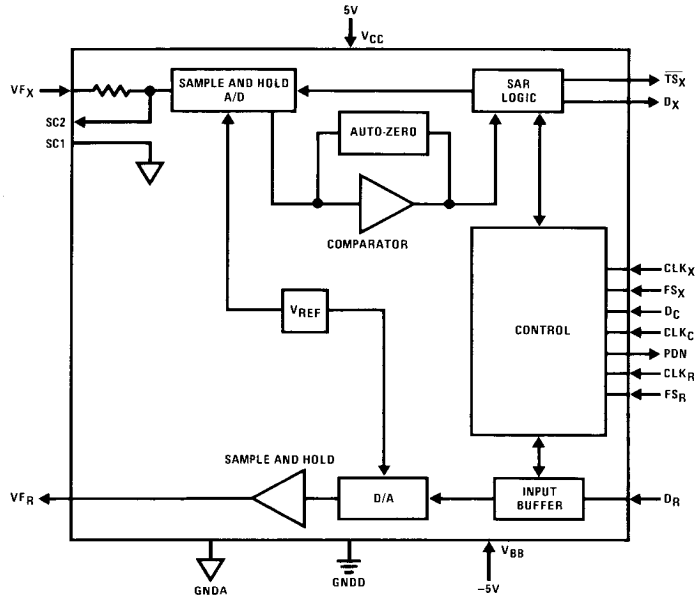
Each device contains separate D/A and A/D circuitry, all necessary sample and hold capacitors, a precision voltage reference and internal auto-zero circuit. A serial control port allows an external controller to individually assign the PCM input and output ports to one of up to 32 time slots or to place the CODEC into a power-down mode. Alternately, the TP3022/TP3023 may be operated in a fixed time slot mode. Both devices are intended to be used with the TP3040 monolithic PCM filter which provides the input anti-aliasing function for the encoder and smoothes the output of the decoder and corrects for the sin x/x distortion introduced by the decoder sample and hold output.

Features

- Low operation power—45 mW typical
- Low standby power—1 mW typical
- ±5V operation
- TTL compatible digital interface
- Time slot assignment or alternate fixed time slot modes
- Internal precision reference
- Internal sample and hold capacitors
- Internal auto-zero circuit
- TP3022—A-law coding, pin compatible with TP3020
- TP3023—μ-law coding, pin compatible with TP3021
- Synchronous or asynchronous operation

61 003681 ORIG 3681 NSC

Simplified Block Diagram



TL/H/5228-1

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 TL/H/5228

IM-B20M73/Printed in U.S.A.

Absolute Maximum Ratings

Operating Temperature	−25°C to +125°C
Storage Temperature	−65°C to +150°C
V_{CC} with Respect to GNDD	7V
V_{CC} with Respect to V_{BB}	14V
V_{BB} with Respect to GNDD	−7V
Voltage at Any Analog Input or Output	V_{BB} − 0.3V to V_{CC} + 0.3V
Voltage at Any Digital Input or Output	GNDD − 0.3V to V_{CC} + 0.3V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

Unless otherwise noted $T_A = 0°C$ to $70°C$, $V_{CC} = 5.0V \pm 5\%$, $V_{BB} = -5.0V \pm 5\%$. Typical characteristics are specified at $V_{CC} = 5.0V$, $V_{BB} = -5.0V$ and $T_A = 25°C$. All digital signals are referenced to GNDD. All analog signals are referenced to GNDA.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DIGITAL INTERFACE						
I_I	Input Current	$0 < V_{IN} < V_{CC}$	−10		10	μA
V_{IL}	Input Low Voltage				0.6	V
V_{IH}	Input High Voltage		2.2			V
V_{OL}	Output Low Voltage	D_X, $I_{OL} = 4.0$ mA SIG_R, $I_{OL} = 0.5$ mA $\overline{TS}_X$, $I_{OL} = 3.2$ mA, Open Drain PDN, $I_{OL} = 1.6$ mA			0.4 0.4 0.4 0.4	V V V V
V_{OH}	Output High Voltage	D_X, $I_{OH} = 6$ mA SIG_R, $I_{OH} = 0.6$ mA	2.4 2.4			V V
ANALOG INTERFACE						
Z_I	VF_X Input Impedance when Sampling	Resistance in Series with Approximately 70 pF	2.0			kΩ
Z_O	Output Impedance at VF_R	$-3.1V < VF_R < 3.1V$		10	20	Ω
V_{OS}	Output Offset Voltage at VF_R	D_R = PCM Zero Code (TP3023) or Alternating ±1 Code (TP3022)	−25		25	mV
I_{IN}	Analog Input Bias Current	$V_{IN} = 0V$	−0.1		0.1	μA
R1 × C1	DC Blocking Time Constant		4.0			ms
C1	DC Blocking Capacitor		0.1			μF
R1	Input Bias Resistor				160	kΩ
POWER DISSIPATION						
I_{CC0}	Standby Current, V_{CC}			0.1	0.4	mA
I_{BB0}	Standby Current, V_{BB}			0.03	0.1	mA
I_{CC1}	Operating Current, V_{CC}			4.5	8.0	mA
I_{BB1}	Operating Current, V_{BB}			4.5	8.0	mA

AC Electrical Characteristics

Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	Absolute Level	The nominal 0 dBm0 levels for the TP3022 and TP3023 are 1.525 Vrms and 1.520 Vrms respectively for the decoder and 1.560 Vrms and 1.555 Vrms respectively for the encoder. This corresponds to a loop gain of −0.2 dB. All gain measurements for the encode and decode portions of the TP3022/TP3023 are based on these nominal levels after the necessary sin x/x corrections are made.				
G_{RA}	Receive Gain, Absolute	$T = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$	−0.175		0.175	dB
G_{RAT}	Absolute Receive Gain Variation with Temperature	$T = 0°C$ to $70°C$	−0.05		0.05	dB
G_{RAV}	Absolute Receive Gain	$V_{CC} = 5V \pm 5\%$	−0.07		0.07	dB
G_{XA}	Transmit Gain, Absolute	$T = 25°C$, $V_{CC} = 5V$, $V_{BB} = -5V$	−0.175		0.175	dB
G_{XAT}	Absolute Transmit Gain Variation with Temperature	$T = 0°C$ to $70°C$	−0.05		0.05	dB
G_{XAV}	Absolute Transmit Gain Variation with Supply Voltage	$V_{CC} = 5V \pm 5\%$, $V_{BB} = -5V \pm 5\%$	−0.07		0.07	dB
G_{RAL}	Absolute Receive Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
G_{XAL}	Absolute Transmit Gain Variation with Level	CCITT Method 2 Relative to −10 dBm0				
		0 dBm0 to 3 dBm0	−0.3		0.3	dB
		−40 dBm0 to 0 dBm0	−0.2		0.2	dB
		−50 dBm0 to −40 dBm0	−0.4		0.4	dB
		−55 dBm0 to −50 dBm0	−1.0		1.0	dB
S/D_R	Receive Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
S/D_X	Transmit Signal to Distortion Ratio	Sinusoidal Test Method Input Level				
		−30 dBm0 to 0 dBm0	35			dBc
		−40 dBm0	29			dBc
		−45 dBm0	25			dBc
N_R	Receive Idle Channel Noise	D_R = Steady State PCM Code			6	dBrnc0
N_X	Transmit Idle Channel Noise	TP3023, $VF_X = 0V$			13	dBrnc0
		TP3022, $VF_X = 0V$			−66*	dBm0p
HD_R	Receive Harmonic Distortion	2nd or 3rd Harmonic			−47	dB
HD_X	Transmit Harmonic Distortion	2nd or 3rd Harmonic			−47	dB

AC Electrical Characteristics (Continued) Unless otherwise noted, the analog input is a 0 dBm0, 1.02 kHz sine wave. The digital input is a PCM bit stream generated by passing a 0 dBm0, 1.02 kHz sine wave through an ideal encoder. All output levels are sin x/x corrected.

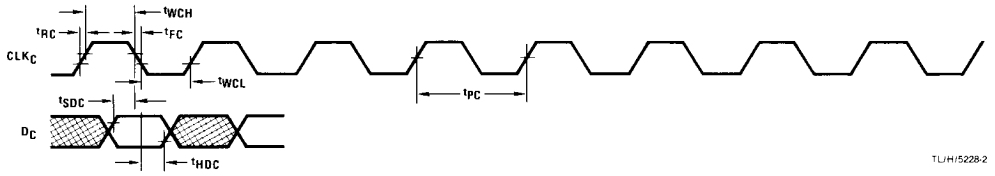
Symbol	Parameter	Conditions	Min	Typ	Max	Units
$PPSR_X$	Positive Power Supply Rejection, Transmit	Input Level = 0V, V_{CC} = 5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$PPSR_R$	Positive Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{CC} = 5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	40			dB
$NPSR_X$	Negative Power Supply Rejection, Transmit	Input Level = 0V, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	50			dB
$NPSR_R$	Negative Power Supply Rejection, Receive	D_R = Steady PCM Code, V_{BB} = −5.0 V_{DC} + 200 mVrms, f = 1.02 kHz	45			dB
CT_{XR}	Transmit to Receive Crosstalk	D_R = Steady PCM Code			−75	dB
CT_{RX}	Receive to Transmit Crosstalk	Transmit Input Level = 0V TP3023 TP3022			 −70 −65*	 dB dB

* Theoretical worst-case for a perfectly zeroed encoder with alternating sign bit, due to the decoding law.

Timing Specifications Unless otherwise noted, T_A = 0°C to 70°C, V_{CC} = 5.0 ± 5%, V_{BB} = −5.0 ± 5%. All digital signals are referenced to GNDD and measured at V_{IL} and V_{IH} levels as indicated in the Timing Waveforms.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{PC}	Period of Clock	CLK_C, CLK_R, CLK_X	485			ns
t_{RC}, t_{FC}	Rise and Fall Time of Clock	CLK_C, CLK_R, CLK_X			30	ns
t_{WCH}	Width of Clock High	CLK_C, CLK_R, CLK_X	165			ns
t_{WCL}	Width of Clock Low	CLK_C, CLK_R, CLK_X	165			ns
$t_{A/D}$	A/D Conversion Time	From End of Encoder Time Slot to Completion of Conversion			16	Time Slots
$t_{D/A}$	D/A Conversion Time	From End of Decoder Time Slot to Transition of VF_R			2	Time Slots
t_{SDC}	Set-Up Time, D_C to CLK_C		100			ns
t_{HDC}	Hold Time, CLK_C to DC		100			ns
t_{SFC}	Set-Up Time, FS_X or CLK_X		100			ns
t_{HFX}	Hold Time, CLK_X to FS_X		100			ns
t_{DZX}	Delay Time to Enable D_X on TS Entry	C_L = 150 pF			125	ns
t_{DDX}	Delay Time, CLK_X to D_X	C_L = 150 pF			125	ns
t_{DXZ}	Delay Time, D_X to High Impedance State on TS Exit	C_L = 0 pF	50		165	ns
t_{DTSL}	Delay to $\overline{TS}_X$ Low	0 ≤ C_L ≤ 150 pF	30		185	ns
t_{DTSH}	Delay to $\overline{TS}_X$ Off	C_L = 0 pF	30		185	ns
t_{SSX}	Set-Up Time, SIG_X to CLK_X		100			ns
t_{HSX}	Hold Time, CLK_X to SIG_X		100			ns
t_{SFR}	Set-Up Time, FS_R to CLK_R		100			ns
t_{HFR}	Hold Time, CLK_R to FS_R		100			ns
t_{SDR}	Set-Up Time, D_R to CLK_R		40			ns
t_{HDR}	Hold Time, CLK_R to D_R		30			ns
t_{DSR}	Delay Time, CLK_R to SIG_R	C_L = 100 pF			300	ns

Timing Waveforms



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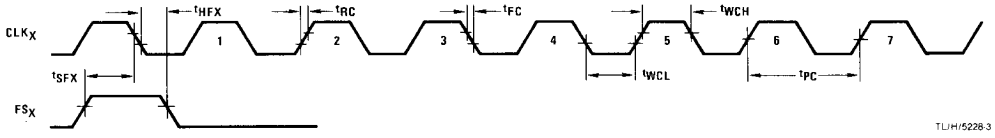

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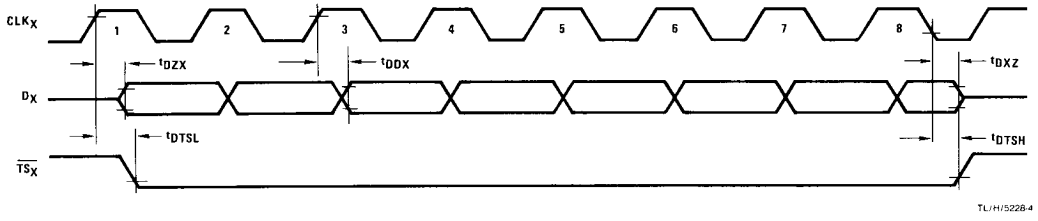

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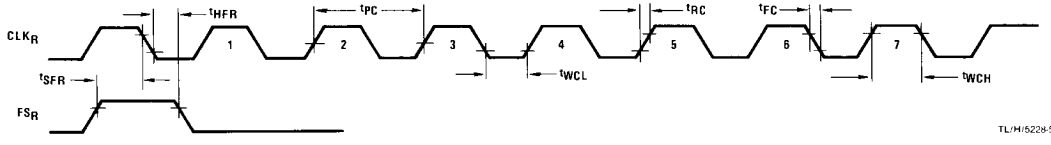

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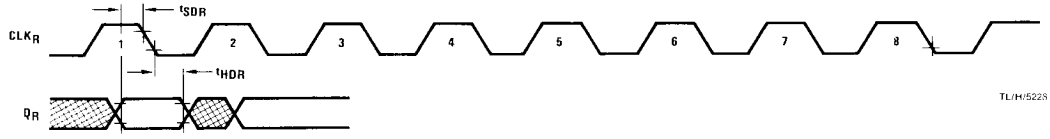

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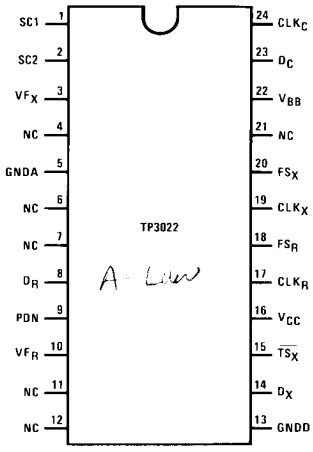
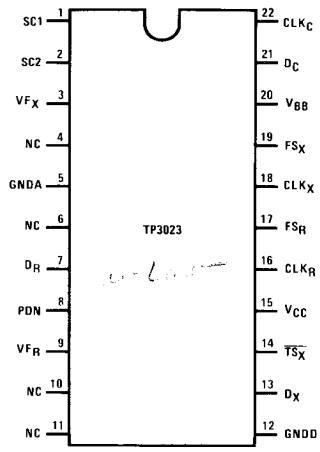
Connection Diagrams

Dual-In-Line Package



TOP VIEW TL/H/5228-7

Dual-In-Line Package



TOP VIEW TL/H/5228-8

Description of Pin Functions

TP3022

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatiblity.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	NC	Unused
8	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
9	PDN	TTL output level which goes high when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
10	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.
11	NC	Unused
12	NC	Unused

TP3022 (Continued)

Pin No.	Name	Function
13	GNDD	Digital ground. All digital levels are referenced to this pin.
14	D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
15	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
16	V_{CC}	5V ($\pm$5%) input.
17	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2048 MHz. May be asynchronous with CLK_X or CLK_C.
18	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide. Extending the width of FS_R to two or more cycles of CLK_R signifies a receive signaling frame.
19	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.

Description of Pin Functions (Continued)

TP3022 (Continued)

Pin No.	Name	Function
20	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide. Extending the width of FS_X to two or more cycles of CLK_X signifies a transmit signaling frame.
21	NC	Unused
22	V_{BB}	$-5V (\pm 5\%)$ input.
23	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
24	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3022 into the fixed time slot mode.

TP3023

Pin No.	Name	Function
1	SC1	Internally connected to GNDA.
2	SC2	Connects VF_X to an external sample/hold capacitor if fitted for use with pin-compatible NMOS CODECs. Ensures gain compatibility.
3	VF_X	Analog input to the encoder. This signal will be sampled at the end of the encoder time slot and the resulting PCM code will be shifted out during the subsequent encode time slot.
4	NC	Unused
5	GNDA	Analog ground. All analog signals are referenced to this pin.
6	NC	Unused
7	D_R	Serial PCM data input to the decoder. During the decoder time slot, PCM data is shifted into D_R, most significant bit first, on the falling edge of CLK_R.
8	PDN	Open drain output which turns off when the CODEC is in the power-down mode. May be used to power-down other circuits associated with the PCM channel. Can be wire ANDed with other PDN outputs.
9	VF_R	Analog output from the decoder. The decoder sample and hold amplifier is updated approximately 15 μs after the end of the decode time slot.

TP3023 (Continued)

Pin No.	Name	Function
10	NC	Unused
11	NC	Unused
12	GNDD	Digital ground. All digital levels are referenced to this pin.
13	D_X	Serial PCM TRI-STATE® output from the encoder. During the encoder time slot, the PCM code for the previous sample of VF_X is shifted out, most significant bit first, on the rising edge of CLK_X.
14	$\overline{TS}_X$	Time slot output. This TTL compatible open-drain output pulses low during the encoder time slot. May be used to enable external TRI-STATE® bus drivers if highly capacitive loads must be driven. Can be wire ANDed with other $\overline{TS}_X$ outputs.
15	V_{CC}	$5V (\pm 5\%)$ input.
16	CLK_R	Master decoder clock input used to shift in the PCM data on D_R and to operate the decoder sequencer. May operate at 1.536 MHz, 1.544 MHz or 2.048 MHz. May be asynchronous with CLK_X or CLK_C.
17	FS_R	Decoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_R cycle wide.
18	CLK_X	Master encoder clock input used to shift out the PCM data on D_X and to operate the encoder sequencer. May operate at 1.536 MHz 1.544 MHz, or 2.048 MHz. May be asynchronous with CLK_R or CLK_C.
19	FS_X	Encoder frame sync pulse. Normally occurring at an 8 kHz rate, this pulse is nominally one CLK_X cycle wide.
20	V_{BB}	$-5V (\pm 5\%)$ input.
21	D_C	Serial control data input. Serial data on D_C is shifted into the CODEC on the falling edge of CLK_C. In the fixed time slot mode, D_C doubles as a power-down input.
22	CLK_C	Control clock input used to shift serial control data into D_C. CLK_C must pulse 8 times during a period of time less than or equal to one frame time, although the 8 pulses may overlap a frame boundary. CLK_C need not be synchronous with CLK_X or CLK_R. Connecting CLK_C continuously high places the TP3023 into the fixed time slot mode.

Functional Description

POWER-UP

Upon application of power, internal circuitry initializes the CODEC and places it into the power-down mode. No sequencing of 5V or −5V is required. In the power-down mode, all non-essential circuits are deactivated and the TRI-STATE® PCM data output D_X is placed in the high impedance state. Once in the power-down mode, the method of activating the TP3022/TP3023 depends on the chosen mode of operation, time slot assignment or fixed time slot.

TIME SLOT ASSIGNMENT MODE

The time slot assignment mode of operation is selected by maintaining CLK_C in a normally low state. The state of the CODEC is updated by pulsing CLK_C eight times within a period of 125 μs or less. The falling edge of each clock pulse shifts the data on the D_C input into the CODEC. The first two control bits determine if the subsequent control bits B3-B8 are to specify the time slot for the encoder (B1 = 0), the decoder (B2 = 0) or both (B1 and B2 = 0) or if the CODEC is to be placed into the power-down mode (B1 and B2 = 1). The desired action will take place upon the occurrence of the second frame sync pulse following the first pulse of CLK_C. Assigning a time slot to either the encoder or decoder will automatically power-up the entire CODEC circuit. The D_X output and D_R input, however, will be inhibited for one additional frame to allow the analog circuitry time to stabilize. If separate time slots are to be assigned to the encoder and the decoder, the encoder time slot should be assigned first. This is necessary because up to four frames are required to assign both time slots separately, but only three frames are necessary to activate the D_X output. If the encode time slot has not been updated the PCM data will be outputted during the previously assigned time slot which may now be assigned to another CODEC.

FIXED TIME SLOT MODE

There are several ways in which the TP3022/TP3023 may operate in the fixed time slot mode. The first and easiest method is to leave CLK_C disconnected or to connect CLK_C to V_{CC}. In this situation, D_C behaves as a power-down input. When D_C goes low, both encode and decode time slots are set to one on the second subsequent frame sync pulse. Time slot one corresponds to the eight CLK_X or CLK_R cycles starting one cycle from the nominal leading edge of FS_X or FS_R respectively. As in the time slot assignment mode, the D_X output is inhibited for one additional frame after the circuit is powered up. A logical "1" on D_C powers the CODEC down on the second subsequent FS_X pulse.

A second fixed time slot method is to operate CLK_C continuously. Placing a "1" on D_C will then cause the serial control register to fill up with ones. With B1 and B2 equal to "1" the CODEC will power-down. Placing a "0" on D_C will cause the serial control register to fill up with zeroes, assigning time slot one to both the encoder and decoder and powering up the device. One important restriction with this method of operation is that the rising transition of D_C must occur at least 8 cycles of CLK_C prior to FS_X. If this restriction is not followed, it is possible that on the frame prior to power-down, the encoder could be assigned to an incorrect time slot (e.g., 1, 3, 7, 15 or 31), resulting in a possible PCM bus conflict.

SERIAL CONTROL PORT

When the TP3022/TP3023 is operated in the time slot assignment mode or the fixed time slot mode with continuous clock, the data on D_C is shifted into the serial control register, bit 1 first. In the time slot assignment mode, depending on B1 and B2, the data in the RCV or XMT time slot registers is updated at the second FS_R or FS_X pulse after the first CLK_C pulse, or the CODEC is powered down. In the continuous clock fixed time slot mode, the CODEC is powered up or down at every second FS_R or FS_X pulse. The control register data is interpreted as follows:

B1	B2	Action
0	0	Assign time slot to encoder and decoder
0	1	Assign time slot to encoder
1	0	Assign time slot to decoder
1	1	Power-down CODEC

B3	B4	B5	B6	B7	B8	Time Slot
0	0	0	0	0	0	1
0	0	0	0	0	1	2
0	0	0	0	1	0	3
0	0	0	0	1	1	4
.	.	.	.	.	.	.
.	.	.	.	.	.	.
.	.	.	.	.	.	.
1	1	1	1	1	0	63
1	1	1	1	1	1	64

During the power-down command, bits 3 through 8 are ignored. Note that with 64 possible time slot assignments it is frequently possible to assign a time slot which does not exist. This can be useful to disable an encoder or decoder without powering down the CODEC.

ENCODING DELAY

The encoding process begins immediately at the end of the encode time slot and is concluded no later than 17 time slots later. In normal applications, this PCM data is not shifted out until the next time slot 125 μs later, resulting in an encoding delay of 125 μs. In some applications it is possible to operate the CODEC at a higher frame rate to reduce this delay. With a 2.048 MHz clock, the FS rate could be increased to 15 kHz reducing the delay from 125 μs to 67 μs.

Functional Description (Continued)

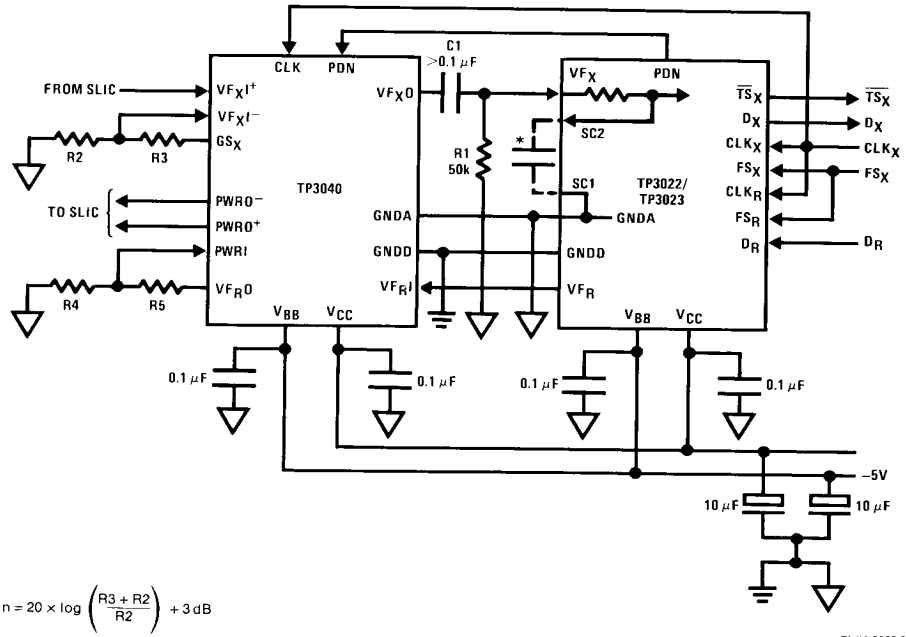
DECODING DELAY

The decoding process begins immediately after the end of the decoder time slot. The output of the decoder sample and hold amplifier is updated 28 CLK_R cycles later. The decoding delay is therefore approximately 28 clock cycles plus one half of a frame time or 81 μs for a 1.544 MHz system with an 8 kHz frame rate or 76 μs for a 2.048 MHz system with an 8 kHz frame rate. Again, for some applications the frame rate could be increased to reduce this delay.

TYPICAL APPLICATION

A typical application of the TP3022/TP3023 used in conjunction with the TP3040 PCM filter is shown. The values of resistor R1 and DC blocking capacitor C1, are non-critical. The capacitor value should exceed 0.1 μF, R1 should not exceed 160 kΩ, and the product R1 x C1 should exceed 4 ms.

Typical Application



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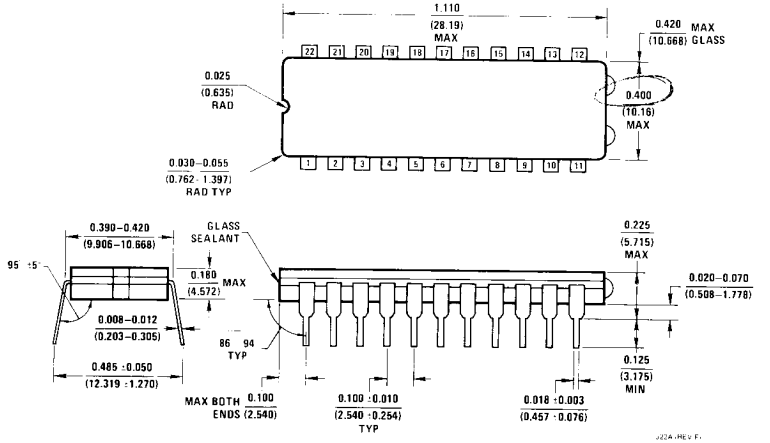
$$\text{XMT gain} = 20 \times \log\left(\frac{R3 + R2}{R2}\right) + 3\,\text{dB}$$

$$\text{RCV gain} = 20 \times \log\left(\frac{R4}{R4 + R5}\right) \text{ for each power amplifier}$$

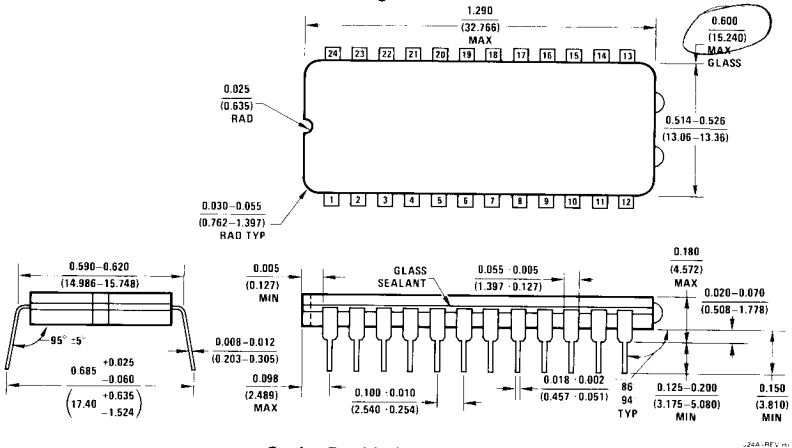
The power supply decoupling capacitors should be 0.1 μF. In order to take advantage of the excellent noise performance of the TP3022/TP3023/TP3040, care must be taken in board layout to prevent coupling of digital noise into the sensitive analog lines.

* The external sample/hold capacitor required for use with pin-compatible NMOS CODECs introduces attenuation due to the capacitive divider formed with C1. The SC2 pin connects VF_X to this sample/hold capacitor via a 300Ω resistor to ensure gain compatibility. The TP3022/TP3023 itself does not require an external sample/hold capacitor for proper operation.

Physical Dimensions (Continued) inches (millimeters)



Cavity Dual-In-Line Package (J)
Order Number TP3023J
NS Package Number J22A



Cavity Dual-In-Line Package (J)
Order Number TP3022J
NS Package Number J24A

LIFE SUPPORT POLICY

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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