

TOSHIBA MOS DIGITAL INTEGRATED CIRCUIT SILICON GATE CMOS

524,288 WORDS × 8 BIT STATIC RAM

DESCRIPTION

The TC554001FI/FTI is a 4,194,304-bit static random access memory (SRAM) organized as 524,288 words by 8 bits. Fabricated using Toshiba's CMOS Silicon gate process technology, this device operates from a single 5V ± 10% power supply. Advanced circuit technology provides both high speed and low power at an operating current of 10mA/MHz(typ) and minimum cycle time of 85 ns. It is automatically placed in low-power mode at 140 μA standby current (max) when chip enable (CE) is asserted high. There are two control inputs. \overline{CE} is used to select the device and for data retention control, and output enable (\overline{OE}) provides fast memory access. This device is well suited to various microprocessor system applications where high speed, low power and battery backup are required. And, with a guaranteed operating range of -40 to 85°C, the TC554001FI/FTI can be used in environments exhibiting extreme temperature conditions. The TC554001FI/FTI is available in a standard plastic 32-pin small-outline package(SOP) and 32-pin thin-small-outline package(TSOP).

FEATURES

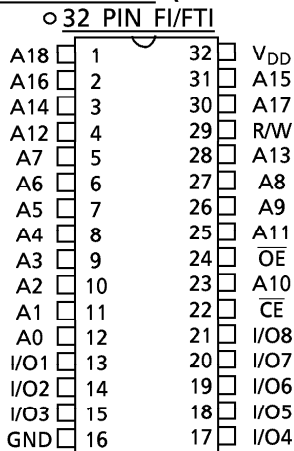
- Low-power dissipation
Operating: 55 mW/MHz (typical)
- Standby current of 8 μA (maximum) at Ta = 25°C
- Single power supply voltage of 5 V ± 10 %
- Power down features using CE
- Data retention supply voltage of 2.0 to 5.5 V
- Directly TTL compatibility for all inputs and outputs
- Wide operating temperature range of - 40° to 85°C

- Access Time (maximum)

	TC551001FI/FTI	
	-85L	-10L
Access Time	85 ns	100 ns
CE Access Time	85 ns	100 ns
OE Access Time	45 ns	50 ns

- Package:
SOP32-P-525-1.27 (FI) (Weight: 1.14 g typ)
TSOP II 32-P-400-1.27 (FTI) (Weight: 0.51 g typ)

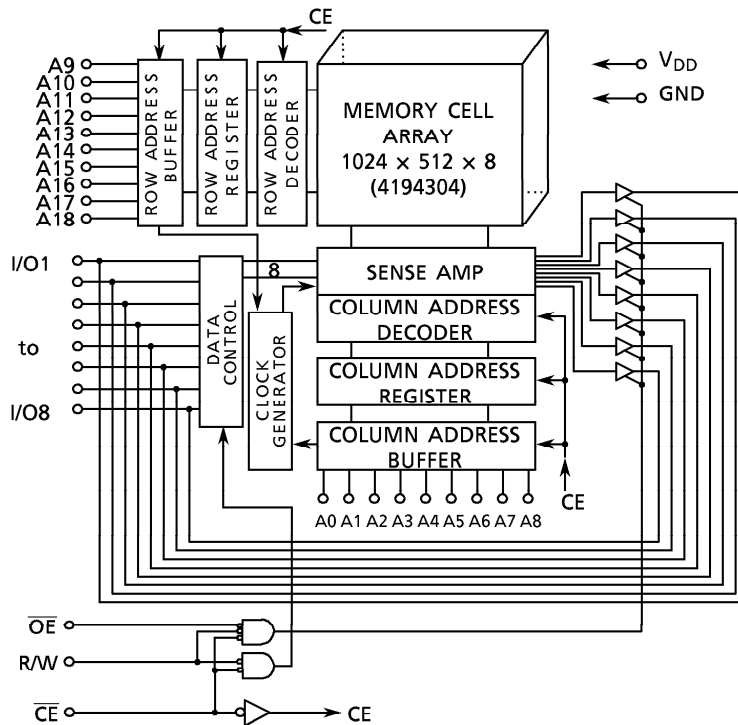
PIN ASSIGNMENT (TOP VIEW)



PIN NAMES

A0 to A18	Address Inputs
R/W	Read/Write Control
\overline{OE}	Output Enable
\overline{CE}	Chip Enable
I/O1 to I/O8	Data Input/Output
V _{DD}	Power (+ 5 V)
GND	Ground

BLOCK DIAGRAM



961001EBA1

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OPERATION MODE

OPERATION MODE	\overline{CE}	\overline{OE}	R/W	I/O1 to I/O8	POWER
Read	L	L	H	D _{OUT}	I _{DDO}
Write	L	x	L	D _{IN}	I _{DDO}
Output Disabled	L	H	H	High-Z	I _{DDO}
Standby	H	x	x	High-Z	I _{DDS}

Note: X = don't care. H=logic high. L=logic low.

ABSOLUTE MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V _{DD}	Power Supply Voltage	- 0.3 to 7.0	V
V _{IN}	Input Voltage	- 0.3* to 7.0	V
V _{I/O}	Input and Output Voltage	- 0.5 to V _{DD} + 0.5	V
P _D	Power Dissipation	0.6	W
T _{solder}	Soldering Temperature (10 s)	260	°C
T _{strg.}	Storage Temperature	- 55 to 150	°C
T _{opr.}	Operating Temperature	- 40 to 85	°C

* - 3.0 V when measured at a pulse width of 50 ns

DC RECOMMENDED OPERATING CONDITIONS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V
V _{IH}	Input High Voltage	2.4	-	V _{DD} + 0.3	V
V _{IL}	Input Low Voltage	- 0.3*	-	0.6	V
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V

* - 3.0 V when measured at a pulse width of 50 ns

DC CHARACTERISTICS (Ta = - 40° to 85°C, V_{DD} = 5 V ± 10%)

SYMBOL	PARAMETER	TEST CONDITION		MIN	TYP	MAX	UNIT	
I _{IL}	Input Leakage Current	V _{IN} = 0 V to V _{DD}		-	-	± 1.0	μA	
I _{OH}	Output High Current	V _{OH} = 2.4 V		- 1.0	-	-	mA	
I _{OL}	Output Low Current	V _{OL} = 0.4 V		2.1	-	-	mA	
I _{LO}	Output Leakage Current	$\overline{CE} = V_{IH}$ or R/W = V _{IL} or $\overline{OE} = V_{IH}$ V _{OUT} = 0 V to V _{DD}		-	-	± 1.0	μA	
I _{DDO1}	Operating Current	$\overline{CE} = V_{IL}$ and R/W = V _{IH} I _{OUT} = 0 mA Other Inputs = V _{IH} /V _{IL}	Tcycle	min	-	-	80	mA
				1 μs	-	15	-	
I _{DDO2}	Operating Current	$\overline{CE} = 0.2 V$ and R/W = V _{DD} -0.2 V I _{OUT} = 0 mA Other Inputs = V _{DD} -0.2 V/0.2 V	Tcycle	min	-	-	70	mA
				1 μs	-	10	-	
I _{DDS1}	Standby Current	$\overline{CE} = V_{IH}$		-	-	3	mA	
I _{DDS2}		$\overline{CE} = V_{DD} - 0.2 V$ V _{DD} = 2.0 to 5.5 V	Ta = 25°C	-	4	8	μA	
		Ta = -40° to 85°C	-	-	140			

CAPACITANCE (Ta = 25°C, f = 1 MHz)

SYMBOL	PARAMETER	TEST CONDITION	MAX	UNIT
C _{IN}	Input Capacitance	V _{IN} = GND	10	pF
C _{OUT}	Output Capacitance	V _{OUT} = GND	10	pF

Note: This parameter is periodically sampled and is not 100% tested.

AC CHARACTERISTICS AND OPERATING CONDITIONS

(Ta = - 40° to 85°C, VDD = 5 V ± 10%)

READ CYCLE

SYMBOL	PARAMETER	TC554001FI/FTI				UNIT
		-85L		-10L		
		MIN	MAX	MIN	MAX	
t _{RC}	Read Cycle Time	85	–	100	–	ns
t _{ACC}	Address Access Time	–	85	–	100	
t _{CO}	Chip Enable Access Time	–	85	–	100	
t _{OE}	Output Enable Access Time	–	45	–	50	
t _{COE}	Chip Enable Low to Output in Active	5	–	5	–	
t _{OOE}	Output Enable Low to Output Active	0	–	0	–	
t _{OD}	Chip Enable Hige to Output High-Z	–	35	–	40	
t _{ODO}	Output Enable Hige to Output High-Z	–	35	–	40	
t _{OH}	Output Data Hold Time	10	–	10	–	

WRITE CYCLE

SYMBOL	PARAMETER	TC554001FI/FTI				UNIT
		-85L		-10L		
		MIN	MAX	MIN	MAX	
t _{WC}	Write Cycle Time	85	–	100	–	ns
t _{WP}	Write Pulse Width	55	–	60	–	
t _{CW}	Chip Enable to End of Write	70	–	80	–	
t _{AS}	Address Setup Time	0	–	0	–	
t _{WR}	Write Recovery Time	0	–	0	–	
t _{ODW}	R/W Low to Output High-Z	–	35	–	40	
t _{OEW}	R/W High to Output Active	0	–	0	–	
t _{DS}	Data Setup Time	35	–	40	–	
t _{DH}	Data Hold Time	0	–	0	–	

AC TEST CONDITIONS

Output Load: 100 pF + one TTL gate

Input Pulse Level: 0.4 V, 2.6 V

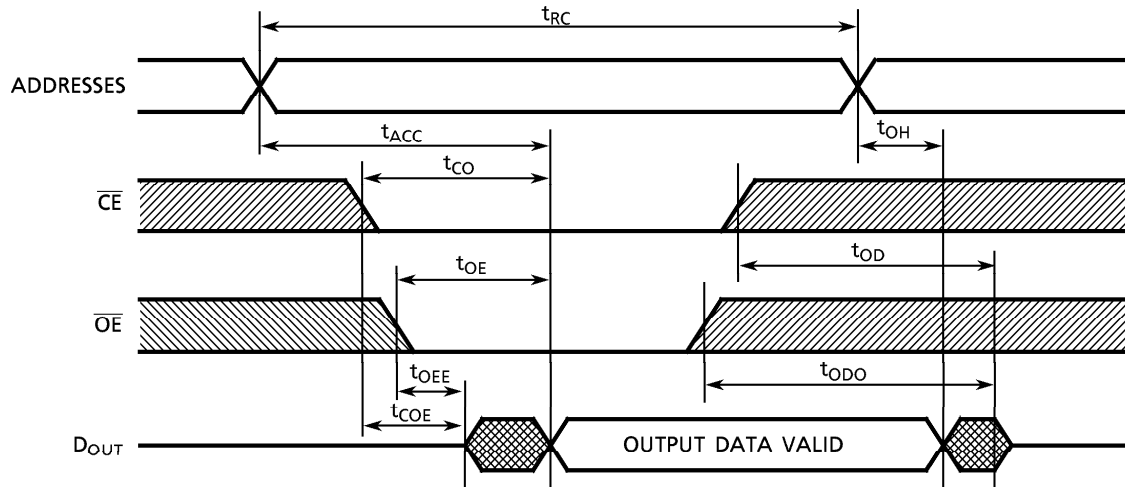
Timing Measurements: 1.5 V

Reference Level: 1.5 V

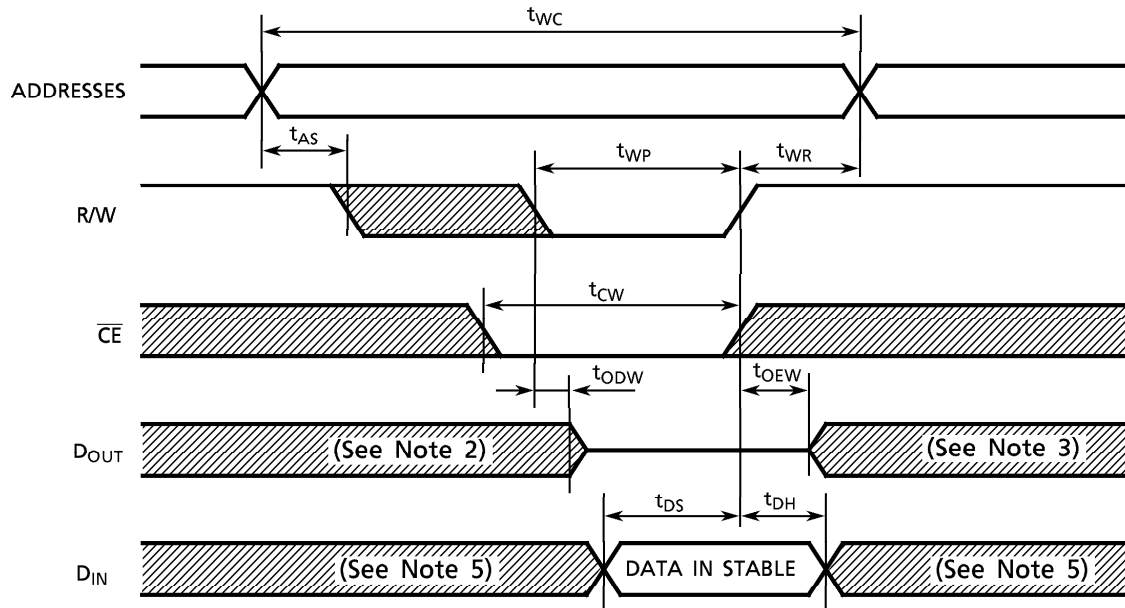
t_r, t_F: 5 ns

TIMING WAVEFORMS

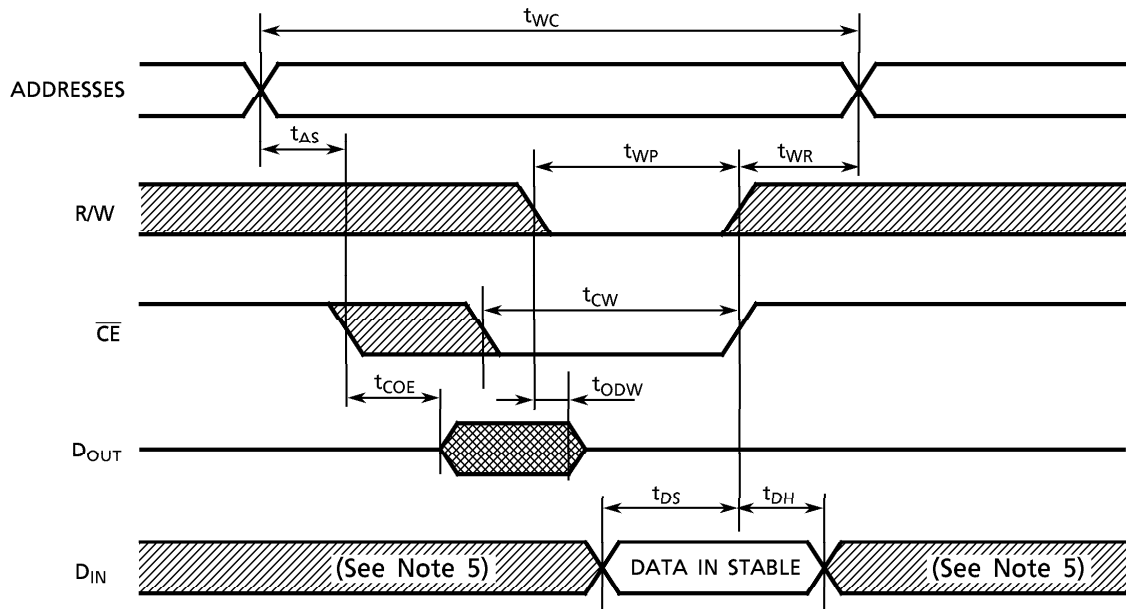
READ CYCLE (See Note 1)



WRITE CYCLE 1 (R/W CONTROLLED) (See Note 4)



WRITE CYCLE 2 (\overline{CE} CONTROLLED) (See Note 4)



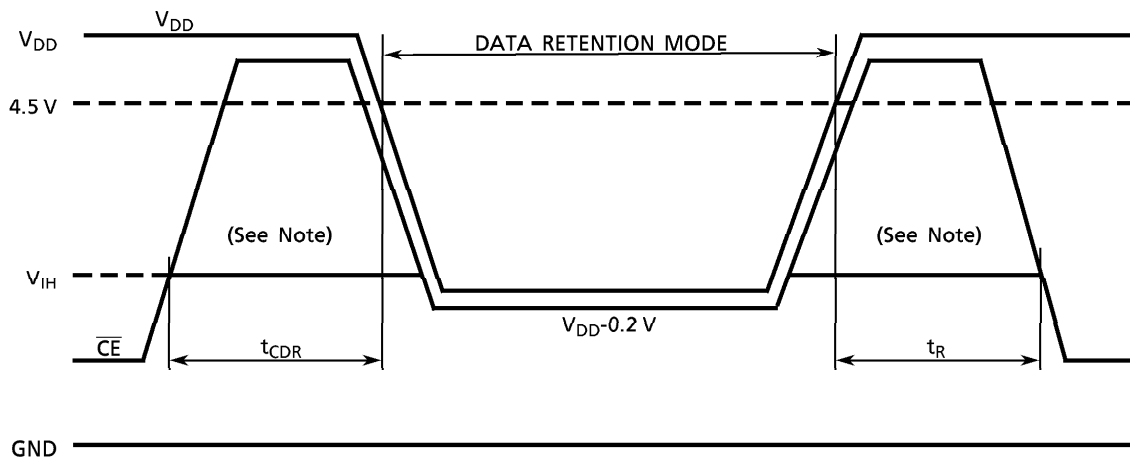
- (1) R/W remains High for Read Cycle.
- (2) If \overline{CE} goes coincident with or after R/W goes LOW, the output will remain at high impedance.
- (3) If \overline{CE} goes HIGH coincident with or before R/W goes HIGH, the output will remain at high impedance.
- (4) IF \overline{CE} is HIGH during the write cycle, the outputs will remain at high impedance.
- (5) Because I/O signals may be in the output state at this time, input signals of reverse polarity must not be applied.

DATA RETENTION CHARACTERISTICS (Ta = - 40° to 85°C)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
V _{DH}	Data Retention Supply Voltage	2.0	-	5.5	V
I _{DDS2}	Standby Current	V _{DH} = 3.0 V	-	70 *	μA
		V _{DH} = 5.5 V	-	140	
t _{CDR}	Chip Deselect to Data Retention Mode Time	0	-	-	nS
t _R	Recovery Time	5	-	-	mS

*) 6 μA (max) Ta = - 40° to 40°C

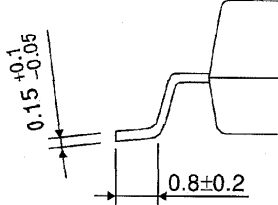
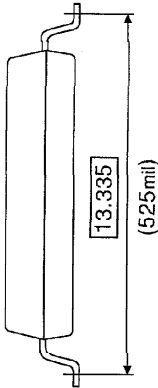
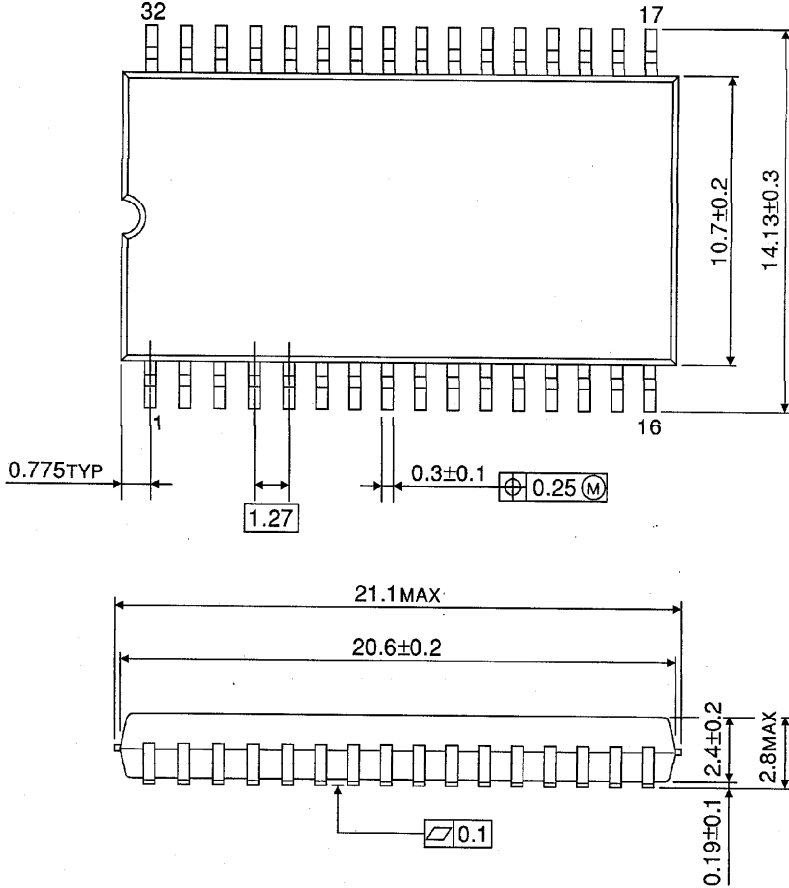
CE Controlled Data Retention Mode



Note: When CE is operating at the V_{IH} level (2.4V), the standby current is given by I_{DDS1} during the transition of V_{DD} from 4.5 to 2.6V.

PACKAGE DIMENSIONS (SOP32-P-525-1.27)

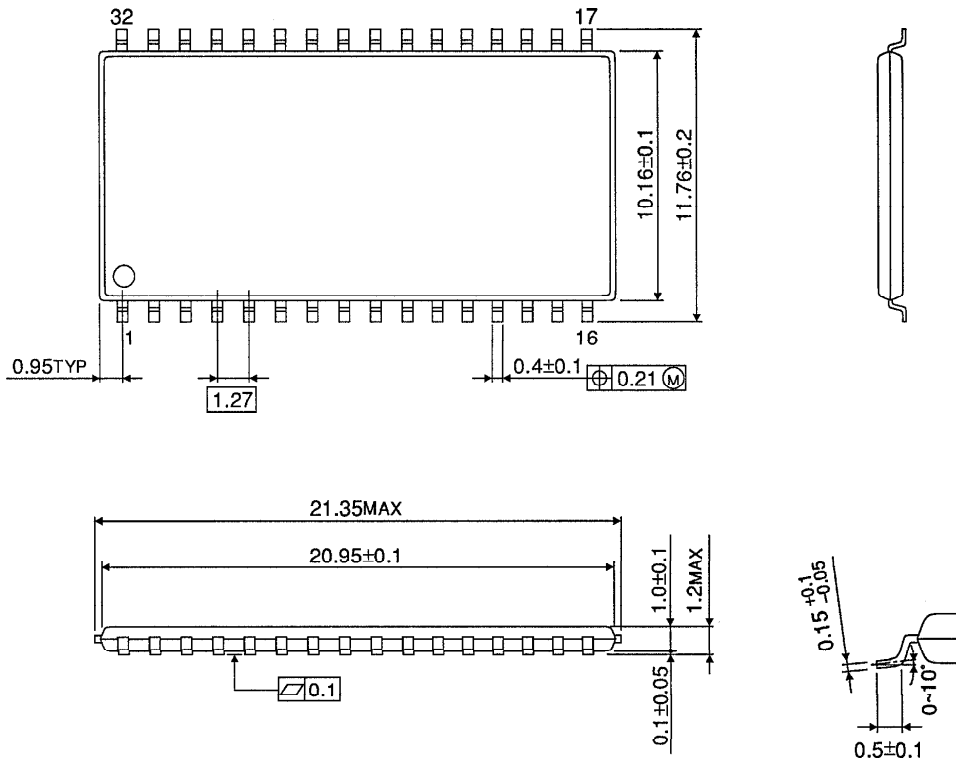
Unit in mm



Weight: 1.14 g (typ)

PACKAGE DIMENSIONS (TSOPII 32-P-400-1.27)

Unit in mm



Weight: 0.51 g (typ)