Am4ILV3204M

Data Sheet

July 2003

The following document specifies Spansion memory products that are now offered by both Advanced Micro Devices and Fujitsu. Although the document is marked with the name of the company that originally developed the specification, these products will be offered to customers of both AMD and Fujitsu.

Continuity of Specifications

There is no change to this datasheet as a result of offering the device as a Spansion product. Any changes that have been made are the result of normal datasheet improvement and are noted in the document revision summary, where supported. Future routine revisions will occur when appropriate, and changes will be noted in a revision summary.

Continuity of Ordering Part Numbers

AMD and Fujitsu continue to support existing part numbers beginning with "Am" and "MBM". To order these products, please use only the Ordering Part Numbers listed in this document.

For More Information

Please contact your local AMD or Fujitsu sales office for additional information about Spansion memory solutions.

Publication Number **30119** Revision **A** Amendment **+1** Issue Date **June 10, 2003**

PRELIMINARY

Am41LV3204M

Stacked Multi-chip Package (MCP) 32 Mbit (4 M x 8 bit/2 M x 16-bit) Flash Memory and 4 Mbit (512K x 8-Bit/256 K x 16-Bit) Static RAM

DISTINCTIVE CHARACTERISTICS

MCP Features

- **Power supply voltage of 2.7 to 3.3 volt**
- **High Performance**
  - — Access time as fast as 100ns initial 30 ns page Flash 70 ns SRAM
- **Package**
  - — 69-Ball FBGA
  - — 8 x 10 x 1.2 mm
- **Operating Temperature**
  - — –40°C to +85°C

Flash Memory Features

ARCHITECTURAL ADVANTAGES

- **Single power supply operation**
  - — 3 V for read, erase, and program operations
- **Manufactured on 0.23 µm MirrorBit process technology**
- **SecSi™ (Secured Silicon) Sector region**
  - — 128-word/256-byte sector for permanent, secure identification through an 8-word/16-byte random Electronic Serial Number, accessible through a command sequence
  - — May be programmed and locked at the factory or by the customer
- **Flexible sector architecture**
  - — Sixty-three 32 Kword/64-kbyte sectors
  - — Eight 4 Kword/8-kbyte boot sectors
- **Compatibility with JEDEC standards**
  - — Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- **Minimum 100,000 erase cycle guarantee per sector**
- **20-year data retention at 125°C**

PERFORMANCE CHARACTERISTICS

- **High performance**
  - — 100 ns access time
  - — 30 ns page read times
  - — 0.5 s typical sector erase time
  - — 15 µs typical write buffer word programming time: 16-word/32-byte write buffer reduces overall programming time for multiple-word updates
  - — 4-word/8-byte page read buffer
  - — 16-word/32-byte write buffer
- **Low power consumption (typical values at 3.0 V, 5 MHz)**
  - — 30 mA typical initial Page read current; 10 mA typical intra-Page read current
  - — 50 mA typical erase/program current
  - — 1 µA typical standby mode current

SOFTWARE & HARDWARE FEATURES

- **Software features**
  - — Program Suspend & Resume: read other sectors before programming operation is completed
  - — Erase Suspend & Resume: read/program other sectors before an erase operation is completed
  - — Data# polling & toggle bits provide status
  - — Unlock Bypass Program command reduces overall multiple-word programming time
  - — CFI (Common Flash Interface) compliant: allows host system to identify and accommodate multiple flash devices
- **Hardware features**
  - — Sector Group Protection: hardware-level method of preventing write operations within a sector group
  - — Temporary Sector Unprotect: V_{ID}-level method of changing code in locked sectors
  - — WP#/ACC input:
    Write Protect input (WP#) protects top or bottom two sectors regardless of sector protection settings
    ACC (high voltage) accelerates programming time for higher throughput during system production
  - — Hardware reset input (RESET#) resets device

SRAM Features

- **Power dissipation**
  - — Operating: 30 mA maximum
  - — Standby: 10 µA maximum
- **CE1s# and CE2s Chip Select**
- **Power down features using CE1s# and CE2s**
- **Data retention supply voltage: 1.5 to 3.3 volt**
- **Byte data control: LB#s (DQ7–DQ0), UB#s (DQ15–DQ8)**

Publication# **30119** Rev: **A** Amendment/**+1**
Issue Date: **June 10, 2003**

GENERAL DESCRIPTION

Am29LV320MT Features

The Am29LV320MT/B is a 32 Mbit, 3.0 volt single power supply flash memory device organized as 2,097,152 words or 4,194,304 bytes. The device has an 8/16-bit bus and can be programmed either in the host system or in standard EPROM programmers. Word mode data appears on DQ15–DQ0. The device is designed to be programmed in-system with the standard 3.0 volt V_{CC} supply, and can also be programmed in standard EPROM programmers.

LV320MT/B has an access time of 100 ns. Note that the access time has a specific operating voltage range (V_{CC}) as specified in the Product Selector Guide and the Ordering Information sections. The device is offered in a 69-ball Fine Pitch BGA.

The devices require only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Device programming and erasure are initiated through command sequences. Once a program or erase operation has begun, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend/Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the Flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses have been stable for a specified period of time.

The **Write Protect (WP#)** feature protects the top or bottom two sectors by asserting a logic low on the WP#/ACC pin. The protected sector will still be protected even during accelerated programming.

The **SecSi™ (Secured Silicon) Sector** provides a 128-word/256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

AMD MirrorBit flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

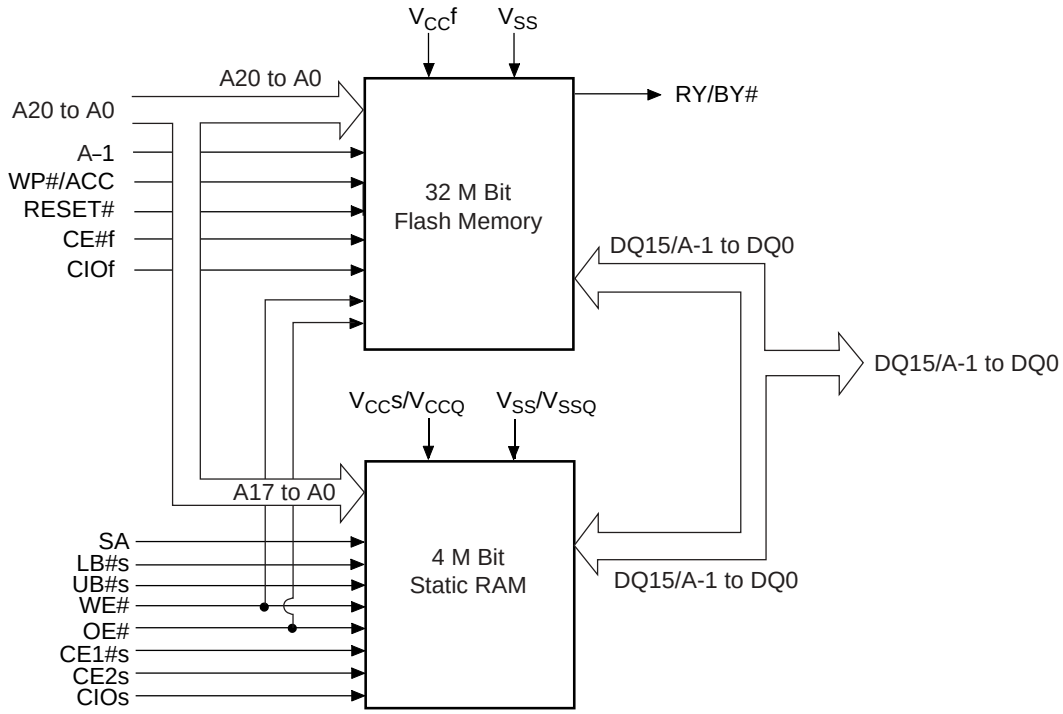
TABLE OF CONTENTS

PRODUCT SELECTOR GUIDE

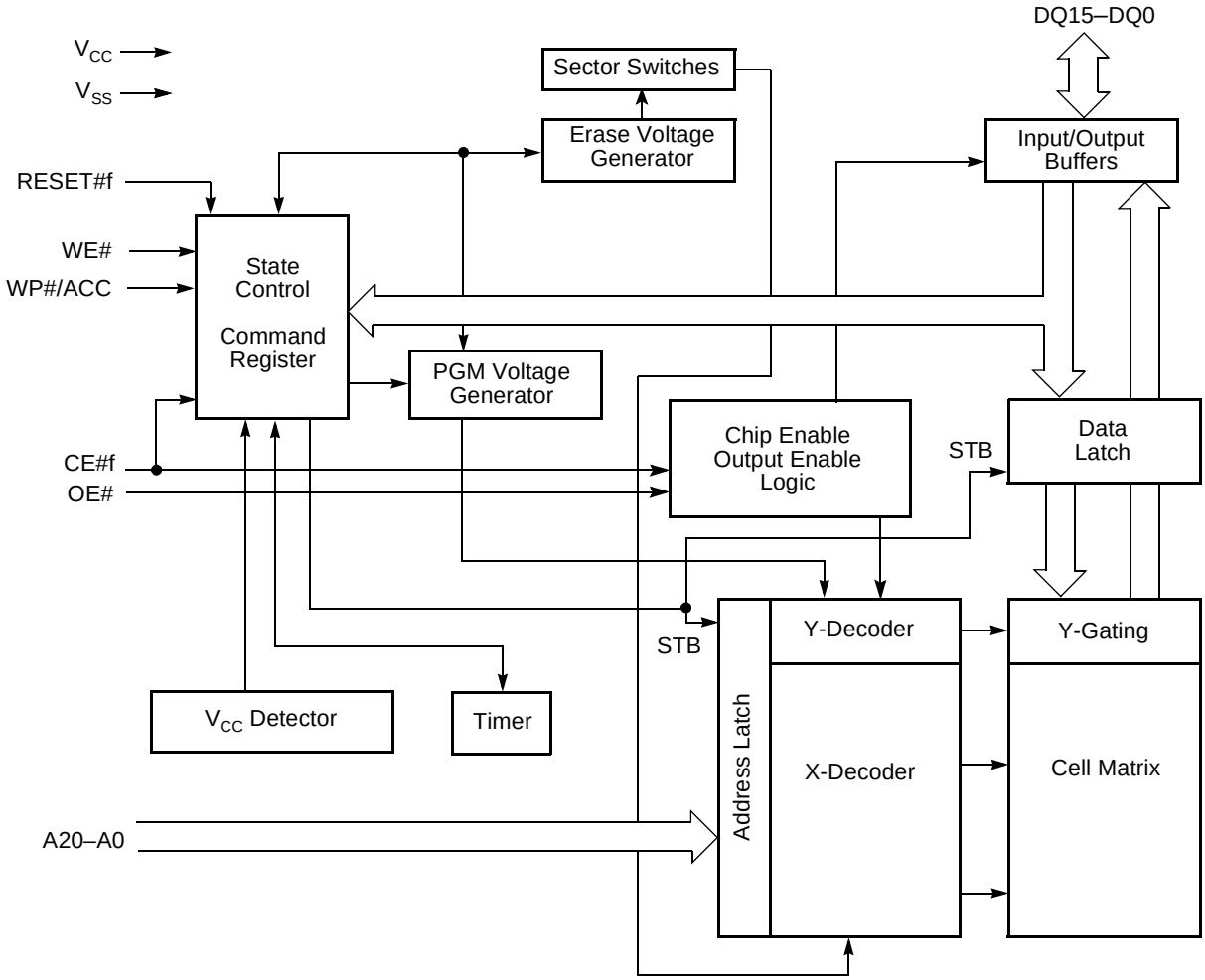
Family Part Number		Am41LV3204M	
		Flash Memory	SRAM
Speed Option	Standard Voltage Range: V_{CC} = 2.7–3.3 V	10	10
Max Access Time (ns)		100	70
Max. CE# Access (ns)		100	70
Max. Page Access Time (t_{PACC})		30	N/A
OE# Access (ns)		30	35

Note: *See "AC Characteristics" for full specifications.*

MCP BLOCK DIAGRAM

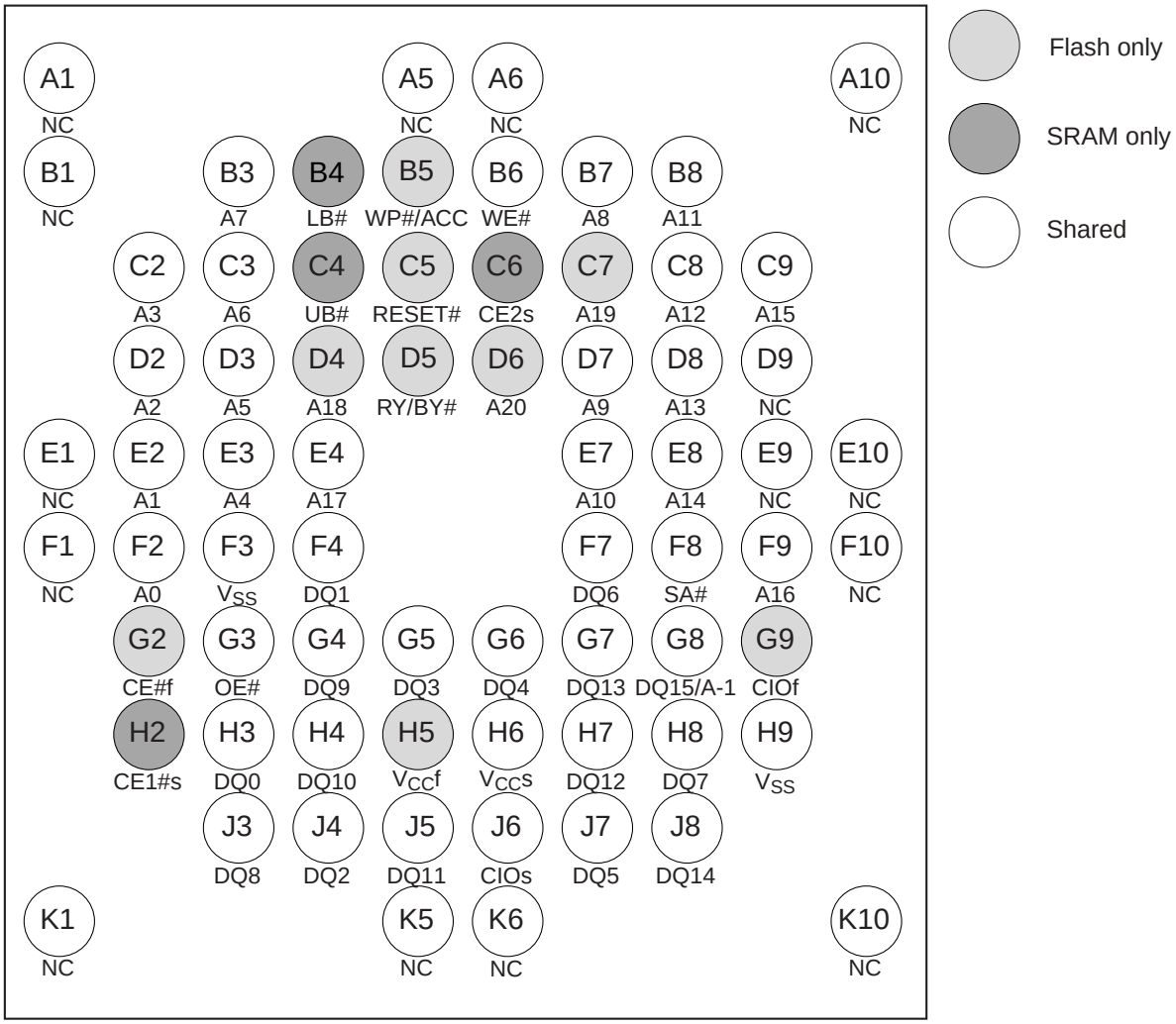


FLASH MEMORY BLOCK DIAGRAM



CONNECTION DIAGRAMS

69-ball Fine-pitch BGA
Top View, Balls Facing Down



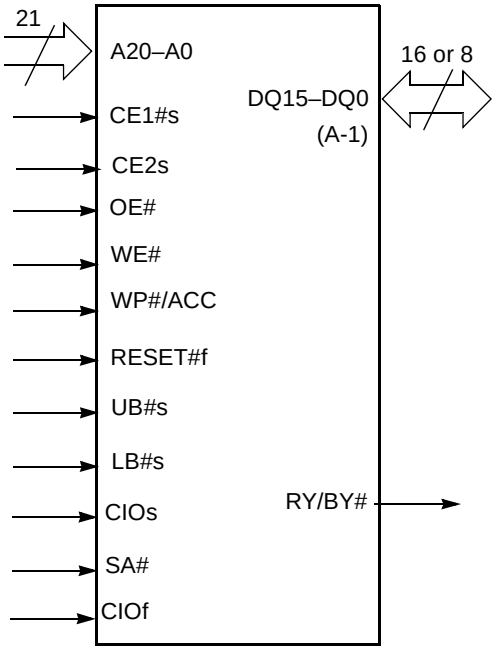
SPECIAL PACKAGE HANDLING INSTRUCTIONS FOR FBGA PACKAGES

Special handling is required for Flash Memory products in molded packages (BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures about 150°C for prolonged periods of time.

PIN DESCRIPTION

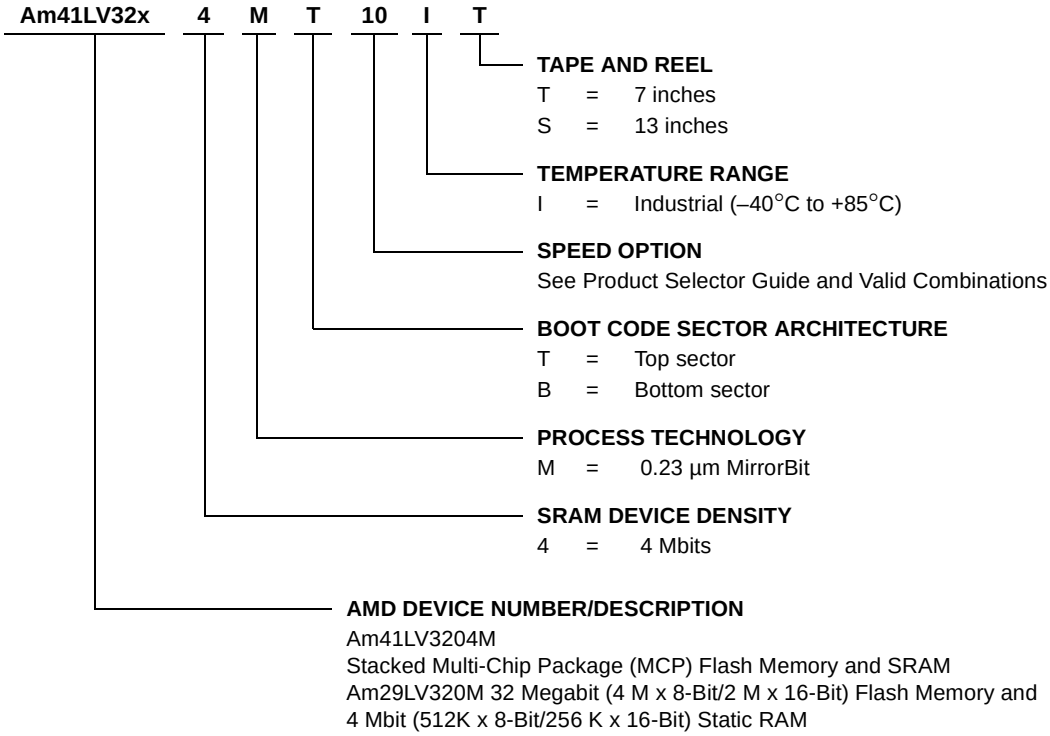
A20–A0	=	21 Address inputs
DQ14–DQ0	=	15 Data inputs/outputs
DQ15/A-1	=	DQ15 (Data input/output, word mode), A-1 (25B Address input, byte mode)
CE#f	=	Chip Enable input (Flash)
CE1#s, CE2s	=	Chip Enable (SRAM)
OE#	=	Output Enable input (Flash)
WE#	=	Write Enable input (Flash)
WP#/ACC	=	Hardware Write Protect input/Programming Acceleration input (Flash)
RESET#f	=	Hardware Reset Pin input (Flash)
V_{CC}f	=	Flash 3.0 volt-only single power supply (see Product Selector Guide for speed options and voltage supply tolerances)
V_{CC}s	=	SRAM Power Supply
V_{SS}	=	Device Ground
NC	=	Pin Not Connected Internally
UB#s	=	Upper Byte Control (SRAM)
LB#s	=	Lower Byte Control (SRAM)
CIOs	=	I/O Configuration (SRAM)
		CIOs = V_{IH} = Word Mode (x16)
		CIOs = V_{IL} = Byte Mode (X8)
SA	=	Highest Order Address Pin (SRAM)
		Byte Mode
CIOf	=	I/O Configuration (Flash)
		CIOf = V_{IH} = Word Mode (x16)
		CIOf = V_{IL} = Byte Mode (X8)

LOGIC SYMBOL



ORDERING INFORMATION

The order number (Valid Combination) is formed by the following:



Valid Combinations		
Order Number		**Package Marking**
Am41LV3204MT10I	T	M410000095
Am41LV3204MB10I		M410000096

Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations and to check on newly released combinations

DEVICE BUS OPERATIONS

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. Table 1 lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 1. Device Bus Operations—Flash Word Mode, CIOf = V_{IH}, SRAM Word Mode, CIOs = V_{IH}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s	UB#s	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 4)	D_{IN}	D_{IN}
		X	L										
Standby	$V_{CC} \pm 0.3$ V	H	X	X	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
		X	L										
Output Disable	L	L	H	H	H	X	X	L	X	H	L/H	High-Z	High-Z
				H	H	X	X	X	L				
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	X	X	X	X	X	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	X	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
								H	L			High-Z	D_{OUT}
								L	H			D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	X	A_{IN}	L	L	H	X	D_{IN}	D_{IN}
								H	L			High-Z	D_{IN}
								L	H			D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

Table 2. Device Bus Operations—Flash Word Mode, CIOf = V_{IH}, SRAM Word Mode, CIOs = V_{IL}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	D_{OUT}
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 3)	D_{IN}	D_{IN}
		X	L										
Standby	$V_{CC} \pm 0.3$ V	H	X	X	X	X	X	X	X	$V_{CC} \pm 0.3$ V	H	High-Z	High-Z
		X	L										
Output Disable	L	L	H	H	H	SA	X	DNU	DNU	H	L/H	High-Z	High-Z
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = H, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	X	X	X	X	A_{IN}	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	SA	A_{IN}	X	X	H	X	D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	SA	A_{IN}	X	X	H	X	D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In, D_{IN} = Data In, D_{OUT} = Data Out, DNU = Do Not Use*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

Table 3. Device Bus Operations—Flash Byte Mode, CIOf = V_{IL}; SRAM Word Mode, CIOs = V_{CC}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	High-Z
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 3)	D_{IN}	High-Z
		X	L										
Standby	V_{CC} ± 0.3 V	H	X	X	X	X	X	X	X	V_{CC} ± 0.3 V	H	High-Z	High-Z
		X	L										
Output Disable	L	L	H	H	H	X	X	L	X	H	L/H	High-Z	High-Z
								X	L				
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	x	X	X	X	A_{IN}	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	X	A_{IN}	L	L	H	X	D_{OUT}	D_{OUT}
								H	L			High-Z	D_{OUT}
								L	H			D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	X	A_{IN}	L	L	H	X	D_{IN}	D_{IN}
								H	L			High-Z	D_{IN}
								L	H			D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In (for Flash Byte Mode, DQ15 = A-1), D_{IN} = Data In, D_{OUT} = Data Out*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "" section.*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

Table 4. Device Bus Operations—Flash Byte Mode, CIOf = V_{IL}; SRAM Byte Mode, CIOs = V_{SS}

Operation (Notes 1, 2)	CE#f	CE1#s	CE2s	OE#	WE#	SA	Addr.	LB#s (Note 3)	UB#s (Note 3)	RESET#	WP#/ACC (Note 4)	DQ7–DQ0	DQ15–DQ8
Read from Flash	L	H	X	L	H	X	A_{IN}	X	X	H	L/H	D_{OUT}	High-Z
		X	L										
Write to Flash	L	H	X	H	L	X	A_{IN}	X	X	H	(Note 3)	D_{IN}	High-Z
		X	L										
Standby	V_{CC} ± 0.3 V	H	X	X	X	X	X	X	X	V_{CC} ± 0.3 V	H	High-Z	High-Z
		X	L										
Output Disable	H	L	H	H	H	SA	X	DNU	DNU	H	L/H	High-Z	High-Z
Flash Hardware Reset	X	H	X	X	X	X	X	X	X	L	L/H	High-Z	High-Z
		X	L										
Sector Protect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	L/H	D_{IN}	X
		X	L										
Sector Unprotect (Note 5)	L	H	X	H	L	X	SADD, A6 = L, A1 = H, A0 = L	X	X	V_{ID}	(Note 6)	D_{IN}	X
		X	L										
Temporary Sector Unprotect	X	H	X	X	X	X	A_{IN}	X	X	V_{ID}	(Note 6)	D_{IN}	High-Z
		X	L										
Read from SRAM	H	L	H	L	H	SA	A_{IN}	X	X	H	X	D_{OUT}	High-Z
Write to SRAM	H	L	H	X	L	SA	A_{IN}	X	X	H	X	D_{IN}	High-Z

Legend: *L = Logic Low = V_{IL}, H = Logic High = V_{IH}, V_{ID} = 11.5–12.5 V, V_{HH} = 9.0 ± 0.5 V, X = Don't Care, SA = SRAM Address Input, Byte Mode, SADD = Flash Sector Address, A_{IN} = Address In (for Flash Byte Mode, DQ15 = A-1), D_{IN} = Data In, D_{OUT} = Data Out, DNU = Do Not Use*

Notes:

1. *Other operations except for those indicated in this column are inhibited.*
2. *Do not apply CE#f = V_{IL}, CE1#s = V_{IL} and CE2s = V_{IH} at the same time.*
3. *Don't care or open LB#s or UB#s.*
4. *If WP#/ACC = V_{IL} , the boot sectors will be protected. If WP#/ACC = V_{IH} the boot sectors protection will be removed. If WP#/ACC = V_{ACC} (9V), the program time will be reduced by 40%.*
5. *The sector protect and sector unprotect functions may also be implemented via programming equipment. See the "".*
6. *If WP#/ACC = V_{IL}, the two outermost boot sectors remain protected. If WP#/ACC = V_{IH}, the two outermost boot sector protection depends on whether they were last protected or unprotected using the method described in "". If WP#/ACC = $V_{HH,}$ all sectors will be unprotected.*

Requirements for Reading Array Data

To read array data from the outputs, the system must drive the CE# and OE# pins to V_{IL}. CE# is the power control and selects the device. OE# is the output control and gates array data to the output pins. WE# should remain at V_{IH}. The CIOf pin determines whether the device outputs array data in words or bytes.

The internal state machine is set for reading array data upon device power-up, or after a hardware reset. This ensures that no spurious alteration of the memory content occurs during the power transition. No command is necessary in this mode to obtain array data. Standard microprocessor read cycles that assert valid addresses on the device address inputs produce valid data on the device data outputs. The device remains enabled for read access until the command register contents are altered.

See “Reading Array Data” for more information. Refer to the AC Flash Read-Only Operations table for timing specifications and to Figure 14 for the timing diagram. Refer to the DC Characteristics table for the active current specification on reading array data.

Page Mode Read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 4 words/8-bytes. The appropriate page is selected by the higher address bits A(max)–A2. Address bits A1–A0 determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE#f is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the “read-page addresses” constant and changing the “intra-read page” addresses.

Writing Commands/Command Sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word or byte, instead of four. The “Word Program Command Sequence” section has details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. Tables 3 and 2 indicates the address space that each sector occupies.

Refer to the DC Characteristics table for the active current specification for the write mode. The AC Characteristics section contains timing specification tables and timing diagrams for write operations.

Write Buffer

Write Buffer Programming allows the system to write a maximum of 16 words/32-bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. See “Write Buffer” for more information.

Accelerated Program Operation

The device offers accelerated program operations through the ACC function. This is one of two functions provided by the WP#/ACC pin. This function is primarily intended to allow faster manufacturing throughput at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the aforementioned Unlock Bypass mode, temporarily unprotects any protected sectors, and uses the higher voltage on the pin to reduce the time required for program operations. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC pin returns the device to normal operation. *Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. In addition, no external pullup is necessary since the WP#/ACC pin has internal pullup to V_{CC}.*

Autoselect Functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings apply in this mode. Refer to the Autoselect Mode and Autoselect Command Sequence sections for more information.

Standby Mode

When the system is not reading or writing to the device, it can place the device in the standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE#f and RESET# pins are both held at V_{CC} ± 0.3 V.

(Note that this is a more restricted voltage range than V_{IH}.) If CE#f and RESET# are held at V_{IH}, but not within V_{CC} ± 0.3 V, the device will be in the standby mode, but the standby current will be greater. The device requires standard access time (t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the DC Characteristics table for the standby current specification.

Automatic Sleep Mode

The automatic sleep mode minimizes Flash device energy consumption. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. The automatic sleep mode is independent of the CE#, WE#, and OE# control signals. Standard address access timings provide new data when addresses are changed. While in sleep mode, output data is latched and always available to the system. Refer to the DC Characteristics table for the automatic sleep mode current specification.

RESET#: Hardware Reset Pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven low for at least a period of t_{RP}, the device immediately terminates any operation in progress, tristates all output pins, and ignores all read/write commands for the duration of the RESET# pulse. The device also resets the internal state machine to reading array data. The operation that was interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at V_{SS}±0.3 V, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL} but not within V_{SS}±0.3 V, the standby current will be greater.

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the Flash memory, enabling the system to read the boot-up firmware from the Flash memory.

Refer to the AC Characteristics tables for RESET# parameters and to Figure 16 for the timing diagram.

Output Disable Mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in the high impedance state.

Table 5. Am29LV320M Top Boot Sector Architecture

Sector	Sector Address A20–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA0	000000xxx	64/32	000000h–00FFFFh	00000h–07FFFh
SA1	000001xxx	64/32	010000h–01FFFFh	08000h–0FFFFh
SA2	000010xxx	64/32	020000h–02FFFFh	10000h–17FFFh
SA3	000011xxx	64/32	030000h–03FFFFh	18000h–1FFFFh
SA4	000100xxx	64/32	040000h–04FFFFh	20000h–27FFFh
SA5	000101xxx	64/32	050000h–05FFFFh	28000h–2FFFFh
SA6	000110xxx	64/32	060000h–06FFFFh	30000h–37FFFh
SA7	000111xxx	64/32	070000h–07FFFFh	38000h–3FFFFh
SA8	001000xxx	64/32	080000h–08FFFFh	40000h–47FFFh
SA9	001001xxx	64/32	090000h–09FFFFh	48000h–4FFFFh
SA10	001010xxx	64/32	0A0000h–0AFFFFh	50000h–57FFFh
SA11	001011xxx	64/32	0B0000h–0BFFFFh	58000h–5FFFFh
SA12	001100xxx	64/32	0C0000h–0CFFFFh	60000h–67FFFh
SA13	001101xxx	64/32	0D0000h–0DFFFFh	68000h–6FFFFh
SA14	001101xxx	64/32	0E0000h–0EFFFFh	70000h–77FFFh
SA15	001111xxx	64/32	0F0000h–0FFFFFh	78000h–7FFFFh
SA16	010000xxx	64/32	100000h–00FFFFh	80000h–87FFFh
SA17	010001xxx	64/32	110000h–11FFFFh	88000h–8FFFFh
SA18	010010xxx	64/32	120000h–12FFFFh	90000h–97FFFh
SA19	010011xxx	64/32	130000h–13FFFFh	98000h–9FFFFh
SA20	010100xxx	64/32	140000h–14FFFFh	A0000h–A7FFFh
SA21	010101xxx	64/32	150000h–15FFFFh	A8000h–AFFFFh
SA22	010110xxx	64/32	160000h–16FFFFh	B0000h–B7FFFh
SA23	010111xxx	64/32	170000h–17FFFFh	B8000h–BFFFFh
SA24	011000xxx	64/32	180000h–18FFFFh	C0000h–C7FFFh
SA25	011001xxx	64/32	190000h–19FFFFh	C8000h–CFFFFh
SA26	011010xxx	64/32	1A0000h–1AFFFFh	D0000h–D7FFFh
SA27	011011xxx	64/32	1B0000h–1BFFFFh	D8000h–DFFFFh
SA28	011000xxx	64/32	1C0000h–1CFFFFh	E0000h–E7FFFh
SA29	011101xxx	64/32	1D0000h–1DFFFFh	E8000h–EFFFFh
SA30	011110xxx	64/32	1E0000h–1EFFFFh	F0000h–F7FFFh
SA31	011111xxx	64/32	1F0000h–1FFFFFh	F8000h–FFFFFh
SA32	100000xxx	64/32	200000h–20FFFFh	F9000h–107FFFh
SA33	100001xxx	64/32	210000h–21FFFFh	108000h–10FFFFh
SA34	100010xxx	64/32	220000h–22FFFFh	110000h–117FFFh
SA35	101011xxx	64/32	230000h–23FFFFh	118000h–11FFFFh
SA36	100100xxx	64/32	240000h–24FFFFh	120000h–127FFFh
SA37	100101xxx	64/32	250000h–25FFFFh	128000h–12FFFFh
SA38	100110xxx	64/32	260000h–26FFFFh	130000h–137FFFh
SA39	100111xxx	64/32	270000h–27FFFFh	138000h–13FFFFh
SA40	101000xxx	64/32	280000h–28FFFFh	140000h–147FFFh
SA41	101001xxx	64/32	290000h–29FFFFh	148000h–14FFFFh
SA42	101010xxx	64/32	2A0000h–2AFFFFh	150000h–157FFFh
SA43	101011xxx	64/32	2B0000h–2BFFFFh	158000h–15FFFFh
SA44	101100xxx	64/32	2C0000h–2CFFFFh	160000h–167FFFh
SA45	101101xxx	64/32	2D0000h–2DFFFFh	168000h–16FFFFh
SA46	101110xxx	64/32	2E0000h–2EFFFFh	170000h–177FFFh
SA47	101111xxx	64/32	2F0000h–2FFFFFh	178000h–17FFFFh
SA48	110000xxx	64/32	300000h–30FFFFh	180000h–187FFFh
SA49	110001xxx	64/32	310000h–31FFFFh	188000h–18FFFFh
SA50	110010xxx	64/32	320000h–32FFFFh	190000h–197FFFh
SA51	110011xxx	64/32	330000h–33FFFFh	198000h–19FFFFh
SA52	100100xxx	64/32	340000h–34FFFFh	1A0000h–1A7FFFh

Table 5. Am29LV320M Top Boot Sector Architecture

Sector	Sector Address A20–A12	Sector Size (Kbytes/Kwords)	(x8) Address Range	(x16) Address Range
SA53	110101xxx	64/32	350000h–35FFFFh	1A8000h–1AFFFFh
SA54	110110xxx	64/32	360000h–36FFFFh	1B0000h–1B7FFFh
SA55	110111xxx	64/32	370000h–37FFFFh	1B8000h–1BFFFFh
SA56	111000xxx	64/32	380000h–38FFFFh	1C0000h–1C7FFFh
SA57	111001xxx	64/32	390000h–39FFFFh	1C8000h–1CFFFFh
SA58	111010xxx	64/32	3A0000h–3AFFFFh	1D0000h–1D7FFFh
SA59	111011xxx	64/32	3B0000h–3BFFFFh	1D8000h–1DFFFFh
SA60	111100xxx	64/32	3C0000h–3CFFFFh	1E0000h–1E7FFFh
SA61	111101xxx	64/32	3D0000h–3DFFFFh	1E8000h–1EFFFFh
SA62	111110xxx	64/32	3E0000h–3EFFFFh	1F0000h–1F7FFFh
SA63	111111000	8/4	3F0000h–3F1FFFh	1F8000h–1F8FFFh
SA64	111111001	8/4	3F2000h–3F3FFFh	1F9000h–1F9FFFh
SA65	111111010	8/4	3F4000h–3F5FFFh	1FA000h–1FAFFFh
SA66	111111011	8/4	3F6000h–3F7FFFh	1FB000h–1FBFFFh
SA67	111111100	8/4	3F8000h–3F9FFFh	1FC000h–1FCFFFh
SA68	111111101	8/4	3FA000h–3FBFFFh	1FD000h–1FDFFFh
SA69	111111110	8/4	3FC000h–3FDFFFh	1FE000h–1FEFFFh
SA70	111111111	8/4	3FE000h–3FFFFFh	1FF000h–1FFFFFh

Sector Group Protection and Unprotection

The hardware sector group protection feature disables both program and erase operations in any sector group. In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Tables 4 and 6). The hardware sector group unprotection feature re-enables both program and erase operations in previously protected sector groups. Sector group protection/unprotection can be implemented via two methods.

Sector protection/unprotection requires V_{ID} on the RESET# pin only, and can be implemented either in-system or via programming equipment. Figure 2 shows the algorithms and Figure 24 shows the timing diagram. This method uses standard microprocessor bus cycle timing. For sector group unprotect, all unprotected sector groups must first be protected prior to the first sector group unprotect write cycle.

The device is shipped with all sector groups unprotected. AMD offers the option of programming and protecting sector groups at its factory prior to shipping the device through AMD's ExpressFlash™ Service. Contact an AMD representative for details.

It is possible to determine whether a sector group is protected or unprotected. See the Autoselect Mode section for details.

Table 6. Am29LV320MT Top Boot Sector Protection

Sector	A20–A12	Sector/ Sector Block Size
SA0-SA3	0000XXXXXh	256 (4x64) Kbytes
SA4-SA7	0001XXXXXh	256 (4x64) Kbytes
SA8-SA11	0010XXXXXh	256 (4x64) Kbytes
SA12-SA15	0011XXXXXh	256 (4x64) Kbytes
SA16-SA19	0100XXXXXh	256 (4x64) Kbytes
SA20-SA23	0101XXXXXh	256 (4x64) Kbytes
SA24-SA27	0110XXXXXh	256 (4x64) Kbytes
SA28-SA31	0111XXXXXh	256 (4x64) Kbytes
SA32–SA35	1000XXXXXh,	256 (4x64) Kbytes
SA36–SA39	1001XXXXXh	256 (4x64) Kbytes
SA40–SA43	1010XXXXXh	256 (4x64) Kbytes
SA44–SA47	1011XXXXXh	256 (4x64) Kbytes
SA48–SA51	1100XXXXXh	256 (4x64) Kbytes
SA52-SA55	1101XXXXXh	256 (4x64) Kbytes
SA56-SA59	1110XXXXXh	256 (4x64) Kbytes
SA60-SA62	111100XXXh 111101XXXh 111110XXXh	192 (3x64) Kbytes
SA63	111111000h	8 Kbytes
SA64	111111001h	8 Kbytes
SA65	111111010h	8 Kbytes
SA66	111111011h	8 Kbytes
SA67	111111100h	8 Kbytes
SA68	111111101h	8 Kbytes
SA69	111111110h	8 Kbytes
SA70	111111111h	8 Kbytes

Table 7. Am29LV320MB Bottom Boot Sector Protection

Sector	A20–A12	Sector/ Sector Block Size
SA0	000000000h	8 Kbytes
SA1	000000001h	8 Kbytes
SA2	000000010h	8 Kbytes
SA3	000000011h	8 Kbytes
SA4	000000100h	8 Kbytes
SA5	000000101h	8 Kbytes
SA6	000000110h	8 Kbytes
SA7	000000111h	8 Kbytes
SA8–SA10	000001XXXh, 000010XXXh, 000011XXXh,	192 (3x64) Kbytes
SA11–SA14	0001XXXXXh	256 (4x64) Kbytes
SA15–SA18	0010XXXXXh	256 (4x64) Kbytes
SA19–SA22	0011XXXXXh	256 (4x64) Kbytes
SA23–SA26	0100XXXXXh	256 (4x64) Kbytes
SA27-SA30	0101XXXXXh	256 (4x64) Kbytes
SA31-SA34	0110XXXXXh	256 (4x64) Kbytes
SA35-SA38	0111XXXXXh	256 (4x64) Kbytes
SA39-SA42	1000XXXXXh	256 (4x64) Kbytes
SA43-SA46	1001XXXXXh	256 (4x64) Kbytes
SA47-SA50	1010XXXXXh	256 (4x64) Kbytes
SA51-SA54	1011XXXXXh	256 (4x64) Kbytes
SA55–SA58	1100XXXXXh	256 (4x64) Kbytes
SA59–SA62	1101XXXXXh	256 (4x64) Kbytes
SA63–SA66	1110XXXXXh	256 (4x64) Kbytes
SA67–SA70	1111XXXXXh	256 (4x64) Kbytes

Write Protect (WP#)

The Write Protect function provides a hardware method of protecting the top two or bottom two sectors without using V_{ID}. WP# is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected using the method described in "Sector Group Protection and Unprotection". Note that if WP#/ACC is at V_{IL} when the device is in

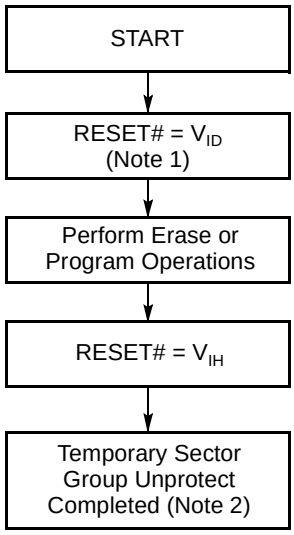
the standby mode, the maximum input load current is increased. See the table in “DC Characteristics”.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the top or bottom two sectors were previously set to be protected or unprotected using the method described in “Sector Group Protection and Unprotection”. *Note: No external pullup is necessary since the WP#/ACC pin has internal pullup to V_{CC}*

Temporary Sector Group Unprotect

*(**Note:** In this device, a sector group consists of four adjacent sectors that are protected or unprotected at the same time (see Table 6).*

This feature allows temporary unprotection of previously protected sector groups to change data in-system. The Sector Group Unprotect mode is activated by setting the RESET# pin to VID. During this mode, formerly protected sector groups can be programmed or erased by selecting the sector group addresses. Once V_{ID} is removed from the RESET# pin, all the previously protected sector groups are protected again. Figure 1 shows the algorithm, and Figure 23 shows the timing diagrams, for this feature.



Notes:

1. *All protected sector groups unprotected (If WP# = V_{IL}, the first or last sector will remain protected).*
2. *All previously protected sector groups are protected once again.*

Figure 1. Temporary Sector Group Unprotect Operation

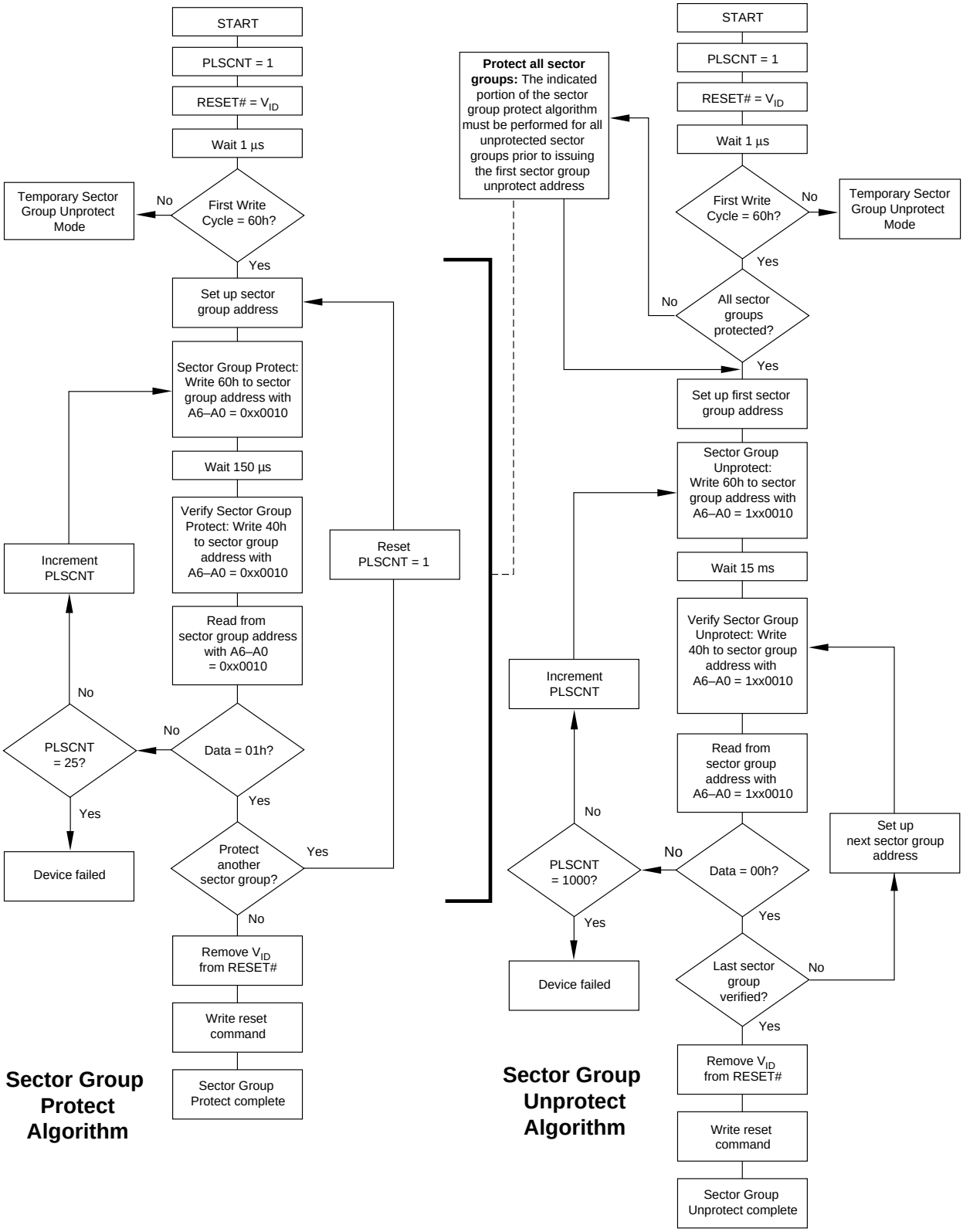


Figure 2. In-System Sector Group Protect/Unprotect Algorithms

SecSi (Secured Silicon) Sector Flash Memory Region

The SecSi (Secured Silicon) Sector feature provides a Flash memory region that enables permanent part identification through an Electronic Serial Number (ESN). The SecSi Sector is 128 words in length, and uses a SecSi Sector Indicator Bit (DQ7) to indicate whether or not the SecSi Sector is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

AMD offers the device with the SecSi Sector either factory locked or customer lockable. The factory-locked version is always protected when shipped from the factory, and has the SecSi (Secured Silicon) Sector Indicator Bit permanently set to a "1." The customer-lockable version is shipped with the SecSi Sector unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the SecSi Sector Indicator Bit permanently set to a "0." Thus, the SecSi Sector Indicator Bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The SecSi sector address space in this device is allocated as follows:

Table 8. SecSi Sector Contents

SecSi Sector Address Range x16	Standard Factory Locked	ExpressFlash Factory Locked	Customer Lockable
000000h–000007h	ESN	ESN or determined by customer	Determined by customer
000008h–00007Fh	Unavailable	Determined by customer	

The system accesses the SecSi Sector through a command sequence (see "Enter SecSi Sector/Exit SecSi Sector Command Sequence"). After the system has written the Enter SecSi Sector command sequence, it may read the SecSi Sector by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit SecSi Sector command sequence, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

Factory Locked: SecSi Sector Programmed and Protected At the Factory

In devices with an ESN, the SecSi Sector is protected when the device is shipped from the factory. The SecSi Sector cannot be modified in any way. See Table 5 for SecSi Sector addressing.

Customers may opt to have their code programmed by AMD through the AMD ExpressFlash service. The devices are then shipped from AMD's factory with the SecSi Sector permanently locked. Contact an AMD representative for details on using AMD's ExpressFlash service.

Customer Lockable: SecSi Sector NOT Programmed or Protected At the Factory

As an alternative to the factory-locked version, the device may be ordered such that the customer may program and protect the 128-word/256-bytes SecSi sector.

The system may program the SecSi Sector using the write-buffer, accelerated and/or unlock bypass methods, in addition to the standard programming command sequence. See Command Definitions.

Programming and protecting the SecSi Sector must be used with caution since, once protected, there is no procedure available for unprotecting the SecSi Sector area and none of the bits in the SecSi Sector memory space can be modified in any way.

The SecSi Sector area can be protected using one of the following procedures:

- Write the three-cycle Enter SecSi Sector Region command sequence, and then follow the in-system sector protect algorithm as shown in Figure 2, except that *RESET# may be at either* V_{IH} *or* V_{ID}. This allows in-system protection of the SecSi Sector without raising any device pin to a high voltage. Note that this method is only applicable to the SecSi Sector.
- To verify the protect/unprotect status of the SecSi Sector, follow the algorithm shown in Figure 3.

Once the SecSi Sector is programmed, locked and verified, the system must write the Exit SecSi Sector Region command sequence to return to reading and writing within the remainder of the array.

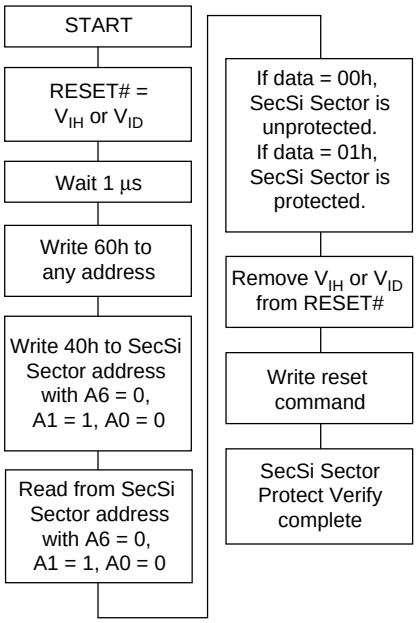


Figure 3. SecSi Sector Protect Verify

Hardware Data Protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to Tables 10 and 13 for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

Low V_{CC} Write Inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program/erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

Write Pulse “Glitch” Protection

Noise pulses of less than 5 ns (typical) on OE#, CE#f or WE# do not initiate a write cycle.

Logical Inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

Power-Up Write Inhibit

If WE# = CE#f = V_{IL} and OE# = V_{IH} during power up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

COMMON FLASH MEMORY INTERFACE (CFI)

The Common Flash Interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI Query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in Tables 6–9. To terminate reading CFI data, the system must write the reset command.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in Tables 6–9. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100, available via the World Wide Web at http://www.amd.com/flash/cfi. Alternatively, contact an AMD representative for copies of these documents.

Table 9. CFI Query Identification String

Addresses (x16)	Addresses (x8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query Unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM Command Set
15h 16h	2Ah 2Ch	0040h 0000h	Address for Primary Extended Table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM Command Set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for Alternate OEM Extended Table (00h = none exists)

Table 10. System Interface String

Addresses (x16)	Addresses (x8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write/erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0007h	Typical timeout per single word write 2^N µs
20h	40h	0007h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	000Ah	Typical timeout per individual block erase 2^N ms
22h	44h	0000h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0001h	Max. timeout for word write 2^N times typical
24h	48h	0005h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0004h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Table 11. Device Geometry Definition

Addresses (x16)	Addresses (x8)	Data	Description
27h	4Eh	0016h	Device Size = 2^N byte
28h 29h	50h 52h	0002h 0000h	Flash Device Interface description (refer to CFI publication 100)
2Ah 2Bh	54h 56h	0005h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	0002h	Number of Erase Block Regions within device (01h = uniform device, 02h = boot device)
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	007Fh 0000h 0020h 0000h	Erase Block Region 1 Information (refer to the CFI specification or CFI publication 100)
31h 32h 33h 34h	62h 64h 66h 68h	003Eh 0000h 0000h 0001h	Erase Block Region 2 Information (refer to CFI publication 100)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase Block Region 3 Information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase Block Region 4 Information (refer to CFI publication 100)

Table 12. Primary Vendor-Specific Extended Query

Addresses (x16)	Addresses (x8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0008h	Address Sensitive Unlock (Bits 1-0) 0 = Required, 1 = Not Required Process Technology (Bits 7-2) 0010b = 0.23 µm MirrorBit
46h	8Ch	0002h	Erase Suspend 0 = Not Supported, 1 = To Read Only, 2 = To Read & Write
47h	8Eh	0001h	Sector Protect 0 = Not Supported, X = Number of sectors in per group
48h	90h	0001h	Sector Temporary Unprotect 00 = Not Supported, 01 = Supported
49h	92h	0004h	Sector Protect/Unprotect scheme 04 = 29LV800 mode
4Ah	94h	0000h	Simultaneous Operation 00 = Not Supported, X = Number of Sectors in Bank
4Bh	96h	0000h	Burst Mode Type 00 = Not Supported, 01 = Supported
4Ch	98h	0001h	Page Mode Type 00 = Not Supported, 01 = 4 Word Page, 02 = 8 Word Page
4Dh	9Ah	00B5h	ACC (Acceleration) Supply Minimum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) Supply Maximum 00h = Not Supported, D7-D4: Volt, D3-D0: 100 mV
4Fh	9Eh	0003h	Top/Bottom Boot Sector Flag 00h = Uniform Device without WP# protect, 02h = Bottom Boot Device, 03h = Top Boot Device, 04h = Uniform sectors bottom WP# protect, 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not Supported, 01h = Supported

COMMAND DEFINITIONS

Writing specific address and data commands or sequences into the command register initiates device operations. Tables 10 and 13 define the valid register command sequences. Writing **incorrect address and data values** or writing them in the **improper sequence** may place the device in an unknown state. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#f, whichever happens later. All data is latched on the rising edge of WE# or CE#f, whichever happens first. Refer to the AC Characteristics section for timing diagrams.

Reading Array Data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after

which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See the Erase Suspend/Erase Resume Commands section for more information.

The system *must* issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See the next section, Reset Command, for more information.

See also Requirements for Reading Array Data in the Device Bus Operations section for more information. The Flash Read-Only Operations table provides the read parameters, and Figure 14 shows the timing diagram.

Reset Command

Writing the reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

Autoselect Command Sequence

The autoselect command sequence allows the host system to read several identifier codes at specific addresses:

Identifier Code	A7:A0 (x16)	A6:A-1 (x8)
Manufacturer ID	00h	00h
Device ID, Cycle 1	01h	02h
Device ID, Cycle 2	0Eh	1Ch
Device ID, Cycle 3	0Fh	1Eh
SecSi Sector Factory Protect	03h	06h
Sector Protect Verify	(SA)02h	(SA)04h

Note: *The device ID is read over three cycles. SA = Sector Address.*

Tables 10 and 13 show the address and data requirements. This method is an alternative to that shown in Table 3, which is intended for PROM programmers and requires V_{ID} on address pin A9. The autoselect command sequence may be written to an address that is either in the read or erase-suspend-read mode. The autoselect command may not be written while the device is actively programming or erasing.

The autoselect command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle that contains the autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another autoselect command sequence.

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

Enter SecSi Sector/Exit SecSi Sector Command Sequence

The SecSi Sector region provides a secured data area containing an 8-word/16-byte random Electronic Serial Number (ESN). The system can access the SecSi Sector region by issuing the three-cycle Enter SecSi Sector command sequence. The device continues to access the SecSi Sector region until the system issues the four-cycle Exit SecSi Sector command sequence. The Exit SecSi Sector command sequence returns the device to normal operation. Tables 10 and 13 show the address and data requirements for both command sequences. See also "SecSi (Secured Silicon) Sector Flash Memory Region" for further information. *Note that the ACC function and unlock bypass modes are not available when the SecSi Sector is enabled.*

Word Program Command Sequence

Programming is a four-bus-cycle operation. The program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written

next, which in turn initiate the Embedded Program algorithm. The system is *not* required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. Tables 10 and 13 show the address and data requirements for the word program command sequence.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to the Write Operation Status section for information on these status bits.

Any commands written to the device during the Embedded Program Algorithm are ignored. Note that a **hardware reset** immediately terminates the program operation. The program command sequence should be reinitiated once the device has returned to the read mode, to ensure data integrity. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

Programming is allowed in any sequence and across sector boundaries. **A bit cannot be programmed from "0" back to a "1."** Attempting to do so may cause the device to set DQ5 = 1, or cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read will show that the data is still "0." Only erase operations can convert a "0" to a "1."

Unlock Bypass Command Sequence

The unlock bypass feature allows the system to program words to the device faster than using the standard program command sequence. The unlock bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the unlock bypass command, 20h. The device then enters the unlock bypass mode. A two-cycle unlock bypass program command sequence is all that is required to program in this mode. The first cycle in this sequence contains the unlock bypass program command, A0h; the second cycle contains the program address and data. Additional data is programmed in the same manner. This mode dispenses with the initial two unlock cycles required in the standard program command sequence, resulting in faster total programming time. Tables 10 and 13 show the requirements for the command sequence.

During the unlock bypass mode, only the Unlock Bypass Program and Unlock Bypass Reset commands are valid. To exit the unlock bypass mode, the system must issue the two-cycle unlock bypass reset command sequence. The first cycle must contain the data 90h. The second cycle must contain the data 00h. The device then returns to the read mode.

Write Buffer Programming

Write Buffer Programming allows the system write to a maximum of 16 words in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the Sector Address in which programming will occur. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system will program 6 unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses will be loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation will abort.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_4. All subsequent address/data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address/data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address/data pairs loaded into the write buffer. This means Write Buffer Programming cannot be performed across multiple write-buffer pages. This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation will abort.

Note that if a Write Buffer address location is loaded multiple times, the address/data pair counter will be decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address will be programmed.

Once the specified number of write buffer locations have been loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The write-buffer programming operation can be suspended using the standard program suspend/resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming Sequence can be aborted in the following ways:

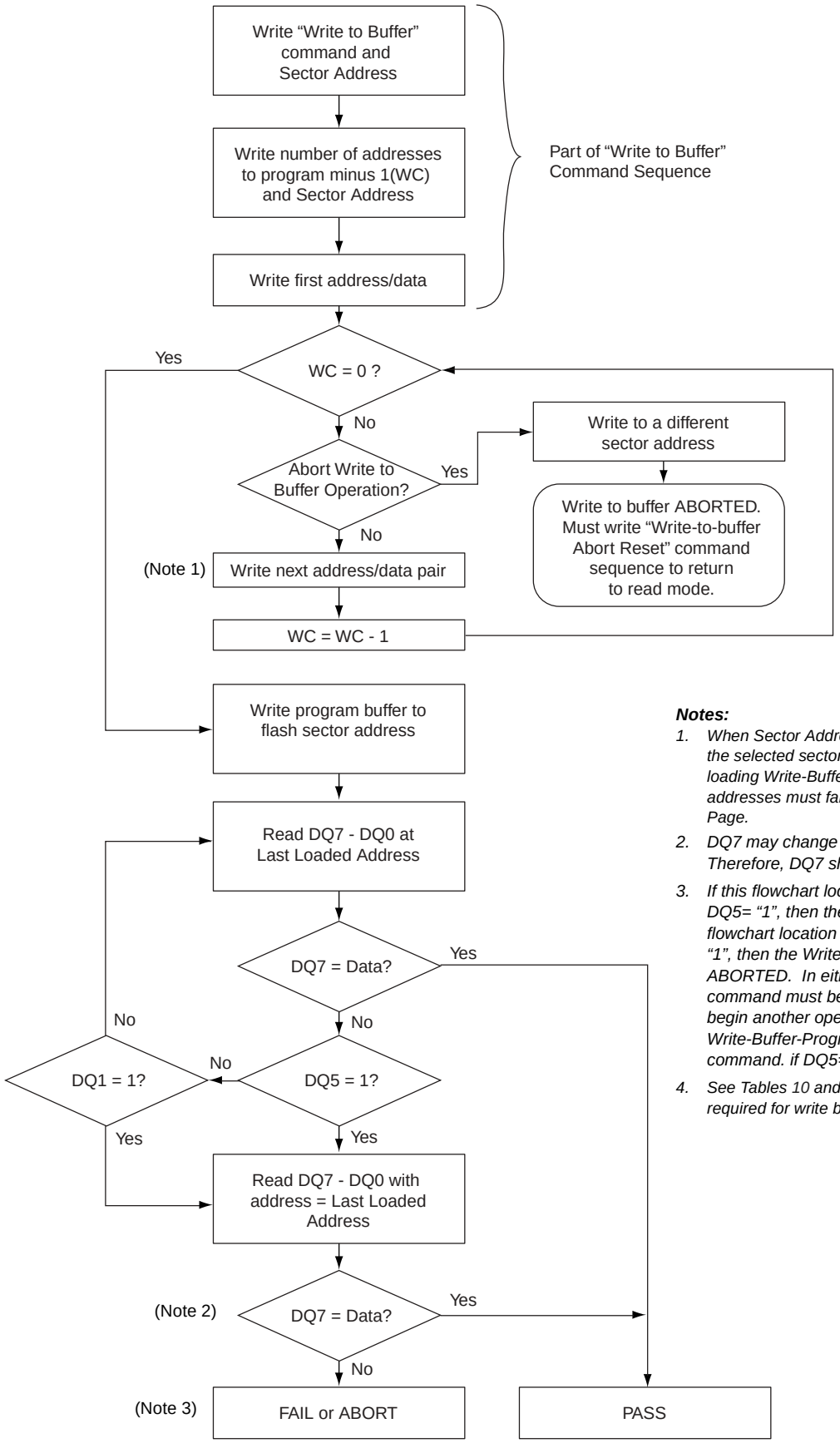
- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address/Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5=0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation. Note that the full 3-cycle Write-to-Buffer-Abort Reset command sequence is required when using Write-Buffer-Programming features in Unlock Bypass mode.

Accelerated Program

The device offers accelerated program operations through the WP#/ACC pin. When the system asserts V_{HH} on the WP#/ACC pin, the device automatically enters the Unlock Bypass mode. The system may then write the two-cycle Unlock Bypass program command sequence. The device uses the higher voltage on the WP#/ACC pin to accelerate the operation. *Note that the* WP#/*ACC pin must not be at* V_{HH} *for operations other than accelerated programming, or device damage may result. In addition, no external pullup is necessary since the WP#/ACC pin has internal pullup to* V_{CC}.

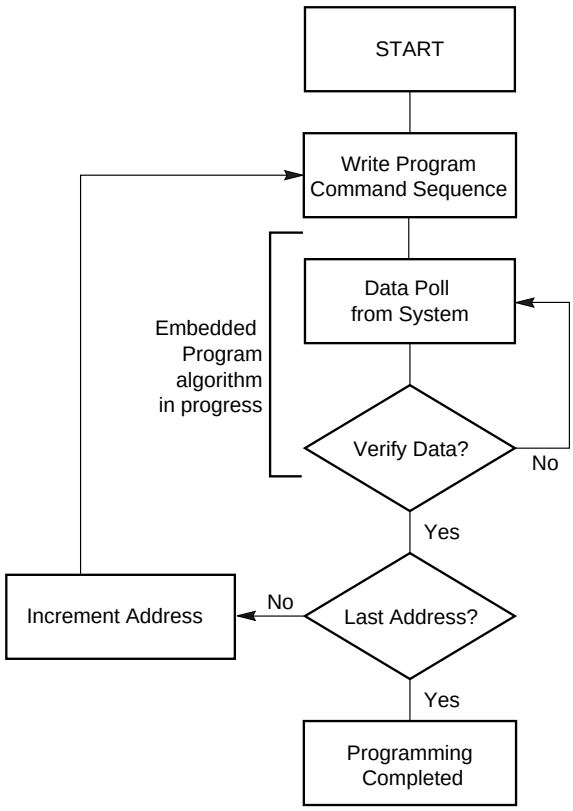
Figure 5 illustrates the algorithm for the program operation. Refer to the Flash Erase and Program Operations table in the AC Characteristics section for parameters, and Figure 17 for timing diagrams.



Notes:

1. *When Sector Address is specified, any address in the selected sector is acceptable. However, when loading Write-Buffer address locations with data, all addresses must fall within the selected Write-Buffer Page.*
2. *DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.*
3. *If this flowchart location was reached because DQ5= "1", then the device FAILED. If this flowchart location was reached because DQ1= "1", then the Write to Buffer operation was ABORTED. In either case, the proper reset command must be written before the device can begin another operation. If DQ1=1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5=1, write the Reset command.*
4. *See Tables 10 and 13 for command sequences required for write buffer programming.*

Figure 4. Write Buffer Programming Operation



Note: *See Tables 10 and 13 for program command sequence.*

Figure 5. Program Operation

Program Suspend/Program Resume Command Sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within 15 µs maximum (5 µs typical) and updates the status bits. Addresses are not required when writing the Program Suspend command.

After the programming operation has been suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the SecSi Sector area (One-time Program area), then user must use the proper command sequences to enter and exit this region.

The system may also write the autoselect command sequence when the device is in the Program Suspend mode. The system can read as many autoselect codes as required. When the device exits the autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See Autoselect Command Sequence for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See Write Operation Status for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device has resume programming.

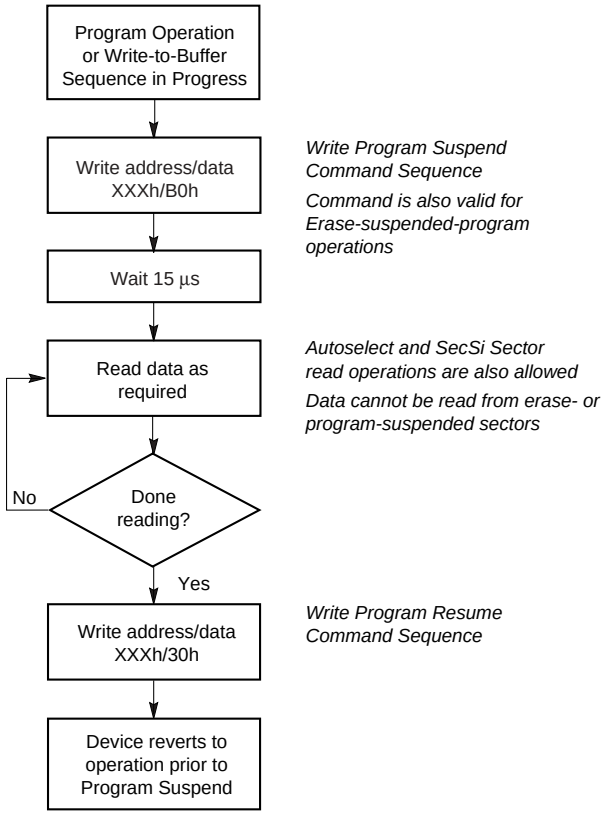


Figure 6. Program Suspend/Program Resume

Chip Erase Command Sequence

Chip erase is a six bus cycle operation. The chip erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the chip erase command, which in turn invokes the Embedded Erase algorithm. The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. Tables 10 and 13 shows the address and data requirements for the chip erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to the Write Operation Status section for information on these status bits.

Any commands written during the chip erase operation are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the chip erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 7 illustrates the algorithm for the erase operation. Refer to the Flash Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.

Sector Erase Command Sequence

Sector erase is a six bus cycle operation. The sector erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the sector erase command. Tables 10 and 13 shows the address and data requirements for the sector erase command sequence. *Note that the SecSi Sector, autoselect, and CFI functions are unavailable when a program operation is in progress.*

The device does *not* require the system to preprogram prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of 50 µs occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. **Any command other than Sector Erase or Erase Suspend during the time-out period resets the device to the read mode.** The system must rewrite the command sequence and any additional addresses and commands.

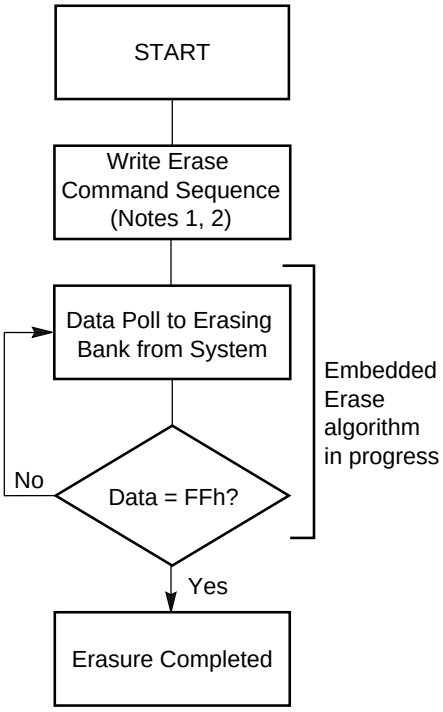
The system can monitor DQ3 to determine if the sector erase timer has timed out (See the section on DQ3:

Sector Erase Timer.). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to the Write Operation Status section for information on these status bits.

Once the sector erase operation has begun, only the Erase Suspend command is valid. All other commands are ignored. However, note that a **hardware reset** immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device has returned to reading array data, to ensure data integrity.

Figure 7 illustrates the algorithm for the erase operation. Refer to the Flash Erase and Program Operations tables in the AC Characteristics section for parameters, and Figure 19 section for timing diagrams.



Notes:

1. *See Tables 10 and 13 for erase command sequence.*
2. *See the section on DQ3 for information on the sector erase timer.*

Figure 7. Erase Operation

Erase Suspend/Erase Resume Commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the 50 µs time-out period during the sector erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires a typical of 5 µs (maximum of 20 µs) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation has been suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device “erase suspends” all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to the Write Operation Status section for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to the Write Operation Status section for more information.

In the erase-suspend-read mode, the system can also issue the autoselect command sequence. Refer to the Autoselect Mode and Autoselect Command Sequence sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. The address of the erase-suspended sector is required when writing this command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip has resumed erasing.

Command Definitions

Table 13. Command Definitions (Flash, x16 mode, CIOf = V_{IH})

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001				
	Device ID (Note 8)	6	555	AA	2AA	55	555	90	X01	227E	X0E	221A	X0F	2201
	SecSi™ Sector Factory Protect (Note 9)	4	555	AA	2AA	55	555	90	X03	(Note 9)				
	Sector Group Protect Verify (Note 10)	4	555	AA	2AA	55	555	90	(SA)X02	00/01				
Enter SecSi Sector Region		3	555	AA	2AA	55	555	88						
Exit SecSi Sector Region		4	555	AA	2AA	55	555	90	XXX	00				
Program		4	555	AA	2AA	55	555	A0	PA	PD				
Write to Buffer (Note 11)		6	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 12)		3	555	AA	2AA	55	555	F0						
Unlock Bypass		3	555	AA	2AA	55	555	20						
Unlock Bypass Program (Note 13)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)		2	XXX	90	XXX	00								
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30
Program/Erase Suspend (Note 15)		1	BA	B0										
Program/Erase Resume (Note 16)		1	BA	30										
CFI Query (Note 17)		1	55	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address . Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A20–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

WC = Word Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *During unlock cycles, when lower address bits are 555 or 2AAh as shown in table, address bits higher than A11 (except where BA, PA, or SA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*
7. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care except for RD, PD, and WC. See the Autoselect Command Sequence section for more information.*
8. *The device ID must be read in three cycles. The data is 2201h for top boot.*
9. *WP# protects the top two address sectors, the data is 98h for factory locked and 18h for not factory locked.*
10. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 21.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

Table 14. Command Definitions (Flash x8 Mode, CIOf = V_{IL})

Command Sequence (Notes)		Cycles	Bus Cycles (Notes 1–4)											
			First		Second		Third		Fourth		Fifth		Sixth	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read (Note 5)		1	RA	RD										
Reset (Note 6)		1	XXX	F0										
Autoselect (Note 7)	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01				
	Device ID (Note 8)	6	AAA	AA	555	55	AAA	90	X02	7E	X1C	1A	X1E	00/01
	SecSi™ Sector Factory Protect (Note 9)	4	AAA	AA	555	55	AAA	90	X06	(Note 9)				
	Sector Group Protect Verify (Note 10)	4	AAA	AA	555	55	AAA	90	(SA)X04	00/01				
Enter SecSi Sector Region		3	AAA	AA	555	55	AAA	88						
Exit SecSi Sector Region		4	AAA	AA	555	55	AAA	90	XXX	00				
Program		4	AAA	AA	555	55	AAA	A0	PA	PD				
Write to Buffer (Note 11)		6	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD
Program Buffer to Flash		1	SA	29										
Write to Buffer Abort Reset (Note 12)		3	AAA	AA	555	55	AAA	F0						
Unlock Bypass		3	AAA	AA	555	55	AAA	20						
Unlock Bypass Program (Note 13)		2	XXX	A0	PA	PD								
Unlock Bypass Reset (Note 14)		2	XXX	90	XXX	00								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30
Program/Erase Suspend (Note 15)		1	BA	B0										
Program/Erase Resume (Note 16)		1	BA	30										
CFI Query (Note 17)		1	AA	98										

Legend:

X = Don't care

RA = Read Address of the memory location to be read.

RD = Read Data read from location RA during read operation.

PA = Program Address . Addresses latch on the falling edge of the WE# or CE# pulse, whichever happens later.

PD = Program Data for location PA. Data latches on the rising edge of WE# or CE# pulse, whichever happens first.

SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A20–A15 uniquely select any sector.

WBL = Write Buffer Location. Address must be within the same write buffer page as PA.

BC = Byte Count. Number of write buffer locations to load minus 1.

Notes:

1. *See Table 1 for description of bus operations.*
2. *All values are in hexadecimal.*
3. *Except for the read cycle and the fourth cycle of the autoselect command sequence, all bus cycles are write cycles.*
4. *During unlock cycles, when lower address bits are 555 or AAAh as shown in table, address bits higher than A11 (except where BA is required) and data bits higher than DQ7 are don't cares.*
5. *No unlock or command cycles required when device is in read mode.*
6. *The Reset command is required to return to the read mode (or to the erase-suspend-read mode if previously in Erase Suspend) when the device is in the autoselect mode, or if DQ5 goes high while the device is providing status information.*
7. *The fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See the Autoselect Command Sequence section for more information.*
8. *The device ID must be read in three cycles. The data is 01h for top boot and 00h for bottom boot*
9. *If WP# protects the top two address sectors, the data is 98h for factory locked and 18h for not factory locked. If WP# protects the bottom two address sectors, the data is 88h for factory locked and 08h for not factor locked.*
10. *The data is 00h for an unprotected sector group and 01h for a protected sector group.*
11. *The total number of cycles in the command sequence is determined by the number of words written to the write buffer. The maximum number of cycles in the command sequence is 37.*
12. *Command sequence resets device for next command after aborted write-to-buffer operation.*
13. *The Unlock Bypass command is required prior to the Unlock Bypass Program command.*
14. *The Unlock Bypass Reset command is required to return to the read mode when the device is in the unlock bypass mode.*
15. *The system may read and program in non-erasing sectors, or enter the autoselect mode, when in the Erase Suspend mode. The Erase Suspend command is valid only during a sector erase operation.*
16. *The Erase Resume command is valid only during the Erase Suspend mode.*
17. *Command is valid when device is ready to read array data or when device is in autoselect mode.*

WRITE OPERATION STATUS

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. Table 11 and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or has been completed.

DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

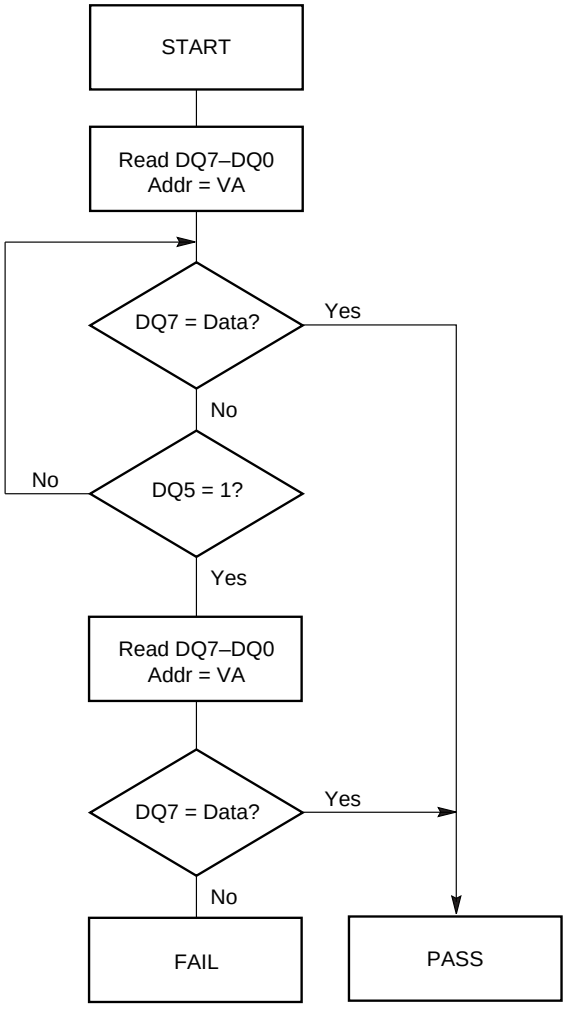
During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately 1 µs, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces a “0” on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces a “1” on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately 100 µs, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted low. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device has completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 will appear on successive read cycles.

Table 11 shows the outputs for Data# Polling on DQ7. Figure 8 shows the Data# Polling algorithm. Figure 20 in the AC Characteristics section shows the Data# Polling timing diagram.



Notes:

1. *VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.*
2. *DQ7 should be rechecked even if DQ5 = “1” because DQ7 may change simultaneously with DQ5.*

Figure 8. Data# Polling Algorithm

RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. Table 11 shows the outputs for RY/BY#.

DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device has entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

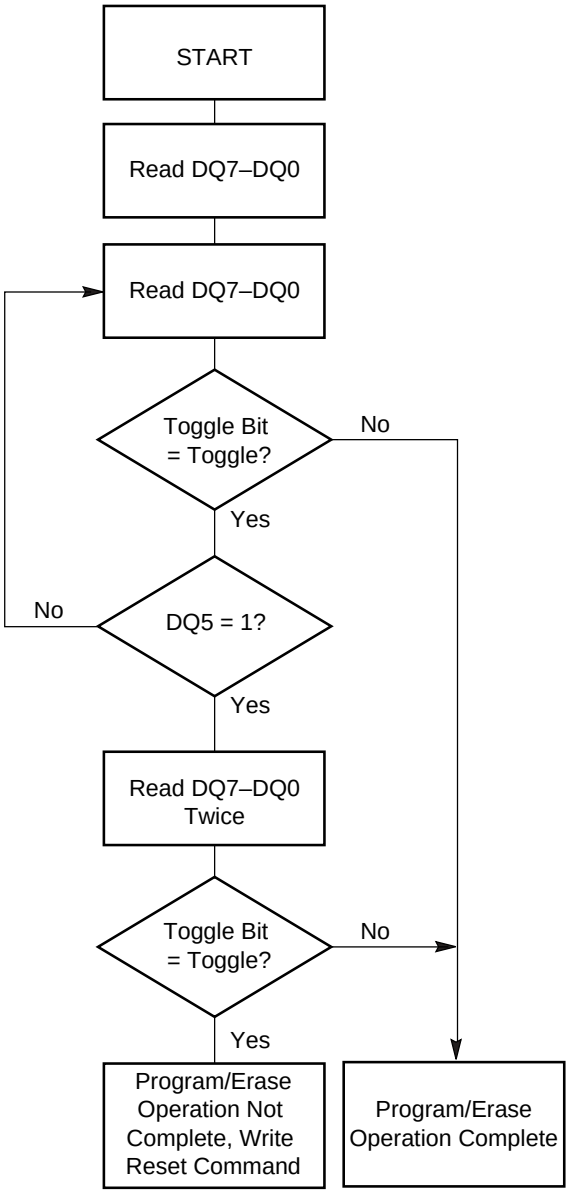
After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately 100 µs, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see the subsection on DQ7: Data# Polling).

If a program address falls within a protected sector, DQ6 toggles for approximately 1 µs after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 11 shows the outputs for Toggle Bit I on DQ6. Figure 9 shows the toggle bit algorithm. Figure 21 in the “AC Characteristics” section shows the toggle bit timing diagrams. Figure 22 shows the differences between DQ2 and DQ6 in graphical form. See also the subsection on DQ2: Toggle Bit II.



Note: *The system should recheck the toggle bit even if DQ5 = "1" because the toggle bit may stop toggling as DQ5 changes to "1." See the subsections on DQ6 and DQ2 for more information.*

Figure 9. Toggle Bit Algorithm

DQ2: Toggle Bit II

The "Toggle Bit II" on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that have been selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to Table 11 to compare outputs for DQ2 and DQ6.

Figure 9 shows the toggle bit algorithm in flowchart form, and the section "DQ2: Toggle Bit II" explains the algorithm. See also the RY/BY#: Ready/Busy# subsection. Figure 21 shows the toggle bit timing diagram. Figure 22 shows the differences between DQ2 and DQ6 in graphical form.

Reading Toggle Bits DQ6/DQ2

Refer to Figure 9 for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device has completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see the section on DQ5). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device has successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform

other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of Figure 9).

DQ5: Exceeded Timing Limits

DQ5 indicates whether the program, erase, or write-to-buffer time has exceeded a specified internal pulse count limit. Under these conditions DQ5 produces a "1," indicating that the program or erase cycle was not successfully completed.

The device may output a "1" on DQ5 if the system tries to program a "1" to a location that was previously programmed to "0." **Only an erase operation can change a "0" back to a "1."** Under this condition, the device halts the operation, and when the timing limit has been exceeded, DQ5 produces a "1."

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode).

DQ3: Sector Erase Timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure has begun. (The sector erase timer does not apply to the chip erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from a "0" to a "1." If the time between additional sector erase commands from the system can be assumed to be less than 50 µs, the system need not monitor DQ3. See also the Sector Erase Command Sequence section.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device has accepted the command sequence, and then read DQ3. If DQ3 is "1," the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is "0," the device will accept additional sector erase commands. To ensure the command has been accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted.

Table 11 shows the status of DQ3 relative to the other status bits.

DQ1: Write-to-Buffer Abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces a "1". The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See Write Buffer

Table 15. Write Operation Status

Status			DQ7 (Note 2)	DQ6	DQ5 (Note 1)	DQ3	DQ2 (Note 2)	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program-Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program)		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy (Note 3)		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort (Note 4)		DQ7#	Toggle	0	N/A	N/A	1	0

Notes:

1. *DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation has exceeded the maximum timing limits. Refer to the section on DQ5 for more information.*
2. *DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.*
3. *The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.*
4. *DQ1 switches to '1' when tthe device has aborted the write-to-buffer operation.*

ABSOLUTE MAXIMUM RATINGS

Storage Temperature
Plastic Packages . . . . . –65°C to +150°C

Ambient Temperature
with Power Applied . . . . . –65°C to +125°C

Voltage with Respect to Ground

V_{CC}f/V_{CC}s (Note 1) . . . . . –0.3 V to +4.0 V

RESET#f (Note 2) . . . . . –0.5 V to +12.5 V

WP#/ACC . . . . . –0.5 V to +10.5 V

All other pins (Note 1) . . . . . –0.5 V to V_{CC} +0.5 V

Output Short Circuit Current (Note 3) . . . . . 200 mA

Notes:

1. *Minimum DC voltage on input or I/O pins is –0.5 V. During voltage transitions, input or I/O pins may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. Maximum DC voltage on input or I/O pins is V_{CC} +0.5 V. See Figure 10. During voltage transitions, input or I/O pins may overshoot to V_{CC} +2.0 V for periods up to 20 ns. See Figure 11.*
2. *Minimum DC input voltage on pins A9, OE#, ACC, and RESET# is –0.5 V. During voltage transitions, A9, OE#, ACC, and RESET# may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See Figure 10. Maximum DC input voltage on pin A9, OE#, ACC, and RESET# is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.*
3. *No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.*

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

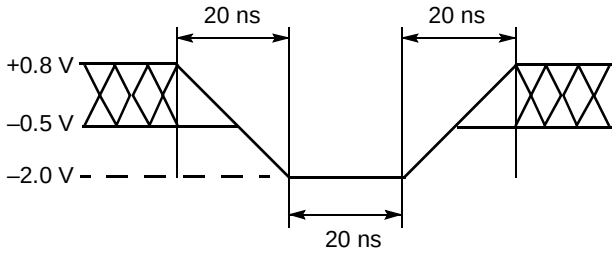


Figure 10. Maximum Negative Overshoot Waveform

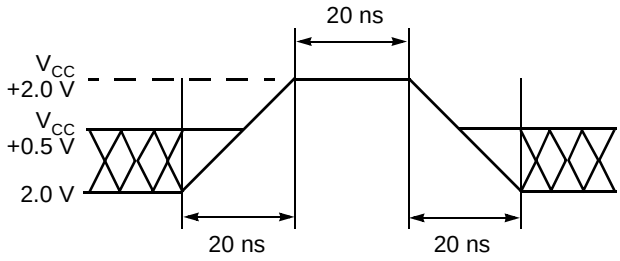


Figure 11. Maximum Positive Overshoot Waveform

OPERATING RANGES

Industrial (I) Devices

Ambient Temperature (T_A) . . . . . –40°C to +85°C

Supply Voltages

V_{CC}f/V_{CC}s for full voltage range . . . . . 2.7–3.3 V

Note: *Operating ranges define those limits between which the functionality of the device is guaranteed.*

DC CHARACTERISTICS

CMOS Compatible

Parameter Symbol	Parameter Description (Notes)	Test Conditions		Min	Typ	Max	Unit
I_{LI}	Input Load Current (1)	$V_{IN} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{LIT}	A9, ACC Input Load Current	$V_{CC} = V_{CC\ max}$; A9 = 12.5 V				35	µA
I_{LR}	Reset Leakage Current	$V_{CC} = V_{CC\ max}$; RESET# = 12.5 V				35	µA
I_{LO}	Output Leakage Current	$V_{OUT} = V_{SS}$ to V_{CC}, $V_{CC} = V_{CC\ max}$				±1.0	µA
I_{CC1}	V_{CC} Active Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH},	5 MHz		15	20	mA
			1 MHz		15	20	
I_{CC2}	V_{CC} Initial Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			30	50	mA
I_{CC3}	V_{CC} Intra-Page Read Current (2, 3)	CE# = V_{IL}, OE# = V_{IH}			10	20	mA
I_{CC4}	V_{CC} Active Write Current (3, 4)	CE# = V_{IL}, OE# = V_{IH}			50	60	mA
I_{CC5}	V_{CC} Standby Current (3)	CE#, RESET# = V_{CC} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC6}	V_{CC} Reset Current (3)	RESET# = V_{SS} ± 0.3 V, WP# = V_{IH}			1	5	µA
I_{CC7}	Automatic Sleep Mode (3, 5)	$V_{IH} = V_{CC}$ ± 0.3 V; $V_{IL} = V_{SS}$ ± 0.3 V, WP# = V_{IH}			1	5	µA
V_{IL}	Input Low Voltage (6)			–0.5		0.8	V
V_{IH}	Input High Voltage (6)			0.7 x V_{CC}		V_{CC} + 0.5	V
V_{ID}	Voltage for Autoselect and Temporary Sector Unprotect	V_{CC} = 2.7 –3.6 V		11.5		12.5	V
V_{OL}	Output Low Voltage	I_{OL} = 4.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$				0.15 x V_{CC}	V
V_{OH1}	Output High Voltage	I_{OH} = –2.0 mA, $V_{CC} = V_{CC\ min} = V_{IO}$		0.85 V_{CC}			V
V_{OH2}		I_{OH} = –100 µA, $V_{CC} = V_{CC\ min} = V_{IO}$		V_{CC}–0.4			V
V_{LKO}	Low V_{CC} Lock-Out Voltage (7)			2.3		2.5	V

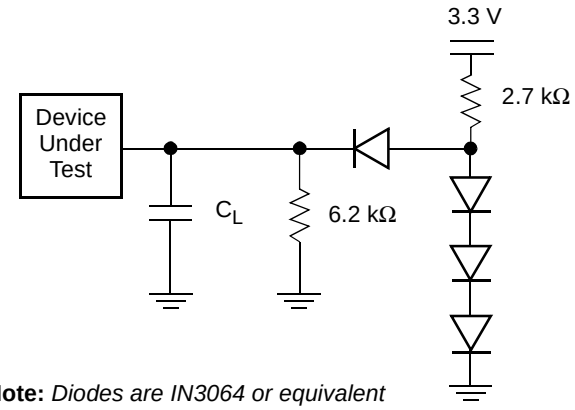
Notes:

1. *On the WP#/ACC pin only, the maximum input load current when WP# = V_{IL} is ± 5.0 µA.*
2. *The I_{CC} current listed is typically less than 2 mA/MHz, with OE# at V_{IH}.*
3. *Maximum I_{CC} specifications are tested with $V_{CC} = V_{CC}$max.*
4. *I_{CC} active while Embedded Erase or Embedded Program is in progress.*
5. *Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns. Typical sleep mode current is 200 nA.*
6. *V_{CC} voltage requirements.*
7. *Not 100% tested.*

SRAM DC AND OPERATING CHARACTERISTICS

Parameter Symbol	Parameter Description	Test Conditions	Min	Typ	Max	Unit
I_{LI}	Input Leakage Current	$V_{IN} = V_{SS}$ to V_{CC}	–1.0		1.0	µA
I_{LO}	Output Leakage Current	CE1#s = V_{IH}, CE2s = V_{IL} or OE# = V_{IH} or WE# = V_{IL}, V_{IO}= V_{SS} to V_{CC}	–1.0		1.0	µA
I_{CC}	Operating Power Supply Current	I_{IO} = 0 mA, CE1#s = V_{IL}, CE2s = WE# = V_{IH}, V_{IN} = V_{IH} or V_{IL}			3	mA
$I_{CC1}s$	Average Operating Current	Cycle time = 1 µs, 100% duty, I_{IO} = 0 mA, CE1#s ≤ 0.2 V, CE2 ≥ V_{CC} – 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} – 0.2 V, CIOs = V_{SS} or V_{CC}			3	mA
$I_{CC2}s$	Average Operating Current	Cycle time = Min., I_{IO} = 0 mA, 100% duty, CE1#s = V_{IL}, CE2s = V_{IH}, V_{IN} = V_{IL} = or V_{IH}, CIOs = V_{SS} or V_{CC}			30	mA
V_{OL}	Output Low Voltage	I_{OL} = 2.1 mA			0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1.0 mA	2.4			V
I_{SB}	Standby Current (TTL)	CE1#s = V_{IH}, CE2 = V_{IL}, Other inputs = V_{IH} or V_{IL}			0.3	mA
I_{SB1}	Standby Current (CMOS)	CE1#s ≥ V_{CC} – 0.2 V, CE2 ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2 ≤ 0.2 V (CE2s controlled) Other input = 0 ~ V_{CC}, CIOs = V_{SS} or V_{CC}			10	µA

TEST CONDITIONS



Note: *Diodes are IN3064 or equivalent*

Figure 12. Test Setup

Table 16. Test Specifications

Test Condition	All Speeds	Unit
Output Load	1 TTL gate	
Output Load Capacitance, C_L (including jig capacitance)	30	pF
Input Rise and Fall Times	5	ns
Input Pulse Levels	0.0–3.0	V
Input timing measurement reference levels	1.5	V
Output timing measurement reference levels	1.5	V

KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't Care, Any Change Permitted	Changing, State Unknown
	Does Not Apply	Center Line is High Impedance State (High Z)

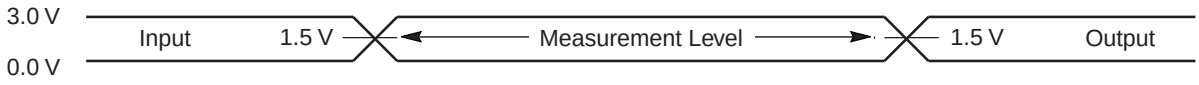


Figure 13. Input Waveforms and Measurement Levels

AC CHARACTERISTICS

Flash Read-Only Operations

Parameter		Description		Test Setup		Speed	Unit
JEDEC	Std.						
t_{AVAV}	t_{RC}	Read Cycle Time (Note 1)			Min	100	ns
t_{AVQV}	t_{ACC}	Address to Output Delay		CE#, OE# = V_{IL}	Max	100	ns
t_{ELQV}	t_{CE}	Chip Enable to Output Delay		OE# = V_{IL}	Max	100	ns
	t_{PACC}	Page Access Time			Max	30	ns
t_{GLQV}	t_{OE}	Output Enable to Output Delay			Max	30	ns
t_{EHQZ}	t_{DF}	Chip Enable to Output High Z (Note 1)			Max	30	ns
t_{GHQZ}	t_{DF}	Output Enable to Output High Z (Note 1)			Max	30	ns
t_{AXQX}	t_{OH}	Output Hold Time From Addresses, CE# or OE#, Whichever Occurs First			Min	0	ns
	t_{OEH}	Output Enable Hold Time (Note 1)	Read		Min	0	ns
			Toggle and Data# Polling		Min	10	ns

Notes:

1. *Not 100% tested.*
2. *See Figure 12 and Table 12 for test specifications.*

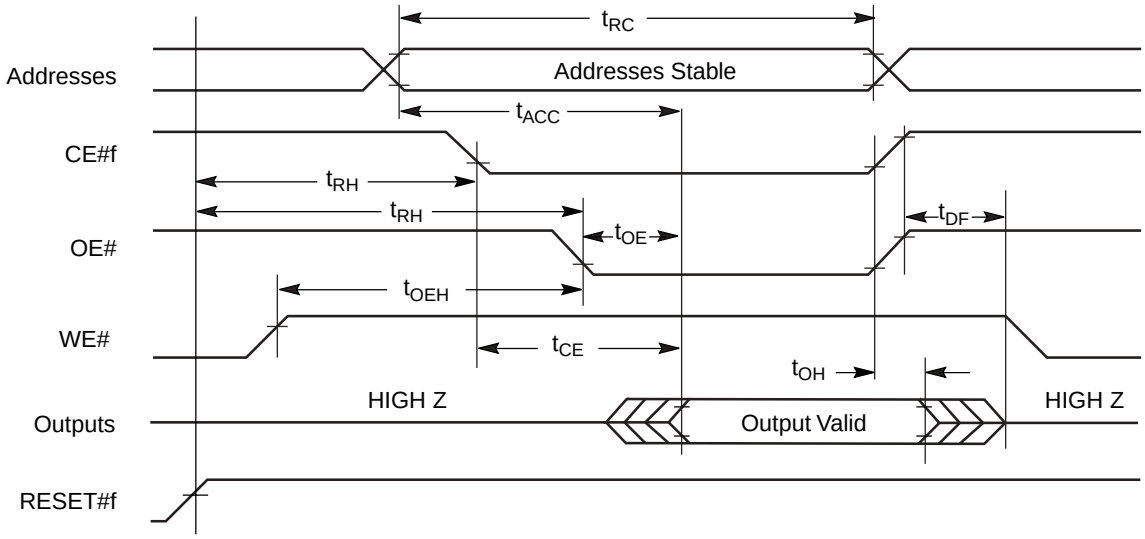


Figure 14. Read Operation Timings

AC CHARACTERISTICS

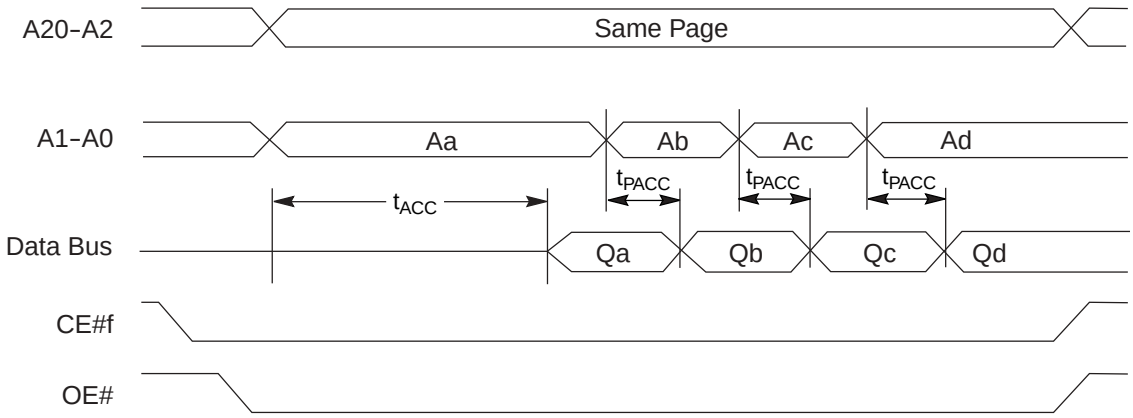


Figure 15. Page Read Timings

AC CHARACTERISTICS

Hardware Reset (RESET#)

Parameter		Description		Speed	Unit
JEDEC	Std.				
	t_{Ready}	RESET# Pin Low (NOT During Embedded Algorithms) to Read Mode (See Note)	Max	500	ns
	t_{RP}	RESET# Pulse Width	Min	500	ns
	t_{RH}	Reset High Time Before Read (See Note)	Min	50	ns
	t_{RPD}	RESET# Low to Standby Mode	Min	20	µs

Note: *Not 100% tested.*

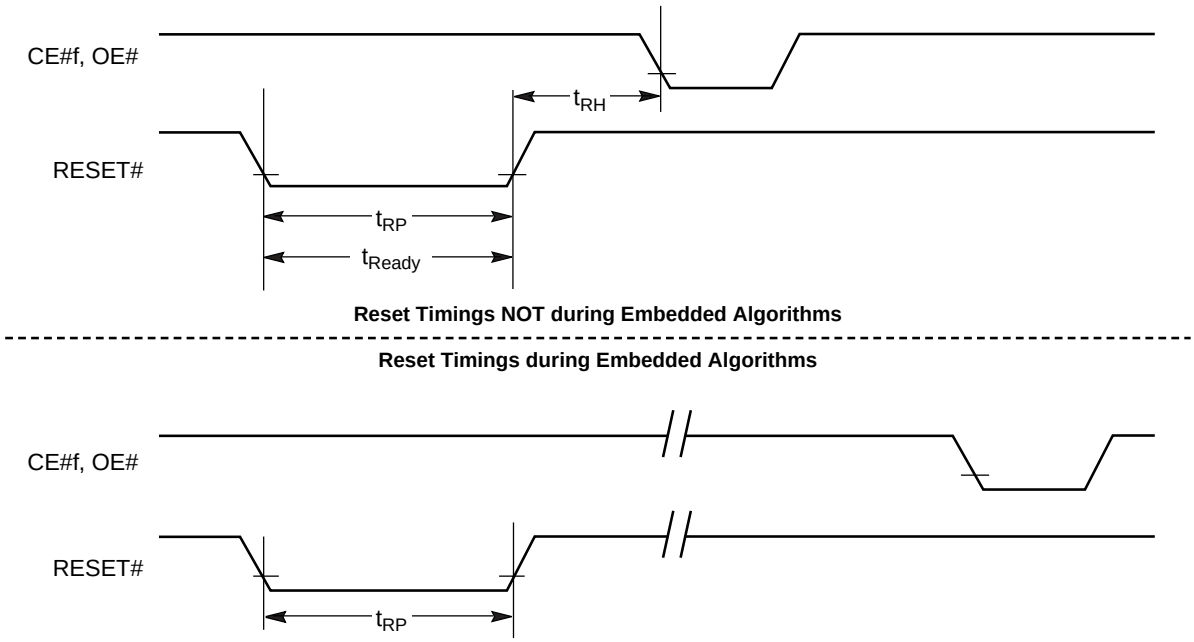


Figure 16. Reset Timings

AC CHARACTERISTICS

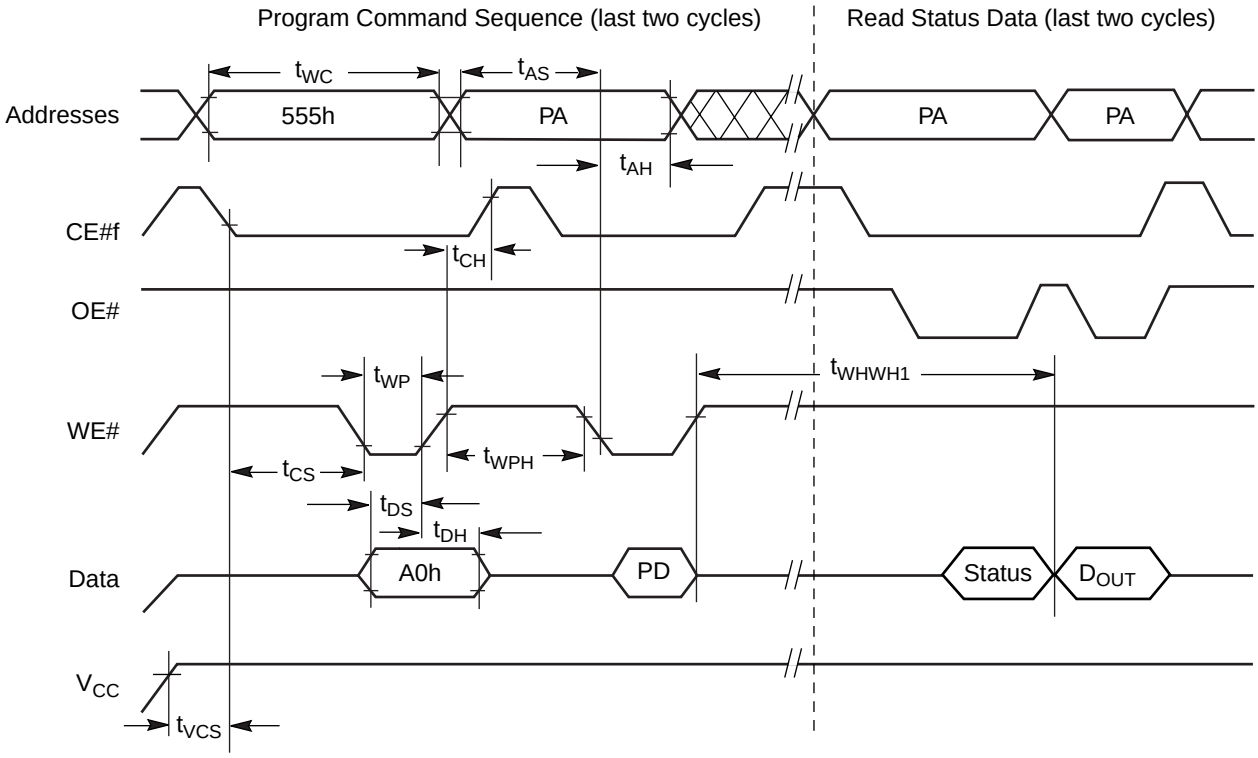
Flash Erase and Program Operations

Parameter		Description			Speed	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
	t_{ASO}	Address Setup Time to OE# low during toggle bit polling		Min	15	ns
t_{WLAX}	t_{AH}	Address Hold Time		Min	45	ns
	t_{AHT}	Address Hold Time From CE# or OE# high during toggle bit polling		Min	0	ns
t_{DVWH}	t_{DS}	Data Setup Time		Min	45	ns
t_{WHDX}	t_{DH}	Data Hold Time		Min	0	ns
	t_{OEPH}	Output Enable High during toggle bit polling		Min	20	ns
t_{GHWL}	t_{GHWL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{ELWL}	t_{CS}	CE# Setup Time		Min	0	ns
t_{WHEH}	t_{CH}	CE# Hold Time		Min	0	ns
t_{WLWH}	t_{WP}	Write Pulse Width		Min	35	ns
t_{WHDL}	t_{WPH}	Write Pulse Width High		Min	30	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240	µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15	µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	11.8	µs
		Single Word Program Operation (Note 2)		Typ	60	µs
		Single Word Accelerated Programming Operation (Note 2)		Typ	54	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5	sec
	t_{VHH}	V_{HH} Rise and Fall Time (Note 1)		Min	250	ns
	t_{VCS}	V_{CC} Setup Time (Note 1)		Min	50	µs

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words programmed.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*

AC CHARACTERISTICS



Notes:

1. *PA = program address, PD = program data, D_{OUT} is the true data at the program address.*
2. *Illustration shows device in word mode.*

Figure 17. Program Operation Timings

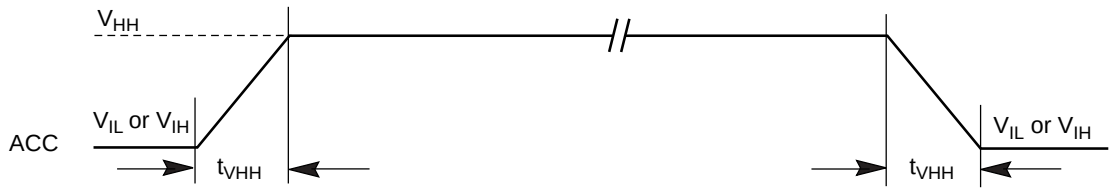
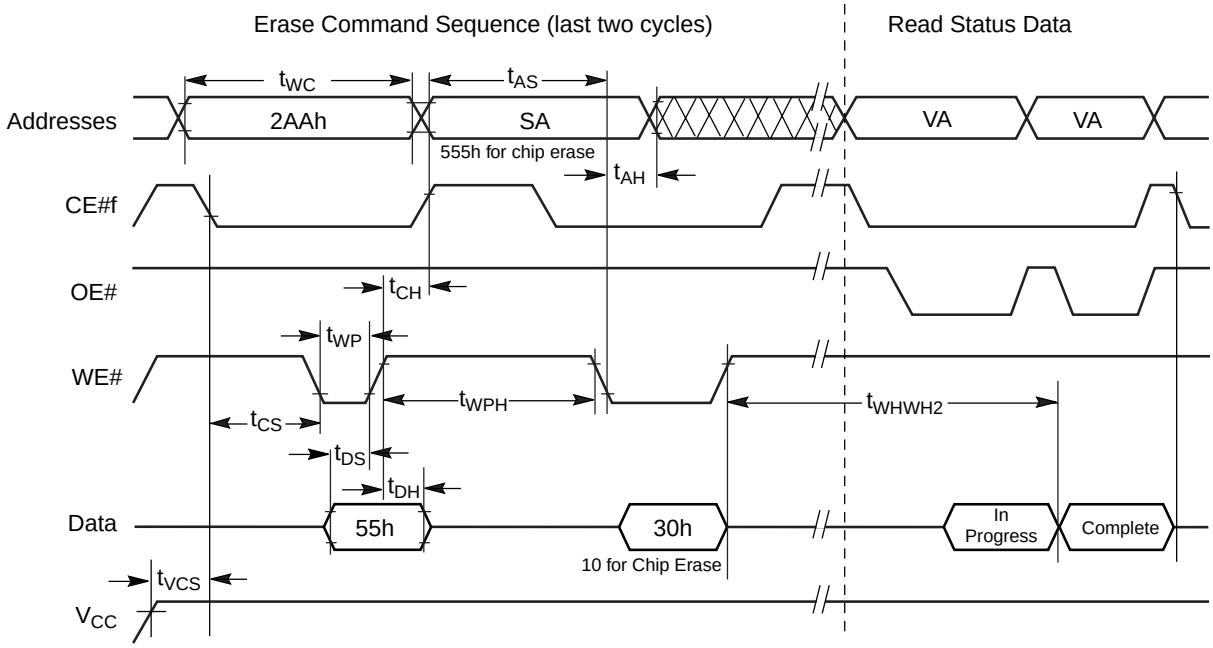


Figure 18. Accelerated Program Timing Diagram

AC CHARACTERISTICS

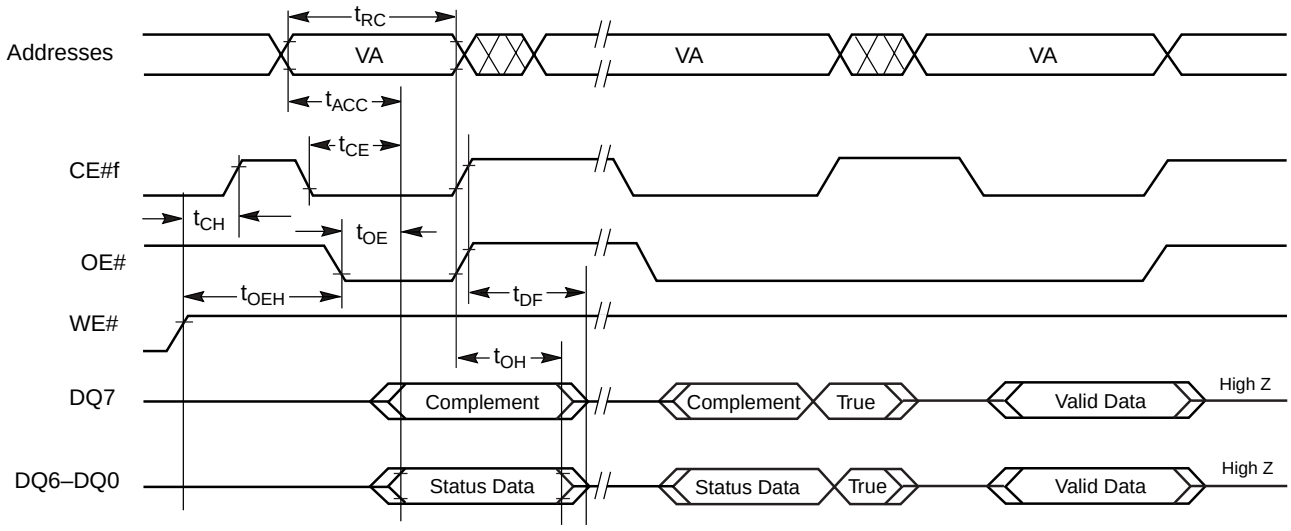


Notes:

1. *SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see "Write Operation Status".*
2. *These waveforms are for the word mode.*

Figure 19. Chip/Sector Erase Operation Timings

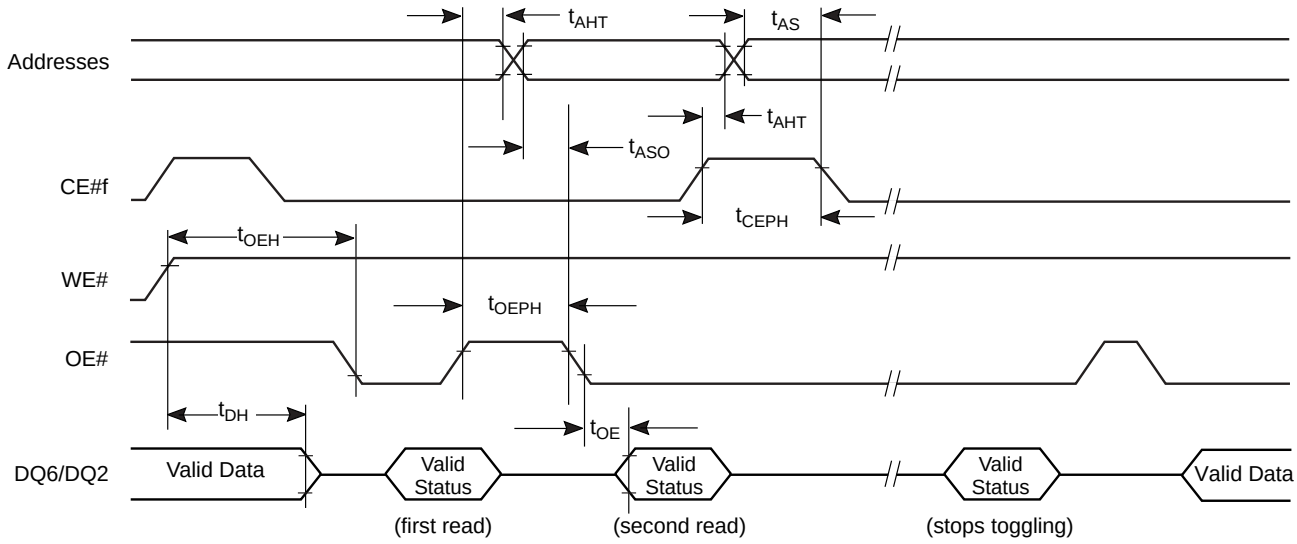
AC CHARACTERISTICS



Note: *VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.*

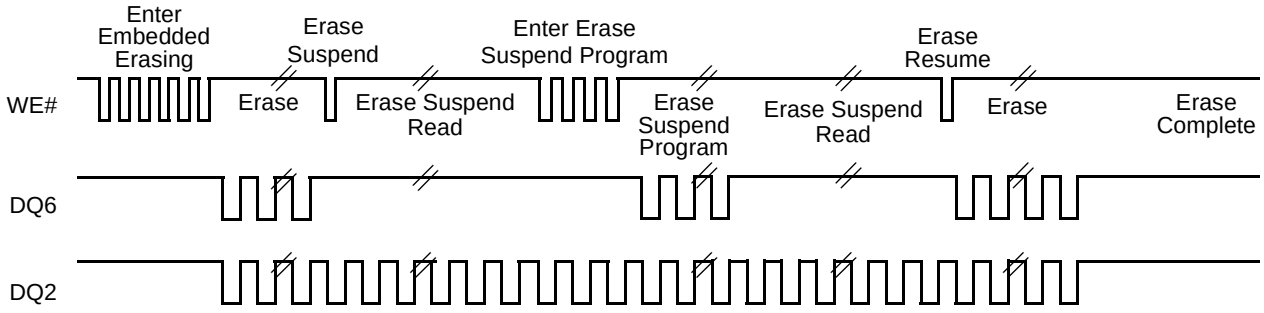
Figure 20. Data# Polling Timings (During Embedded Algorithms)

AC CHARACTERISTICS



Note: *VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle*

Figure 21. Toggle Bit Timings (During Embedded Algorithms)



Note: *DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.*

Figure 22. DQ2 vs. DQ6

AC CHARACTERISTICS

Temporary Sector Unprotect

Parameter					
JEDEC	Std	Description		All Speed Options	Unit
	t_{VIDR}	V_{ID} Rise and Fall Time (See Note)	Min	500	ns
	t_{RSP}	RESET# Setup Time for Temporary Sector Unprotect	Min	4	µs

Note: *Not 100% tested.*

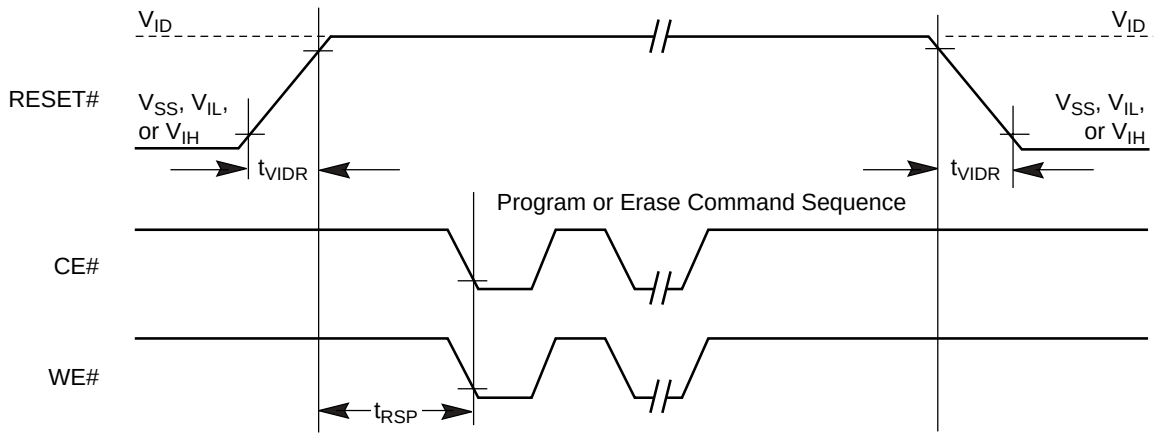
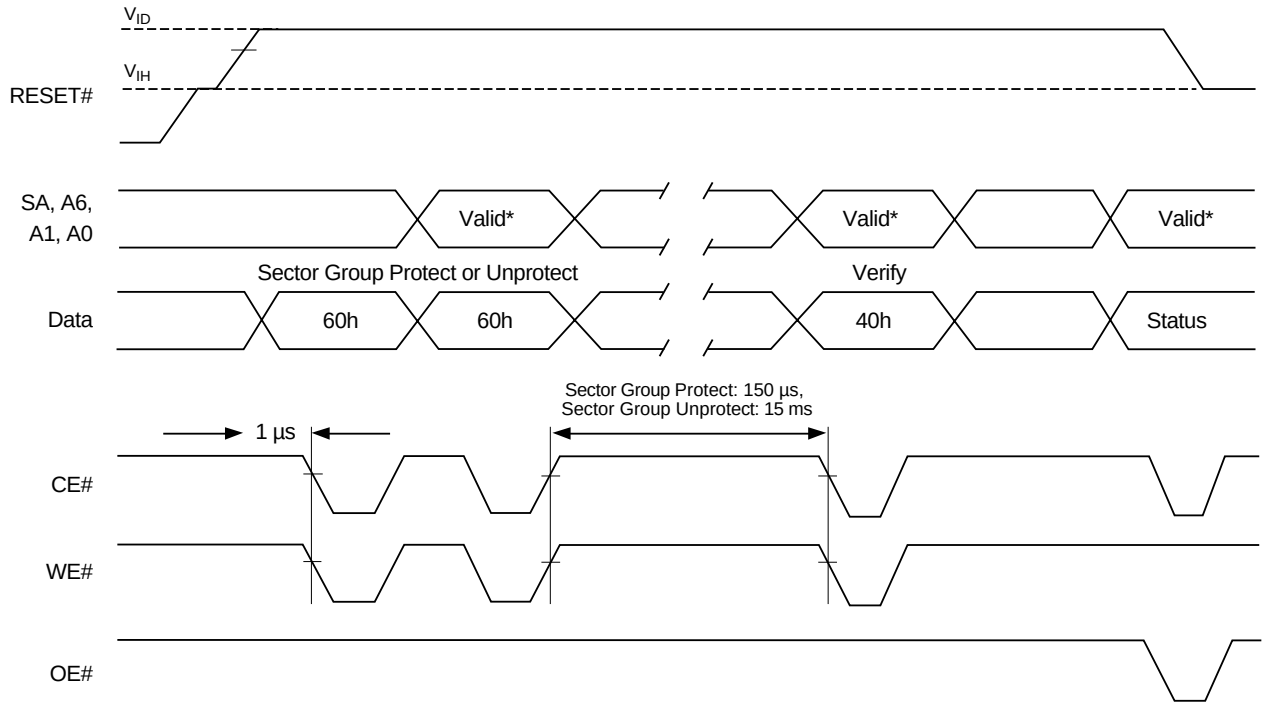


Figure 23. Temporary Sector Group Unprotect Timing Diagram

AC CHARACTERISTICS



* *For sector group protect, A6–A0 = 0xx0010. For sector group unprotect, A6–A0 = 1xx0010.*

Figure 24. Sector Group Protect and Unprotect Timing Diagram

AC CHARACTERISTICS

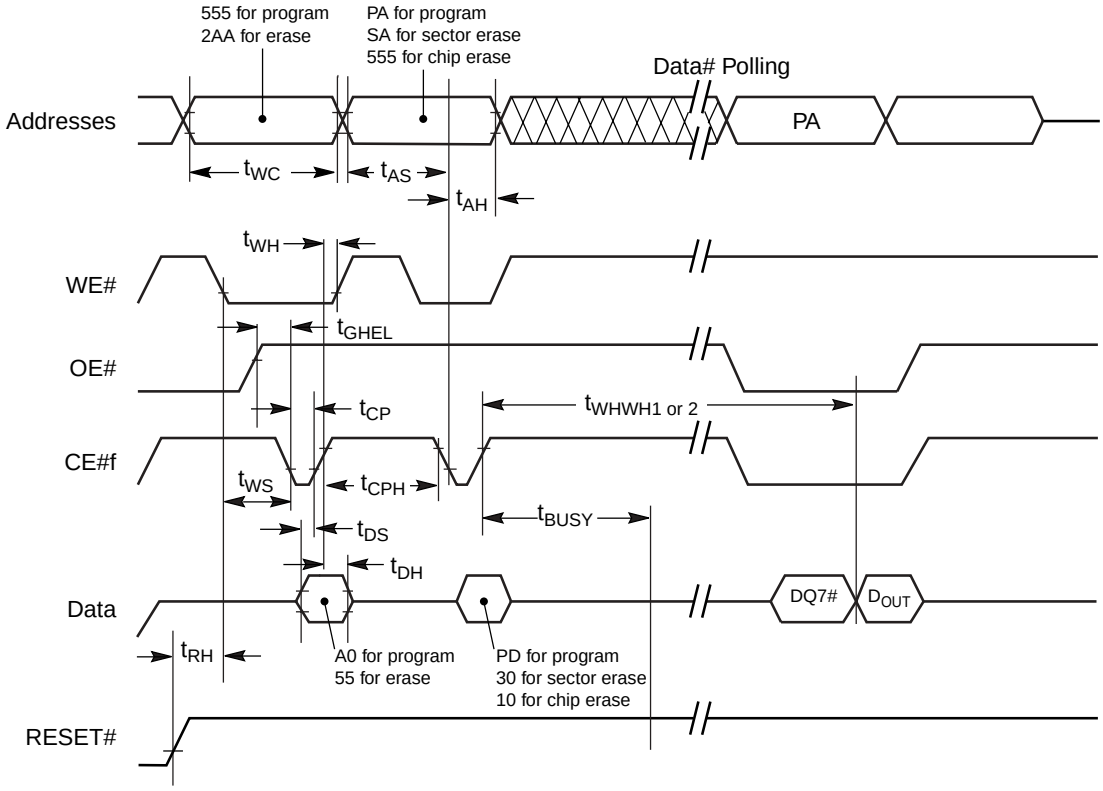
Alternate CE# Controlled Erase and Program Operations

Parameter		Description			Speed	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write Cycle Time (Note 1)		Min	100	ns
t_{AVWL}	t_{AS}	Address Setup Time		Min	0	ns
t_{ELAX}	t_{AH}	Address Hold Time		Min	45	ns
t_{DVEH}	t_{DS}	Data Setup Time		Min	45	ns
t_{EHDX}	t_{DH}	Data Hold Time		Min	0	ns
t_{GHEL}	t_{GHEL}	Read Recovery Time Before Write (OE# High to WE# Low)		Min	0	ns
t_{WLEL}	t_{WS}	WE# Setup Time		Min	0	ns
t_{EHWH}	t_{WH}	WE# Hold Time		Min	0	ns
t_{ELEH}	t_{CP}	CE# Pulse Width		Min	45	ns
t_{EHEL}	t_{CPH}	CE# Pulse Width High		Min	30	ns
t_{WHWH1}	t_{WHWH1}	Write Buffer Program Operation (Notes 2, 3)		Typ	240	µs
		Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	15	µs
		Accelerated Effective Write Buffer Program Operation (Notes 2, 4)	Per Word	Typ	11.8	µs
		Single Word Program Operation (Note 2)		Typ	60	µs
		Single Word Accelerated Programming Operation (Note 2)		Typ	54	µs
t_{WHWH2}	t_{WHWH2}	Sector Erase Operation (Note 2)		Typ	0.5	sec
	t_{RH}	RESET# High Time Before Write (Note 1)		Min	50	ns

Notes:

1. *Not 100% tested.*
2. *See the "AC Characteristics" section for more information.*
3. *For 1–16 words programmed.*
4. *Effective write buffer specification is based upon a 16-word write buffer operation.*

AC CHARACTERISTICS



Notes:

1. *Figure indicates last two bus cycles of a program or erase operation.*
2. *PA = program address, SA = sector address, PD = program data.*
3. *DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.*

Figure 25. Alternate CE# Controlled Write (Erase/Program) Operation Timings

AC CHARACTERISTICS

SRAM Read Cycle

Parameter Symbol	Description		Speed Option	Unit
			10	
t_{RC}	Read Cycle Time	Min	70	ns
t_{AA}	Address Access Time	Max	70	ns
t_{CO1}, t_{CO2}	Chip Enable to Output	Max	70	ns
t_{OE}	Output Enable Access Time	Max	35	ns
t_{BA}	LB#s, UB#s to Access Time	Max	70	ns
t_{LZ1}, t_{LZ2}	Chip Enable (CE1#s Low and CE2s High) to Low-Z Output	Min	10	ns
t_{BLZ}	UB#, LB# Enable to Low-Z Output	Min	10	ns
t_{OLZ}	Output Enable to Low-Z Output	Min	5	ns
t_{HZ1}, t_{HZ2}	Chip Disable to High-Z Output	Max	25	ns
t_{BHZ}	UB#s, LB#s Disable to High-Z Output	Max	25	ns
t_{OHZ}	Output Disable to High-Z Output	Max	25	ns
t_{OH}	Output Data Hold from Address Change	Min	10	ns

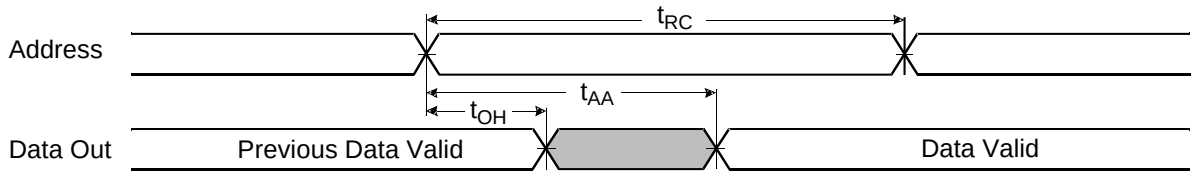


Figure 26. SRAM Read Cycle—Address Controlled

Note: *CE1#s = OE# = V_{IL}, CE2s = WE# = V_{IH}, UB#s and/or LB#s = V_{IL}*

AC CHARACTERISTICS

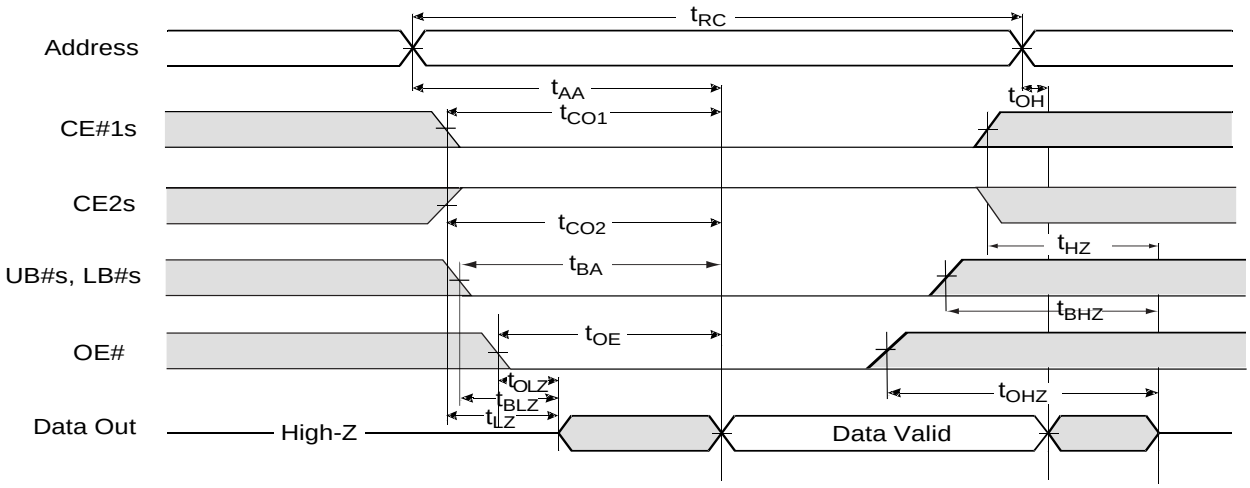


Figure 27. SRAM Read Cycle

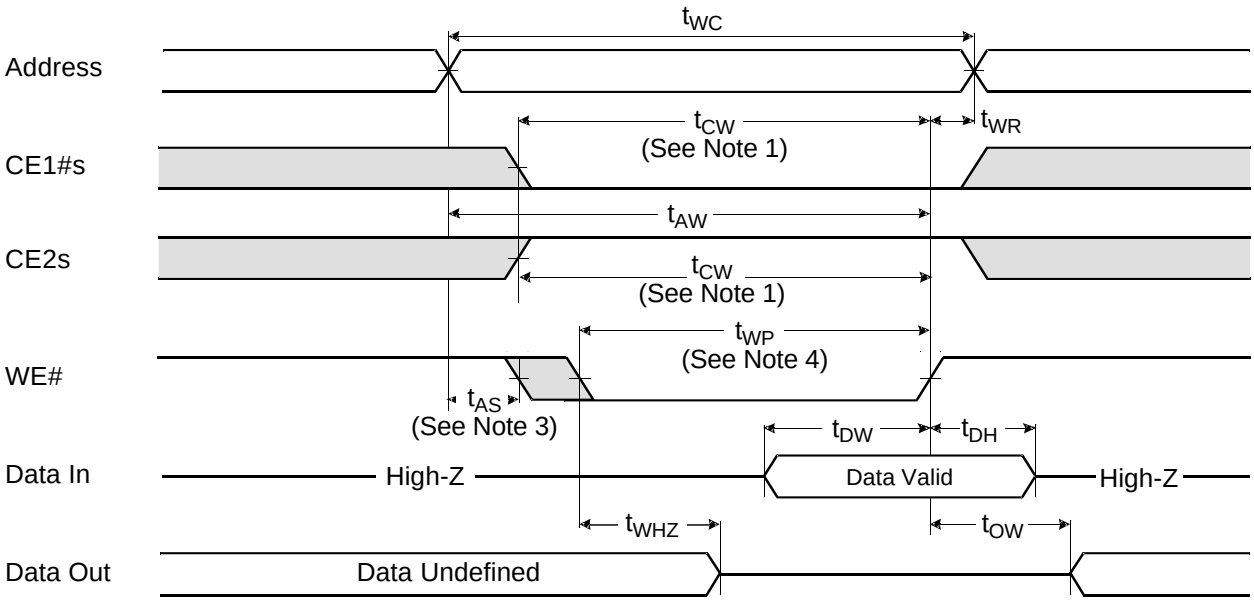
Notes:

1. *WE# = V_{IH}, if CIOs is low.*
2. *t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
3. *At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device interconnection.*

AC CHARACTERISTICS

SRAM Write Cycle

Parameter Symbol	Description		Speed Option	Unit
			10	
t_{WC}	Write Cycle Time	Min	70	ns
t_{Cw}	Chip Enable to End of Write	Min	60	ns
t_{AS}	Address Setup Time	Min	0	ns
t_{AW}	Address Valid to End of Write	Min	60	ns
t_{BW}	UB#s, LB#s to End of Write	Min	60	ns
t_{WP}	Write Pulse Time	Min	50	ns
t_{WR}	Write Recovery Time	Min	0	ns
t_{WHZ}	Write to Output High-Z	Min	0	ns
		Max	20	
t_{DW}	Data to Write Time Overlap	Min	30	ns
t_{DH}	Data Hold from Write Time	Min	0	ns
t_{OW}	End Write to Output Low-Z	Min	5	ns

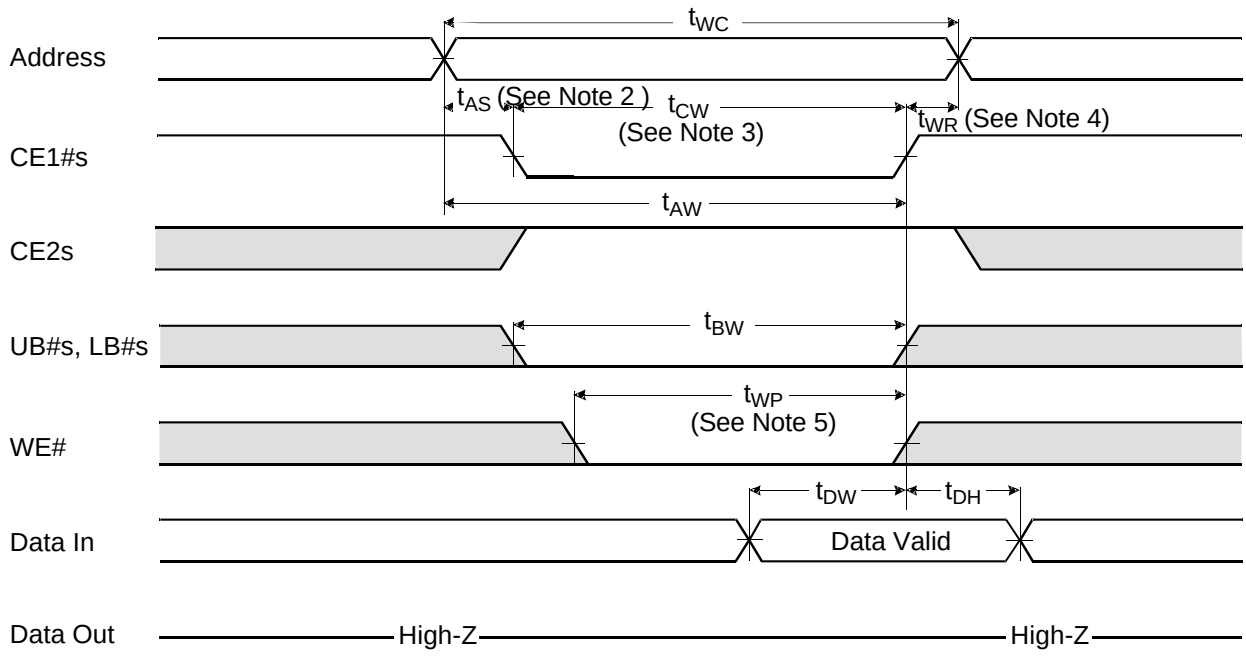


Notes:

1. *WE# controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 28. SRAM Write Cycle—WE# Control

AC CHARACTERISTICS

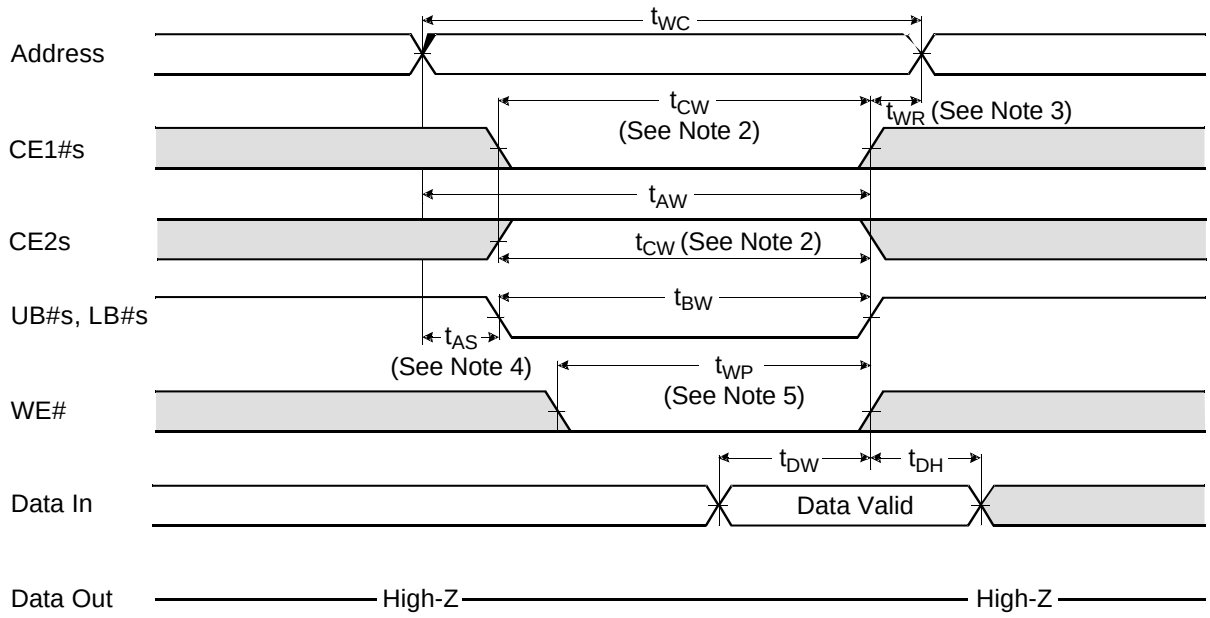


Notes:

1. *CE1#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 29. SRAM Write Cycle—CE1#s Control

AC CHARACTERISTICS



Notes:

1. *UB#s and LB#s controlled.*
2. *t_{CW} is measured from CE1#s going low to the end of write.*
3. *t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as CE1#s or WE# going high.*
4. *t_{AS} is measured from the address valid to the beginning of write.*
5. *A write occurs during the overlap (t_{WP}) of low CE#1 and low WE#. A write begins when CE1#s goes low and WE# goes low when asserting UB#s or LB#s for a single byte operation or simultaneously asserting UB#s and LB#s for a double byte operation. A write ends at the earliest transition when CE1#s goes high and WE# goes high. The t_{WP} is measured from the beginning of write to the end of write.*

Figure 30. SRAM Write Cycle—UB#s and LB#s Control

ERASE AND PROGRAMMING PERFORMANCE

Parameter		Typ (Note 1)	Max (Note 2)	Unit	Comments
Sector Erase Time		0.5	3.5	sec	Excludes 00h programming prior to erasure (Note 6)
Chip Erase Time		32	64	sec	
Single Word/Byte Program Time (Note 3)	Byte	60	600	µs	Excludes system level overhead (Note 7)
	Word	60	600	µs	
Accelerated Single Word/Byte Program Time (Note 3)	Byte	54	540	µs	
	Word	54	540	µs	
Total Write Buffer Program Time (Note 4)		240	1200	µs	
Effective Write Buffer Program Time (Note 5)	Per Byte	7.5	38	µs	
	Per Word	15	75	µs	
Total Accelerated Write Buffer Program Time (Note 4)		200	1040	µs	
Effective Accelerated Write Buffer Program Time (Note 5)	Per Byte	6.25	33	µs	
	Per Word	12.5	65	µs	
Chip Program Time		31.5	73	sec	

Notes:

1. *Typical program and erase times assume the following conditions: 25°C, 3.0 V V_{CC}, Programming specification assume that all bits are programmed to 00h.*
2. *Maximum values are measured at V_{CC} = 3.0, worst case temperature. Maximum values are valid up to and including 100,000 program/erase cycles.*
3. *Word/Byte programming specification is based upon a single word/byte programming operation not utilizing the write buffer.*
4. *For 1-16 words or 1-32 bytes programmed in a single write buffer programming operation.*
5. *Effective write buffer specification is calculated on a per-word/per-byte basis for a 16-word/32-byte write buffer operation.*
6. *In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.*
7. *System-level overhead is the time required to execute the command sequence (s) for the program command. See Table11 for further information on command definitions.*
8. *The device has a minimum erase and program cycle endurance of 100,000 cycles.*

FLASH LATCHUP CHARACTERISTICS

Description	Min	Max
Input voltage with respect to V_{SS} on all pins except I/O pins (including OE#, and RESET#f)	–1.0 V	12.5 V
Input voltage with respect to V_{SS} on all I/O pins	–1.0 V	V_{CC} + 1.0 V
V_{CC} Current	–100 mA	+100 mA

Note: *Includes all pins except V_{CC}. Test conditions: V_{CC} = 3.0 V, one pin at a time.*

PACKAGE PIN CAPACITANCE

Parameter Symbol	Parameter Description	Test Setup		Typ	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0	Fine-Pitch BGA	4.2	5.0	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0	Fine-Pitch BGA	5.4	6.5	pF
C_{IN2}	Control Pin Capacitance	V_{IN} = 0	Fine-Pitch BGA	3.9	4.7	pF

Notes:

1. *Sampled, not 100% tested.*
2. *Test conditions T_A = 25°C, f = 1.0 MHz.*

DATA RETENTION

Parameter Description	Test Conditions	Min	Unit
Minimum Pattern Data Retention Time	150°C	10	Years
	125°C	20	Years

SRAM DATA RETENTION

Parameter Symbol	Parameter Description	Test Setup	Min	Typ	Max	Unit
V_{DR}	V_{CC} for Data Retention	CE1#s ≥ V_{CC} – 0.2 V (Note 1)	2.7		3.3	V
I_{DR}	Data Retention Current	V_{CC} = 3.0 V, CE1#s ≥ V_{CC} – 0.2 V (Note 1)		1.0 (Note 2)	10	µA
t_{SDR}	Data Retention Set-Up Time	See data retention waveforms	0			ns
t_{RDR}	Recovery Time		t_{RC}			ns

Notes:

1. *CE1#s ≥ V_{CC} – 0.2 V, CE2s ≥ V_{CC} – 0.2 V (CE1#s controlled) or CE2s ≤ 0.2 V (CE2s controlled).*
2. *Typical values are not 100% tested.*

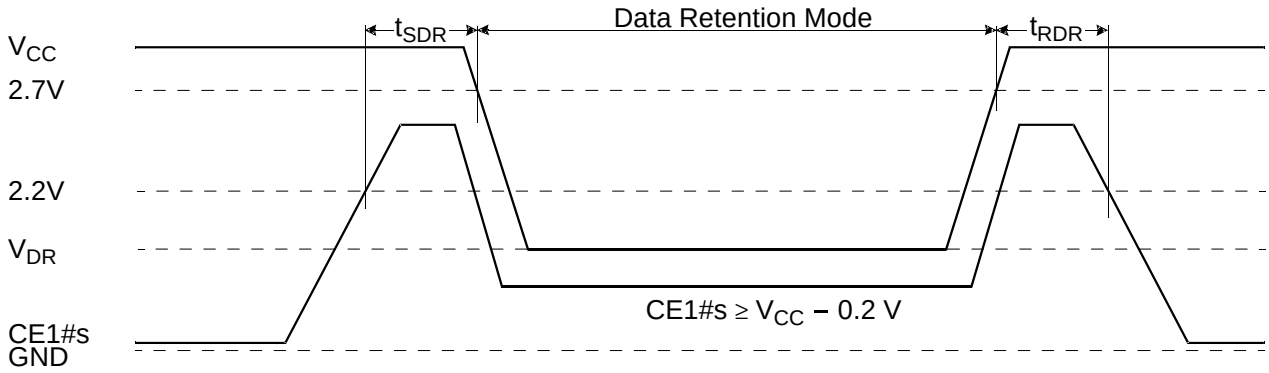


Figure 31. CE#1 Controlled Data Retention Mode

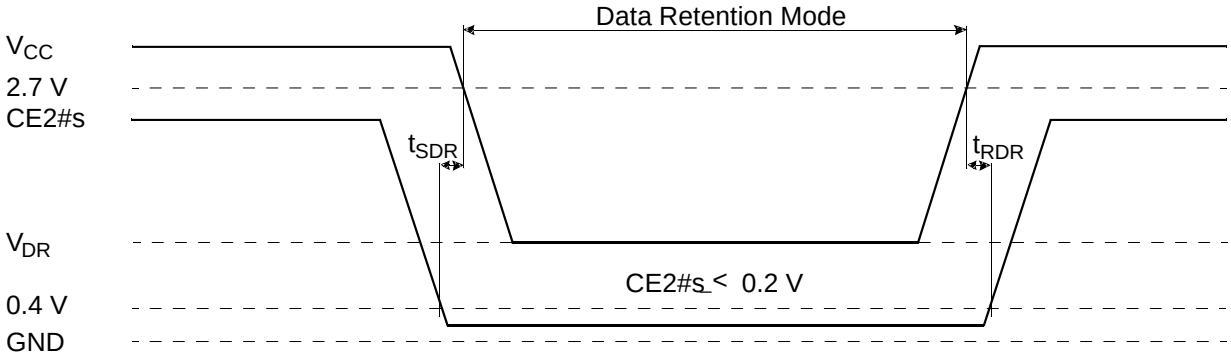


Figure 32. CE2s Controlled Data Retention Mode

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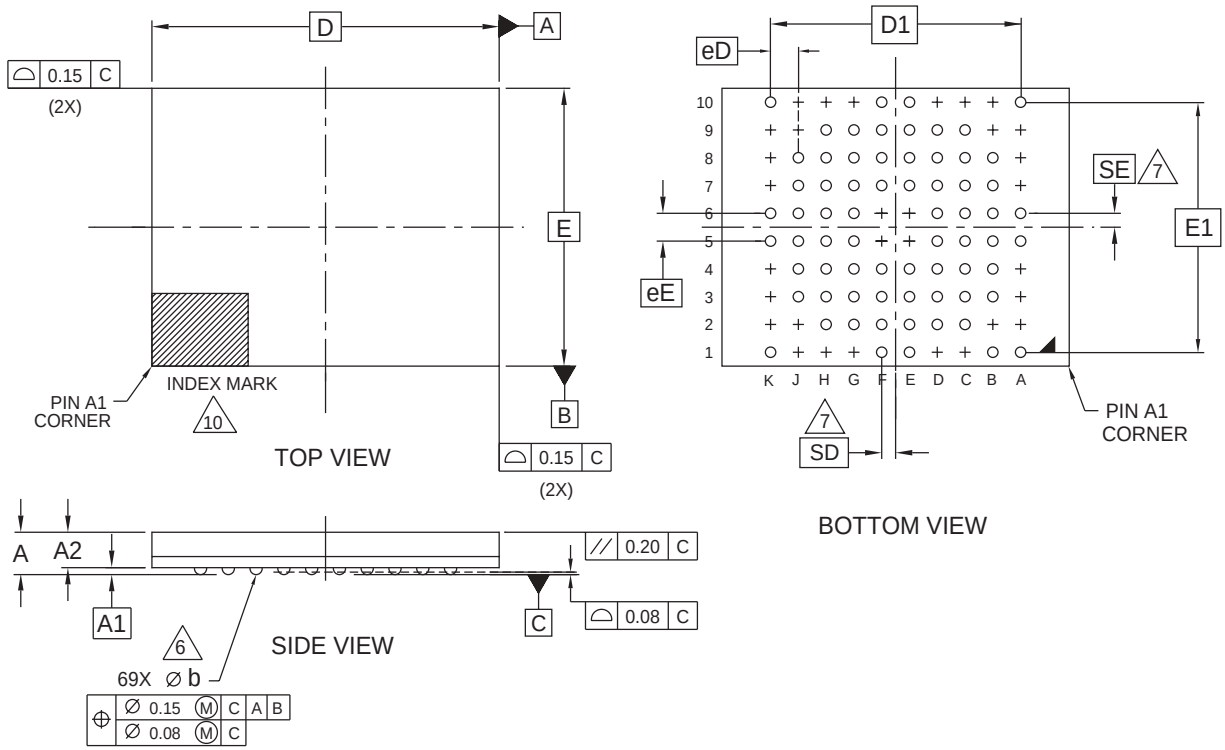
PHYSICAL DIMENSIONS

TLB069—69-Ball Fine-pitch Ball Grid Array (FBGA) 8 x 10 mm Package



PACKAGE	TLB 069			NOTE
JEDEC	N/A			
	10.00 mm X 8.00 mm PACKAGE			
SYMBOL	MIN.	NOM.	MAX.	
A	---	---	1.20	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.81	---	0.97	BODY THICKNESS
D	10.00 BSC			BODY SIZE
E	8.00 BSC			BODY SIZE
D1	7.20 BSC			MATRIX FOOTPRINT
E1	7.20 BSC			MATRIX FOOTPRINT
MD	10			MATRIX SIZE D DIRECTION
ME	10			MATRIX SIZE E DIRECTION
n	69			BALL COUNT
Øb	0.33	---	0.43	BALL DIAMETER
eE	0.80 BSC			BALL PITCH
eD	0.80 BSC			BALL PITCH
SD/SE	0.40 BSC			SOLDER BALL PLACEMENT
	A2,A3,A4,A7,A8,A9,B2,B9,B10 C1,C10,D1,D10,E5,E6,F5,F6 G1,G10,H1,H10 J1,J2,J9,J10,K2,K3,K4,K7,K8,K9			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JESD 95-1, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX IN THE "E" DIRECTION.
   n IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = E/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. NOT USED.
10. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

w052903-163814C

REVISION SUMMARY

Revision A (March 21, 2003)

Initial release.

Revision A+1 (June 10, 2003)

Global

Changed datasheet name to Am41LV3204.

Connection Diagram

Corrected pinout numbering.

Pin Description

Added CIOf and DQ15/A-1