IBM Processor for Network Resources

Version 2.61

Databook

Preliminary

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Note: This document contains information on products in the sampling and/or initial production phases of development. This information is subject to change without notice. Verify with your IBM field applications engineer that you have the latest version of this document before finalizing a design.

IBM Microelectronics Division
1580 Route 52, Bldg. 504
Hopewell Junction,
NY 12533-6351

The IBM home page can be found at
http://www.ibm.com

The IBM Microelectronics Division home page
can be found at http://www.chips.ibm.com

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Contents

List of Figures

List of Tables

1. General Information

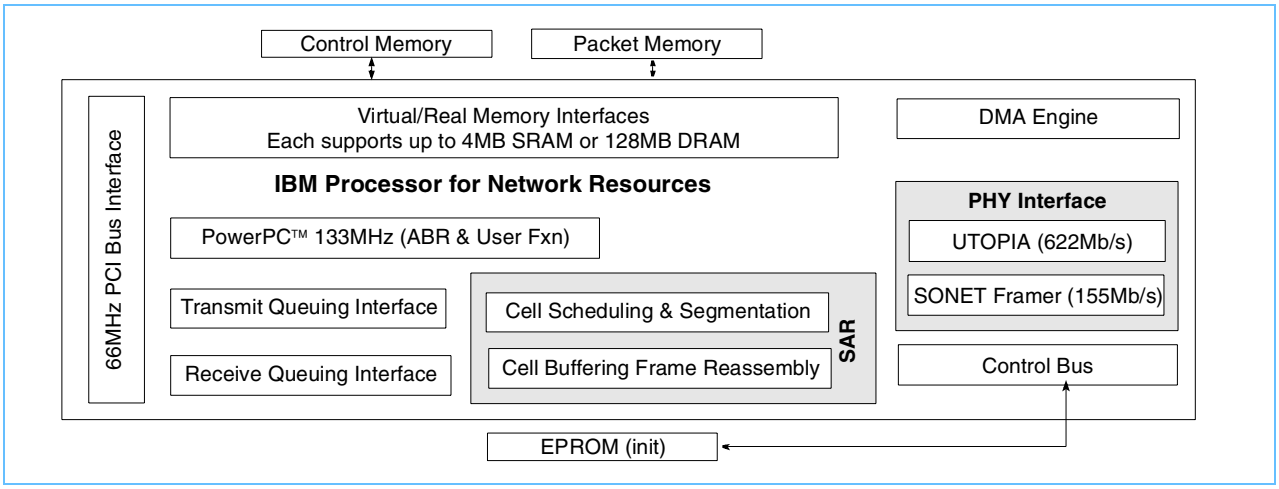
1.1 Features

- Supports multiple protocols, including ATM, POS, Frame Relay, and 10/100/Gigabit Ethernet
- Customizable on-chip 133 MHz IBM PowerPC™ processor core
- Manages up to 65535 simultaneous logical channels, individually or in groups
- Integrated 155 Mb/s SONET (Synchronous Optical Network) Framer for simpler, low bandwidth designs
- Flexible ATM Forum-compliant UTOPIA II interface with up to four PHYs
- Switch Interface Extensions
- PCI 32/64-bit interface up to 66MHz
- Configurable for sustained performance through the subsystem:
  - 155Mb/s full duplex internal SONET framer
  - 622Mb/s full duplex using an external SONET framer
  - 622Mb/s across up to four full duplex 155Mb/s links using an external quad framer
- JTAG Test Interface
- Package: 624 lead, 32 mm x 32 mm CBGA
- Power Supply: 2.6 V ±2%; 3.3 V ±5%.

1.2 Description

IBM32NPCXX1EPABBE66, the IBM Processor for Network Resources (PNR), is an Asynchronous Transfer Mode (ATM) support device. It is an interface and translator between a Peripheral Component Interconnect (PCI) bus and an ATM Utopia or similar interface to an ATM PHY. The PNR has an integrated Packet/Frame Memory (DRAM controller) and performs Segmentation and Reassembly (SAR) functions for several of the ATM Adaptation Layers (AALs). The PNR functions are illustrated below and in *Figure 3: Block Diagram* on page 8 and listed in *Table 1: Summary of Entities* on page 9.

Figure 1: Functional Units in the IBM Processor for Network Resources

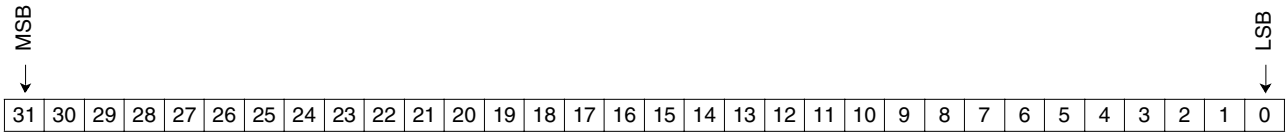


1.3 Ordering Information

Part Number	Description
IBM32NPCXX1EPABBE66	IBM Processor for Network Resources version 2.61

1.4 Conventions and Notation

In most of this document, bit notation is non-IBM, meaning that bits and bytes are numbered in descending order from left to right. Thus, for a four-byte word, bit 31 is the most significant bit and bit 0 is the least significant bit.



Exception: In section *3.19 Embedded PowerPC Processor (COBRA)* on page 469, IBM bit notation is used, meaning that for a four-byte word, bit 0 is the most significant bit and bit 31 is the least significant bit.

The internal addressing view of the PNR registers and memory is big endian. In most cases, a system will wire its PCI bus interface to make the register view transparent, that is, the most significant bit in this specification will be the most significant bit in the register. If registers are read and written 32 bits at a time (which is the only way to access many of the registers), the endian-ness should not be a programming issue with respect to the registers.

The PNR DMA controller can transfer data in either big endian or little endian mode. See *3.2 General Purpose DMA (GPDMA)* on page 73 for details.

Register access conventions:

- Read/Write - bits of the register can be read or written.
- Read Only - bits of the register can only be read. Writes have no effect.
- Clear/Set - if writing to the base address of the register, writing a ‘1’ to a register bit causes the bit to be cleared. If writing to the base address of the register+4, writing a ‘1’ to a register bit causes the bit to be set. Either address can be used to read the register.

Numeric notation is as follows:

- Hexadecimal values are preceded by x and enclosed in single quotation marks. For example: x’0B00’. For individual registers, Address values are hexadecimal without any special markings and may use an X as a placeholder. For example, XXXX 1C3C.
- Binary values in text are either spelled out (zero and one) or appear in single quotation marks. For example: ‘1010’.
- Binary values in the Default and Description columns of the register sections are often isolated from text as in this example:

  0 No action on read access

  1 Auto-reset interrupt request register upon read access

1.5 Standards Compliance

The IBM Processor for Network Resources (PNR), part number IBM32NPCXX1EPABBE66, has been designed with a number of standards in mind. These standards are listed below, grouped according to the area of functionality they address.

- Network (defined by ITU-TS (formerly CCITT), ANSI and ATM Forum)
  - ITU Recommendation I-361 - B-ISDN ATM layer specification
  - ITU Recommendation I.362 - B-ISDN ATM Adaptation Layer (AAL) functional description
  - ITU Recommendation I.363 - B-ISDN ATM Adaptation Layer (AAL) specification
  - ITU Recommendation I.413 - B-ISDN user-network interface
  - ITU Recommendation I-432 - B-ISDN user-network interface - Physical Layer specification
  - ITU Recommendation I-610 - OAM principles of B-ISDN access
  - ANSI T1.ATM-199x Draft, Broadband ISDN - ATM Layer Functionality and Specification
  - ANSI T1.CBR-199x Draft, Broadband ISDN - ATM Adaptation Layer for Constant Bit Rate Service Functionality and Specification
  - ATM Forum 93-620R2 - ATM User-Network Interface Specification - Version 2.3 (July 27, 1993)
  - Bellcore TA-NWT-001248 Generic Requirements for Operations of Broadband Switching Systems (October 1993)
- System Interface
  - PCI Local Bus Specification, Production Version, Revision 2.2, December 18, 1998. Interface Technical Reference
- PHY Interface
  - SATURN User Network Interface, PMC-Sierra, Inc., February 1995
  - ATM Forum 93-727 An ATM PHY Data path interface, Version 2.01, March 24, 1994

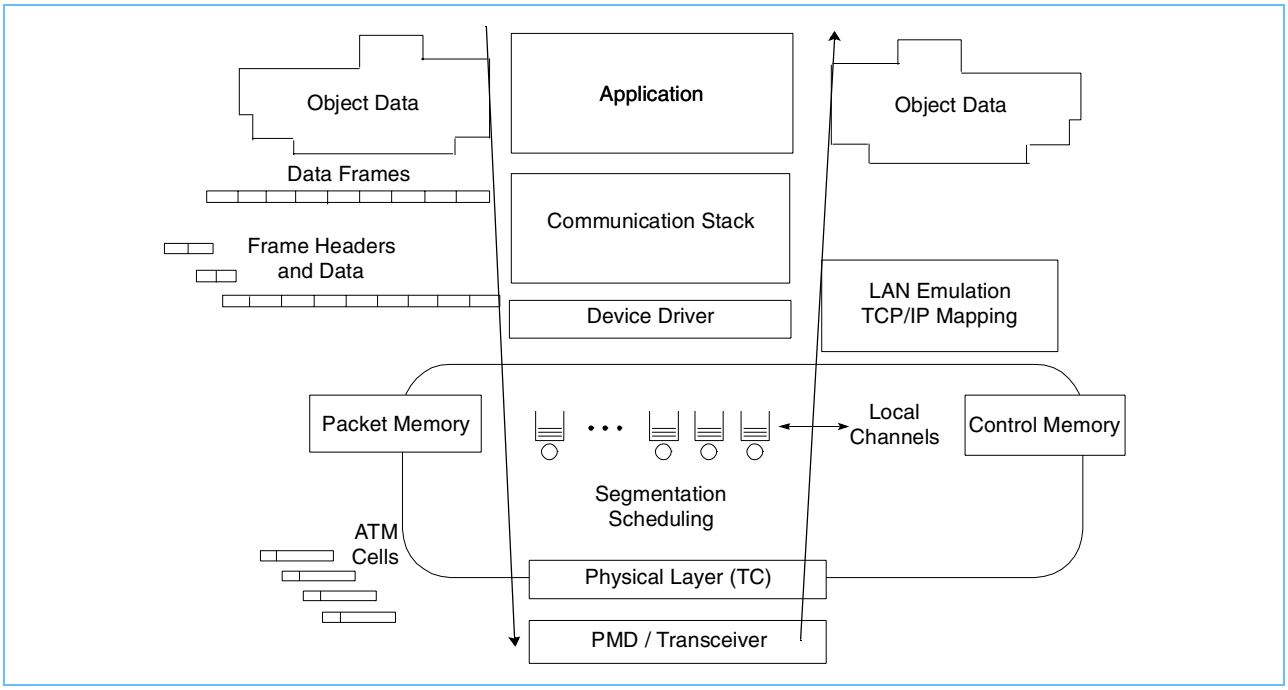
1.6 References

International Technical Support Centers: Asynchronous Transfer Mode (Broadbacn ISDN) Technical Overview. International Technical Support Organization. Raleigh Center, June 1994, GG24-4330-00

1.7 System Environment

The dataflow context of an ATM subsystem is shown in Figure 2. The purpose of the communications subsystem of any digital device is to allow the application to share data and to arbitrate the flow of control with other devices.

Figure 2: System Context of an ATM Subsystem



Data, in the form of application objects or control structures, are divided into communication frames at the communication stack interface. The stack may further partition the frames to fit reliability, efficiency, latency, and protocol requirements.

In most cases, the communication stack encapsulates the data frame with protocol headers and/or trailers. These header blocks are often located in memory in areas apart from the data frames. A device driver is often given the task of moving this scattered memory to the actual transmission device. Scatter DMA is often used to make this operation efficient.

In the case of the IBM Processor for Network Resources, the data can be DMAed into virtually contiguous buffers connected to and controlled by the PNR. It is also possible to write the frame headers directly from the processor to PNR memory. The fully assembled frame is enqueued for transmission over a particular logical channel. (See more on the richness of logical channels in ATM and the PNR in *section 7. Application Notes: Data Structures* on page 673).

The logical channels with pending work are serviced by the ATM Segmentation Layer which breaks the enqueued data into 48-byte chunks (depending on the ATM Adaptation Layer (AAL)) and prefixes it with a five-byte header (yielding a 53-byte ATM cell) in preparation for transmission.

A Transmission Convergence (TC) sublayer appropriate for the Physical Layer (PHY) and Physical Media Dependent (PMD) connection is then exercised, making ATM cells suitable for transmission.

The receiving process is the reverse of the transmission process, except that the scheduling performed during transmission is replaced by an identification-demultiplexing step during the reception of cells.

Note: Not all of these separate parts or steps described in this section are necessary for a dedicated function system. PNR can easily be used in dedicated systems due to the goal of minimal processor intervention for steady state operations.

1.7.1 Logical Channel Support

The Logical Channel is the unit of resource allocation in ATM. At one level, the End Station negotiates with the Network Interface to determine the characteristics of each End-Station-to-End-Station connection. The resources that may be reserved in the network are defined in the ATM UNI (User Network Interface) Specification (see references in *Standards Compliance* on page 3). These resources include (but are not limited to) the peak and average bandwidth to be used by the logical channel, the maximum burst length that may be transmitted at the burst rate, the latency and variance of the connection, and the loss probability.

The term Logical Channel rather than virtual circuit or VPI/VCI is used in this databook to provide a level of abstraction from these specific instances.

A Switched Virtual Circuit (SVC) can be negotiated with specific characteristics.

A virtual path can be negotiated with the network. Several virtual circuits within that path can then be multiplexed, using the VCI on that single VPI, without having to renegotiate for each additional VCI. The Logical channel, with respect to the network, would be the Virtual Path. There would be multiple logical channels internal to the End Station based on the Virtual Circuits used within the path.

All of these Logical Channels are dealt with uniformly in the PNR. A hierarchy of Logical Channel Descriptors can be built up, and frames or buffers can be queued to each of the LCDs. See *3.12 Transmit Scheduler (CSKED)* on page 243 for details.

1.7.2 Virtual Memory Support

The Packet Memory space appears on the bus as a group buffers whose size is configurable up to 128 KB). A level of indirection has been added to the addressing of Packet memory to provide these large frame buffers without requiring memory behind all of them at the same time. This has been done for a number of reasons:

- The frames on the network can be up to 64 KB long.
- The receiver does not know how long a frame will be until it is completely received.
- Software generally has a much easier time dealing with contiguous memory.

The memory does not page or swap. There are two major internal strategies for improving efficiency:

- The first N bytes of memory in a buffer are referenced directly.
- The blocks that make up the buffers are of multiple sizes.

1.7.3 Queues

The IBM Processor for Network Resources makes extensive use of cached single memory operation atomic queues:

Transmit Queues The interface to the scheduling entity. Blocks and Frames can be queued to Logical Channels.

Receive Queues Based on the settings in the Logical Channel Descriptor (receive side). Cells arriving can be queued individually, collected into frames.

Event Queues When a frame is transmitted, its memory can be “garbage collected” or a reference to the frame can be placed on an event queue for software to handle.

If either a FIFO buffer scheme or a frame buffer scheme is used to source or sink data on a logical channel, it is possible to set thresholds on the buffering that will cause events to be queued. When a threshold is crossed (for instance if a transmitting LC is about to run out of data to transmit), an event will be queued. Software can read these events either by polling or by being interrupted and can schedule tasks to provide more data.

Events can be scheduled on the reception of the first N bytes of a frame so that header processing can begin even before the complete frame is received. This will allow “cut-through” routing to be supported.

Note: In order to maintain the atomicity of 64-bit atomic transfers, the user must ensure that 64-bit transfers are bus atomic within the particular bus system in which the PNR is being used.

1.7.4 Scheduling

There is extensive support for transmit scheduling. Please see *1.9.1 Transmit Path* on page 10 and *Figure 4: Transmit Scheduling Capabilities* on page 11 for details.

1.8 Key Interfaces

The IBM Processor for Network Resources has four major interfaces: host bus interfacing, memory management for buffers and control, cell segmentation and reassembly, and Physical Layer (PHY) hardware control for an ATM adapter.

A **System Bus** acts as an actively cached memory slave and as a master for the PCI 32- or 64-bit bus.

The **PHY Interface** supports several physical layer hardware devices that perform parallel to serial data conversion and the rest of the transmission convergence.

The PHY interface connects to several available hardware support devices. This layer of hardware converts a parallel data stream into a serial data stream to be shipped to and from the Physical Media Dependent (PMD) layer.

The PHY and PMD end of a card design can be implemented as one of several encoding schemes and speeds, supporting both copper and fiber optic serial links. The interface complies with the Utopia Level II and Packet Over Sonet (POS) Specifications supporting up to 4 PHYs. (See *1.5 Standards Compliance* on page 3 for documents that describe these interfaces.)

The PMD Layer interface connects to the line drivers and receivers. This could be either a copper or a fiber optic transceiver.

Two External DRAM Interfaces can each support various configurations of synchronous DRAM (SDRAM) or synchronous static RAM (SRAM). The interfaces are totally independent of one another; for example, one can be connected to SDRAM and the other to SRAM. However, each interface can only support one type of memory; that is, SDRAM and SRAM cannot be connected to the same interface. The interface is a direct drive to the DRAM.

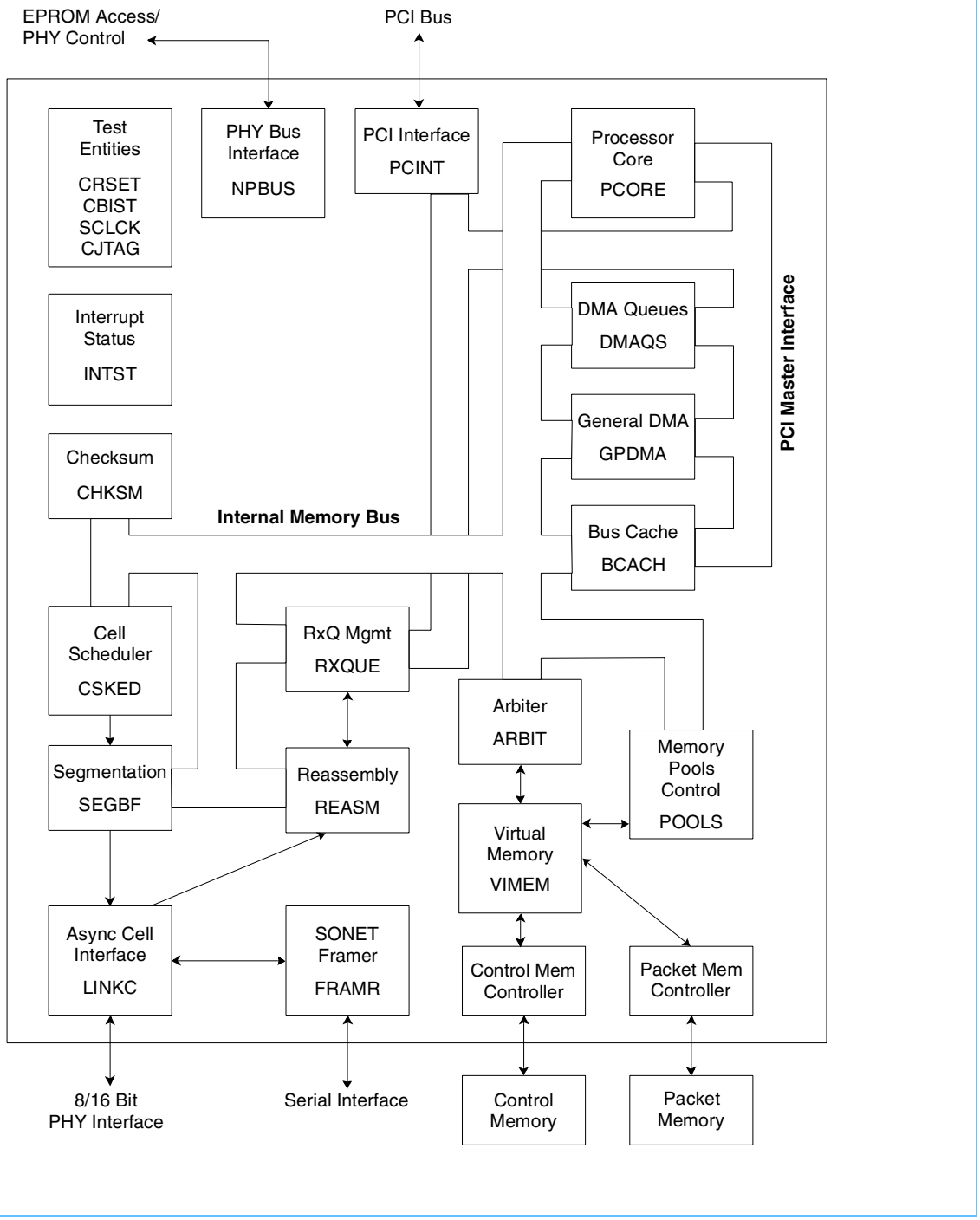
In standard operation, the arrays connected to the two memory interfaces of the PNR are used for the storage of packet data and control structures. Both the Packet and Control Memory arrays are 32 bits wide plus any error detection/correction enabled by the user.

When running at 155Mb/s or slower (full duplex aggregate throughput), a single array of memory can be used. Both control and data store are contained in this single array of memory. For a detailed description of the external memory organization refer to *3.6 The DRAM Controllers (COMET/PAKIT)* on page 137.

The **Control and Configuration Interface** covers a number of functions. It gives access from the system bus to the PHYs and the EPROM. The EPROM can also be used to hold initial device configuration, up to and including PVC configurations.

The four major interfaces allow the PNR to be used in both “deep” and “shallow” adaptors with minimal external logic.

Figure 3: Block Diagram



1.9 Functional Description

The PNR has been designed by breaking the implementation of the various functions and dataflows into separate entities (major functional units).

This processor acts as a conversion unit from a bus memory interface (which is Work Queue oriented) to a PHY level ATM. To accomplish this, the PNR contains the major functional units listed in *Table 1: Summary of Entities* on page 9 and shown in *Figure 3: Block Diagram* on page 8.

The entities and their registers are described in this document starting on the page listed in *Table 1*.

Table 1: Summary of Entities

Major Function	Entity Name	Description	See Page
Control Processor Bus Interface	PCINT	Provides PCI specific interfacing between the external connection and the internal entities.	33
	GPDMA	Provides DMA control between System Memory and PNR Packet Memory.	73
	INTST	Contains the masking registers that choose which interrupt or status source will be gated onto one of the two available interrupt I/O pins.	85
	DMAQS	Provides the interface to the PNR's DMA master capability. It provides three DMA queues that hold DMA descriptor chains that are executed in a multiplexed fashion. Together with GPDMA, a very powerful interface is provided the to software to complete complex tasks including TCP/IP checksumming for transmit and receive packets.	115
Memory Control	COMET/PAKIT	Contains the memory controllers. COMET controls Control Memory and PAKIT controls Packet Memory.	137
	CHKSM	This entity has two functions. First, it is capable of initializing and/or testing Packet and Control Memory. Second, it can perform TCP checksums (Two's complement, 16-bit sum with "end-around-carry").	153
	VIMEM	Responsible for adjusting all addresses provided to the memory control entities.	191
	ARBIT	Memory subsystem requestor arbitration.	211
	BCACH	Provides the caching function for data transfers on the PCI bus.	233
	POOLS	Memory Pool manager.	395
Transmit Data Path	CSKED	Transmit Cell Scheduler. Responsible for receiving a packet from the processor, determining when cells from the packets need to be transmitted, and passing this information to the segmentation buffer entity.	243
	SEGBF	Segmentation Buffer. Accepts frames from the cell scheduler (CSKED) or software, then generates ATM cells to send out over the external physical interface. This entity knows or cares nothing about scheduling cells over time; it will simply construct a cell when it is provided an address of a logical circuit descriptor to operate on. All rate and scheduling concerns must be addressed by the CSKED logic or software prior to queueing a frame to SEGBF.	281
Receive Data Path	REASM	Cell and Packet Reassembly. Top level receive entity that encapsulates all of the receive subentities and includes AAL processing.	301
	RXQUE	Receive Queue manager.	351
PHY Level Interfaces	LINKC	Provides the interface between the PNR and either an ATM PHY device or, when the internal framer is selected, a serializer/deserializer device.	165
	NPBUS	Nodal Processor Bus interface.	387
	FRAMR	Full SONET OC-3/STM-1 framing support logic.	507
Hardware Protocol Assist	PCORE	Embedded 401 Processor Core interface logic.	423
	COBRA	Chip OnBoard Risc Architecture, the Embedded 401 Processor Core.	469

Table 1: Summary of Entities (Continued)

Major Function	Entity Name	Description	See Page
Base Device Functions	SCLCK	System Clock Generation and Repowering.	
	CRSET	Hardware and Software Reset Controlling.	105
	CBIST	Built-In Self Test logic.	105
	CJTAG	JTAG Test Interface Logic.	501

1.9.1 Transmit Path

A typical transmit operation begins with the software requesting a buffer from POOLS and filling it with data via slave DMA, master DMA, or processor writes. If virtual buffers are being used, the data write operation can fail due to lack of physical buffers. In the event of a failure, the header of the packet is updated to indicate the failure. If using master DMA, the failed buffer can be freed to POOLS. If not, the software can audit the header after the buffer has been completely transferred, and either take action to recover the data immediately or allow CSKED to generate an event later in the transmit cycle for any buffers that have had a data write failure.

Before the data can be transmitted, the buffer header must be updated to contain information required for correct transmission. Information such as data length, starting offset, and Logical Channel (LC) address are just a few of the fields that must be correctly reflected in the buffer header. For a complete list of the fields in the buffer header refer to *7.1 Packet Header* on page 673.

In addition to the fields in the buffer header, the scheduling and segmentation sections of the Logical Channel Descriptor (LCD), such as peak rate, average rate, and AAL type, must also be set up correctly prior to transmission. For a complete list of the fields in the LCD, refer to *7.3 Transmit LCD Data Structures* on page 678. To improve performance, the LCDs are cached in the TXLCD entity.

After the data have been transferred into packet storage and both the buffer header and the LCD structure have been correctly initialized, the buffer address is queued to CSKED. When it receives a buffer, CSKED checks the buffer header (Packet Memory) to make sure that the data transfer operation that filled the buffer completed without error. If it finds an error, CSKED posts an event to software and does nothing further with this buffer. If no error is indicated in the buffer header, CSKED fetches several fields from the LCD indicated in the buffer header to determine the current state of that LCD. If the LCD is busy sending another buffer, the new buffer is queued to this LCD and will be processed when all previously enqueued buffers have been transmitted. If the LCD is not busy, CSKED updates the LCD based on several fields in the buffer header and a request is sent to SEGBF to send a cell from this LCD. If more cells need to be sent, CSKED queues the LCD to the timewheel (which is comprised of a series of queues that determine when a cell is transmitted).

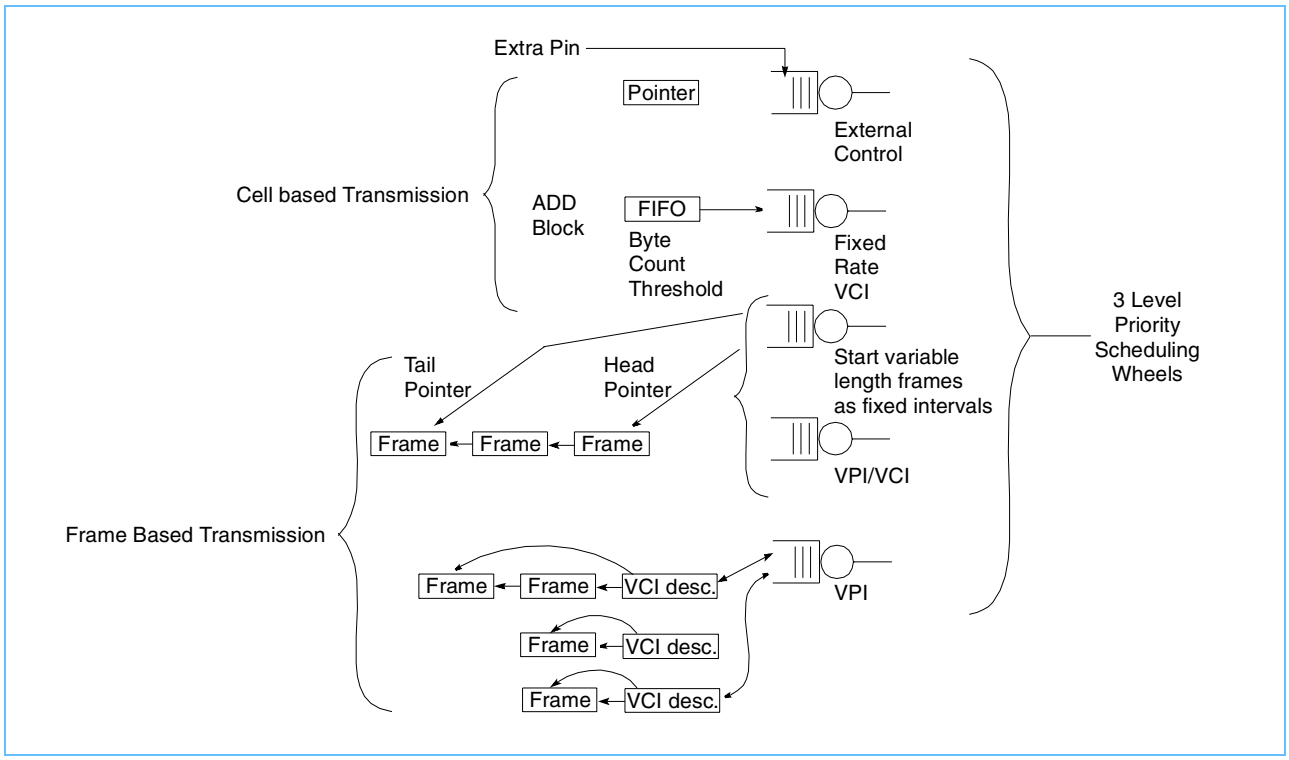
When CSKED detects a previously enqueued LCD on the time wheel, several fields are retrieved from the LCD. Among other things, these fields are used by CSKED to determine where on the time wheel to reschedule this LCD. The LCD address is then provided to SEGBF for processing.

When CSKED provides an LCD address to SEGBF, the segmentation portion of the LCD is used to determine both the current address at which to continue buffer segmentation and the type of cell to construct. Depending on the AAL type bits in the segmentation portion of the LCD, the cell is constructed in an internal array using data from the LCD as well as data fetched from Packet Memory. When the cell construction is complete, status is raised to LINKC indicating that a new cell is available for transmission.

Transmit opportunities are repeatedly provided to SEGBF by CSKED at the desired rate until all the data in the buffer has been passed to LINKC via the cell buffer array. When SEGBF detects that no more data exists for a buffer, an indication is passed to CSKED. If more buffers are queued, the LCD is updated and the segmentation process continues until all buffers on the LCD queue are serviced. A bit in the buffer header generates a transmit complete event when all of the data in the buffer has been transmitted.

In POS mode, CSKED will only provide one transmit request per buffer to SEGBF. SEGBF will segment the entire buffer before accepting another request from CSKED. Up to four physical drops can be configured in LINKC. A field in the LCD is used to assign a connection to a physical drop.

Figure 4: Transmit Scheduling Capabilities



1.9.2 Receive Path

As cells arrive, they pass from LINKC to REASM. REASM uses a portion of the ATM packet header to look up the LCD address for this cell. The LCD address is then passed to RXLCD. RXLCD reads the receive portion of the LCD, and then REASM processes the cell based on the LCD information. For example, the LCD specifies what AAL to use and maintains the current reassembly state. Using the current reassembly state, the cell data is written to Packet Memory. While the data is written to Packet Memory, other functions such as CRC and TCP/IP checksum verification are performed in parallel. If a packet is complete, all trailer verification is performed. If the packet is good, an event is placed on a receive queue in the RXQUE entity. For error scenarios, see *3.15 Receive Queues (RXQUE)* on page 351. At this point, software can dequeue the packet event from RXQUE using the dequeue operation. It can then examine headers, DMA the data into user space, and perform TCP checksums. When these actions are complete, the buffer is returned to the PNR by performing a POOLS free buffer operation.

1.9.3 Register Addressing Overview

Table 2: Memory Map for Registers and Arrays

Address	Entity	Elements Accessed	Notes
XXXX 0000 - 00FF	PCINT	Registers *3.1 The IOP Bus Specific Interface Controller (PCINT)* on page 33	
XXXX 0100 - 01FF	GPDMA	Registers & Array *3.2 General Purpose DMA (GPDMA)* on page 73	1, 2
XXXX 0400 - 04FF	INTST	Registers *3.3 Interrupt and Status/Control (INTST)* on page 85	
XXXX 0500 - 05FF	CRSET	Registers *3.4 Reset and Power-on Logic (CRSET/CBIST)* on page 105	
XXXX 0600 - 08FF	DMAQS	Registers *3.5 DMA Queues (DMAQS)* on page 115	1
XXXX 0900 - 09FF	COMET/PAKIT	Registers *3.6 The DRAM Controllers (COMET/PAKIT)* on page 137	
XXXX 0A00 - 0AFF	CHKSM	Registers *3.7 On-chip Checksum and DRAM Test Support (CHKSM)* on page 153	1
XXXX 0B00 - 0BFF	LINKC	Registers *3.8 The PHY Interface (LINKC)* on page 165	
XXXX 0D00 - 0DFF	VIMEM	Registers *3.9 Virtual Memory Logic (VIMEM)* on page 191	
XXXX 0E00 - 0EFF	ARBIT	Registers *3.10 Memory Arbitration Logic (ARBIT)* on page 211	
XXXX 1000 - 1FF	BCACH	Registers *3.11 The Bus DRAM Cache Controller (BCACH)* on page 233	
XXXX 1100 - 117F	BCACH	Array *3.11 The Bus DRAM Cache Controller (BCACH)* on page 233	
XXXX 1200 - 3FF	CSKED	Registers & Array *3.12 Transmit Scheduler (CSKED)* on page 243	
XXXX 1400 - 5FF	SEGBF	Registers & Array *3.13 Transmit Buffer Segmentation (SEGBF)* on page 281	
XXXX 1600 - 7FF	REASM	Registers & Array *3.14 Cell/Packet Reassembly (REASM)* on page 301	
XXXX 1800 - FFF	RXQUE	Registers *3.15 Receive Queues (RXQUE)* on page 351	
XXXX 2000 - 2018	NPBUS	Registers & External EEPROM & Soner Framer Core *3.16 Nodal Processor Bus Interface Logic (NPBUS)* on page 387	3
XXXX 2400 - 7FF	PHY 1	Registers *3.16.6 PHY 1 Registers* on page 393	
XXXX 2800 - 2BFF	PHY 2	Registers *3.16.7 PHY 2 Registers* on page 394	
XXXX 2C00 - 2FFF	Reserved	Reserved	
XXXX 3000 - 3FFF	POOLS	Registers & Arrays *3.17 Buffer Pool Management (POOLS)* on page 395	

1. Not all addresses are used in this space.
2. *GPDMA Array* on page 83 tells how to get at the arrays since the array is not memory mapped.
3. *NPBUS EPROM Address/Command Register* on page 392 tells how to access EEPROMs and the Sonet Framer Core.

Table 2: Memory Map for Registers and Arrays (Continued)

Address	Entity	Elements Accessed	Notes
XXXX 4000 - 4FFF	PCORE	Registers & Arrays *3.18 Processor Core (PCORE)* on page 423	
XXXX 5000 - 5FFF	PPOCM	Arrays *3.18.50 PCORE OCM Window Address Register* on page 463	

1. Not all addresses are used in this space.
2. *GPDMA Array* on page 83 tells how to get at the arrays since the array is not memory mapped.
3. *NPBUS EPROM Address/Command Register* on page 392 tells how to access EEPROMs and the Sonet Framer Core.

2. Input/Output Definitions

The several interfaces to the PNR are described in the following sections. There are 443 active I/O pins, assigned as follows:

- 90 for the PCI bus
- 160 for the DRAM Memory Bus
- 85 for the NPBUS
- 70 for the PHY bus
- 38 for Clock, Configuration, and LSSD

For I/O pin locations, see *Figure 37: Pinout Viewed from Above* on page 634 and *Table 38: Signal Pin Listing By Signal Name* on page 635.

2.1 PCI Bus Interface

Figure 5: PCI Bus Connections

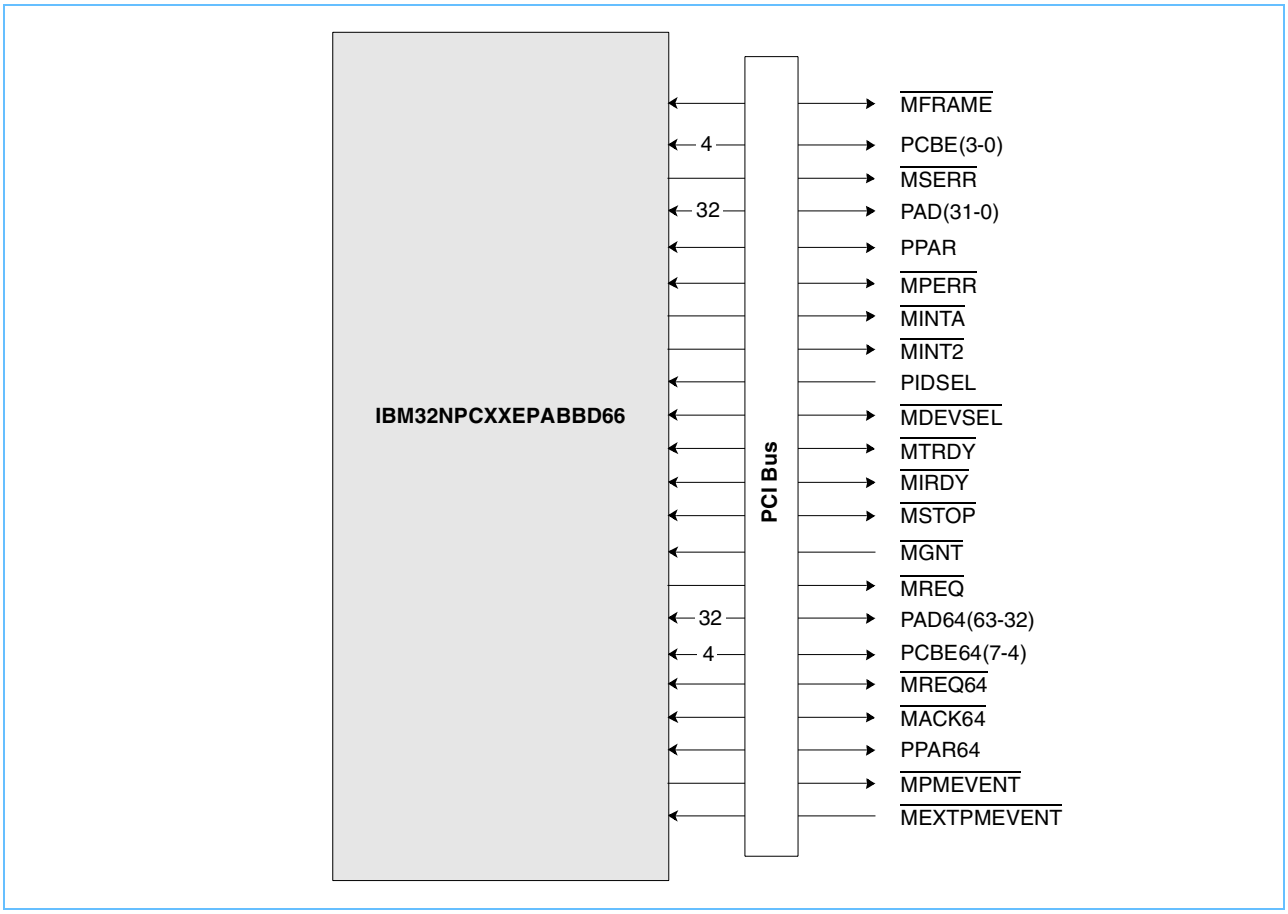


Table 3: PCI Bus Interface Signal Descriptions

Signal Name	Quantity	Type	Description
$\overline{\text{MFRAME}}$	1	S/T/S	Cycle Frame is driven by the current master to indicate the beginning and duration of an access.
PCBE(3-0)	4	T/S	Bus Command and Byte Enables are multiplexed on the same PCI pins. During address phase they define the bus command; during data phase they define the byte enables.
$\overline{\text{MSERR}}$	1	O/D	System Error reports address parity errors, data parity errors on the Special Cycle command, or any other system error where the result will be catastrophic.
PAD(31-0)	32	S/T/S	Address and Data are multiplexed on the same pins. A bus transaction consists of one address phase and one or more data phases.
PPAR	1	T/S	Parity is even parity across ad(31-0) and C/BE(3-0). Parity generation is required by all PCI agents.
$\overline{\text{MPERR}}$	1	S/T/S	Parity Error is for reporting data parity errors during all PCI bus transactions except Special Cycle.
$\overline{\text{MINTA}}$	1	O/D	Interrupt A is used to request an interrupt.
$\overline{\text{MINT2}}$	1	O/D or S/T/S	This is an interrupt line that will go active low when sources within the PNR go active. It can be optionally connected to PCI interrupt B. See *3.3: Interrupt and Status/Control (INTST)* on page 85 for more details.
PIDSEL	1	IN	Initialization Device Select is a chip select during configuration transactions.
$\overline{\text{MDEVSEL}}$	1	S/T/S	Device Select indicates the driving device has decoded its address as the target of the current transaction.
$\overline{\text{MTRDY}}$	1	S/T/S	Target Ready signals the target agent's ability to complete the current data phase of the transaction.
$\overline{\text{MIRDY}}$	1	S/T/S	Initiator Ready indicates the bus master's ability to complete the current data phase.
$\overline{\text{MSTOP}}$	1	S/T/S	Stop indicates the current target is requesting the master to stop the current transaction.
$\overline{\text{MGNT}}$	1	IN	Receives the Bus Grant line after a request has been made.
$\overline{\text{MREQ}}$	1	S/T/S	Requests the bus for an initiator transfer.
PAD64(63-32)	32	S/T/S	Address and Data are multiplexed on the same pins and provide 32 additional bits. Also, these pins are multiplexed with the ENSTATE outputs, which allow debug of various internal state machines and signals.
PCBE64(7-4)	4	T/S	Bus Command and Byte Enables are multiplexed on the same PCI pins for 64-bit transfer support.
$\overline{\text{MREQ64}}$	1	S/T/S	Request 64-bit transfer. Has the same timing as $\overline{\text{MFRAME}}$.
$\overline{\text{MACK64}}$	1	S/T/S	Acknowledge 64-bit transfer. Has the same timing as $\overline{\text{MDEVSEL}}$.
PPAR64	1	S/T/S	Parity Upper DWORD is the even parity bit that protects PAD64(63-32) and PCBE(7-4). When not on a PCI bus supporting 64 bits, this will drive ENSTATE outputs.
$\overline{\text{MPMEVENT}}$	1	O/D	As a $\overline{\text{PME}}$ source, this signal is active low and indicates a power management event signalled from the PNR. The output need to be conditioned with a card-level FET circuit so that the resulting signal ($\overline{\text{PME}}$ on the PCI bus) can be driven with the proper driver characteristics. This signal can also function as the PME_enable function for an external source when programmable in this mode in PCINT.
$\overline{\text{MEXTPMEVENT}}$	1	IN	Active low by default but programmable, this input indicates a power management event signalled from some other card component to the PNR.

S/T/S = a sustained tri-state pin owned and driven by one and only one agent at a time. The agent that drives the S/T/S pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a S/T/S signal any sooner that one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it, and must be provided by the central resource.

2.2 DRAM Memory Bus Interface

One Control Memory and one Packet Memory bus provide the attachment to the external DRAM. Up to two arrays of 32 data bits plus potential error detection bits may be connected to each bus.

Figure 6: DRAM Memory Bus Connections

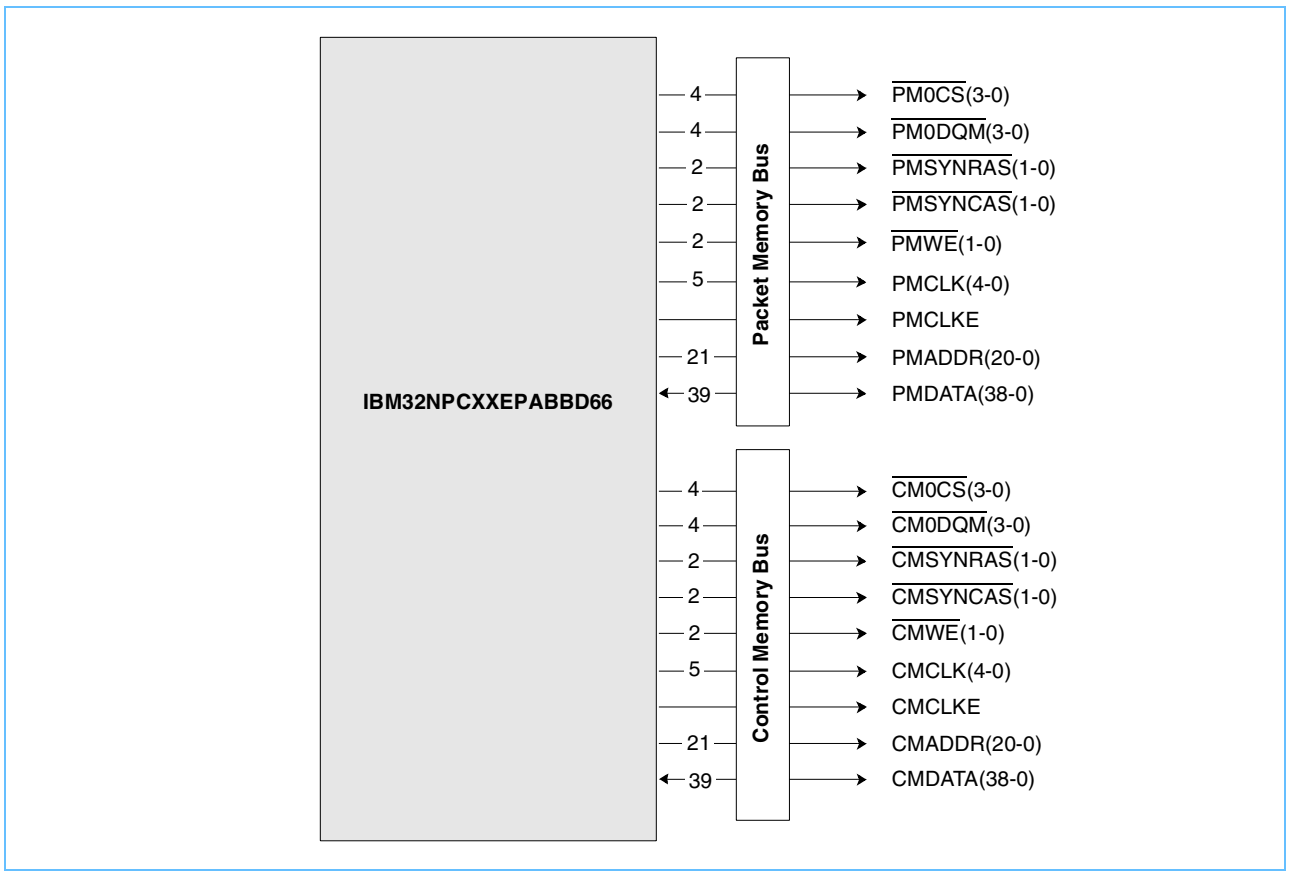


Table 4: DRAM Memory Bus Interface Signal Descriptions

Signal Name	Quantity	Type	Function	Description
PM0CS(3-0)	4	Output	Packet Memory SRAM chip selects	PM0CS(3-2) are bank address lines 1 and 0 and PM0CS(1-0) are the chip selects for the two arrays when using SDRAM for Packet Memory. When using SRAM, they are either the four chip selects or are eight-encoded chip selects and a valid signal.
CM0CS(3-0)	4	Output	Control Memory SRAM chip selects	CM0CS(3-2) are bank address lines 1 and 0 and CM0CS(1-0) are the chip selects for the two arrays when using SDRAM for Control Memory. When using SRAM, they are either the four chip selects or are eight-encoded chip selects and a valid signal.
PM0DQM(3-0)	4	Output	Packet memory DQM lines	PMDQM(3-0) are the DQM lines when using SDRAM for Packet Memory. They are identical copies of output enable when using SRAM. PMDQM(3-2) is just another copy of PMDQM(1-0) to reduce loading on the nets.
CM0DQM(3-0)	4	Output	Control memory DQM lines	CM0DQM(3-0) are the DQM lines when using SDRAM for Control Memory. They are identical copies of output enable when using SRAM. CM0DQM(3-2) is just another copy of CM0DQM(1-0) to reduce loading on the nets.
PMSYNRAS(1-0)	2	Output	RAS signal for packet synchronous DRAM	PMSYNRAS(1-0) are identical copies of the RAS signal for Packet Memory when using SDRAM. They are byte enables (3-2) when using SRAM.
CMSYNRAS(1-0)	2	Output	RAS signal for control synchronous DRAM	CMSYNRAS(1-0) are identical copies of the RAS signal for Control Memory when using SDRAM. They are byte enables (3-2) when using SRAM.
PMSYNCAS(1-0)	2	Output	CAS signal for packet synchronous DRAM	PMSYNCAS(1-0) are identical copies of the CAS signal for Packet Memory when using SDRAM. They are byte enables (1-0) when using SRAM.
CMSYNCAS(1-0)	2	Output	CAS signal for control synchronous DRAM	CMSYNCAS(1-0) are identical copies of the CAS signal for Control Memory when using SDRAM. They are byte enables (1-0) when using SRAM.
PMWE(1-0)	2	Output	Packet Memory write enable	Packet memory write enable.
CMWE(1-0)	2	Output	Control Memory write enable	Control memory write enable.
PMCLK(4-0)	5	Output	Packet Memory clock	Five identical copies of the Packet Memory clock. When wiring Packet Memory to the PNR, it should be noted that the clock skews (relative to the fastest copy of the Packet Memory clock) increase in the following order: PMCLK(0), PMCLK(1), PMCLK(2), PMCLK(3), PMCLK(4). Therefore, systems not using all the available copies of the Packet Memory clock should wire clocks to memory modules beginning with the first in this list.
PMCLKE	1	Output	Packet Memory clock enable	Clock enable for Packet Memory when using SDRAM.
CMCLK(4-0)	5	Output	Control Memory clock	Five identical copies of the Control Memory clock. When wiring Control Memory to the PNR, it should be noted that the clock skews (relative to the fastest copy of the Control Memory clock) increase in the following order: CMCLK(1), CMCLK(4), CMCLK(2), CMCLK(3), and CMCLK(0). Therefore, systems not using all the available copies of the Control Memory clock should wire clocks to memory modules beginning with the first in this list.

Table 4: DRAM Memory Bus Interface Signal Descriptions (Continued)

Signal Name	Quantity	Type	Function	Description
CMCLKE	1	Output	Control Memory clock enable	Clock enable output for Control Memory when using SDRAM.
PMADDR(20-0)	21	Output	Address signals to Packet Memory	
CMADDR(20-0)	21	Output	Address signals to Control Memory	
PMDATA(38-0)	39	Input/Output	Data signals to and from the Packet Memory	
CMDATA(38-0)	39	Input/Output	Data signals to and from the Control Memory.	

Table 5: Memory I/O Cross Reference By Device Type

PNR I/O	Sync DRAM 2-Bank Device	Sync DRAM 4-Bank Device	SRAM
xxADDR(20-0)	Address(20-0)	Address(20-0)	Address(20-0)
$\overline{\text{xxCS}}$(3)	N/A	Bank Address(1)	Chip Select(3)
$\overline{\text{xxCS}}$(2)	Bank Address(0)	Bank Address(0)	Chip Select(2)
$\overline{\text{xxCS}}$(1-0)	Chip Select(1-0)	Chip Select(1-0)	Chip Select(1-0)
$\overline{\text{xxDQM}}$(3-2)	DQM(1-0)	DQM(1-0)	OE(1-0)[1]
$\overline{\text{xxDQM}}$(1-0)	DQM(1-0)	DQM(1-0)	OE(1-0)[1]
xxCLKE	CKE	CKE	
$\overline{\text{xxWE}}$(1-0)	WE(1-0)[1]	WE(1-0)[1]	WE(1-0)[1]
$\overline{\text{xxSYNRAS}}$(1-0)	RAS(1-0)[1]	RAS(1-0)[1]	Byte Enable(3-2)
$\overline{\text{xxSYNCAS}}$(1-0)	CAS(1-0)[1]	CAS(1-0)[1]	Byte Enable(1-0)
xxDATA(31-0)	Data(31-0)	Data(31-0)	Data(31-0)
xxDATA(35-32)	ECC(3-0)	ECC(3-0)	Parity(3-0)
xxDATA(38-36)	ECC(6-4)	ECC(6-4)	N/A

1. All signal groups marked by an asterisk are active at the same time.
2. xx = CM for Control Memory or PM for Packet Memory.
3. For SDRAMs, the DQM signals are active independently for shared ECC configurations.
4. For SDRAMs with split ECC, the DQMs are usually active unless doing burst length two and the DQM is needed to terminate a burst.

Table 6: Possible Memory Configurations Using SDRAM With Shared ECC

Module Size	One Array plus ECC		Two Arrays plus ECC	
	Storage Size	Number of Devices	Storage Size	Number of Devices
1Mx16	4MB	3	8MB	5
2Mx8	8MB	5		
4Mx16	16MB	3	32MB	5
8Mx8	32MB	5		
16Mx16	64MB	3	128MB	5
32Mx8	128MB	5		

Note: While it is possible to connect more than five SDRAM modules to each controller on the PNR, it is likely the capacitive loading will not allow the interface to work at 7.5ns. The memory interface would need to be slowed down to allow the interface to work.

Table 7: Possible Memory Configurations Using SRAM (see notes 1 and 2)

Module Size	Memory Size for One Module	Memory Size for Two Modules	Memory Size for Four Modules
2Mx18	N/A	8MB	16MB
1Mx18	N/A	4MB	8MB
512Kx18	N/A	2MB	4MB
256Kx18	N/A	1MB	2MB
1Mx36	4MB	8MB	16MB
512Kx36	2MB	4MB	8MB
256Kx36	1MB	2MB	4MB
128Kx36	N/A	1MB	2MB

1. For x18 SRAM modules, half the data bus goes to one module, and the other half goes to a second module. The chip select to the two modules is common. Therefore, two x18 modules can be connected to a single chip select while only one x32 module can. Therefore, given a constant number of chip selects, using pairs of x18 “x” Mb modules results in a memory that is twice as deep as what is possible with x32 modules. Using x18 modules also lowers the overall capacitance on the memory data nets.
2. While it is possible with the number of chip selects available (multiplexed or not) to connect more than four SRAM modules to each controller on the PNR, it is likely the capacitive loading will not allow the interface to work at 7.5ns. The memory interface would need to be slowed down to allow the interface to work.

2.3 NPBUS Interface

The NPBUS supports access to either an EPROM or PHY level hardware microprocessor interface. The NPBUS can operate with an eight-bit multiplexed addr/data bus or an eight-bit data bus with 18 separate address pins. Generic transfer control signals work with the PHY level hardware microprocessor interface or EPROM to accomplish data transfers.

Figure 7: NPBUS Connections

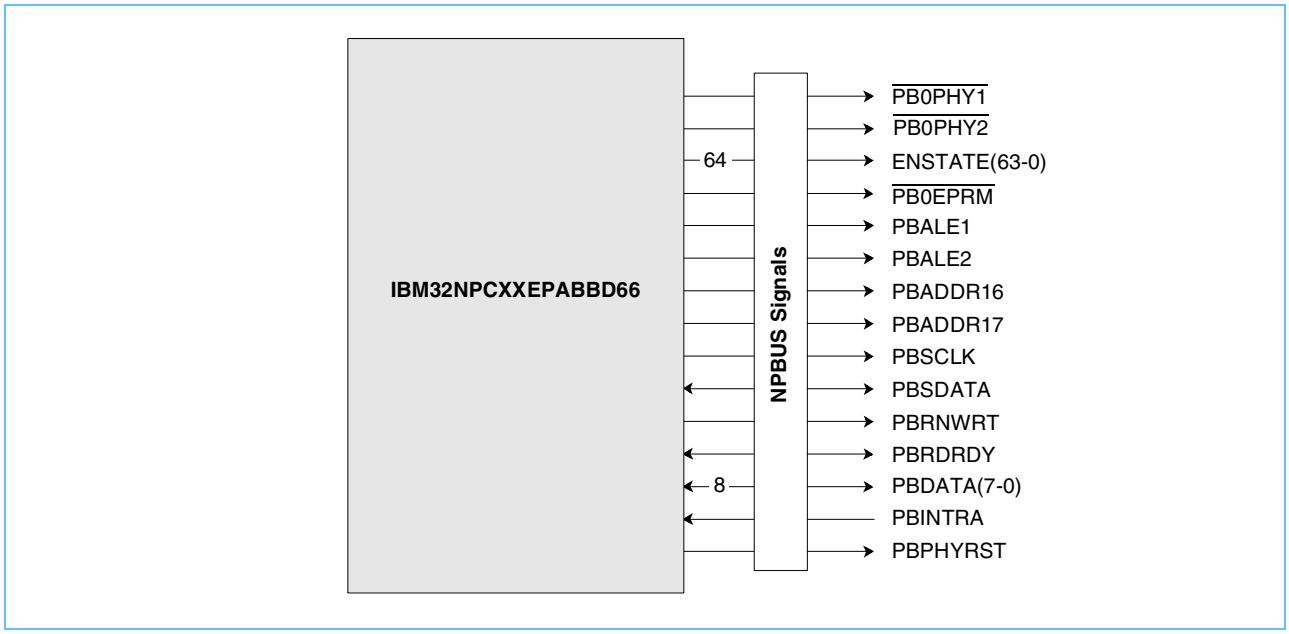


Table 8: NPBUS Signal Descriptions

Signal Name	Quantity	Type	Function	Description
$\overline{\text{PB0PHY1}}$	1	Output	Select PHY 1	When low, indicates that the PNR has selected PHY 1 to write to control registers inside PHY 1 or to read either the control or status registers.
$\overline{\text{PB0PHY2}}$	1	Output	Select PHY 2	When low, indicates that the PNR has selected PHY 2 to write to control registers inside PHY 2 or to read either the control or status registers. See *3.16.1: NPBUS Control Register* on page 387 for more details. If configured, this pin can also be odd parity across the eight-bit wide bidirectional data bus. It can also be configured as MPMDSEL: this control pin, under register bit control, can drive a logical value out. The intention is to select between the different PMD types on the 155 Mb/s copper card (UTP verses STP). If it is in cascade mode, this bit functions as PIDSELO (+idsel out), which the primary PNR will drive to the secondary PNR when trying to update configuration space via configuration cycles. This multi-plexed pin also carries the PBDATAP signal.
ENSTATE (63-0)	64	Output		When programmed, drives out the real-time state-of-entity state machines, counters, etc. for debug purposes. The (47-32) bits of this bus are also PBADDR(15-0), which are the address lines for the external parallel EPROM or PHY. Additionally, bits 47-40 can be used as bi-directional data bus bits to extend the PBDATA bus by providing bits 15-8 of this bus. This allows operation with PHY parts that have a fixed 16-bit data but limits the addressing to this PHY to only eight address bits. (*LSSD test function - scanout(13 to 0) -SO -BDY*)
$\overline{\text{PB0EPRM}}$	1	Output	EPROM Select	When low, indicates that the PNR has selected the external EPROM to read from. After reset, the PNR will start accessing the optional on-card ROM/EPROM and do the chip initialization func-tion if it does not find a serial EPROM attached.
PBALE1	1	Output	Address Latch Enable 1	When high, indicates that the PNR has generated an address on the PBDATA bus and should be latched by either a PHY that sup-ports this muxing or an external octal latch TTL part. For an exter-nal EPROM, it will also latch bits 7-0 of the address for an external EPROM access.
PBALE2	1	Output	Address Latch Enable 2	When high, indicates that the PNR has generated an address on the PBDATA bus and should be latched by an external octal latch TTL part that holds bits 15-8 of the address for an external EPROM or PHY access.
PBADDR16	1	Output	Address Send 16	Supplies address 16 to an external EPROM. The pin will also func-tion as PBALE3, an address latch enable, that indicates that the PNR has generated an address on the PBDATA bus and should be latched by an external octal latch TTL part that holds bits 23-16 of the address for an external EPROM access. The mechanism used to set this mode is to put a pull-down resistor on this pin. At reset time, it will be detected and set this bit in PBALE3 mode. Otherwise it will be in PBADDR16 mode.
PBADDR17	1	Output	Address Send 17	Supplies address 17 to an external EPROM.
PBSCLK	1	Output	Clock for the I^2C serial EPROM accesses	

S/T/S = a sustained tri-state pin owned and driven by one and only one agent at a time. The agent that drives the S/T/S pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a S/T/S signal any sooner that one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it and must be provided by the central resource.

Table 8: NPBUS Signal Descriptions (Continued)

Signal Name	Quantity	Type	Function	Description
PBSDATA	1	Output or Data		This is the data bit that connects to the external serial EPROM to read from or write to. It must have a pullup resistor attached and supports the I^2C protocol. The range of supported serial EPROM is from 256 to 2 KB. After reset, the PNR will start accessing the optional on-card serial EPROM and do the chip initialization function. If this pin is pulled down (or no pullup), the PNR will assume that no serial EPROM is attached and will go try to fetch from a parallel EPROM.
PBRNWRT	1	Output	Read or Write	This pin allows the PNR to read from or write to internal registers of the PHY parts. This signal acts as the write strobe when talking to PMC-Sierra chips such as the Suni-Lite.
PBRDRDY	1	S/T/S		This pin allows the PNR to read from or write into internal registers of the PHYs by acting as a data acknowledge signal from the memory slaves. This signal acts as the read strobe when talking to PMC-Sierra chips such as the Suni-Lite.
PBDATA(7-0)	8	Input/Output		The PB-Bus is an eight-bit wide bidirectional data bus used to interface the PHYs to the PNR. When a data transfer is not happening, the lower four bits act as MLED(3-0) - four control pins that, under register bit control, can drive general status to LED devices. If no EPROM is connected to the PNR, PBDATA(7) and PBDATA(6) should have external pullup resistors placed on them.
PBINTRA	1	Input		This input from PHY A is an attention line that, when low, indicates that one or more unmasked flags are set in the status registers of PHY 1. If additional PHY parts are added, they should also dot their interrupt line onto this input.
PBPHYRST	1	Output	Implements the network safety features of the device	This signal implements the network safety features of the PNR. It is the ORed value of RESET and all of the status bits cause the PNR to stop transferring data. It is asserted for a pulse, and then removed. This signal is asserted low.

S/T/S = a sustained tri-state pin owned and driven by one and only one agent at a time. The agent that drives the S/T/S pin low must drive it high for at least one clock before letting it float. A new agent cannot start driving a S/T/S signal any sooner that one clock after the previous owner tri-states it. A pullup is required to sustain the inactive state until another agent drives it and must be provided by the central resource.

2.4 PHY Bus Interface

The PHY Bus consists of a transmit data path, receive data paths, and control signals.

Figure 8: PHY Bus Interface Connections

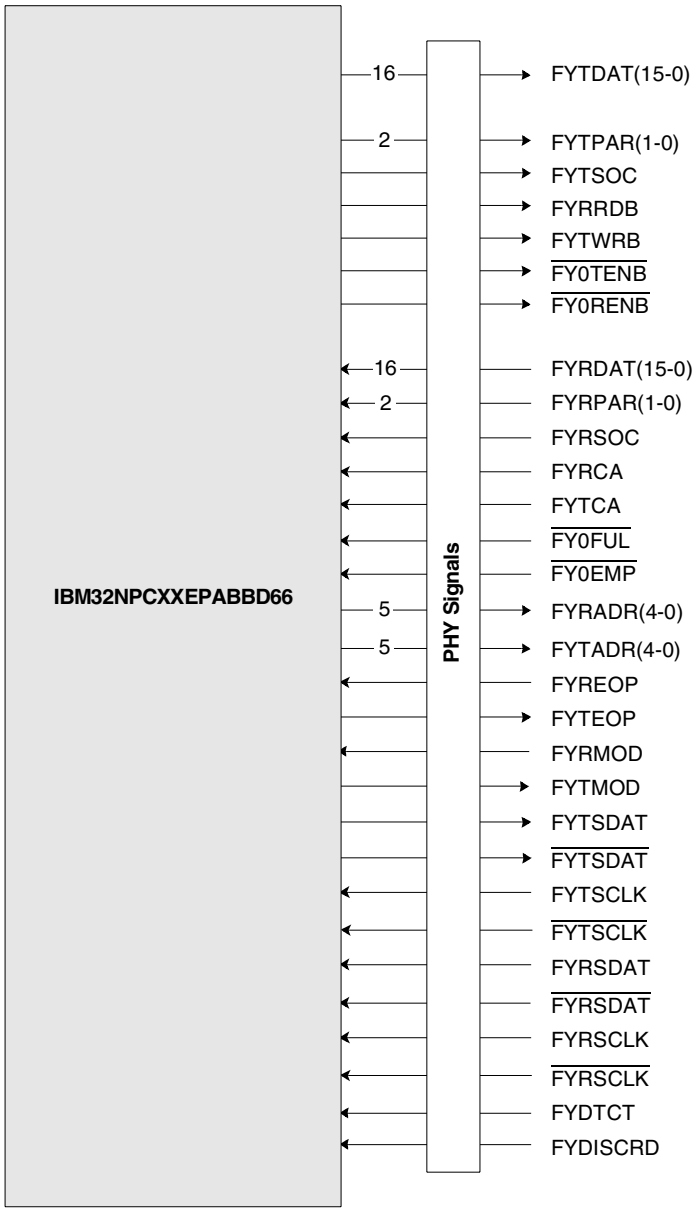


Table 9: PHY Bus Signal Descriptions (Page 1 of 3)

Signal Name	Quantity	Type	Function	Description
FYTDAT (15-0)	16	Output	PHY Transmit Data	When using an external PHY, this 16-pin bus carries the ATM CELL octets that are loaded in the PHY Transmit FIFO. When using the internal framer, bits 15, 14, and 13 are used for the RX HDLC interface signals OFPrxR1Data, OFPrxR1DS, and OFPrxRclk, respectively.
FYTPAR (1-0)	2	Output	Transmit Data Parity	When using an external PHY, these are byte parity signals for FYTDAT. When using the internal framer, bit 1 provides the RX Out-Of-Frame indication, OOF, and bit 0 provides the optical/electrical module transmit shutdown control signal, OFPtxSDown. When using a POS-PHY, bit zero provides the TERR signal.
FYTSOC	1	Output	Transmit start of Cell	When using an external PHY, this indicates the start of cell on FYTDAT. When using the internal framer, this provides the TX HDLC interface signal, OFPtxT1Dclk. When using a POS-PHY, this indicates TSOP.
FYTWRB	1	Output	Transmit write strobe	When using an external PHY, this signal is used to write ATM cells to the transmit FIFO. When using the internal framer, this signal provides the 19.44MHz TX clock, RefClkT. When using a Utopia Cell or POS-PHY interface, this signal provides the write clock based on the clock received on the TXCLK pin.
$\overline{\text{FY0TENB}}$	1	Output	Transmit write enable	When using an external PHY, this indicates that transmit data to the PHY is valid. When using the internal framer, this provides the TX HDLC interface signal, OFPtxT1DS.
$\overline{\text{FY0RENB}}$	1	Output	Receive write enable	When using an external PHY, this indicates to the PHY that the PNR is ready to accept data. When using the internal framer, this provides the clock recovery reset signal, RSTCRec1.
FYRRDB	1	Output	Receive ready strobe	When using an external PHY, this is used to read ATM cells from the PHY receive FIFO. When using the internal framer, this signal provides the 19.44MHz RX clock, RxByClk. When using a Utopia Cell or POS-PHY interface, this signal provides the write clock based on the clock received on the RXCLK pin.
FYRDAT(15-0)	16	Input	PHY Receive Data	When using an external PHY, this 16-pin bus carries the ATM CELL octets that are read from the PHY Receive FIFO.
FYRPAR(1-0)	2	Input	PHY Receive Data Parity	When using an external PHY, these are byte parity signals for FYRDAT. When using the internal framer, bit 1 provides the optical/electrical module low power indication signal, OFPtxLPow, and bit 0 is not used. When using a POS-PHY, bit 0 should be connected to RERR.
FYRSOC	1	Input	Receive start of Cell	When using an external PHY, this signal indicates the start of cell on the FYRDAT bus.
FYRCA	1	Input	Receive Cell Available	When using an external PHY, this indicates that a cell is available in the receive FIFO. When using an internal framer, this signal is not used. When using a POS-PHY, this signal must be connected to PRPA.

Note: Because some of the PHY transmit I/Os are used for receive framer functions and vice versa, there are some restrictions on how the interfaces can be used.

1. If the transmit path is using an external PHY and the receive path is using the internal framer, FYTPAR(1) will provide Out of Frame (OOF) status to the framer and will not be available as a parity output. This is only a concern if the PHY uses a 16-bit data interface and parity is being used.
2. If the receive path is using an external PHY and the transmit path is using the internal framer, FYRPAR(1) will provide OFPtxLPow status to the framer and will not be available as a parity input. This is only a concern if the PHY uses a 16-bit data interface.

If the transmit path is using an external PHY and the receive path is using the internal framer, and the external PHY has a 16-bit data interface, then the receive HDLC interface cannot be used. The three I/O for the RX HDLC interface will instead take on the function of FYTDAT(15-13).

Table 9: PHY Bus Signal Descriptions (Page 2 of 3)

Signal Name	Quantity	Type	Function	Description
FYTCA	1	Input	Transmit Cell Available	When using an external PHY, this indicates that room for a cell is available in the PHY transmit FIFO. When using the internal framer, this provides the TX HDLC interface signal, OFPtxT1Data. When interfacing to POS-PHY, this signal should be connected to PTPA.
$\overline{\text{FY0FUL}}$	1	Input	PHY Transmit Full	When using an external PHY, this is asserted low by the PHY when it can accept no more than four more data transfers before it is full. This pin should be pulled up to the inactive state when using a PHY that does not drive it. When using the internal framer, this provides the TX HDLC interface signal, OFPtxT1DFrm. When using a POS-PHY interface, this signal must be connected to STPA
$\overline{\text{FY0EMP}}$	1	Input	PHY Receive Empty	When using an external PHY, this is asserted low by the PHY to indicate that in the current cycle there is no valid data for delivery to the PNR. When the PHY does not drive $\overline{\text{FY0EMP}}$, this input should be tied to the inactive state. When using the internal framer, this signal is not used. When using a POS-PHY interface, this signal is connected to RVAL.
FYRADR(4-0)	5	Output	PHY Receive Address	When using an external PHY (Cell or POS-PHY based), this address is used to select and poll up to 31 PHYs on the receive side. Bits (1-0) are used to select which of the four PHYs and bit two is used to indicate the null address. When bit two is B'1', bits 1-0 are also '1'. When bit 2 is '0', bits 1-0 are '00', '01', '10', or '11'.
FYTADR(4-0)	5	Output	PHY Transmit Address	When using an external PHY (Cell or POS-PHY based), this address is used to select and poll up to 31 PHYs on the transmit side. Bits (1-0) are used to select which of the four PHYs and bit two is used to indicate the null address. When bit two is '1', bits 1-0 are also '1'. When bit 2 is '0', bits 1-0 are '00', '01', '10', or '11'.
FYREOP	1	Input	PHY Receive EOP	When using an external POS-PHY, this signal indicates if the FYRDATA (15-0) contains the last data of a packet. If the external PHY is not a POS-PHY, this signal should be tied to GND.
FYTEOP	1	Output	PHY Transmit EOP	When using an external POS-PHY, this signal indicates if the FYTDATA (15-0) contains the last data of a packet. If the external PHY is not a POS-PHY, this signal should ignored.
FYRMOD	1	Input	PHY Receive MOD	When using an external POS-PHY, this signal indicates if the FYRDATA (7-0) contains valid data. If FYRMOD is '1', FYRDATA(7-0) is ignored. FYRMOD is only relevant when FYREOP is '1'. A value of '1' any other time will be ignored. If a POS-PHY is not connected, this signal should be tied to GND.
FYTMOD	1	Output	PHY Transmit MOD	When using an external POS-PHY, this signal indicates if the FYTDATA (7-0) contains valid data. If FYTMOD is '1', FYRDATA(7-0) will be ignored. FYTMOD is only driven to a '1' when FYTEOP is '1'.

Note: Because some of the PHY transmit I/Os are used for receive framer functions and vice versa, there are some restrictions on how the interfaces can be used.

1. If the transmit path is using an external PHY and the receive path is using the internal framer, FYTPAR(1) will provide Out of Frame (OOF) status to the framer and will not be available as a parity output. This is only a concern if the PHY uses a 16-bit data interface and parity is being used.
2. If the receive path is using an external PHY and the transmit path is using the internal framer, FYRPAR(1) will provide OFPtxLPow status to the framer and will not be available as a parity input. This is only a concern if the PHY uses a 16-bit data interface.

If the transmit path is using an external PHY and the receive path is using the internal framer, and the external PHY has a 16-bit data interface, then the receive HDLC interface cannot be used. The three I/O for the RX HDLC interface will instead take on the function of FYTDAT(15-13).

Table 9: PHY Bus Signal Descriptions (Page 3 of 3)

Signal Name	Quantity	Type	Function	Description
FYTSDAT	1	Output	SERDES Transmit Data (Differential Pair)	When using the internal framer and the internal SERDES, these signals provide the serial transmit data stream.
$\overline{\text{FYTSDAT}}$	1			
FYTSCLK	1	Input	SERDES Transmit Clock (Differential Pair)	When using the internal framer and the internal SERDES, the reference 155.52MHz clock is supplied on these signals. When not in use, pull FYTSCLKP low and pull FYTSCLKN high.
$\overline{\text{FYTSCLK}}$	1			
FYRSDAT	1	Input	SERDES Receive Data (Differential Pair)	When using the internal framer and the internal SERDES, the recovered receive data is supplied on these signals. When not in use, pull FYRSDATP low and pull FYRSDATN high.
$\overline{\text{FYRSDAT}}$	1			
FYRSCLK	1	Input	SERDES Receive Clock (Differential Pair)	When using the internal framer and the internal SERDES, the recovered 155.52MHz clock is supplied on these signals. When not in use, pull FYRSCLKP low and pull FYRSCLKN high.
$\overline{\text{FYRSCLK}}$	1			
FYDTCT	1	Input	PHY Carrier Detect	When using an external PHY, the PHY uses this signal to indicate carrier detect. When using the internal framer, this signal provides the deserializer lock detect signal, ELockDet, from the deserializer.
FYDISCRD	1	Input	PHY Cell Discard	When using an external PHY, this signal causes the current cell being received to be discarded. In this case it should only be asserted for the duration of one of the 53 bytes of the ATM cell. When using the internal framer, this signal provides the optical/electrical module Loss-Of-Signal indication, LossSig.

Note: Because some of the PHY transmit I/Os are used for receive framer functions and vice versa, there are some restrictions on how the interfaces can be used.

1. If the transmit path is using an external PHY and the receive path is using the internal framer, FYTPAR(1) will provide Out of Frame (OOF) status to the framer and will not be available as a parity output. This is only a concern if the PHY uses a 16-bit data interface and parity is being used.
2. If the receive path is using an external PHY and the transmit path is using the internal framer, FYRPAR(1) will provide OFPtxLPow status to the framer and will not be available as a parity input. This is only a concern if the PHY uses a 16-bit data interface.

If the transmit path is using an external PHY and the receive path is using the internal framer, and the external PHY has a 16-bit data interface, then the receive HDLC interface cannot be used. The three I/O for the RX HDLC interface will instead take on the function of FYTDAT(15-13).

Table 10: Transmit PHY I/O Cross Reference

PNR I/O	Suni-Lite	Utopia	POS-PHY	Internal Framer
FYTWRB	TFCLK	TxCLK	TFCLK	RefClkT
FYTCA	TCA	TxClav	PTPA	OFPtxT1Data
$\overline{\text{FY0FUL}}$	N/A	$\overline{\text{TxFull}}$	STPA	OFPtxT1DFrm
$\overline{\text{FY0TENB}}$	$\overline{\text{TWRENB}}$	$\overline{\text{TxEnb}}$	$\overline{\text{TEnb}}$	OFPtxT1DS
FYTSOC	TSOC	TxSOC	TSOP	OFPtxT1Dclk
FYTDAT(15)	N/A	TxData(15)	TData(15)	OFPrxR1Data
FYTDAT(14)	N/A	TxData(14)	TData(14)	OFPrxR1DS
FYTDAT(13)	N/A	TxData(13)	TData(13)	OFPrxR1Dclk
FYTDAT(12-8)	N/A	TxData(12-8)	TData(12-8)	N/A
FYTDAT(7-0)	TDAT(7-0)	TxData(7-0)	TData(7-0)	TxExtDat(7-0)
FYTPAR(1)	N/A	TxPrty(1)	TPRTY	OOF
FYTPAR(0)	N/A	TxPrty(0)	TERR	OFPtxSDown
FYTADR(4-0)	N/A	TxADDR(4-0)	TADR(4-0)	N/A
FYTMOD	N/A	N/A	TMOD	N/A
FYTEOP	N/A	N/A	TEOP	N/A
FYTDAT	N/A	N/A	N/A	TSDAT
$\overline{\text{FYTDAT}}$	N/A	N/A	N/A	$\overline{\text{TSDAT}}$
FYTCLK	N/A	N/A	N/A	TSCLK
$\overline{\text{FYTCLK}}$	N/A	N/A	N/A	$\overline{\text{TSCLK}}$

Note: Signals marked with an overbar are active low. Inputs listed as N/A should be tied to their inactive Utopia state.

Table 11: Receive PHY I/O Cross Reference

PNR I/O	Suni-Lite	Utopia	POS-PHY	Internal Framer
FYRRDB	RFCLK	RxCLK	RFClk	RxByClk
FYRCA	RCA	RxClav	PRPA	N/A
$\overline{\text{FY0EMP}}$	N/A	$\overline{\text{RxEmpty}}$	RVAL	N/A
$\overline{\text{FYRENB}}$	$\overline{\text{RRDENB}}$	$\overline{\text{RxEnb}}$	$\overline{\text{RENB}}$	RSTCRec1
FYRSOC	RSOC	RxSOC	RSOP	N/A
FYRDAT(15-8)	N/A	RxData(15-8)	RDat(15-8)	N/A
FYRDAT(7-0)	RDAT(7-0)	RxData(7-0)	RDat(7-0)	N/A
FYRPAR(1)	N/A	RxPrty(1)	RPRTY	OFPtxLPow
FYRPAR(0)	N/A	RxPrty(0)	RERR	N/A
FRYADR(4-0)	N/A	RXADDR(4-0)	RADR(4-0)	N/A
FYRMOD	N/A	N/A	RMOD	N/A
FYREOP	N/A	N/A	REOP	N/A
FYRSDAT	N/A	N/A	N/A	RSDAT
$\overline{\text{FYRSDAT}}$	N/A	N/A	N/A	$\overline{\text{RSDAT}}$
FYRSCLK	N/A	N/A	N/A	RSCLK
$\overline{\text{FYRSCLK}}$	N/A	N/A	N/A	$\overline{\text{RSCLK}}$
FYDTCT	N/A	N/A	N/A	DTCT
FYDISCRD	N/A	N/A	N/A	DISCRD

Note: Signals marked with an overbar are active low. Inputs listed as N/A should be tied to their inactive Utopia state.

2.5 Clock, Configuration, and LSSD Interface

Figure 9: Clock, Configuration, and LSSD Connections

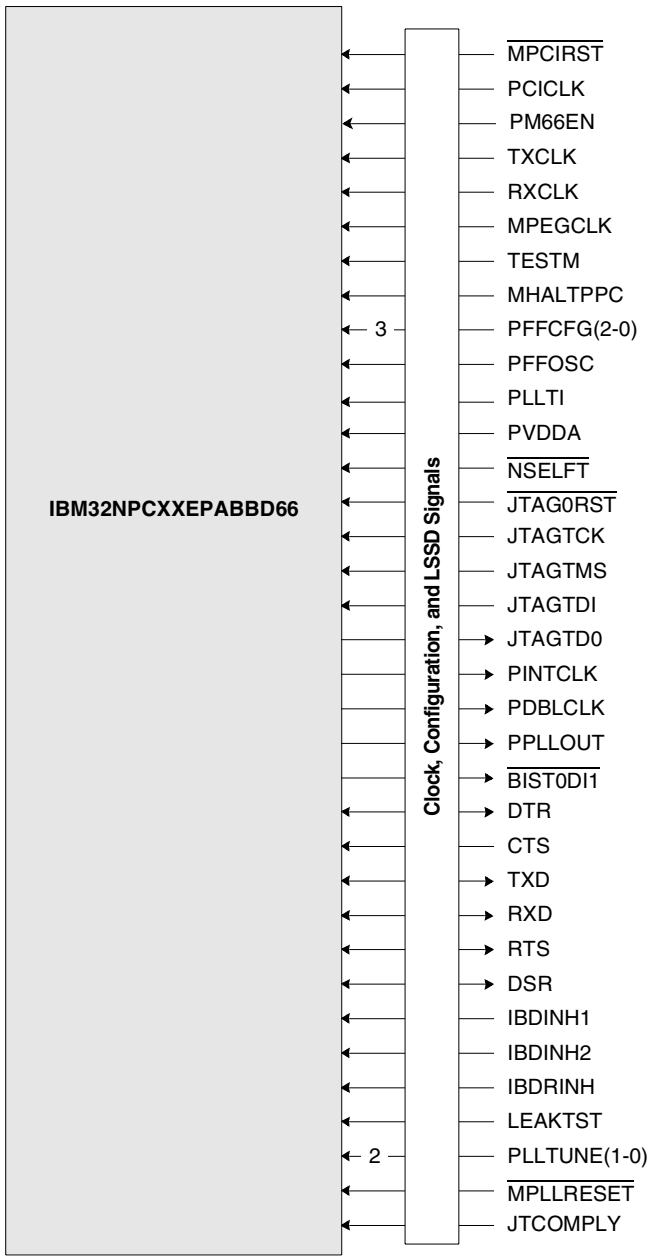


Table 12: Clock, Configuration, and LSSD Signal Descriptions

Signal Name	Quantity	Type	Description
$\overline{\text{MPCIRST}}$	1	Input	This signal causes a hardware reset when asserted low. See *3.4: Reset and Power-on Logic (CRSET/CBIST)* on page 105 for more details on resets.
PCICLK	1	Input	The PC Bus clock called CLK is a 0-66 MHz clock.
PM66EN	1	Input	This pin is high when on a PCI bus that runs at 66 MHz. It is used to tell the on-chip PLL how to generate clocks.
TXCLK	1	Input	This is the LinkC asynchronous transmit clock.
RXCLK	1	Input	This is the LinkC asynchronous receive clock. An oscillator should be connected to RXCLK even if it is not functionally used. Without the RXCLK input oscillating, the chip may not reset properly.
MPEGCLK	1	Input	This is the MPEG asynchronous clock.
TESTM	1	Input	When the test mode pin is not asserted, this chip runs as specified. When the test mode pin is asserted, the chip is in LSSD test mode. Transparent latches become clocked latches and I/Os change to primary test inputs and test outputs. This signal is asserted high when in test mode.
MHALTPPC	1	Input	Used by RISCWatch to halt the Power PC core for debug purposes. *This does not need to be in a TEST/NOSCAN I/O location*.
PFFCFG (2-0)	3	Input	These bits control the “find frequency” function which sets the range bits of the PLL. Below is the encoded meaning of these bits. 000 Reserved (Used for quicksim) 001 Disable auto range function: set range to < 25.0MHz operation 010 Disable auto range function: set range to 25.0-35.0 MHz 011 Disable auto range function: set range to 35.0 - 60.0 MHz operation 100 Enable auto range function for 19.44 MHz 101 Enable auto range function for 19.44 MHz but with internal PLL resets disabled. 110 Enable auto range function for 25.0 MHz 111 Enable auto range function for 32.0 MHz
PFFOSC	1	Input	This input is the auto range known frequency input that is used to time the PCI clock input. This should be connected to some oscillator on the card, for example, the PHY oscillator.
PLLTI	1	Input	When tied to ‘1’, this input will cause the PLL to do a parametric testing at the wafer and module level. Normal mode for this pin is ‘0’, so this pin should be pulled low or grounded.
PVDDA	1	Input	Filtered V_{DD} source to the PLL logic. See technology application notes for filter circuit.
$\overline{\text{NSELFT}}$	1	Input	Minus active SELFTEST input. Normal mode is a ‘1’.
$\overline{\text{JTAG0RST}}$	1	Input	JTAG Test Reset provides an asynchronous initialization of the TAP controller.
JTAGTCK	1	Input	JTAG Test Clock is used to clock state information and test data into and out of the device during operation of the TAP.
JTAGTMS	1	Input	JTAG Test Mode Select is used to control the state of the TAP controller in the device. (*LSSD test function - RARRYTCLKC - SC*)
JTAGTDI	1	Input	JTAG Test Data Input is used to serially shift test data and test instructions into the device during TAP operation. (*LSSD test function - CLKDIVTCLKC-SC*)
JTAGTDO	1	Output	Test Data Output is used to serially shift test data and test instructions out of the device during TAP operation. (*LSSD test function - PRSRAMABDONE and PLLLOCK output*)
PINTCLK	1	Output	This is the external test point to measure the jitter effects of the phase-lock loop circuit. *PINTCLK does not serve any LSSD or MFG test function. It does not need to be on a TEST/NOSCAN location.*
PDBLCLK	1	Output	This is the external test point that is double the frequency of the PINTCLK. It is used to clock ENSTATE state signals at this frequency. *PDBLCLK does not serve any LSSD or MFG test function. It does not need to be on a TEST/NOSCAN location.*

Table 12: Clock, Configuration, and LSSD Signal Descriptions (Continued)

Signal Name	Quantity	Type	Description
PPLLOUT	1	Output	This is an observation output only. This makes the output of the PLL observable. This is also the DTR signal when the SELRS232 is active.
$\overline{\text{BIST0DI1}}$	1	Output	Drives the DI input during BIST. Connect the BIST0DI1 output to the IBDINH1 input so the chip drivers are driven to high impedance during a chip reset or while BIST is running. Add a pullup resistor to this net.
DTR	1	Input/Output	RS232 DTR for the core debugger. (*LSSD test function - TCLKA-AC)*
CTS	1	Input	RS232 CTS for the core debugger. (*LSSD test function - LPRA bypass-TI)*
TXD	1	Input/Output	RS232 TXD for the core debugger. (*LSSD test function - CLKDIVTCLKB-BC)*
RXD	1	Input/Output	RS232 RXD for the core debugger. (*LSSD test function - BSCANTCLKB-BC)*
RTS	1	Input/Output	RS232 RTS for the core debugger. (*LSSD test function - BSCANTCLKC-SC)*
DSR	1	Input/Output	RS232 DSR for the core debugger. (*LSSD test function - pll testout)*
IBDINH1	1	Input	This is the Boundary Scan input for BSINH1. Should be connected to the BIST0DI1 output.
IBDINH2	1	Input	This is the Boundary Scan input for BSINH2(*).
IBDRINH	1	Input	This is the Boundary Scan input for rinh. This pin should be pulled up for normal operation.
LEAKTST	1	Input	This is the STI driver/receiver leak test input.
PLLTUNE(1-0)	2	Input	These inputs help tune the PLL operation. (*LSSD test function - SCANOUT(15,14))*
$\overline{\text{MPLLRESET}}$	1	Input	This input is active low and resets the PLL at power up to avoid VCO runaway. This requires a reset circuit that delays a low-to-high level after power-on-reset by 150 µs. (*LSSD test function - this pin functions as the TESTCT [Test Clock Tree] input. When not asserted, this chip runs as specified. When asserted, the clock tree uses this input to control the clokc tree outputs - TI)*
JTCOMPLY	1	Input	This input is high for JTAG compliance and low for RISCWatch/BIST-friendly use. When this pin is high, JTAG boundary scan operations may be used to test chip I/O operation and card wiring without supplying clocks to the rest of the chip. Also, when the TAP controller enters the TEST LOGIC RESET state, the JTAG instruction is IDCODE. When this pin is low, the JTAG boundary scan logic works only if the other chip clocks are running in a normal functional manner. When the TAP controller enters the TEST LOGIC RESET state, the JTAG instruction is BYPASS in order to make this more compatible with RISCWatch. (*LSSD test function - SRAM BIST result output)*

3. Register Descriptions by Entity

3.1 The IOP Bus Specific Interface Controller (PCINT)

This entity provides PCI specific interfacing between the external connection and the internal entities. It will support the following functions:

- PCI memory target
- PCI master
- Address and data latching
- Parity error detection and generation
- Configuration space registers
- 64-bit data path for master and slave operation
- 64-bit addressing support for master and slave operation
- Auto 64-bit slot detection supported
- 66 MHz PCI bus clock operation supported

3.1.1 PCI Options Taken

- Medium address decode design point
- Interrupt A will be supported, with interrupt 2 as a sideband signal
- All register accesses will be responded to as target disconnects

3.1.2 PCI Target Response

- A Target Retry is issued if a burst crosses the end of the PNR's memory space.
- A Target Abort will be issued if AD and command bus have bad parity (address phase parity error). Optionally, if $\overline{\text{SERR}}$ is enabled, it will also be returned.
- If enabled, the $\overline{\text{PERR}}$ signal will be driven on bad parity during data write cycles (data phase parity error) when the PNR is the target of the command.
- A Target Retry will be issued by the PNR if internal contention will cause a large bus access delay.

3.1.3 PCI Master Response

- A Master Abort will be issued if $\overline{\text{DEVSEL}}$ is not asserted after five clocks.
- If enabled, the $\overline{\text{PERR}}$ signal will be driven on bad parity during data read cycles (data phase parity error) when the PNR is the initiator of the command.

3.1.4 PCI Master Retry

- PNR will retry when requested by the slave.

3.1.5 PCINT Config Word 0

Identifies this device and vendor type, allocated by PCI SIG.

Length 32 bits

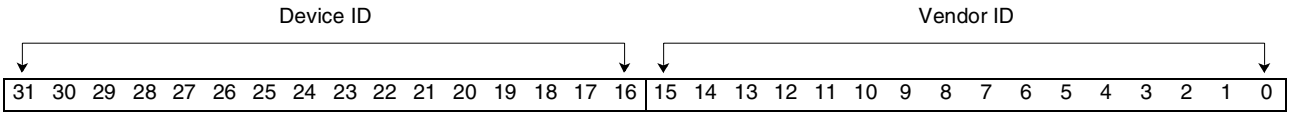
Type Read Only

Address XXXX 0000

Restrictions Can be read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.

Power On Reset Value (Big Endian) x‘00A1 1014’, but alterable at power-up/reset time with external EPROM code. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.

Power On Reset Value (Little Endian) x‘1410 A100’



Bit(s)	PCI Spec	Name	Description
31-16	15-0	Device ID	This is a unique two-byte device ID assigned to this adapter.
15-0	15-0	Vendor ID	This is a unique two-byte vendor ID.

3.1.6 PCINT Config Word 1

The Status register is used to record status information for the PCI bus related events. Writing ‘1’ to a bit in this register will reset that bit. The Command register provides coarse control over a device’s ability to generate and respond to PCI cycles. Access type of the Command register is read/write. See bit definitions.

Length 32 bits

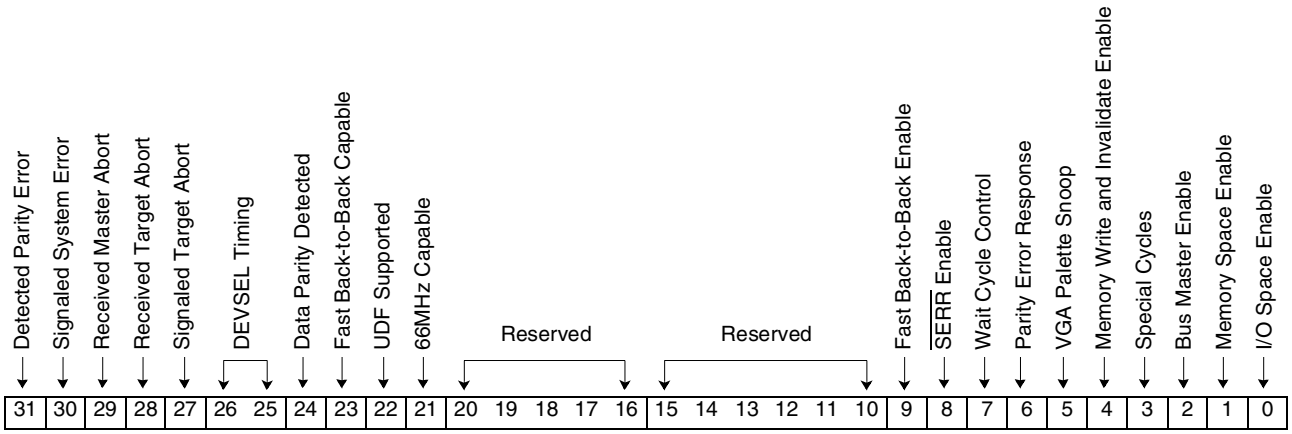
Type Read/Write and Read/Reset

Address XXXX 0004

Power On Reset Value (Big Endian) x‘02B0 0000’

Power On Reset Value (Little Endian) x‘0000 B002’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	PCI Spec	Name	Description
31	15	Detected Parity Error	This bit is set by the device whenever it detects a parity error, even if parity error handling is disabled (as controlled by bit 6 of PCINT Configuration Word 1).
30	14	Signaled System Error	This bit is set whenever the device asserts $\overline{\text{SERR}}$.
29	13	Received Master Abort	This bit is set by a master device whenever its transaction is terminated with master-abort, except for Special Cycle.
28	12	Received Target Abort	This bit is set by a master device whenever its transaction is terminated with target-abort.
27	11	Signaled Target Abort	This bit is set by a target device whenever its transaction is terminated with target-abort.
26-25	10-9	DEVSEL Timing	These bits are hard-wired to ‘01’, assuming medium address decode.

Bit(s)	PCI Spec	Name	Description
24	8	Data Parity Detected	This bit is implemented by this bus master. It is set when this agent asserts $\overline{\text{PERR}}$ or observeS $\overline{\text{PERR}}$ asserted, and this agent setting the bit acted as the bus master for the operation in which the error occurred, and bit 6 of PCINT Configuration Word 1 is set.
23	7	Fast Back-to-Back Capable	Defaults to '1' unless by external EPROM code. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
22	6	Reserved	Defaults to '0' unless set by external EPROM. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
21	5	66MHz Capable	Defaults to '1' unless set by external EPROM. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
20	4	Capabilities List	This bit on indicates that this device implements the pointer for a New Capabilities linked list at the offset 34th. See the PCI spec revision 2.2 for more details on New Capabilities. Defaults to '1' unless set by external EPROM code. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
19-16	3-0	Reserved	Reserved.
15-10	15-10	Reserved	Reserved.
9	9	Fast Back-to-Back Enable	This bit can be set to a value, but is ignored by this DMA master since it never drives these types of cycles. This slave, as indicated by bit 23, however, can handle fast back-to- back addresses to it. Initialization software will set this bit if all targets are fast back-to-back capable.
8	8	$\overline{\text{SERR}}$ Enable	If this bit is '1', the $\overline{\text{SERR}}$ driver is enabled.
7	7	Wait Cycle Control	This bit is hard-wired to '0' because stepping is not supported by this master.
6	6	Parity Error Response	When this bit is '1', normal action is taken when a parity error is detected. When it is '0', any parity errors detected are ignored and normal operation is continued.
5	5	VGA Palette Snoop	This bit is not implemented.
4	4	Memory Write and Invalidate Enable	This bit is not implemented.
3	3	Special Cycles	This bit is set to '0', and will not monitor Special Cycle operations.
2	2	Bus Master Enable	If this bit is '1', this device will be allowed to act as a bus master.
1	1	Memory Space Enable	If this bit is '1', this device will respond to memory space accesses.
0	0	I/O Space Enable	If this bit is '1', this device will respond to I/O space accesses.

3.1.7 PCINT Config Word 2

The Class Code is used to identify the generic function for this device. The Revision ID is used to identify the level of function for this device. See bit definitions.

Length 32 bits

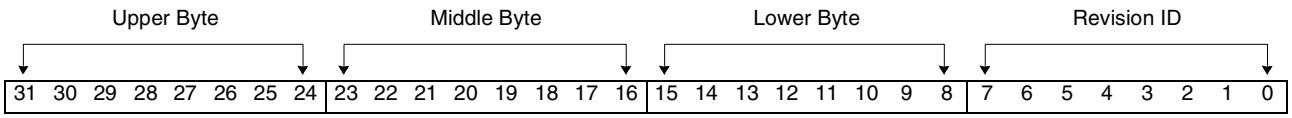
Type Read Only

Address XXXX 0008

Power On Reset Value (Big Endian) x‘0203 0026’

Power On Reset Value (Little Endian) x‘2600 0302’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	PCI Spec	Name	Description
31-24	23-16	Upper Byte	The upper byte of the Class Code is a base code that broadly classifies the type of function this device performs. Code chosen is: x‘02’ - Network controller. This register can be written to any value by external EPROM code so that it can report being an different type of function.
23-16	15-8	Middle Byte	The middle byte of the Class Code is a sub-class code that identifies more specifically the function of this device. Code chosen is: x‘03’ - ATM controller. This register can be written to any value by external EPROM code so that it can report being an different type of device.
15-8	7-0	Lower Byte	The lower byte of the Class Code identifies a specific register-level programming interface so that device independent software can interact with this device.
7-0	7-0	Revision ID	This is the revision level of this chip.

3.1.8 PCINT Config Word 3

This word specifies the system cache size in units of 32-bit words, the value of the Latency Timer for this PCI bus master, the Header Type which identifies the layout of bytes in configuration space, and the register for the control and status of BIST (built-in self-test). See bit definitions.

Length 32 bits

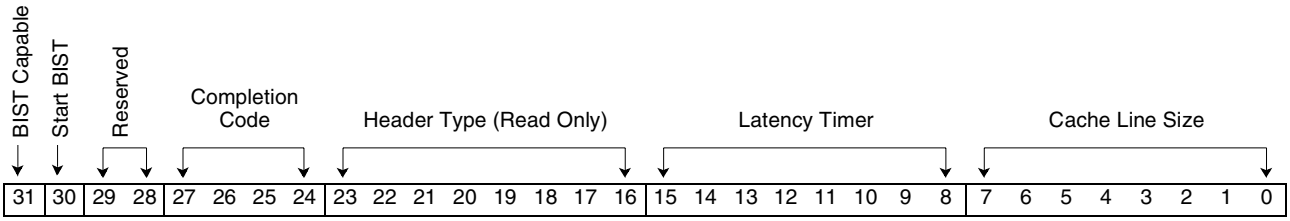
Type Read/Write

Address XXXX 000C

Power On Reset Value (Big Endian) x‘8000 0000’

Power On Reset Value (Little Endian) x‘0000 0080’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	PCI Spec	Name	Description
31	7	BIST Capable	This bit is a ‘1’ because this device supports BIST.
30	6	Start BIST	Writing this bit ‘1’ invokes BIST. This bit is reset to ‘0’ after BIST is complete. This bit has two seconds to reset after a start BIST action.
29-28	5-4	Reserved	Reserved.
27-24	3-0	Completion Code	A value of ‘0’ means this device has passed BIST. If bit 27 is on, the PRPG value failed. If bit 26 is on, the MISR value failed. Bits 25 and 24 are always ‘0’.
23-16	7-0	Header Type (Read Only)	The encoding chosen is x‘00’.
15-8	7-0	Latency Timer	This register specifies a value of latency in units of PCI bus clocks.
7-0	7-0	Cache Line Size	This register is used to best determine what read command should be used by this master. Any cache line size is supported.

3.1.9 PCINT Base Address 1 (I/O for Register)

This register specifies the base address of where in PCI I/O or memory space the PNR registers will be mapped. When written with '1's and read back, the least significant bits read back as '0' will indicate the amount of I/O space required for this device to operate. For example, when a value of x'FFFF FFFF' is written, a value read of x'FFFF FF00' indicates that 256 bytes of address space is required. See bit definitions.

The programming of this bit depends on whether the PNR is in 64-bit addressing mode or not. When in 64-bit addressing mode, bit 7 of the PCINT 64-bit Controller Register is set to '1', and this register specifies a memory address. When the PNR is not in 64-bit addressing mode because bit 7 of the PCINT 64-bit Control Register is set to '0', this register specifies an I/O address. See bit definitions and *3.1.21: PCINT 64-bit Control Register* on page 56.

Length 32 bits

Type Read/Write

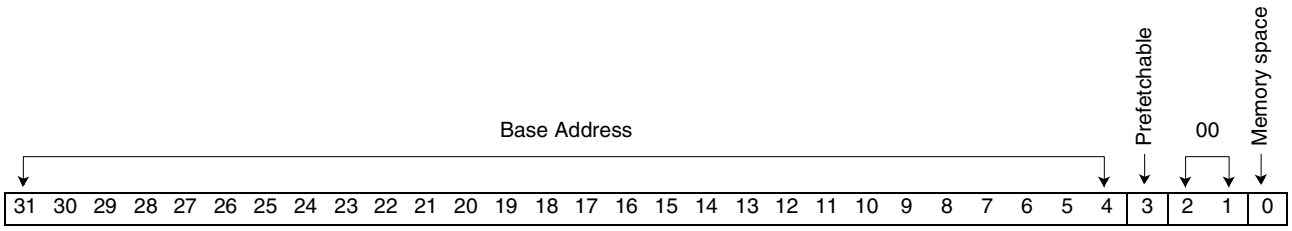
Address XXXX 0010

Power On Reset Value (Big Endian) x'0000 0001'

Power On Reset Value (Little Endian) x'0100 0000'

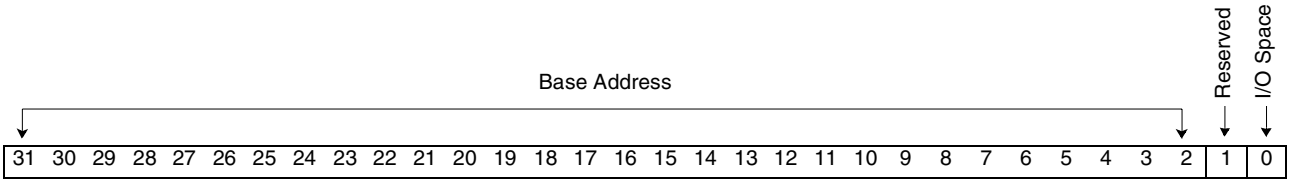
Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register. Bit 17 in the PCINT Base Address Control Register must be set to allow the PNR to decode addresses for this range.

When in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '1'):



Bit(s)	PCI Spec	Name	Description
31-4	31-4	Base Address	This register is used to hold the address where the target device will decode for memory accesses. The size is 32 KB of addressing, naturally aligned. This means that only bits 31-15 are writable.
3	3	Prefetchable	Reserved and set to '0'.
2-1	2-1	00	This base address can be mapped anywhere in 32-bit address space. The value of these bits is '00'.
0	0	Memory Space	This is memory space, so the bit is set to '0'.

When not in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '0'):



Bit(s)	PCI Spec	Name	Description
31-2	31-2	Base Address	This register is used to hold the address where the target device will decode for I/O accesses. The size is 32KB of addressing, naturally aligned. This means that only bits 31-15 are writable. The PCI specification only allows 256 bytes of I/O Base Address, so this address is only for special applications. Using the feature of non-postable writes for I/O cycles must accompany enough I/O space in the system memory map.
1	1	Reserved	Set to '0'.
0	0	I/O Space	Set to '1'.

3.1.10 PCINT Base Address 2 (Mem for Register)

This register specifies the base address of where in PCI memory space the PNR registers will be mapped. When written with '1's and read back, the least significant bits read back as '0' will indicate the amount of memory space required for this device to operate. For example, when a value of x'FFFF FFFF' is written, a value read of x'FFFF FF00' indicates that 256 bytes of address space this required. See bit definitions.

The programming of this bit depends on whether the PNR is in 64-bit addressing mode. When in 64-bit addressing mode, bit 7 of the PCINT 64 bit Controller Register is set to '1', and this register specifies a memory address. When the PNR is not in 64-bit addressing mode because bit 7 of the PCINT 64-bit Control Register is set to '0', this register specifies an I/O address. See bit definitions and *3.1.21: PCINT 64-bit Control Register* on page 56.

Length 32 bits

Type Read/Write

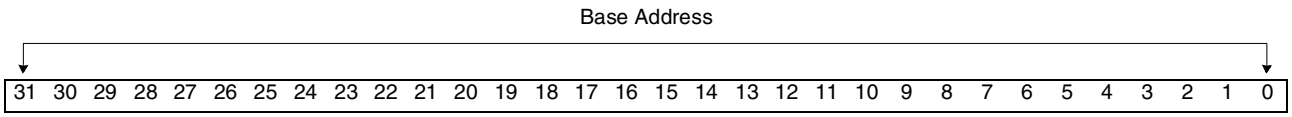
Address XXXX 0014

Power On Reset Value (Big Endian) x'0000 0000'

Power On Reset Value (Little Endian) x'0000 0000'

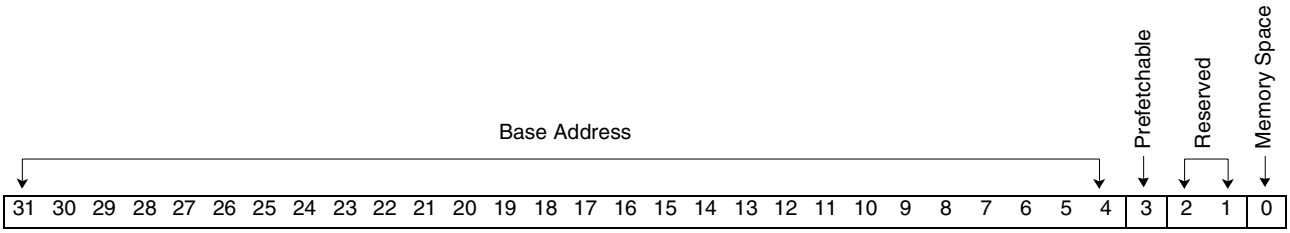
Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register. Bit 16 in the PCINT Base Address Control Register must be set to allow the PNR to decode addresses for this range.

When in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '1'):



Bit(s)	PCI Spec	Name	Description
31-0	31-0	Upper Part of Base Address	This register is used to hold the upper 32 bits of address during a 64 bit addressing dual cycle access.

When not in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '0'):



Bit(s)	PCI Spec	Name	Description
31-4	31-4	Base Address	This register is used to hold the address where the target device will decode for memory accesses. The size is 32 KB of addressing, naturally aligned. This means that only bits 31-15 are writable.
3	3	Prefetchable	This memory space is non-prefetchable, so this bit is set to '0'. This means that there are side effects on reads.
2-1	2-1	Reserved	This base address can be mapped anywhere in 32 bit address space. The value of these bits is set to '00'.
0	0	Memory Space	This is memory space, so this bit is set to '0'.

3.1.11 PCINT Base Addresses 3-6 (Memory)

This register specifies the base address of where in PCI memory space the PNR memory will be mapped. When written with '1's and read back, the least significant bits read back as '0' will indicate the amount of memory space required for this device to operate. For example, when a value of x'FFFF FFFF' is written, a value read of x'FFFF FF00' indicates that 256 bytes of address space this required. See bit definitions.

The mapping for the base address of registers into PNR's memory is one-to-one, assuming a memory windowing option is not set in the PCINT Base Addr Control Register for that base address register (BAR). Multiple BARs are only used to use a given system memory map more efficiently. As required by the BAR, the addresses are size-aligned. For example, a 16 MB size could be represented with one BAR as one 16 MB size aligned on a 16 MB boundary. However, four 4 MB BARs could represent the same 16 MB size but be aligned on any 4 MB boundary. The value in any of the BARs does not map directly to any particular PNR memory structure, such as Control Memory. The addresses are mapped using the Virtual, Packet, and Control base address registers in VIMEM.

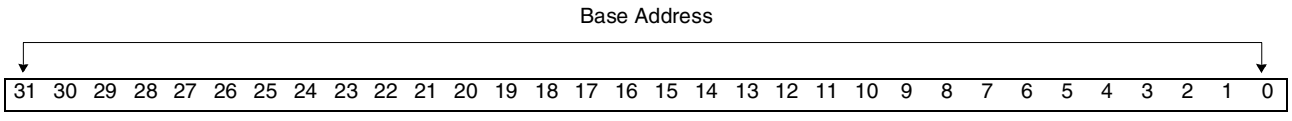
Length	32 bits	
Type	Read/Write	
Address	Reg 3	XXXX 0018
	Reg 4	XXXX 001C
	Reg 5	XXXX 0020
	Reg 6	XXXX 0024
Power On Reset Value (Big Endian)		x'0000 0008'
Power On Reset Value (Little Endian)		x'0800 0000'

Restrictions

Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.

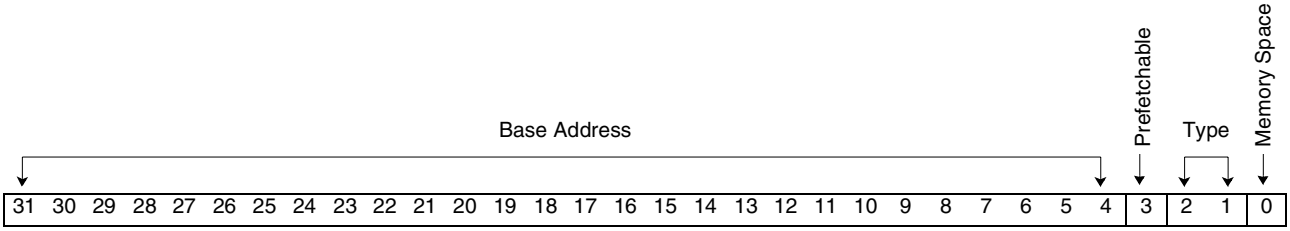
If one of these registers is not enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), then a read of that register will return all '0's. The power on value stated below assumes that the register is enabled. Normally, configuration code will just read these registers to find out what is there. To enable more that the default of registers 3 and 4, the use of external EPROM code could be used. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.

When in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '1'):



Bit(s)	PCI Spec	Name	Description
31-0	31-0	Upper Part of Base Address	This register is used to hold the upper 32 bits of address during a 64-bit addressing dual cycle access.

When not in 64-bit Addressing Mode (Bit 7 of PCINT 64-bit Control Register is set to '0'):



Bit(s)	PCI Spec	Name	Description
31-4	31-4	Base Address	This register is used to hold the address where the target device will decode for memory accesses. The size of addressing is naturally aligned and determined by what is set in the PCINT Base Address Control Register.
3	3	Prefetchable	This memory space is prefetchable, so this bit is set to a '1'. This means that there are no side effects on reads, all bytes are returned on reads regardless of byte enables, and host bridges can merge processor writes into this range without causing errors.
2-1	2-1	Type	This base address can be mapped anywhere in 32-bit address space. The value of these bits is '00'.
0	0	Memory Space	Set to '0'.

Note: These registers power up to x'0800 0000' if accessed little endian.

3.1.12 PCINT CardBus CIS Pointer

This register contains the offset to where the Card Information Structure (CIS) is located. See bit definitions.

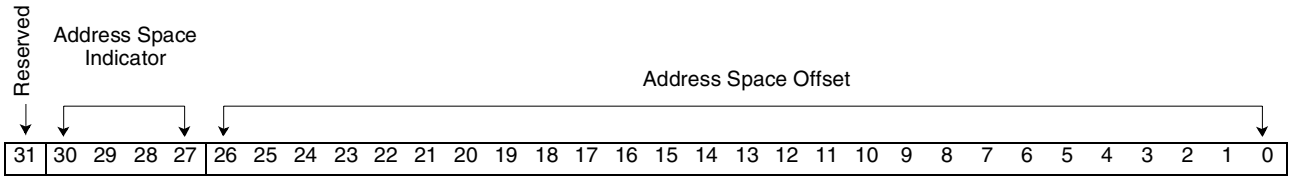
Length 32 bits

Type Read/Write

Address XXXX 0028

Power On Reset Value x‘0000 0000’

Restrictions Cannot be written unless by external EPROM, or the PCI configuration space override write bit is on. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.



Bit(s)	Name	Description
31	Reserved	Reserved.
30-27	Address Space Indicator	Can be set by external EPROM code, likely to be in expansion ROM space. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
26-0	Address Space Offset	This field has the offset into expansion ROM that is the location of the CIS. See the PCMCIA v2.10 specification for details of the CIS.

3.1.13 PCINT Subsystem ID/Vendor ID

This register contains the Subsystem ID and Subsystem Vendor ID. See bit definitions.

Other possible codes that could be returned for the Subsystem ID are listed below. The correctness of their value is superseded by higher (IOA card) levels of documentation.

Length 32 bits

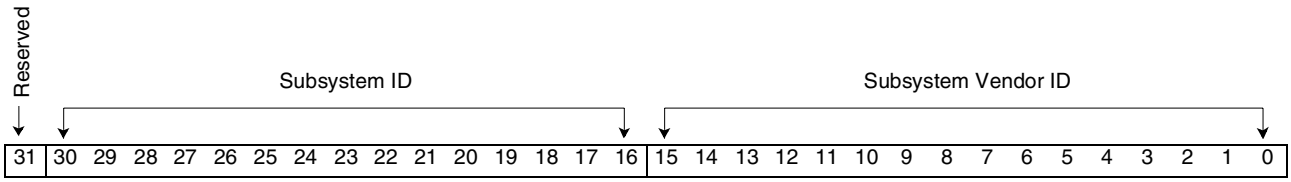
Type Read/Write

Address XXXX 002C

Power On Reset Value (Big Endian) x‘xxxx 1014’

Power On Reset Value (Little Endian) x‘1410 xxxx’

Restrictions Cannot be written unless by external EPROM, or if bit 19 of the *3.1.18: PCINT Base Address Control Register* on page 51 is on.



Bit(s)	Name	Description
31	Reserved	Reserved.
30-16	Subsystem ID	Generally will be set by external EPROM code. If not set by external EPROM, this value defaults to zero. See *3.16: Nodal Processor Bus Interface Logic (NPBUS)* on page 387 for details.
15-0	Subsystem Vendor ID	Default value is the IBM vendor ID.

3.1.14 PCINT ROM Base Address

This register specifies the base address of where in PCI memory space the PNR ROM will be mapped. When written with ‘1’s and read back, the least significant bits read back as ‘0’ will indicate the amount of memory space required for this device to operate. For example, when a value of x‘FFFF FFFF’ is written, a value read of x‘FFFF FF00’ indicates that 256 bytes of address space is required. See bit definitions.

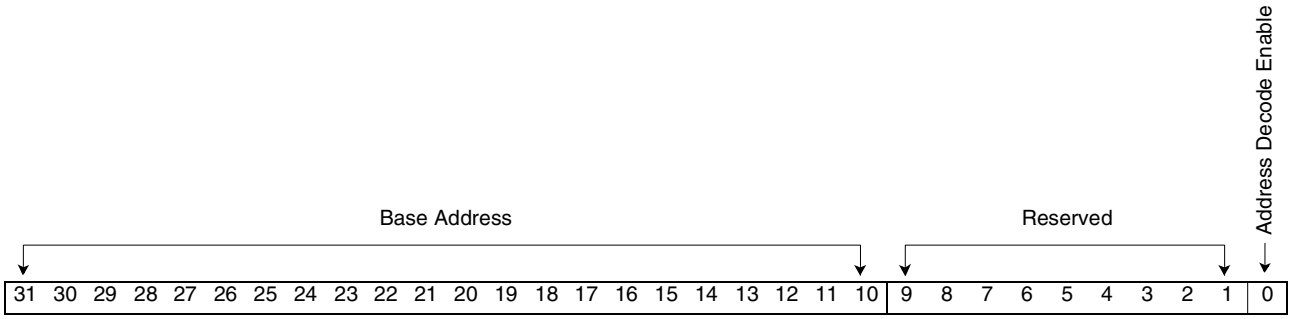
Length 32 bits

Type Read/Write

Address XXXX 0030

Power On Reset Value x‘0000 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as Big Endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	PCI Spec	Name	Description
31-10	31-11	Base Address	This register is used to hold the address where the target device will decode for expansion ROM. The size is fixed at 2 KB of addressing, naturally aligned.
9-1	10-1	Reserved	Reserved and set to ‘0’.
0	0	Address Decode Enable	This bit set to ‘1’ will enable accesses to expansion ROM only if Memory Space Enable bit (bit 1 in PCINT Configuration Word 1) is also set.

3.1.15 Capabilities Pointer

This register contains the Capabilities Pointer. See bit definitions.

Length 32 bits

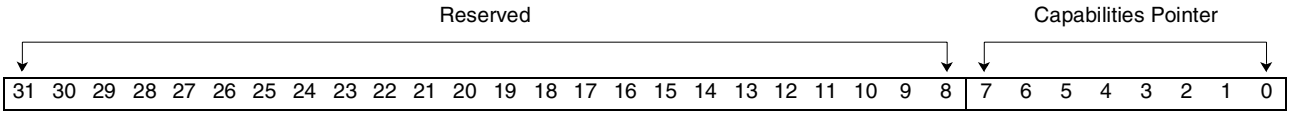
Type Read only

Address XXXX 0034

Power On Reset Value (Big Endian) x‘0000 00C0’

Power On Reset Value (Little Endian) x‘C000 0000’

Restrictions Cannot be written by external EPROM or when bit 19 of *3.1.18: PCINT Base Address Control Register* on page 51 is set.



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Capabilities Pointer	Used to point to a linked list of new capabilities implemented by this device. The register is valid only if bit 20 of *3.1.6: PCINT Config Word 1* on page 35 is set. Bits 0 and 1 are always ‘0’.

3.1.16 PCINT Config Word 15

This register is used to communicate interrupt line routing information, tell which interrupt pin this device uses, and specify the desired setting for Latency Timer values. See bit definitions.

Length 32 bits

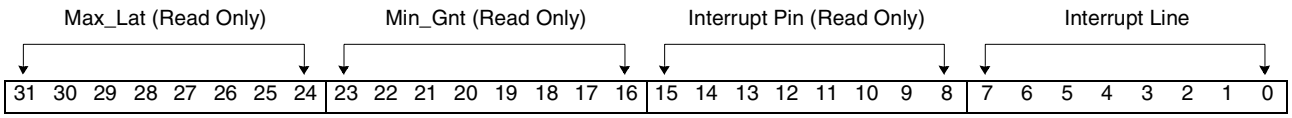
Type Read/Write

Address XXXX 003C

Power On Reset Value (Big Endian) x‘0001 0100’

Power On Reset Value (Little Endian) x‘0001 0100’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as Big Endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	PCI Spec	Name	Description
31-24	7-0	Max_Lat (Read Only)	This value specifies a period of time in units of 1/4 microsecond. Max_Lat is used for specifying how often this device needs to gain access to the PCI bus.
23-16	7-0	Min_Gnt (Read Only)	This value specifies a period of time in units of 1/4 microsecond. Min_Gnt is used for specifying how long a burst period this device needs, assuming a 33MHz clock rate.
15-8	7-0	Interrupt Pin (Read Only)	This device used $\overline{\text{INTA}}$ for its PCI bus interrupt. Value of this field is ‘01’.
7-0	7-0	Interrupt Line	Software will write the routing information into this register as it initializes and configures the system.

3.1.17 PCINT Endian Control Register

This register allows control and status to the big/little endian address selection. It controls the byte order across the PCI bus. See bit definitions.

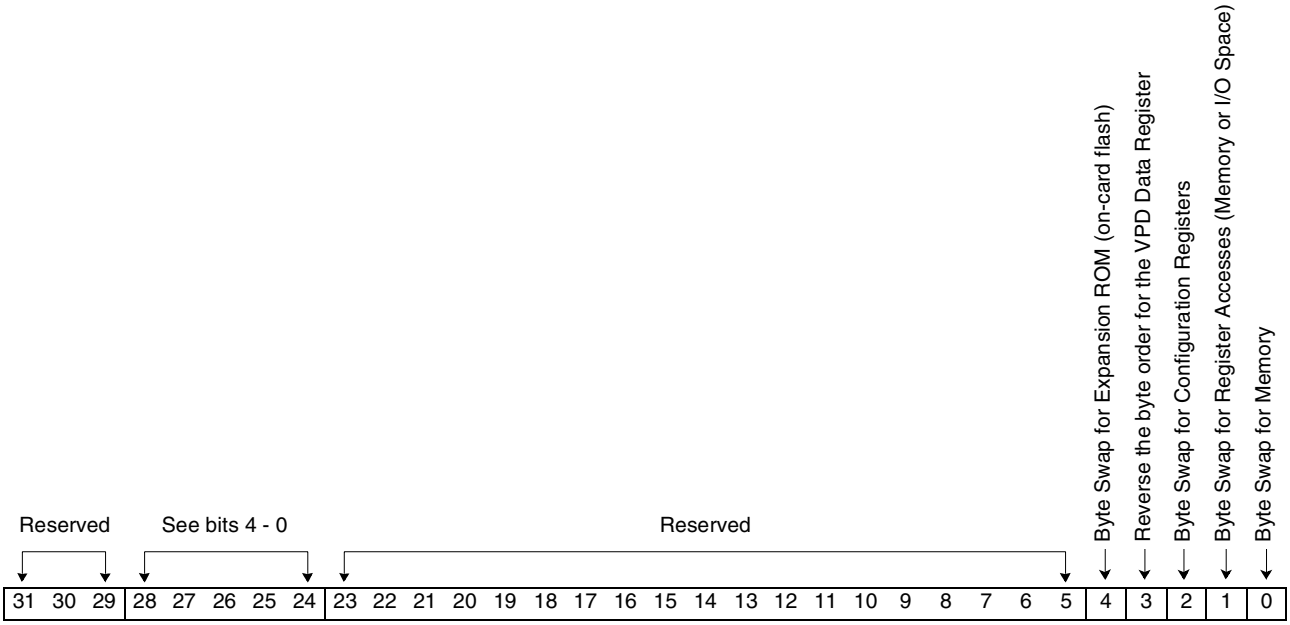
Length 32 bits

Type Read/Write

Address XXXX 0058

Power On Reset Value x‘0000 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle.



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28-24	See bits 4-0	Same as the definitions for bits 4-0.
23-5	Reserved	Reserved.
4	Byte Swap For Expansion ROM (on-card flash)	When this bit is set to ‘1’, the bytes of an internal Expansion ROM access (big endian view) will be swapped to and from the PCI interface.
3	Reverse the Byte Order for the VPD Data Register	When this bit is set to ‘1’, the bytes of the Vital Product Data Interface - Word 2 register access will be swapped in reverse order to which bits 2 or 1 are set.
2	Byte Swap for Configuration Registers	When this bit is set to ‘1’, the bytes of an internal Configuration register access (big endian view) will be swapped to and from the PCI interface.
1	Byte Swap for Register Access (Memory or I/O space)	When this bit is set to ‘1’, the bytes of an internal register access (big endian view) will be swapped to and from the PCI interface.
0	Byte Sway for Memory	When this bit is set to ‘1’, the bytes of an internal packet/control/virtual memory access (big endian view) will be swapped to which bits 2 or 1 are set.

3.1.18 PCINT Base Address Control Register

This register controls all the base address registers that map to memory. See bit definitions.

Length 32 bits

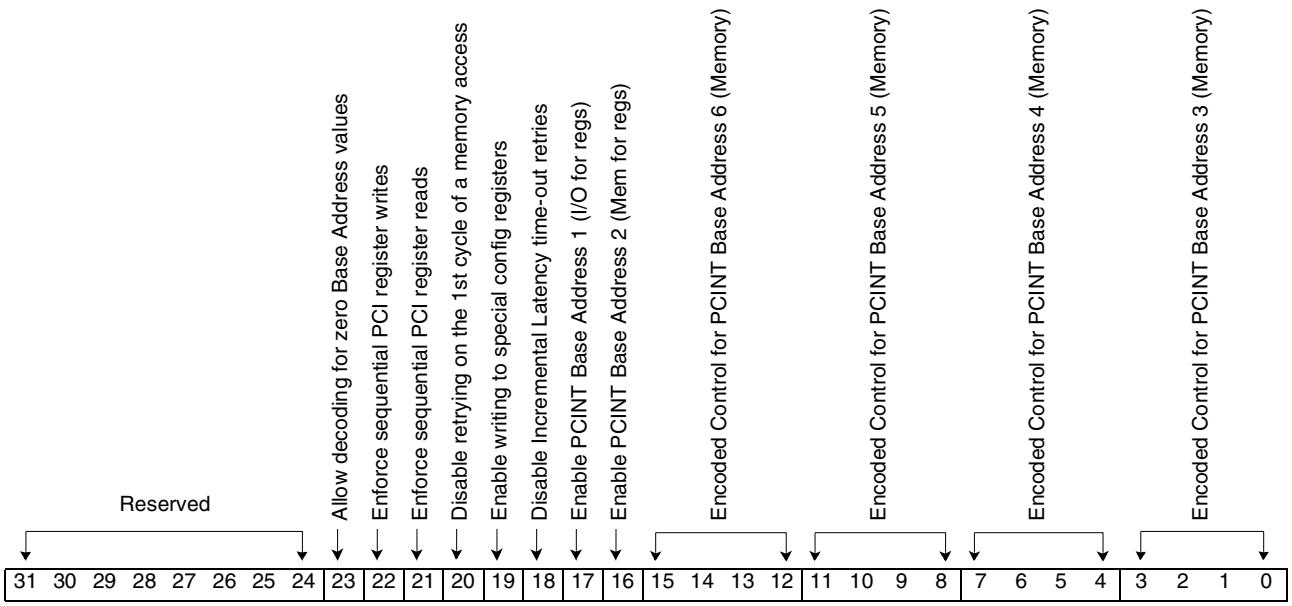
Type Read/Write

Address XXXX 005C

Power On Reset Value (Big Endian) x‘0011 000F’

Power On Reset Value (Little Endian) x‘0F00 1100’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



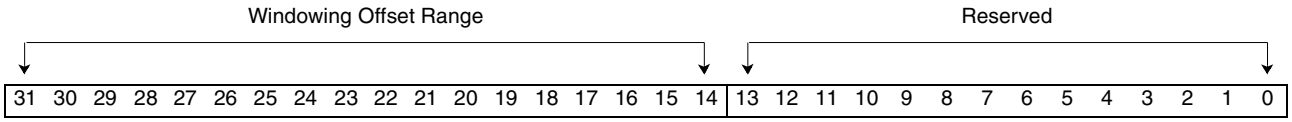
Bit(s)	Name	Description
31-24	Reserved	Reserved.
23	Allow Decoding for Zero Base Address Values	Setting this bit to ‘1’ will enables decoding of a BAR address that is set to ‘0’. Normally, the PCI specification does not allow for a zero address to be a valid decode.
22	Enforce Sequential PCI Register Writes	Setting this bit to ‘1’ ensures that PCI register writes will occur in sequential order of prior memory accesses or register reads. The cost for doing this is possible extra retry cycles for accesses not dependent on other posted accesses to complete.
21	Enforce Sequential PCI Register Reads	Setting this bit to ‘1’ ensures that PCI register reads will occur in sequential order of prior memory accesses or register writes. The cost for doing this is possible extra retry cycles for accesses not dependent on other posted accesses to complete.

Bit(s)	Name	Description
20	Disable Retrying on the 1st Cycle of a Memory Access	Setting this bit to '1' disables the retrying of a memory access to PNR. This causes a PCI spec violation, but not a data integrity problem. It solves the rare problem in which two masters are accessing Control Memory at the same time and retries happen to both endlessly.
19	Enable Writing to Special Config Registers	Setting this bit to '1' enables writing to certain registers that are normally read-only. An example of this is the vendor and function ID register (PCINT Configuration Word 0).
18	Disable Incremental Latency Time-out Retries	Setting this bit to '1' disables PCI retries due to cycles taking more than eight cycles on burst accesses after the first access.
17	Enable PCINT Base Address 1 (I/O for regs)	Setting this bit to '1' enables PCINT Base Address 1 (I/O for registers). This does the same function as bit 0 in the PCINT Configuration Word 1 register, but also makes the PCINT Base Address 1 (I/O for regs) read back '0's even when written to with values. It guards against anything that BIOS code may do to PCINT Configuration Word 1 register bit 0 if I/O accesses are not desired.
16	Enable PCINT Base Address 2 (Mem for regs)	Setting this bit to '1' enables PCINT Base Address 2 (Mem for regs) so PNR registers can be accessed by PCI memory cycles.
15-12	Encoded Control for PCINT Base Address 6 (Memory)	Same as bits 3-0.
11-8	Encoded Control for PCINT Base Address 5 (Memory)	
7-4	Encoded Control for PCINT Base Address 4 (Memory)	
3-0	Encoded Control for PCINT Base Address 3 (Memory)	Encoding of bits: x'0' Disable this Base Address. x'1' Configured to respond to a 2 GB address size. x'2' Configured to respond to a 1 GB address size. x'3' Configured to respond to a 512 MB address size. x'4' Configured to respond to a 256 MB address size. x'5' Configured to respond to a 128 MB address size. x'6' Configured to respond to a 64 MB address size. x'7' Configured to respond to a 32 MB address size. x'8' Configured to respond to a 16 MB address size. x'9' Configured to respond to a 8 MB address size. x'A' Configured to respond to a 4 MB address size. x'B' Configured to respond to a 2 MB address size. x'C' Configured to respond to a 1 MB address size. x'D' Configured to respond to a 64-KB address size, and enables internal windowing of memory. x'E' Configured to respond to a 32-KB address size, and enables internal windowing of memory. x'F' Configured to respond to a 16-KB address size, and enables internal window.

3.1.19 PCINT Window Offsets for Base Addresses 3-6

These registers specify the amount of memory space required for this device to operate. See bit definitions.

Length	32 bits	
Type	Read/Write	
Address	Reg 3	XXXX 0060
	Reg 4	XXXX 0064
	Reg 5	XXXX 0068
	Reg 6	XXXX 006C
Power On Reset Value		x‘0000 0000’
Restrictions	Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.	



Bit(s)	Name	Description
31-14	Windowing Offset Range	This register is used to hold the address offset, which is added to the PCI address (when windowing is enabled) to form the internal memory address. Bits 15 and 14 may or may not be used, depending on how bits are set in the PCINT Base Address Control Register. When bit 20 of PCINT Count Timeout Register is set, Window Offset register three can be updated with the address returned from a good get buffer from POOLS. This will save a write from code to this register. When bit 20 of PCINT Count Timeout Register is set, Window Offset register four can be updated with the address returned from a dequeue from the receive queue. This will save a write from code to this register.
13-0	Reserved	Reserved.

3.1.20 PCINT Count Timeout Register

This register holds the count limit of PCI slave retry cycles. See bit definitions.

Length 32 bits

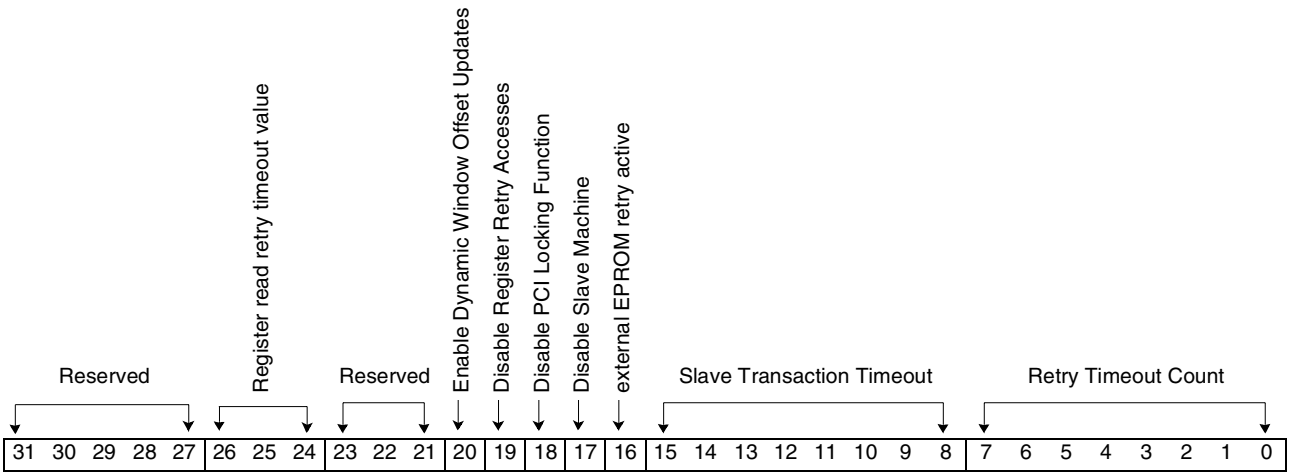
Type Read/Write

Address XXXX 0070

Power On Reset Value (Big Endian) x‘0300 FFFF’

Power On Reset Value (Little Endian) x‘FFFF 0003’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as Big Endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-27	Reserved	Reserved.
26-24	Register Read Retry Timeout Value	The bits can be set to determine how many PCI cycles a register access will wait for an internal cycle to complete for a read access. It can be programmed to wait for up to seven cycles. A value of ‘0’ will not timeout this access with a retry.
23-21	Reserved	Reserved.
20	Enable Dynamic Window Offset Updates	Setting this bit to a ‘1’ enables the PCINT Window Offsets for Base Addresses 3-4 to be updated. See *3.1.19: PCINT Window Offsets for Base Addresses 3-6* on page 53 for more information.
19	Disable Register Retry Accesses	Setting this bit to ‘1’ disables PCI retry signaling during a register or primitive access.
18	Disable PCI Locking Function	Setting this bit to ‘1’ disables this PCI locking function when set to ‘1’
17	Disable Slave Machine	This bit is for external EPROM code use. When set to ‘1’, it disables all responses to the PCI bus in slave mode. In general, never turn this bit on. Bit 19 of the PCINT Base Address Control Register must be set before this bit can be changed.

Bit(s)	Name	Description
16	Reserved	Reserved.
15-8	Slave Transaction Timeout	These bits hold a value that is used to count the number of PCI clocks times 256 when a PCI slave cycle is in progress. If the count is reached, due to some internal chip hang condition, a target abort is issued. A value of ‘0’ disables target aborts from this function.
7-0	Retry Timeout Count	These bits hold a value that is used to count the number of PCI retries. The maximum count is 256 times, 16 retries. If the count is reached, a target abort is issued. A value of ‘0’ will disable target aborts from this function.

3.1.21 PCINT 64-bit Control Register

This register contains miscellaneous control bits.

Length 32 bits

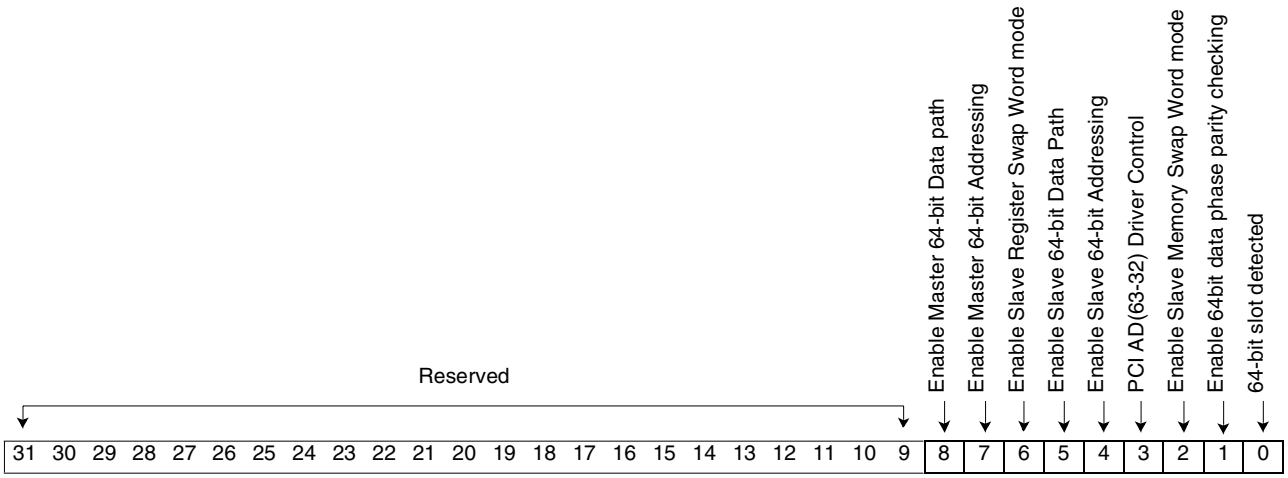
Type Read/Write

Address XXXX 0078

Power On Reset Value (Big Endian) x‘0000 0XXX’, where the ‘X’ values depend on whether bit 0 is set and values of the enable bits in PCINT 64-bit Enable Register.

Power On Reset Value (Little Endian) x‘XX0X 0000’, where the ‘X’ values depend on whether bit 0 is set and values of the enable bits in PCINT 64-bit Enable Register.

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-9	Reserved	Reserved.
8	Enable Master 64-Bit Data Path	This bit set to ‘1’ will enable master 64-bit data path for dma transfers. This does the same as bit 0 (only inverted) of the *3.1.26: PCI Master Options Control* on page 62 but with the added control of *3.1.22: PCINT 64-bit Enable Register* on page 57.
7	Enable Master 64-Bit Addressing	This bit set to ‘1’ will enable master 64-bit addressing. When this bit is set, the DMA descriptor formats changes such that an extra DWORD of addressing must be added. Also, the DMAQS enque register address changes such that x‘4’ will be subracted. (Example would be x‘06a4’ would become x‘06a0’)
6	Enable Slave Register Swap Word Mode	This bit set to ‘1’ will enable word swapping of the each of the four groups of data bytes in an eight-byte register transfer.
5	Enable Slave 64-Bit Data Path	This bit set to ‘1’ will enable the slave 64-bit data path for registers and packet/control/virtual memory.

Bit(s)	Name	Description
4	Enable Slave 64-Bit Addressing	This bit set to ‘1’ will enable slave 64-bit addressing, making base addresses 1 and 2 available for register accesses (memory cycles only) and base addresses 3 and 4 available for packet/control/virtual memory. This mode is unrelated to DMA addressing (bit 7 of this register). The base address registers (BAR) will now all be 64 bits in size. When the higher order 4 bytes of these registers are zero, that means that they will be operating in a 32-bit addressing environment.
3	PCI AD(63-32) Driver Control	This bit set to ‘1’ will cause the AD(63-32) PCI drivers to force to tri-state unless a 64-bit access is occurring. Otherwise, when set to ‘0’, the drivers will always drive active.
2	Enable Slave Memory Swap Word Mode	This bit set to ‘1’ will enable word swapping of the each of the four groups of data bytes in an eight-byte slave memory transfer through BCACH.
1	Enable 64-Bit Data Phase Parity Checking	This bit set to ‘1’ will enable the data phase parity checking on bits 32 to 63 of the AD PCI bus.
0	64-Bit Slot Detected	This bit will set when the $\overline{\text{REQ64}}$ I/O pin was low bus when $\overline{\text{RST}}$ went inactive. This bit is a read-only status bit. This bit on, combined with the status of the corresponding bit in the PCINT 64-bit Enable Register will determine the value of other bits in this register.

3.1.22 PCINT 64-bit Enable Register

See *3.1.21: PCINT 64-bit Control Register* on page 56 for the bitwise description that the corresponding bit in this register will enable (a value of ‘1’ means enabled). Any bit in this register ANDed with bit 0 of PCINT 64-bit Control Register will determine if the other bits in PCINT 64-bit Control Register are set.

Length 32 bits

Type Read/Write

Address XXXX 0088

Power On Reset Value (Big Endian) x‘0000 0008’

Power On Reset Value (Little Endian) x‘0800 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.

3.1.23 PCINT Perf Counters Control Register

This register contains control bits for the PCINT performance Counter 1 and PCINT Performance Counter 2.

Length 32 bits

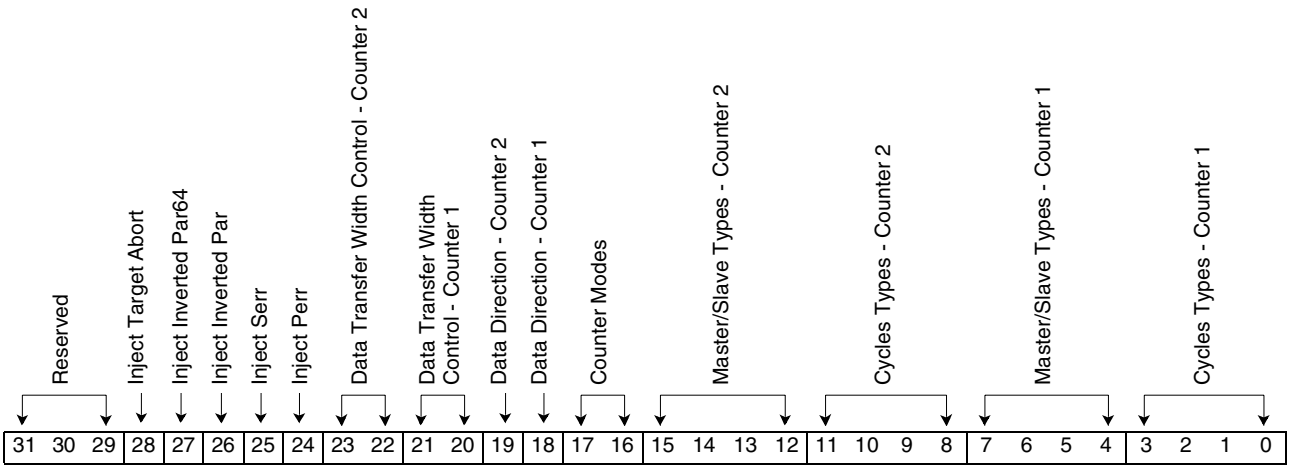
Type Read/Write

Address XXXX 007C

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28	Inject Target Abort	This bit on will make the target respond with a target abort sequence, provided all the other conditions are set correctly in this register.
27	Inject Inverted Par64	This bit on will invert the value of PCI PAR64, provided all the other conditions are set correctly in this register.
26	Inject Inverted Par	This bit on will invert the value of PCI PAR, provided all the other conditions are set correctly in this register.
25	Inject Serr	This bit on will flow a PCI $\overline{\text{Serr}}$, provided all the other conditions are set correctly in this register. Bit 8 of the PCINT Config Word 1 does not need to be set to cause this condition.
24	Inject Perr	This bit on will flow a PCI $\overline{\text{Perr}}$, provided all the other conditions are set correctly in this register. Bit 6 of the PCINT Config Word 1 does not need to be set to cause this condition.
23-22	Data Transfer Width Control - Counter 2	These bits will determine which kind of cycle to count based on the transfer size for counter 2. See bits 21-20.

Bit(s)	Name	Description
21-20	Data Transfer Width Control - Counter 1	These bits will determine which kind of cycle to count based on the transfer size for counter 1. x'0' All transfers x'1' 32 bit transfers only x'2' 64 bit transfers only x'3' Enable Data Direction (bits 18 or 19)
19	Data Direction - Counter 2	These bits will determine which kind of cycle to count based on the data direction - in or out of the PNR for counter 2.
18	Data Direction - Counter 1	These bits will determine which kind of cycle to count based on the data direction - in or out of the PNR for counter 1. x'0' Data In x'1' Data Out
17-16	Counter Modes	These bits will determine which kind of mode both counters will operate in. x'0' Stop on overflow x'1' Interrupt on wrap x'2' Event on wrap x'3' Inject active errors on overflow
15-12	Master/Slave Types - Counter 2	These bits determine which kind of PCI cycle owners to be counted for counter 2. See bits 7-4.
11-8	Cycles Types - Counter 2	These bits determine what kind of PCI events are to be counted for counter 2. See Bits 3-0.
7-4	Master/Slave Types - Counter 1	These bits determine which kind of PCI cycle owners to be counted for counter 1. x'0' All Devices on the PCI bus x'1' All Devices but PNR x'2' PNR only (master or slave) x'3' PNR master x'4' PNR slave (all types) x'5' PNR slave register accesses x'6' PNR slave memory accesses
3-0	Cycles Types - Counter 1	These bits will determine what kind of PCI events are to be counted for counter 1. x'0' Off x'1' All PCI clock cycles x'2' Active PCI bus cycles (frame + irdy + trdy) x'3' PCI Data Xfer Opportunities ((irdy + trdy) & devsel) x'4' PCI Data Xfers (irdy & trdy) x'5' PCI Retries (irdy & no trdy & devsel & stop) x'6' PCI Address Phase (frame & not frame delayed) x'7' PCI Disconnects (irdy & trdy & devsel & stop)

3.1.24 PCINT Perf Counter 1

This register contains PCI performance counter 1.

Length 32 bits

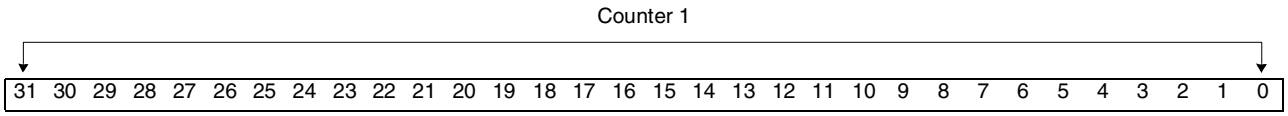
Type Read/Write

Address XXXX 0080

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-0	Counter 1	See *3.1.23: PCINT Perf Counters Control Register* on page 58 for information on how this counter will increment.

3.1.25 PCINT Perf Counter 2

This register contains PCI performance counter 2.

Length 32 bits

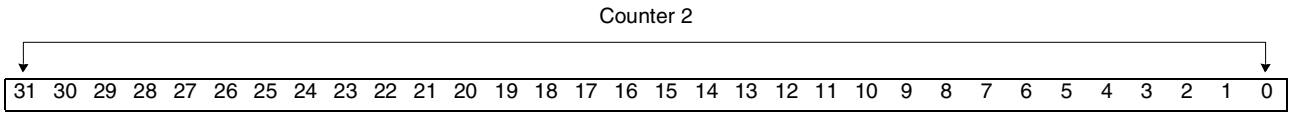
Type Read/Write

Address XXXX 0084

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions Can be written or read during configuration cycle, memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-0	Counter 2	See *3.1.23: PCINT Perf Counters Control Register* on page 58 for information on how this counter will increment.

3.1.26 PCI Master Options Control

This register contains the control register when the PNR is the PCI master.

Length 32 bits

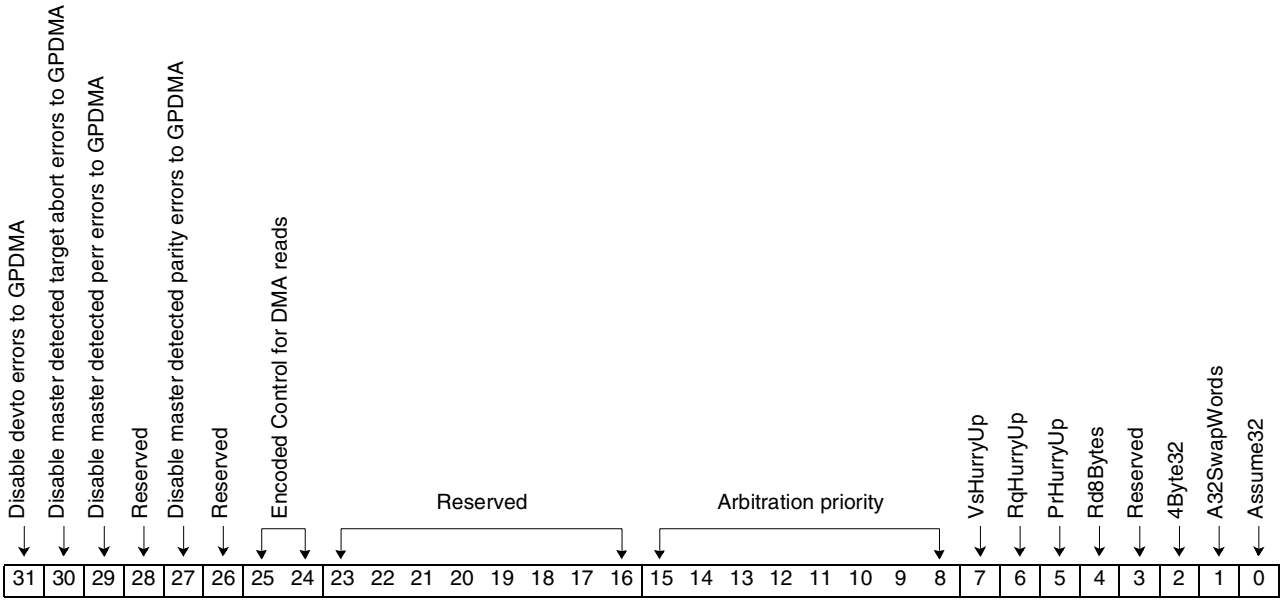
Type Read/Write

Address XXXX 008C

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31	Disable Devto Errors to GPDMA	Setting this bit to ‘1’ will disable device timeout errors from stopping a GPDMA transfer.
30	Disable Master Detected Target Abort Errors to GPDMA	Setting this bit to ‘1’ will disable master detected target abort errors from stopping a GPDMA transfer.
29	Disable Master Detected Perr Errors to GPDMA	Setting this bit to ‘1’ will disable master detected perr errors from stopping a GPDMA transfer.
28	Reserved	Reserved.
27	Disable Master Detected Parity Errors to GPDMA	Setting this bit to ‘1’ will disable master detected parity errors from stopping a GPDMA transfer
26	Reserved	Reserved.

Bit(s)	Name	Description
25-24	Encoded Control for DMA Reads	Encoding of bits: x‘0’ Let the PNR pick the best memory read command based on the cacheline size bits and the DMA count. x‘1’ Fix the read DMA command to Memory Read Multiple. x‘2’ Fix the read DMA command to Memory Read Line. x‘3’ Fix the read DMA command to Memory Read.
23-16	Reserved	Reserved.
15-8	Arbitration Priority	PCI master will cease using a default round-robin scheme for internal requestor arbitration if these bits are not all ‘0’. Bits 15-14 are the priority level for GPDMA. Bits 13-12 are the priority level for PCORE. Bits 11-10 are the priority level for RXQUE. Bits 9-8 are the priority level for INTST. Valid levels are 3, 2, 1, and 0. Only 4 levels can be used.
7	VsHurryUp	PCI master will inform GPDMA to HurryUp if VSTAT is waiting.
6	RqHurryUp	PCI master will inform GPDMA to HurryUp if RXQUE is waiting.
5	PrHurryUp	PCI master will inform GPDMA to HurryUp if PCORE is waiting.
4	Rd8Bytes	PCI master will force all byte enables active for reads.
3	Reserved	Reserved.
2	4Byte32	PCI master will transfer a four-byte DMA as a 32-bit transfer.
1	A32SwapWords	PCI master will always swap words for any Assume32 transfer.
0	Assume32	PCI master will not request a 64-bit transfer.

3.1.27 Power Management Program Control

This register contains the control register for power management signalling.

Length 32 bits

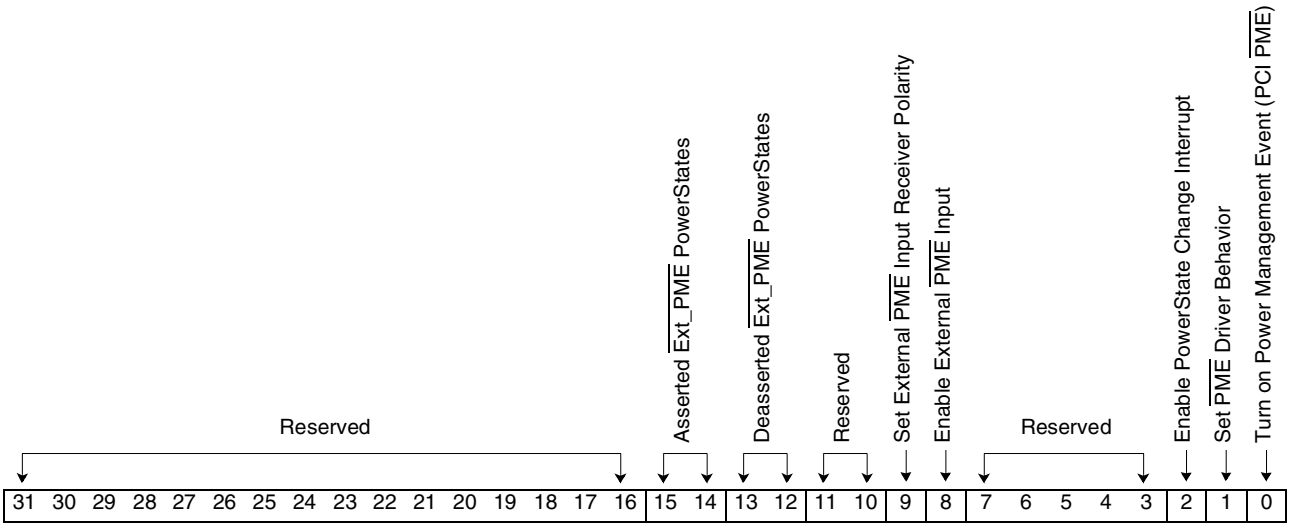
Type Read/Write

Address XXXX 0090

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions Can be written or read during configuration cycle or memory cycle when enabled (see *3.1.18: PCINT Base Address Control Register* on page 51), or as an I/O cycle. This register is documented as big endian, but how data is presented on the PCI bus depends on how the controls are set in the PCINT Endian Control Register.



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-14	Asserted Ext_PME PowerStates	These bits reflect what power state the Ext_PME pin will indicate that it is in when the Ext_PME is asserted.
13-12	Deasserted Ext_PME Power-States	These bits reflect what power state the Ext_PME pin will indicate that it is in when the Ext_PME is de-asserted. Also, these are the default bits read back for the pmi2 power-states bits 1-0 when Ext_PME is not enabled.
11-10	Reserved	Reserved.
9	Set External PME Input Receiver Polarity	Setting this bit to ’1’ will make the chip input called Ext_PME to be used as a positive active signal. Otherwise it is negative active.
8	Enable External PME Input	Setting this bit to ’1’ will enable the chip input called Ext_PME to be used as a source to driver the PM state.
7-3	Reserved	Reserved.

Bit(s)	Name	Description
2	Enable PowerState Change Interrupt	Setting this bit to '1' will enable a change of power states to cause an interrupt bit to turn on in INTST.
1	Set $\overline{\text{PME}}$ Driver Behavior	Setting this bit to '1' will make the $\overline{\text{PME}}$ driver behave like a push-pull driver. Setting this bit to '0' will make the $\overline{\text{PME}}$ driver behave like an open-drain.
0	Turn on Power Management Event (PCI $\overline{\text{PME}}$)	Setting this bit will assert the PCI bus signal $\overline{\text{PME}}$.

3.1.28 Message Signaled Interrupts-Word 1

This register contains the part of the Message Signaled Interrupts structure. See bit definitions.

Length 32 bits

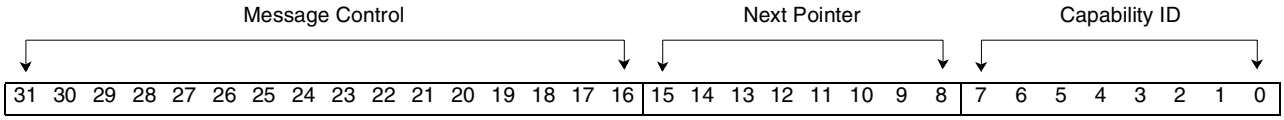
Type Read Only/Read/Write

Address XXXX 00C0

Power On Reset Value (Big Endian) x'0082 D005'

Power On Reset Value (Little Endian) x'05D0 8200'

Restrictions Cannot be written unless by external EPROM, or the PCI config space override write bit is on.



Bit(s)	Name	Description
31-16	Message Control	See PCI spec revision 2.2 for more details. Bits 31-24 are 0, and bit 23 is 1. Bits 22-20 are the Multiple Message Enable field, and bits 19-17 are the Multiple Message Capable field. Bit 16 is MSI Enable. Only bits 16, 20, 21, and 22 are writable.
15-8	Next Pointer	Pointer to the next item in the capabilities list.
7-0	Capability ID	Set to 05h to identify this function as Message Signaled Interrupt capable.

3.1.29 Message Signaled Interrupts-Word 2

This register contains the part of the Message Signaled Interrupts structure. See bit definitions.

Length 32 bits

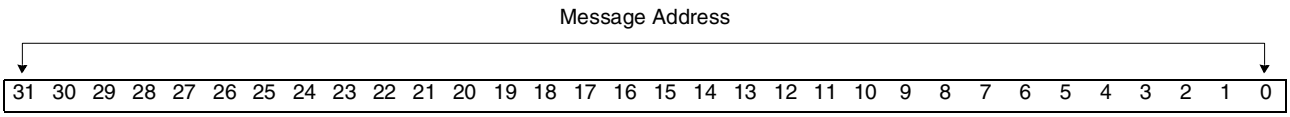
Type Read/Write

Address XXXX 00C4

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Message Address	See PCI spec revision 2.2 for more details. Bits 31-24 are ‘0’, and bit 23 is ‘1’. Bits 22-20 are the Multiple Message Enable field, and bits 19-17 are the Multiple Message Capable field. Bit 16 is MSI Enable. Only bits 16, 20, 21, and 22 are writable.

3.1.30 Message Signaled Interrupts-Word 3

This register contains the part of the Message Signaled Interrupts structure. See bit definitions.

Length 32 bits

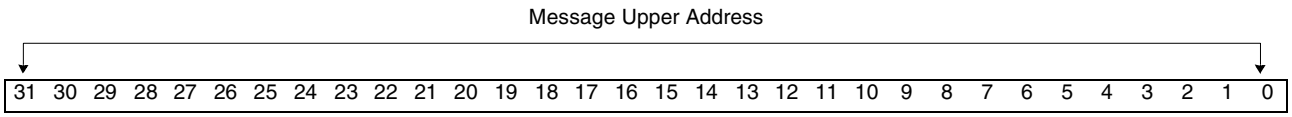
Type Read/Write

Address XXXX 00C8

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Message Upper Address	See PCI spec revision 2.2 for more details. Bits 31-0 hold the upper 32 bits of system address for the MSI memory write DMA transaction.

3.1.31 Message Signaled Interrupts-Word 4

This register contains the part of the Message Signaled Interrupts structure. See bit definitions.

Length 32 bits

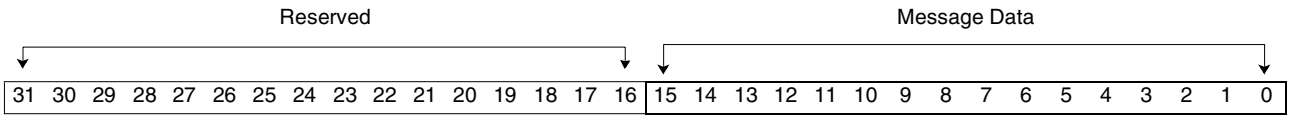
Type Read/Write

Address XXXX 00CC

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Message Data	See PCI spec revision 2.2 for more details. Bits 15-0 hold the data for the MSI memory write DMA transaction.

3.1.32 Power Management Interface-Word 1

This register contains the part of the Power Management Interface structure. See bit definitions.

Length 32 bits

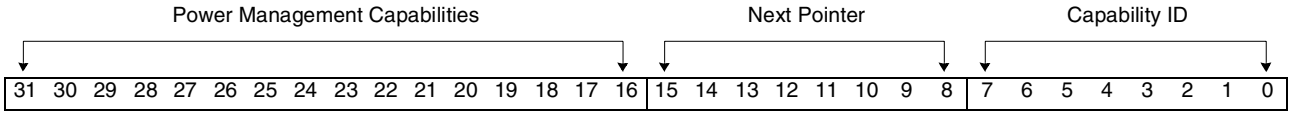
Type Read Only

Address XXXX 00D0

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions Cannot be written unless by external EPROM, or the PCI config space override write bit is on.



Bit(s)	Name	Description
31-16	Power Management Capabilities	See PCI Bus Power Management Interface Spec, Version 1.0 for more details. Bits 31-27 are for PME_Support. Bit 26 is for D2_Support. Bit 25 is for D1_Support. Bits 24-22 are reserved. Bit 21 is the Device Specific Initialization bit. Bit 20 is reserved. Bit 19 is for PME Clock. Bits 18-16 are version compliance level.
15-8	Next Pointer	Pointer to the next item in the capabilities list.
7-0	Capability ID	Set to x‘01’ to identify this function as PCI Bus Power Management Interface.

3.1.33 Power Management Interface-Word 2

This register contains the part of the Power Management Interface structure. See bit definitions.

Length 32 bits

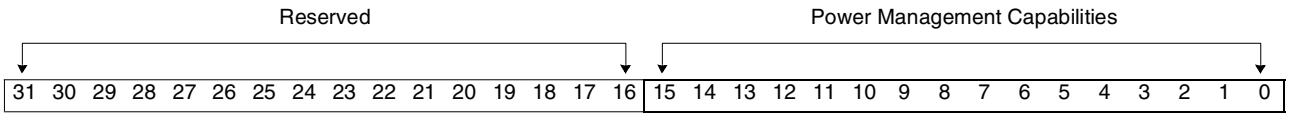
Type Read Only/Read Clear/Read Write

Address XXXX 00D4

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Power Management Capabilities	See PCI Bus Power Management Interface Spec Version 1.0 for more details. Bit 15 is for PME_Status. Bit 14-13 are not used. Bits 12-9 are not used. Bit 8 is PME_En. Bits 7-2 are reserved. Bit 1-0 are the PowerState.

3.1.34 Vital Product Data Interface-Word 1

This register contains the part of the Vital Product Data Interface structure. See bit definitions.

Length 32 bits

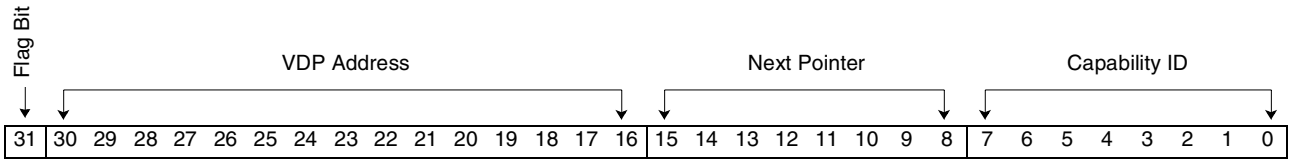
Type Read Only/Read Write

Address XXXX 00D8

Power On Reset Value (Big Endian) x‘0000 0003’

Power On Reset Value (Little Endian) x‘0300 0000’

Restrictions Cannot be written unless by external EPROM, or if the PCI config space override write bit is on.



Bit(s)	Name	Description
31	Flag Bit	See PCI Spec Revision 2.2, Appendix 1 for more details. Read/Write Flag bit. For VPD reads, this bit is set to ‘0’ and the VPD Address is set. When the hardware sets the bit to ‘1’, valid VPD data can be read. For VPD writes, the VPD Data is written first. Then this bit is set to ‘1’, along with the VPD Address. The write is active until the hardware resets this bit.
30-16	VDP Address	The field translates into the external EPROM address. See PCI Spec Revision 2.2, Appendix 1 for more details.
15-8	Next Pointer	Pointer to the next item in the capabilities list.
7-0	Capability ID	Set to 03h to identify this function as Vital Product Data Interface.

3.1.35 Vital Product Data Interface-Word 2

This register contains the part of the Vital Product Data Interface structure. See bit definitions.

Length 32 bits

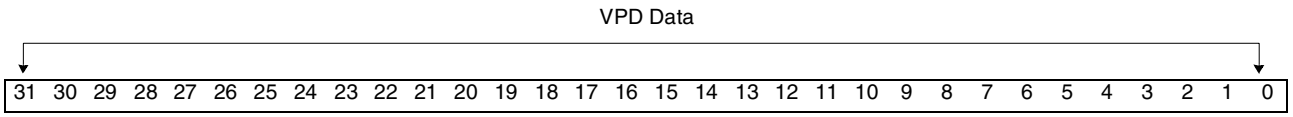
Type Read/Write

Address XXXX 00DC

Power On Reset Value (Big Endian) x‘0000 0000’

Power On Reset Value (Little Endian) x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	VPD Data	See PCI Spec Revision 2.2, Appendix 1 for more details. Four bytes of data are always read or written through this data field.

3.2 General Purpose DMA (GPDMA)

This entity provides DMA control between System Memory and PNR Packet Memory.

DMA transfers must be enabled in the GPDMA control registers for transmit and/or receive. There are two ways to initiate DMA transfers. The first is by directly writing the Source Address, Destination Address, and Transfer Count and Flag Registers. The second is by using DMA descriptors and enqueueing them using DMAQS. These two methods should not be used simultaneously. If using descriptors, refer to the DMAQS section beginning on *3.5 DMA Queues (DMAQS)* on page 115 for more information.

DMA transfers to system I/O space are not allowed.

3.2.1 GPDMA Interrupt Status Register

This register indicates the source(s) of the interrupt(s) pending, or is used as a status register when the bits are enabled.

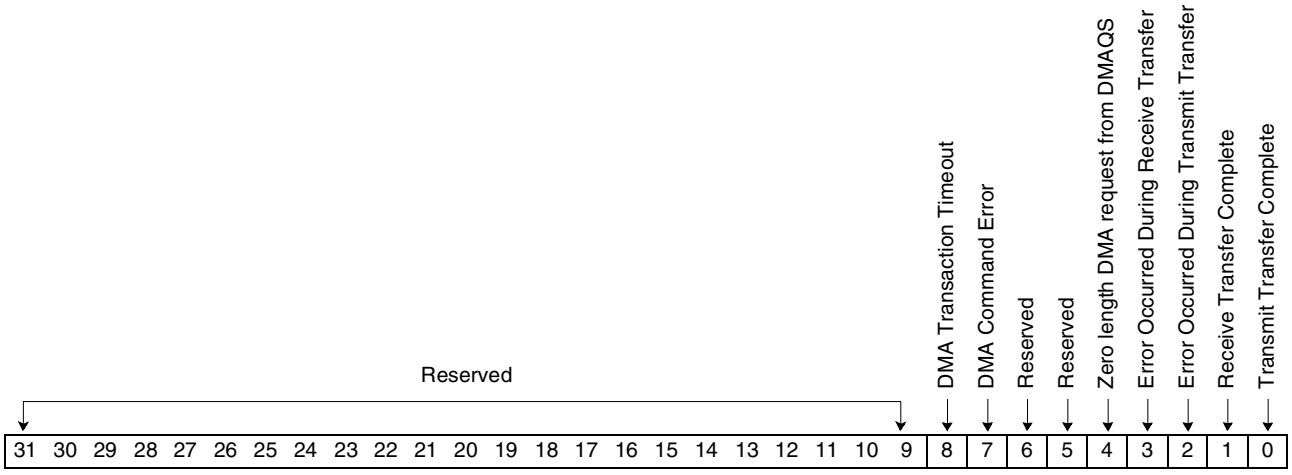
Length 32 bits

Type Clear/Set

Address XXXX 0108 and 010C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-9	Reserved	Reserved.
8	DMA Transaction Timeout	The DMA Transaction Timeout specified in the GPDMA Interrupt Enable timed out.
7	DMA Command Error	An invalid transfer was described by the value loaded into the Transfer Count and Flag Register.
6	Reserved	Reserved.
5	Reserved	Reserved.

Bit(s)	Name	Description
4	Zero Length DMA Request from DMAQS	DMAQS has requested a DMA with a length of zero. This bit is for information use only. This bit is not an error that will prevent GPDMA from processing additional DMA requests.
3	Error Occurred During Receive Transfer	Hardware errors occurred during the last transfer. The transfer stopped after detecting the error.
2	Error Occurred During Transmit Transfer	Hardware errors occurred during the last transfer. The transfer stopped after detecting the error.
1	Receive Transfer Complete	The receive transfer is complete.
0	Transmit Transfer Complete	The transmit transfer is complete.

3.2.2 GPDMA Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *GPDMA Interrupt Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from GPDMA to INTST if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0110 and 0114

Power On Reset Value x'0000 009C'

Restrictions None

3.2.3 GPDMA Control Register

Used to set options for DMA operations.

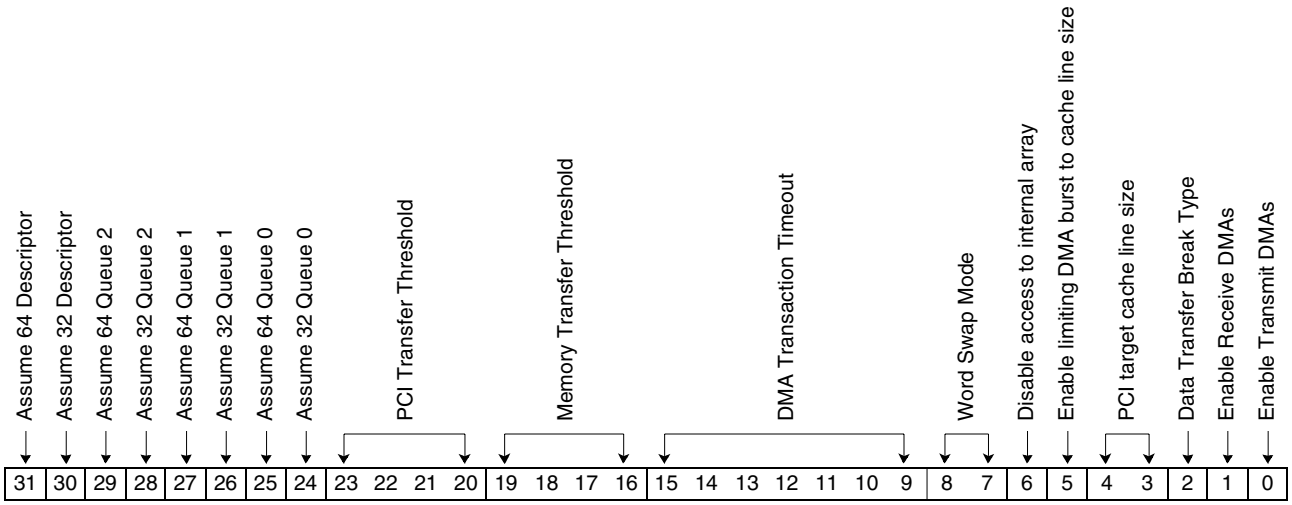
Length 32 bits

Type Clear/Set

Address XXXX 0118 and 011C

Power On Reset Value x‘0088 00C7’

Restrictions None



Bit(s)	Name	Description
31	Assume 64 Descriptor	Assume 64-bit PCI Interface for Descriptor Transfers.
30	Assume 32 Descriptor	Assume 32-bit PCI Interface for Descriptor Transfers.
29	Assume 64 Queue 2	Assume 64-bit PCI Interface for Queue 2 Transfers.
28	Assume 32 Queue 2	Assume 32-bit PCI Interface for Queue 2 Transfers.
27	Assume 64 Queue 1	Assume 64-bit PCI Interface for Queue 1 Transfers.
26	Assume 32 Queue 1	Assume 32-bit PCI Interface for Queue 1 Transfers.
25	Assume 64 Queue 0	Assume 64-bit PCI Interface for Queue 0 Transfers.
24	Assume 32 Queue 0	Assume 32-bit PCI Interface for Queue 0 Transfers.
23-20	PCI Transfer Threshold	The value of these bits multiplied by eight determines the number of bytes that must be ready to transfer before a DMA transfer is initiated on the PCI bus. This can be used to tune the performance of the PCI bus. If the number of bytes left to transfer is less than the threshold, the transfer will start when all remaining bytes are ready to be transferred.
19-16	Memory Transfer Threshold	The value of these bits multiplied by eight determine the number of bytes that must be ready to transfer before a transfer is initiated on the internal memory bus. This can be used to tune the performance of the memory subsystem.
15-9	DMA Transaction Timeout	These bits hold a value that is used to count the number of cycles that an unacknowledged DMA cycle is in progress. If the count is reached, due to an internal chip hang condition, the DMA is terminated. A value of ‘0’ disables this function.

Bit(s)	Name	Description
8-7	Word Swap Mode	This field controls word swapping for data being transferred to PCINT. The word swapping is done as part of endian alignment. The bits are defined as follows: 00 No Swap: The 32-bit words being transferred will not be swapped by PCINT. 01 Swap: The 32-bit words being transferred will always be swapped by PCINT. 10 Endian Swap: The words will be swapped if byte swapping is being done. 11 Anti-endian Swap: The words will be swapped if byte swapping is not being done.
6	Disable access to internal array	When this bit is set, the internal array cannot be read or written. This can be used to ensure that the array is not inadvertently read or written while DMAs are in progress, causing unpredictable results.
5	Enable limiting DMA burst to cache line size	This bit on causes a DMA burst to terminate upon crossing a cache line boundary of the PCI target.
4-3	PCI target cache line size	This field indicates the cache line size if aligning DMAs to the cache line size of the PCI target (see bit 5). 00 32 bytes 01 64 bytes 10 128 bytes 11 256 bytes
2	Data Transfer Break Type	This bit on causes a re-arbitrate request from PCI to immediately stop moving data and resurface a new request to move the remainder of the data. When reset, GPDMA stops data movement at the next Cache line boundary.
1	Enable Receive DMAs	This bit on enables DMA transfers out of the PNR.
0	Enable Transmit DMAs	This bit on enables DMA transfers into the PNR.

3.2.4 GPDMA Source Address Register

Used to set and keep track of the Source Address during a DMA transfer. This is the system address that increments during a DMA transfer. A bit in the Transfer Count and Flag Register determines if the source address is internal to the PNR or is a system address.

Length 64 bits

Type Read/Write

Address XXXX 0128

Power On Reset Value x‘0000 0000 0000 0000’

Restrictions None

3.2.5 GPDMA Destination Address Register

Used to set and keep track of the Destination address during a DMA transfer. This is the Destination address that increments during a DMA transfer. A bit in the Transfer Count and Flag Register determines if the destination address is internal to the PNR or is a system address.

Length	64 bits
Type	Read/Write
Address	XXXX 0130
Power On Reset Value	x‘0000 0000 0000 0000’
Restrictions	None

3.2.6 GPDMA Transfer Count and Flag Register

Specifies the type and number of bytes transferred during a DMA transfer. The lower 16 bits are a counter of the number of bytes transferred during a DMA transfer. It is a count down counter; when zero is reached, the transfer ends. Writing a non-zero value to the lower 16 bits starts the DMA transfer. The upper 16 bits specify the type of transfer as follows.

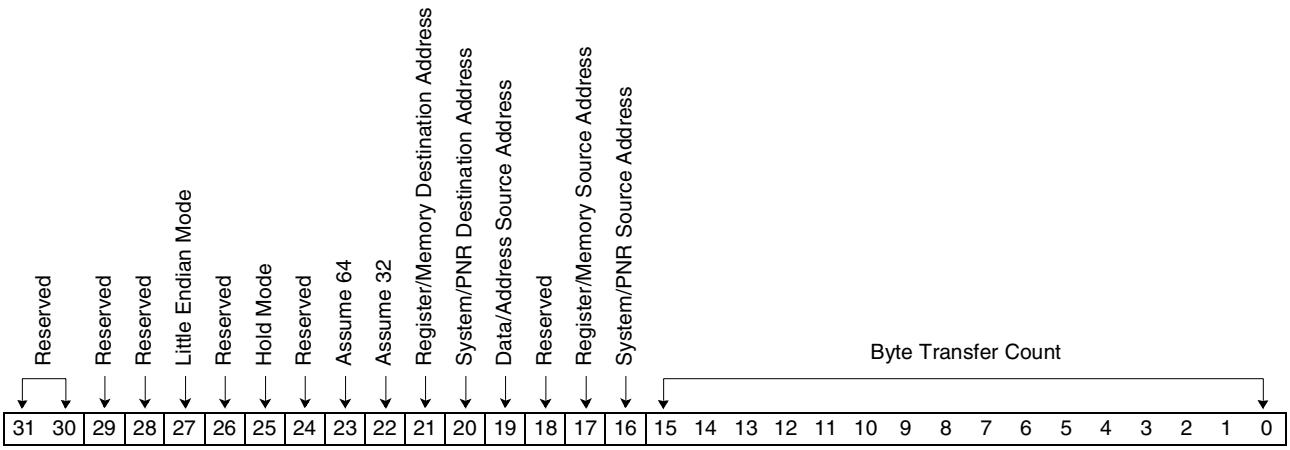
Length 32 bits

Type Read/Write

Address XXXX 0138

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-30	Reserved	These bits must be ‘0’.
29	Reserved	Reserved.
28	Reserved	Reserved.
27	Little Endian Mode	When this bit is written to ‘0’, this DMA channel operates in big endian mode. When ‘1’, it operates in little endian mode. When in little endian mode, both the source and destination must be aligned on four-byte boundaries.
26	Reserved	Reserved.
25	Hold Mode	When set, bits 28-29 are redefined to allow the source or destination address to be held instead of incremented. Bit 29 becomes the hold destination address and bit 28 becomes the hold source address. The address being held must be a register address. When holding, the maximum length is 240 bytes.
24	Reserved	Reserved.
23	Assume 64	Assume the PCI Interface is 64 bits wide.
22	Assume 32	Assume the PCI Interface is 32 bits wide.
21	Register/Memory Destination Address	If this bit is set, the destination address is a register address. If this bit is not set, the destination address is a memory address. If the destination address is a system address, this bit should cleared. I/O DMA cycles on the PCI bus are not implemented.

Bit(s)	Name	Description
20	System/PNR Destination Address	If this bit is set, the destination address is a PCI bus address. If this bit is not set, the destination address is internal to the chip.
19	Data/Address Source Address	If this bit is set, the Source Address Register contains the source data. If this bit is not set, the Source Address Register contains the source address.
18	Reserved	Reserved.
17	Register/Memory Source Address	If this bit is set, the source address is a register address. If this bit is not set, the source address is a memory address. If the source address is a system address, this bit should cleared. I/O DMA cycles on the PCI bus are not implemented.
16	System/PNR Source Address	If this bit is set, the source address is a PCI bus address. If this bit is not set, the source address is internal to the chip.
15-0	Byte Transfer Count	These bits indicate the number of bytes to transfer. A non-zero value in this field starts the DMA transfer.

3.2.7 GPDMA DMA Max Burst Time

Used to limit the number of cycles a master can burst on the PCI bus. When a DMA burst is started, a counter is loaded with the value in this register. When the counter expires and the current access completes, the PCI bus is released for use by another bus master. Writing a non-zero value to this register enables this function.

Length 32 bits

Type Read/Write

Address XXXX 0158

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	Maximum Burst Time	Maximum Burst Time.

3.2.8 GPDMA Maximum Memory Transfer Count

Used to limit the size of data requests to the Control/Packet Memories. This register defines the maximum number of bytes to be transferred in a single storage request to PNR Storage.

Length 32 bits

Type Read/Write

Address XXXX 0150

Power On Reset Value x‘0000 0040’

Restrictions None

Bit(s)	Name	Description
31-7	Reserved	Reserved.
6-0	Maximum Memory Transfer Value	Maximum number of bytes transferable in a single request to PNR Storage.

3.2.9 GPDMA Checksum Register

This register contains the accumulated checksum value. It can also be used to initialize the checksum with a seed value. The most significant bit contains the alignment state (1 = odd, 0 = even alignment). This register can be read at four different addresses. The base address returns the unmodified accumulated checksum. The base address + 4 returns the inverted accumulated checksum. The base address + 8 returns the byte-swapped accumulated checksum. The base address + 12 returns the inverted byte-swapped accumulated checksum.

Length 32 bits

Type Read/Write

Address XXXX 0160

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Checksum	Accumulated checksum.

3.2.10 GPDMA Read DMA Byte Count

This register counts the bytes transferred into the PNR by the DMA controller. Descriptor bytes can be included as options. (See the *3.2.3 GPDMA Control Register* on page 75 for details.)

Length	32 bits
Type	Read/Write
Address	XXXX 0178
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.2.11 GPDMA Write DMA Byte Count

This register counts the bytes transferred out of the PNR by the DMA controller.

Length	32 bits
Type	Read/Write
Address	XXXX 017C
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.2.12 GPDMA Array Read Address

This register is used to read the GPDMA internal array. The internal array is used to hold data for the DMA. The array is organized as 64 32-bit words. The GPDMA Array Read Address is written with the address of the word that is to be read. The GPDMA Array Data Register is read to obtain the contents of the addressed word. The GPDMA Array Read Address is incremented each time the GPDMA Array Data Register is read, causing repeated reads of the GPDMA Array Data Register to obtain sequential words from the array.

Length 32 bits

Type Read/Write

Address XXXX 0140

Power On Reset Value x‘0000 0000’

Restrictions This address space is for diagnostic use only. It should not be read or written during normal operation. The low order two bits of GPDMA Array Read Address are place holders and are ignored. They should be set to ‘0’.

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Array Read Address	GPDMA Array Read Address

3.2.13 GPDMA Array Write Address

This register is used to write the GPDMA internal array. The internal array is used to hold data for the DMA. The array is organized as 64 32-bit words. The GPDMA Array Write Address is written with the address of the word that is to be written. The GPDMA Array Data Register is written to write the addressed word. The GPDMA Array Write Address is incremented each time the GPDMA Array Data Register is written, causing repeated writes of the GPDMA Array Data Register to write sequential words in the array.

Length 32 bits

Type Read/Write

Address XXXX 0144

Power On Reset Value x‘0000 0000’

Restrictions This address space is for diagnostic use only. It should not be read or written during normal operation. The low order two bits of GPDMA Array Read Address are place holders and are ignored. They should be set to ‘0’.

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Array Write Address	GPDMA Array Write Address.

3.2.14 GPDMA Array

Reads the contents of the internal array. The internal array is used to hold data for the DMA.

Length	64 words x 32 bits
Type	Read/Write
Address	XXXX 0148
Power On Reset Value	x‘0000 0000’
Restrictions	This address space is for diagnostic use only. It should not be read or written during normal operation. The array is read/written at the location indicated by the GPDMA Array Read Address or GPDMA Array Write Address.

3.3 Interrupt and Status/Control (INTST)

This entity contains the masking registers that choose which interrupt/status source will be gated onto one of the two available interrupt I/O pins. A delayed interrupt function allows PNR status registers to be read and placed in system memory before the interrupt signal is raised. For details, see section *3.5 DMA Queues (DMAQS)* on page 115.

A bus timer function is provided in this entity that times a single bus access to make sure that the cycle is terminated before the system timer times out. This allows the user code an opportunity to recover from the error as opposed to the subsystem common code.

Below is a summary of this entity's functions:

- Interrupt Prioritized Status Registers
- Interrupt Source Register
- Interrupt Enable Registers
- Bus timer function
- Control Processor error register with enable and halt chip registers

3.3.1 INTST Interrupt 1 Prioritized Status Register

Used to help quickly parse which interrupting entity of the PNR is active.

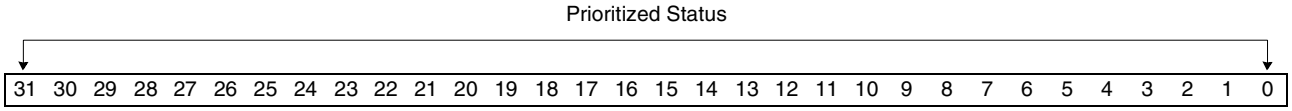
Length 32 bits

Type Read Only

Address XXXX 0400

Restrictions None

Power On Reset Value x'0000 0000'



Bit(s)	Name	Description
31-0	Prioritized Status	Reading this register gives a prioritized value of the bits in the INTST Interrupt Source and INTST Enable for Interrupt 1 (MINTA) registers ANDed together, returning a value that will be a hex number equal to bit number n + 1. For example, if bit 31 is on, x'20' will be read back.

3.3.2 INTST Interrupt 2 Prioritized Status Register

Used to help quickly parse which interrupting entity of the PNR is active.

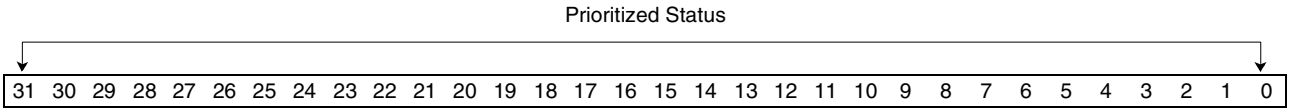
Length 32 bits

Type Read Only

Address XXXX 0404

Restrictions None

Power On Reset Value x‘0000 0000’



Bit(s)	Name	Description
31-0	Prioritized Status	Reading this register will give a prioritized value of the bits in the INTST Interrupt Source and INTST Enable for Interrupt 2 (MINT2) registers ANDed together, returning a value that will be a hex number equal to bit number n + 1. For example, if bit 31 is on, x‘20’ will be read back.

3.3.3 INTST Control Register

This register is used to control various PNR functions.

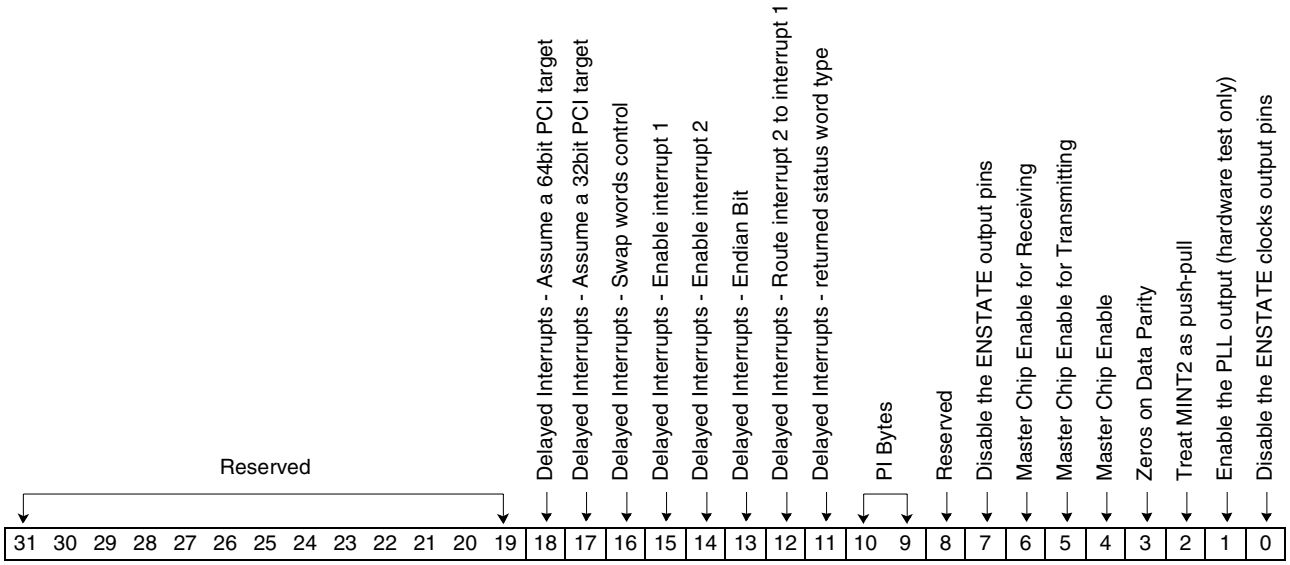
Length 32 bits

Type Clear/Set

Address XXXX 0408 and 040C

Restrictions None

Power On Reset Value x ‘0001 0202’



Bit(s)	Name	Description
31-19	Reserved	Reserved.
18	Delayed Interrupts - Assume a 64-bit PCI Target	This bit set will help the mastering logic determine how to best move data to a 64-bit PCI target. This bit is set when software has system knowledge of its targets.
17	Delayed Interrupts - Assume a 32-bit PCI Target	This bit set will help the mastering logic determine how to best move data to a 32-bit PCI target. This bit is set when software has system knowledge of its targets.
16	Delayed Interrupts - Swap Words Control	This bit determines the word order of the status word DMA transfer for delayed ints. The default value of ‘1’ is to swap the words. A value of ‘0’ will not swap them.
15	Delayed Interrupts - Enable Interrupt 1	When set, the delayed int mechanism for int 1 is enabled.
14	Delayed Interrupts - Enable Interrupt 2	When set, the delayed int mechanism for int 2 is enabled.
13	Delayed Interrupts - Endian Bit	This bit determines the endian made of the status word DMA transfer for delayed ints. When this bit is set, the endian is little. The default of ‘0’ is big endian.
12	Delayed Interrupts - Route Interrupt 2 to Interrupt 1	When set, the int 2 signal is routed and raised as int 1. This bit allows both sets of int masks in INST to be used, while still using only a single hardware interrupt. When set, both delayed interrupts should be enabled if they are being used.

Bit(s)	Name	Description
11	Delayed Interrupts - Returned Status Word Type	When this bit is set, the INTST Interrupt Source word will be ANDed with the corresponding enable register. Otherwise, the INTST Interrupt Source register alone will be returned.
10-9	CPI Bytes	These bits are encoded to tell how many bytes long the AAL 5 CPI field is. The following are the encodings: 00 CPI field is zero bytes long. In this case, the two bytes containing the CPI field and the AAL5 user-to-user byte are copied into the packet header. See the definition of the packet header for the locations. 01 CPI field is one byte long and is always '0'. In this case, the one byte AAL5 user-to-user byte is copied into the packet header. 10 CPI field is two bytes long and is always '0'. 11 Treated the same as '00'.
8	Reserved	Reserved.
7	Disable the ENSTATE Output Pins	When this bit is set to '0', the chip I/O ENSTATES will be driven with the output of the internally muxed debug states. When set to '1', these outputs will be quiet.
6	Master Chip Enable for Receiving	When this bit is set to '1', various state machines in the receive part of the chip will be enabled.This bit can be reset by the hardware, based on what is set in *3.3.8 INTST CPB Status Register* on page 92 and what bits are set in *3.3.10 INTST PNR Halt Enable* on page 94.
5	Master Chip Enable for Transmitting	When this bit is set to '1', various state machines in the transmit part of the chip will be enabled. This bit can be reset by the hardware, based on what is set in *3.3.8 INTST CPB Status Register* on page 92 and what bits are set in *3.3.10 INTST PNR Halt Enable* on page 94.
4	Master Chip Enable	When this bit is set to '1', various state machines in the chip will be enabled. This must be set to '1' to transmit or receive anything. This bit can be reset by the hardware, based on what is set in *3.3.8 INTST CPB Status Register* on page 92 and what bits are set in *3.3.10 INTST PNR Halt Enable* on page 94.
3	Zeros on Data Parity	When this bit is set to '1', zeros will be forced on the data bus parity line(s) during a slave read data phase or a master address phase or a master write data phase.
2	Treat MINT2 as Push-Pull	When this bit is set to '1', the chip I/O MINT2 will be driven active high as well as low, like a push-pull driver. This is for use as a specific sideband application, not as a general shared open-drain interrupt line.
1	Enable the PLL Output (hardware test only)	When this bit is set to '1', the chip I/O PPLLOUT will be driven with the output of the internal PLL. When set to '0', this output will be quiet.
0	Disable the ENSTATE Clocks Output Pins	When this bit is set to '0', the chip I/O PINTCLK and PDBLCLK will be driven with the output of the internal clock tree. When set to '1', these outputs will be quiet.

3.3.4 INTST Interrupt Source Register

This register indicates the source(s) of the interrupt(s) pending. It can also be used as a status register when the bits are enabled. Note that bits in this register always reflect the state of the source register bit: writing a value will have no effect. Reserved bits will not take on the written value. The delay of running through a latch has been removed. For the delayed interrupts feature, writing this register at the end of an interrupt handling routine will guarantee that interrupt1 and interrupt2 (if enabled) will pulse off, allowing the logic to get ready for the next interrupt DMA.

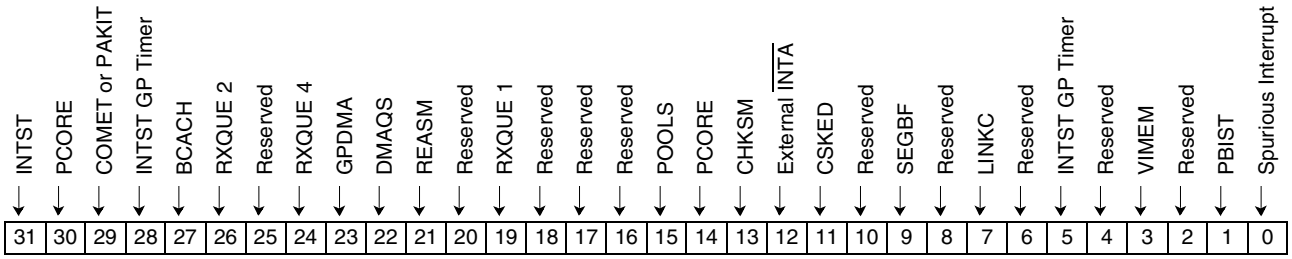
Length 32 bits

Type Read Only

Address XXXX 0410 and 0414

Restrictions None

Power On Reset Value x‘0000 0000’



Bit(s)	Name	Description
31	INTST	A Control Processor related condition has occurred. A read of the INTST CPB Status and INTST CPB Status Enable must be done. For more information, See *3.3.8 INTST CPB Status Register* on page 92 and *3.3.9 INTST CPB Interrupt Enable Register* on page 94.
30	PCORE	The PCORE entity has hardware interrupts that need handling.
29	COMET or PAKIT	The COMET or PAKIT entities have interrupts that need handling.
28	INTST GP Timer	The INTST General Purpose Timer Counter has reached the INTST General Purpose Timer Compare value and caused an interrupt.
27	BCACH	The BCACH entity has interrupts that need handling.
26	RXQUE 2	The RXQUE entity has interrupts that need handling.
25	Reserved	Reserved.
24	RXQUE 4	The RXQUE entity has interrupts that need handling.
23	GPDMA	The GPDMA entity has interrupts that need handling.
22	DMAQS	The DMAQS entity has interrupts that need handling.
21	REASM	The REASM entity has interrupts that need handling.
20	Reserved	Reserved.
19	RXQUE 1	The RXQUE entity has interrupts that need handling.
18	Reserved	Reserved.
17	Reserved	Reserved.

Bit(s)	Name	Description
16	Reserved	Reserved.
15	POOLS	The POOLS entity has interrupts that need handling.
14	PCORE	The PCORE entity has User Defined interrupts that need handling.
13	CHKSM	The CHKSM entity has interrupts that need handling.
12	External $\overline{\text{INTA}}$	This bit is set when the PNR detects that MINTA is low and, conditionally, when the same bit in INTST Enable for PCORE Normal Interrupt or INTST Enable for PCORE Critical Interrupt is set. This bit is for use by the PCORE entity, and it is recommended that interrupts directed out which drive output (MINTA) be disabled.
11	CSKED	The CSKED entity has interrupts that need handling.
10	Reserved	Reserved.
9	SEGBF	The SEGBF entity has interrupts that need handling.
8	Reserved	Reserved.
7	LINKC	The LINKC entity has interrupts that need handling.
6	Reserved	Reserved.
5	INTST GP Timer	The INTST General Purpose Timer Counter has reached the INTST General Purpose Timer Compare value and caused an interrupt.
4	Reserved	Reserved.
3	VIMEM	The VIMEM entity has interrupts that need handling.
2	Reserved	Reserved.
1	PBIST	This bit is set when the PBIST entity did not indicate that it was done. It is also not clearable.
0	Spurious Interrupt	Under normal conditions, this bit should never be set. However, if one of the other bits in this register turns on, then off, a spurious interrupt condition will occur. The manual vector passed to the processor will point to this bit being on.

3.3.5 INTST Interrupt 1 Enable Register ($\overline{\text{MINTA}}$)

This register serves as an enable for interrupt 1. It allows the user to enable interrupts for each of the conditions reported in the *INTST Interrupt Source Register*. Each bit corresponds to the same bit in the status register and when set to ‘1’ generates an interrupt on the $\overline{\text{MINTA}}$ pin if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0418 and 041C

Restrictions None

Power On Reset Value x‘0000 0000’

3.3.6 INTST Interrupt 2 Enable Register (MINT2)

This register serves as an enable for interrupt 2. It allows the user to enable interrupts for each of the conditions reported in the *INTST Interrupt Source Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt on the MINT2 pin if the condition is detected. See section *3.3.4 INTST Interrupt Source Register* on page 89 for the bitwise description that the corresponding bit in this register will enable.

Length 32 bits

Type Clear/Set

Address XXXX 0420 and 0424

Restrictions None

Power On Reset Value x'0000 0000'

3.3.7 INTST Interrupt Source Without Enables Register

This register is used to help quickly parse which interrupting bit of INTST Interrupt Source is active. It does not matter to what state the Enable registers are set because the value returned does not depend on them.

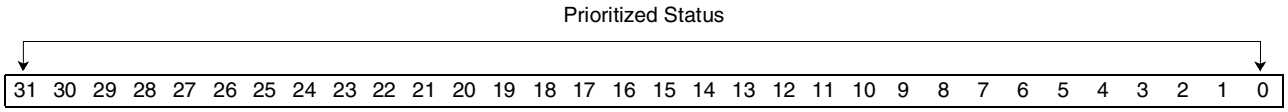
Length 32 bits

Type Read Only

Address XXXX 0428

Restrictions None

Power On Reset Value x'0000 0000'



Bit(s)	Name	Description
31-0	Prioritized Status	Reading this register gives a prioritized value of the bits in the INTST Interrupt Source, returning a value that is a hex number equal to bit number n + 1. For example, if bit 31 is on, x'20' will be read back.

3.3.8 INTST CPB Status Register

This register holds the status bits for errors on the Control Processor bus. These bits, when disabled, will set a bit in the INTST Interrupt Source register.

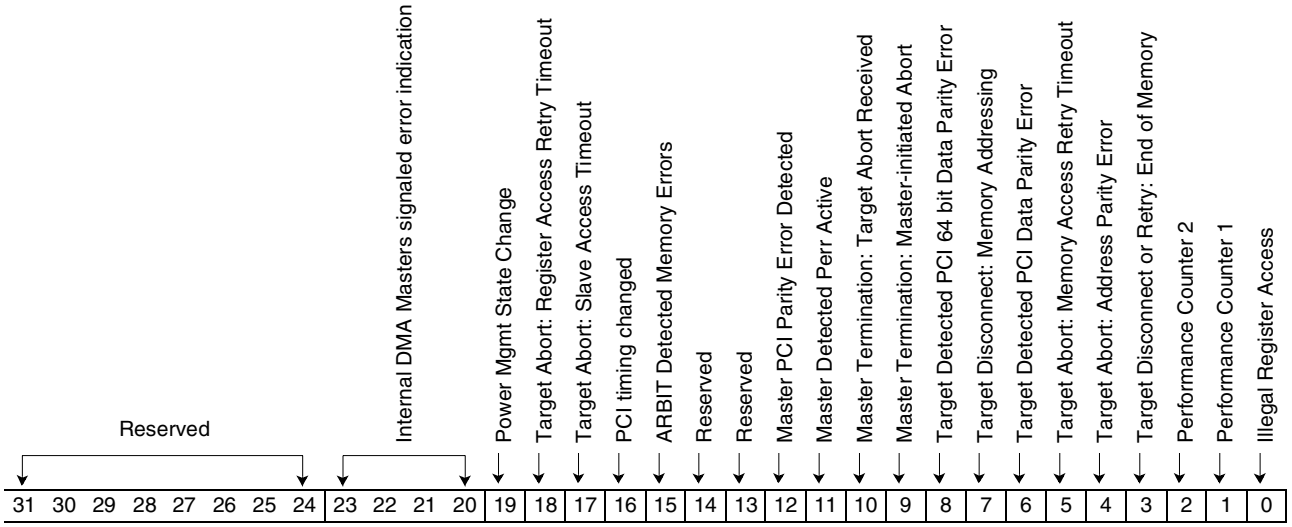
Length 32 bits

Type Clear/Set

Address XXXX 0430 and 0434

Restrictions None

Power On Reset Value x‘0000 0000’



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-20	Internal DMA Masters Signaled Error Indication	The PCINT entity will set these bits when it signals a DMA error indication to one of the internal requesting masters. Bit 23 is GPDMA, bit 22 is PCORE, bit 21 is RXQUE, and bit 20 is INTST.
19	Power Mgmt State Change	This bit is set when the conditions in PCINT are met to trigger a Power Management State change.
18	Target Abort: Register Access Retry Timeout	This bit is set when this slave does more retry cycles than the specified amount in the PCINT Count Timeout Register during a register access.
17	Target Abort: Slave Access Timeout	This bit is set when this slave does not access the PNR in the specified amount in the PCINT Count Timeout Register.
16	PCI Timing Changed	The PCI bus clock has changed range. The PNR should be reset and re-initialized. See *3.4.1 Reset Status Register* on page 105 for more information.
15	ARBIT Detected Memory Errors	This bit is set when error conditions detected by ARBIT are enabled. Note: This bit is a reflection of the arbitrator status bits and does not need to be reset if the arbitrator condition has been reset.
14	Reserved	Reserved.
13	Reserved	Reserved.

Bit(s)	Name	Description
12	Master PCI Parity Error Detected	This bit is set when a PCI bus data parity error is detected in master mode.
11	Master Detected Perr Active	This bit is set when a target has driven $\overline{\text{PERR}}$.
10	Master Termination: Target Abort Received	This bit is set when in master mode and the transfer is aborted by the target.
9	Master Termination: Master-initiated Abort	This bit is set when in master mode and the transfer is aborted by this master.
8	Target Detected PCI 64 Bit Data Parity Error	This bit is set when a PCI data parity error is detected in 64 bit target mode (the upper DWORD has the data parity error).
7	Target Disconnect: Memory Addressing	This is set when a memory access is occurring and bits 0 and 1 of the address are not ‘0’.
6	Target Detected PCI Data Parity Error	This bit is set when a PCI data parity error is detected in target mode.
5	Target Abort: Memory Access Retry Timeout	This bit is set when this slave does more retry cycles than the specified amount in the PCINT Count Timeout Register during a memory access.
4	Target Abort: Address Parity Error	This bit is set when an address parity error is detected.
3	Target Disconnect or Retry: Wrap of 2 GB Internal Address Slave Counter	This bit is set when the slave address counter is its maximum counter value. It will indicate a termination condition on the PCI bus. This is primarily a debug bit and can turn on during normal operation. It most likely will be useful when the PNR slave mode is configured in 64-bit addressing mode.
2	Performance Counter 2	The PCINT Performance Counter 2 has overflowed.
1	Performance Counter 1	The PCINT Performance Counter 1 has overflowed.
0	Illegal Register Access	This bit is set when a PNR register is being accessed by fewer than four bytes at a time. This is not true for configuration registers during a configuration cycle.

3.3.9 INTST CPB Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *INTST CPB Status Register*. Each bit corresponds to the same bit in the status register and when set to ‘1’ causes bit 31 of the *INTST Interrupt Source Register* on page 89 to come on if the condition is detected.

Length	32 bits
Type	Clear/Set
Address	XXXX 0438 and 043C
Restrictions	None
Power On Reset Value	x‘0006 9F71’

3.3.10 INTST PNR Halt Enable

This register serves as an enable for the INTST CPB Status register and gates which errors will reset bit 4 (Master chip enable), bit 5 (Master chip enable for Transmitting), and bit 6 (Master chip enable for Receiving), all in the INTST Control Register register. This allows selected bits to disable the PNR, especially in the case of severe hardware detected errors. See section *3.3.8 INTST CPB Status Register* on page 92 for the bitwise description that the corresponding bit in this register will enable. This enable will initialize to the disabled state.

Length	32 bits
Type	Clear/Set
Address	XXXX 0440 and 0444
Restrictions	None
Power On Reset Value	x‘0006 9F71’

3.3.11 INTST CPB Capture Enable

This register no longer captures addresses reliably due to internal chip changes, but can be used as a general purpose register to write and read values for testing or other such purposes.

Length 32 bits

Type Clear/Set

Address XXXX 0450 and 0454

Restrictions None

Power On Reset Value x‘0006 9F71’

Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	General Use Bits	These bits can be used for any general purpose.

3.3.12 INTST CPB Captured Address

This register no longer captures addresses correctly as it has in prior revisions. It can be used as a general purpose read/write register for testing and diagnostic code.

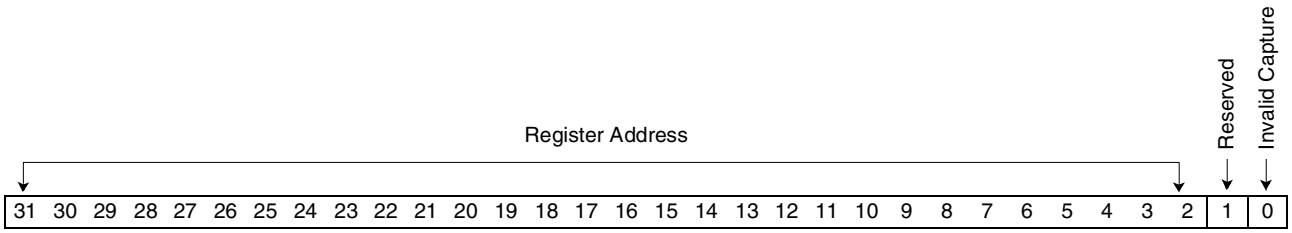
Length 32 bits

Type Read/Write

Address XXXX 0458

Restrictions None

Power On Reset Value x‘0000 0001’



Bit(s)	Name	Description
31-2	Register Address	Captured PNR register address.
1	Reserved	Reserved.
0	Invalid Capture	When this bit is reset to ‘0’, a valid capture has been made.

3.3.13 INTST General Purpose Timer Pre-scaler

This is the pre-scaler for the INTST General Purpose Timer Compare.This register will hold the value of the pre-scale count. The default value is 1 tick every 10.02µS, assuming a 33MHz or 66MHz PCI Bus clock, producing a 66MHz system clock (count is system clock). The pre-scale count value is n-1, where n is the desired increment count.

Length	32 bits
Type	Read/Write
Address	XXXX 0464
Restrictions	None
Power On Reset Value	x‘0000 029B’

3.3.14 INTST General Purpose Timer Compare

This is the compare value for the general purpose timer. This register holds the value of the data that is compared to the count value in the INTST General Purpose Timer Counter, setting the INTST General Purpose Timer Status bits. See section *3.3.17 INTST General Purpose Timer Mode Control* on page 99 for details on the operation of this register.

Length	32 bits
Type	Read/Write
Address	XXXX 0468
Restrictions	None
Power On Reset Value	x‘0800 0000’

3.3.15 INTST General Purpose Timer Counter

This is the general purpose timer counter.This register holds the value of the counter. It always counts up. See section *3.3.17 INTST General Purpose Timer Mode Control* on page 99 for details on operation of this register.

Length	32 bits
Type	Read/Write
Address	XXXX 046C
Restrictions	None
Power On Reset Value	x‘0000 0000’

3.3.16 INTST General Purpose Timer Status

This is the status of the general purpose timer counter.

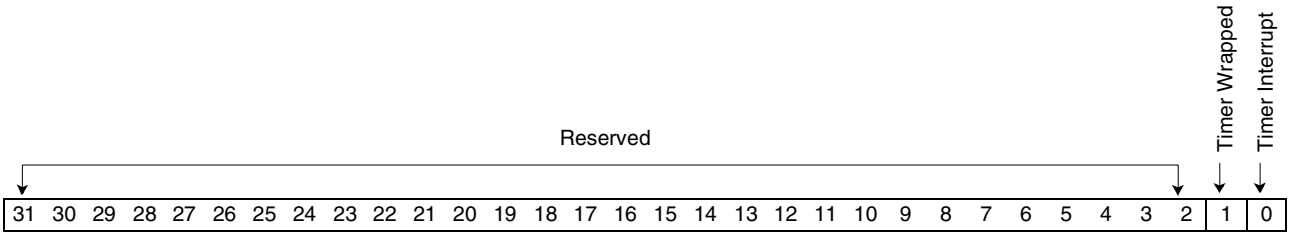
Length 32 bits

Type Clear/Set

Address XXXX 0470 and 0474

Restrictions None

Power On Reset Value x‘0000 0000’



Bit(s)	Name	Description
31-2	Reserved	Reserved.
1	Timer Wrapped	This bit is set when the INTST General Purpose Timer Counter wraps around to a ‘0’ count value.
0	Timer Interrupt	See *3.3.17 INTST General Purpose Timer Mode Control* on page 99 for details on how this bit is set. For mode 0: This bit is set when the INTST General Purpose Timer Counter matches the value in the INTST General Purpose Timer Compare register. The comparing condition must be changed (write INTST General Purpose Timer Counter or INTST General Purpose Timer Compare) before resetting this bit, or the bit will set again.

3.3.17 INTST General Purpose Timer Mode Control

This register controls the operating modes of the general purpose timer counter.

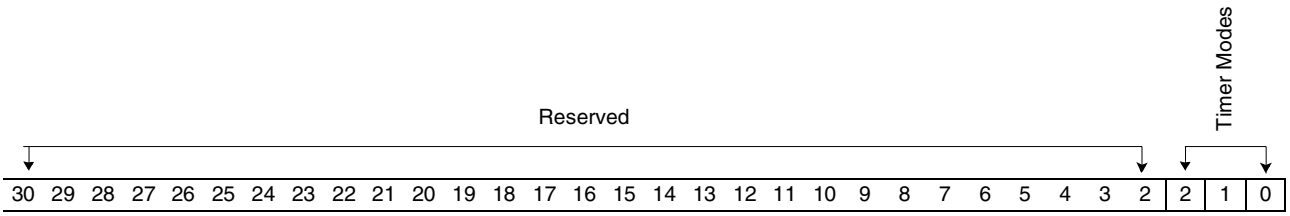
Length 32 bits

Type Clear/Set

Address XXXX 0478 and 047C

Restrictions None

Power On Reset Value x‘0000 0004’



Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	Timer Modes	These bits are encoded to provide eight different timer operation modes. Encoding is as follows: x‘0’ The INTST General Purpose Timer Counter is a free-running up-counter and sets bit 0 of INTST General Purpose Timer Status when equal to INTST General Purpose Timer Compare. x‘1’ The INTST General Purpose Timer Counter is a free-running up-counter and sets bit 0 of INTST General Purpose Timer Status when equal to INTST General Purpose Timer Compare. A write to INTST General Purpose Timer Compare will reset bit 0 of INTST General Purpose Timer Status. x‘2’ The INTST General Purpose Timer Counter is a free-running up-counter and sets bit 0 of INTST General Purpose Timer Status when equal to or greater than INTST General Purpose Timer Compare. A write to INTST General Purpose Timer Compare will reset bit 0 of INTST General Purpose Timer Status. x‘3’ The INTST General Purpose Timer Counter is an up-counter and sets bit 0 of INTST General Purpose Timer Status when equal to or greater than the INTST General Purpose Timer Compare. The INTST General Purpose Timer Counter is also reset when a comparison is made. A write to INTST General Purpose Timer Compare will reset bit 0 of INTST General Purpose Timer Status and INTST General Purpose Timer Counter. x‘4’ The INTST General Purpose Timer Counter is disabled and no status bits will be set. x‘5-7’ Reserved.

3.3.18 INTST Enable for PCORE Normal Interrupt

This register serves as an enable for the PCORE normal interrupt input. It allows the normal interrupt from PCORE to activate bit 14 of the *INTST Interrupt Source Register* on page 89.

Length	32 bits
Type	Clear/Set
Address	XXXX 0480 and 0484
Restrictions	None
Power On Reset Value	x‘0000 0000’

3.3.19 INTST Enable for PCORE Critical Interrupt

This register serves as an enable for the PCORE normal interrupt input. It allows the critical interrupt from PCORE to activate bit 30 of the *INTST Interrupt Source Register* on page 89.

Length	32 bits
Type	Clear/Set
Address	XXXX 0488 and 048C
Restrictions	None
Power On Reset Value	x‘0000 0000’

3.3.20 INTST Debug States Control

This register serves as the control for external debug states.

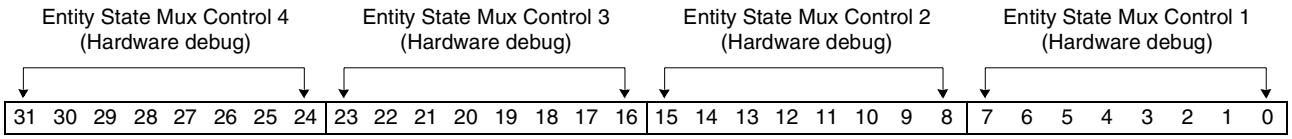
Length 32 bits

Type Read/Write

Address XXXX 0490

Restrictions None

Power On Reset Value x‘3003 0201’



Bit(s)	Name	Description
31-24	Entity State Mux Control 4 (Hardware debug)	Selection of these bits allows internal state machines, counters, etc. to show up on chip outputs enstate (63-48). Selection encoding is the same as multiplexer 1 control.
23-16	Entity State Mux Control 3 (Hardware debug)	Selection of these bits allows internal state machines, counters, etc. to show up on chip outputs enstate (47-32). Selection encoding is the same as multiplexer 1 control.
15-8	Entity State Mux Control 2 (Hardware debug)	Selection of these bits allows internal state machines, counters, etc. to show up on chip outputs enstate (31-16).

Bit(s)	Name	Description
7-0	Entity State Mux Control 1 (Hardware debug)	Selection of these bits allows internal state machines, counters, etc. to show up on chip outputs enstate (15-0). x‘00’ Disabled (no transition on outputs) x‘01’ Select CRSET 15-0 states. x‘02’ Select NPBUS 15-0 states. x‘03’ Select PCINT 15-0 states. x‘04’ Select PCINT 31-16 states. x‘05’ Select COMET 15-0 states. x‘06’ Select COMET 31-16 states. x‘07’ Select PAKIT 15-0 states. x‘08’ Select PAKIT 31-16 states. x‘09’ Select RXQUE 15-0 states. x‘0A’ Select RXQUE 31-16 states. x‘0B’ Select REASM 15-0 states. x‘0C’ Select LINKC 15-0 states. x‘0D’ Select SEGBF 15-0 states. x‘0E’ Select SEGBF 31-16 states. x‘0F’ Select SEGBF 47-32 states. x‘10’ Select SEGBF 63-48 states. x‘11’ Select CSKED 15-0 states. x‘12’ Select CHKSM 31-16 states. x‘13’ Select CHKSM 31-16 states. x‘14’ Select GPDMA 15-0 states. x‘15’ Select BCACH 15-0 states. x‘16’ Select BCACH 31-16 states. x‘17’ Select POOLS 15-0 states. x‘18’ Select POOLS 31-16 states. x‘19’ Select POOLS 47-32 states. x‘1A’ Select POOLS 63-48 states. x‘1B’ Select POOLS 79-64 states. x‘1C’ Select POOLS 95-80 states. x‘1D’ Select POOLS 111-96 states. x‘1E’ Select POOLS 127-112 states. x‘1F’ Select VIMEM 15-0 states. x‘20’ Select VIMEM 31-16 states. x‘21’ Select VIMEM 47-32 states. x‘22’ Select ARBIT 15-0 states. x‘23’ Select ARBIT 31-16 states. x‘24’ Select ARBIT 47-32 states. x‘25’ Select ARBIT 63-48 states. x‘26’ Select PCORE 15-0 states. x‘27’ Select PCORE 31-16 states. x‘28’ Select PCORE 47-32 states. x‘29’ Select PCORE 63-48 states. x‘2A’ Select DMAQS 15-0 states. x‘2B’ Select DMAQS 31-16 states. x‘2C’ Select DMAQS 47-32 states. x‘2D’ Select DMAQS 63-48 states. x‘2E’ Select SCLCK 15-0 states. x‘2F’ Select SCLCK 31-16 states. x‘30’ Select SCLCK 47-32 states. x‘31’ Select CSKED 31-16 states. x‘32’ Select CSKED 47-32 states. x‘33’ Select CSKED 63-48 states. x‘34’ Select VIMEM 63-48 states. x‘35’ Select TXLCD 15-0 states. x‘36’ Select TXLCD 31-16 states. x‘37’ Select TXLCD 47-32 states. x‘38’ Select TXLCD 63-48 states. x‘39’ Select REASM 31-16 states. x‘3A’ Select REASM 47-32 states. x‘3B’ Select REASM 63-48 states. x‘3C’-x ‘FF’ Reserved (do not toggle outputs)

3.3.21 INTST Delayed Interrupts DMA System Address 1

This register serves as the Delayed Interrupts DMA System Address. This register holds the value of the system DMA address to which the delay interrupt status data will be moved.

Length	64 bits
Type	Read/Write
Address	XXXX 0498 and 049C
Restrictions	None
Power On Reset Value	x‘0000 0000 0000 0000’

3.3.22 INTST Delayed Interrupts DMA System Address 2

This register serves as the Delayed Interrupts DMA System Address. This register holds the value of the system DMA address to which the delay interrupt status data will be moved.

Length	64 bits
Type	Read/Write
Address	XXXX 04A0 and 04A4
Restrictions	None
Power On Reset Value	x‘0000 0000 0000 0000’

3.3.23 Current PCI Master Address Counter for Debug

This register holds the current PCI Master address counter value. This register holds the value of the PCI Master DMA address. The function of this register is primarily for debug when a severe error occurs that stops the DMA engine from running.

Length	64 bits
Type	Read Only
Address	XXXX 04A8 and 04AC
Restrictions	None
Power On Reset Value	x‘0000 0000 0000 0000’

3.3.24 External Entity States Read

This register will get a snapshot value of the enstates pin I/O. This register will return whatever is on the output of the enstates mux output. It is strictly for debug and a convenient way to look at the current state of PNR internal logic. It is controlled by INTST Debug States Control.

Length	64 bits
Type	Read Only
Address	XXXX 04B0 and 04B4
Restrictions	None
Power On Reset Value	x‘0000 0000 xxxx xxxx’

3.4 Reset and Power-on Logic (CRSET/CBIST)

These entities perform BIST and flush operations. Chip software resets and clock selection can be controlled by the CRSET entity.

3.4.1 Reset Status Register

This register is used to indicate the last type of reset that occurred. A hardware reset will clear software reset status bits, but a software reset will not affect the hardware status bits.

Length 32 bits

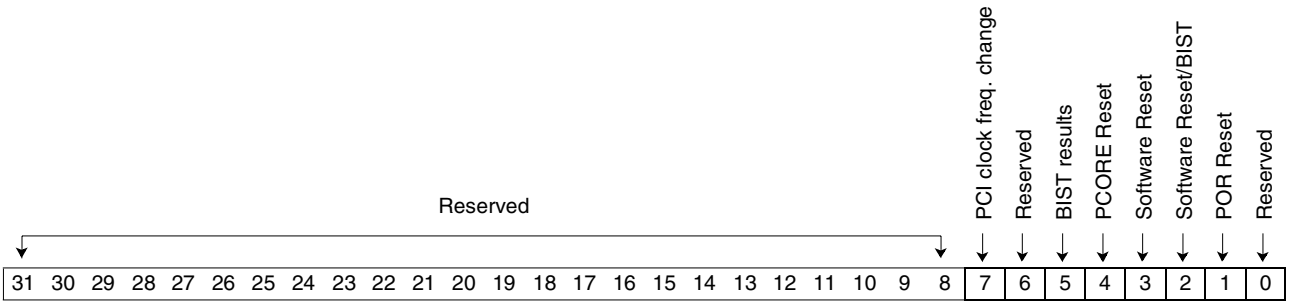
Type Read/Write

Address XXXX 0500

Power On Reset Value x‘0000 0002’

Software Reset Value After a software reset, bits 31-8 will read as x‘00 0000’ while bits 7-0 will read as ‘00B001Q0’ or ‘00B010Q0’ (binary), where Q is the state of the bit before the software reset and B is the state of the BIST results.

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7	PCI Clock Frequency Change	A value of ‘1’ means that the real time PCI frequency calculator has detected a major change in frequency and has calculated new range bits for the PLL. This bit will be set only when bit 9 of the *CRSET Control Register* is set to ‘0’ and the frequency change condition occurs. This will also set bit 16 in *3.3.8 INTST CPB Status Register* on page 92.
6	Reserved	Reserved. (Engineering note: A value of ‘1’ means that the out-of-phase detector circuit has triggered. This is just an indicator and is normal operation.)
5	BIST Results	A value of ‘1’ means that a failure occurred within the BIST checking logic.
4	PCORE Reset	The PCORE entity has been reset via a software reset request (bit 3 of Software Reset Register).
3	Software Reset	A Software Reset has occurred; the chip was flushed.
2	Software Reset/BIST	A Software Reset has occurred; and BIST/flush was run.
1	POR Reset	A POR Hardware Reset that flushed the chip has occurred.
0	Reserved	Reserved.

3.4.2 Software Reset Enable Register

This register protects the Software Reset Register. If this register is not set, then a reset will not occur. Write a x‘B4’ to this register to enable software reset. A software reset clears this register.

Length 32 bits

Type Read/Write

Address XXXX 0504

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Software Reset Enable	Setting these bits to x‘B4’ enables a software reset. If not set, a software reset will not occur.

3.4.3 Software Reset Register

This register generates a scan path flush reset of the chip, or a software initiated run of BIST, with the exception of the registers in the reset entity.

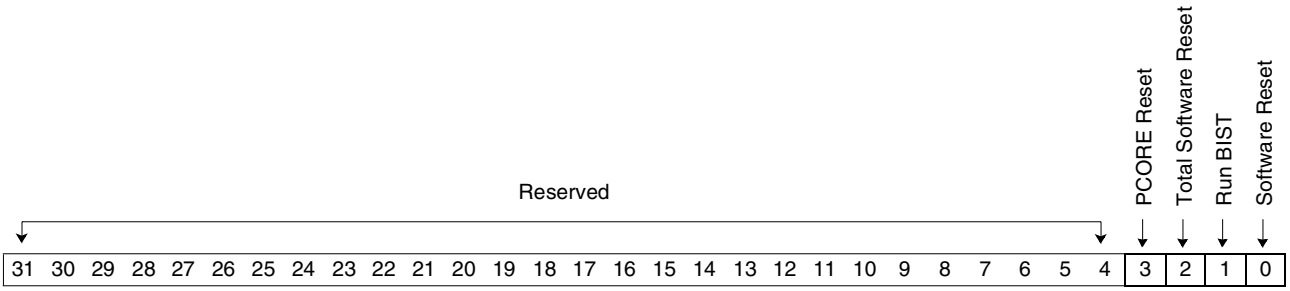
Length 32 bits

Type Write Only

Address XXXX 0508

Power On Reset Value x‘0000 0000’

Restrictions Writing to this register without first setting the Software Reset Enable Register will have no affect. The register will not be set, thus the order of writing the enable and the software reset is important; the enable must be written first. Additionally, all current operations being performed by the PNR must be terminated before doing a reset operation. A minimum number of enable bits to turn off would be bits 4, 5, and 6 in INTST Control Register and bit 2 in PCINT Config Word 1.



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3	PCORE Processor Reset	Writing this bit to a ‘1’ causes the internal processor core to reset.
2	Total Software Reset	Writing this bit to a ‘1’ causes a software reset and will be cleared after the software reset has occurred. The config registers in PCINT will also be put to their reset state.
1	Run BIST	Writing this bit to a ‘1’ causes BIST to run and will be cleared after the software reset has occurred. This function is primarily for pre-loading the BIST registers to get more test coverage.
0	Software Reset	Writing this bit to a ‘1’ causes a software reset and will be cleared after the software reset has occurred. The config registers in PCINT will not be affected by this reset.

3.4.4 Memory Type Register

This register indicates the type of memory used for control and Packet Memory so that reset hardware will know how to preserve it properly during a reset.

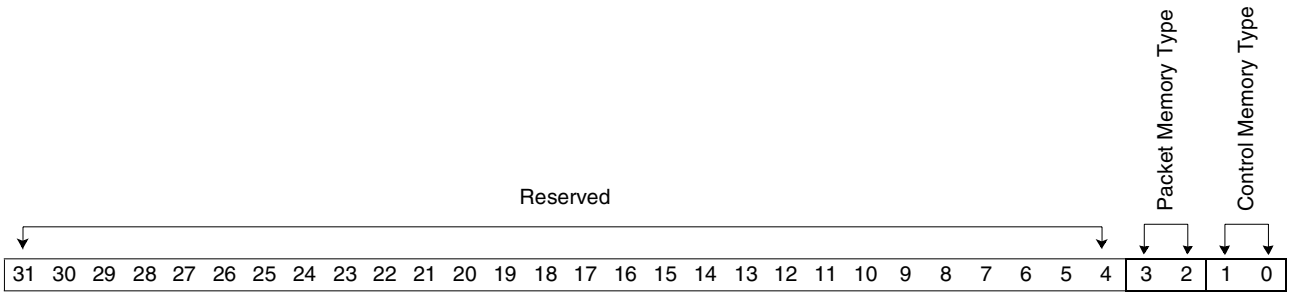
Length 32 bits

Type Read/Write

Address XXXX 050C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-2	Packet Memory Type	Decodes the same as bits 9-8 of *3.6.2 COMET/PAKIT Control Register* on page 138.
1-0	Control Memory Type	Decodes the same as bits nine through eight of *3.6.2 COMET/PAKIT Control Register* on page 138.

3.4.5 CRSET PLL Range Debug

Used to debug the PPL operation.

Length 32 bits

Type Read Only

Address XXXX 0518

Power On Reset Value x‘xxxx xxxx’

Bit(s)	Name	Description
31-30	Reserved	Reserved.
29-20	System Clock Counter	Read access to counter testing system clock operation.
19-14	PLL Tune Bits	Read access to tuning information sent to the PLL.
13-8	Phy Counter	Read access to counter testing PHY clock operation.
7	Reserved	Reserved.
6-4	FFCFG Bits(2-0)	Allows sampling of the FFCFG inputs.
3-2	PLL Range Bit A (1-0)	The current operational range of the PLL.
1	66 MHz Enable	The PCI clock is detected as being in the range of 66 MHz.
0	Under 25 MHz	The PCI clock is running at less than 25 MHz.

3.4.6 CRSET Control Register

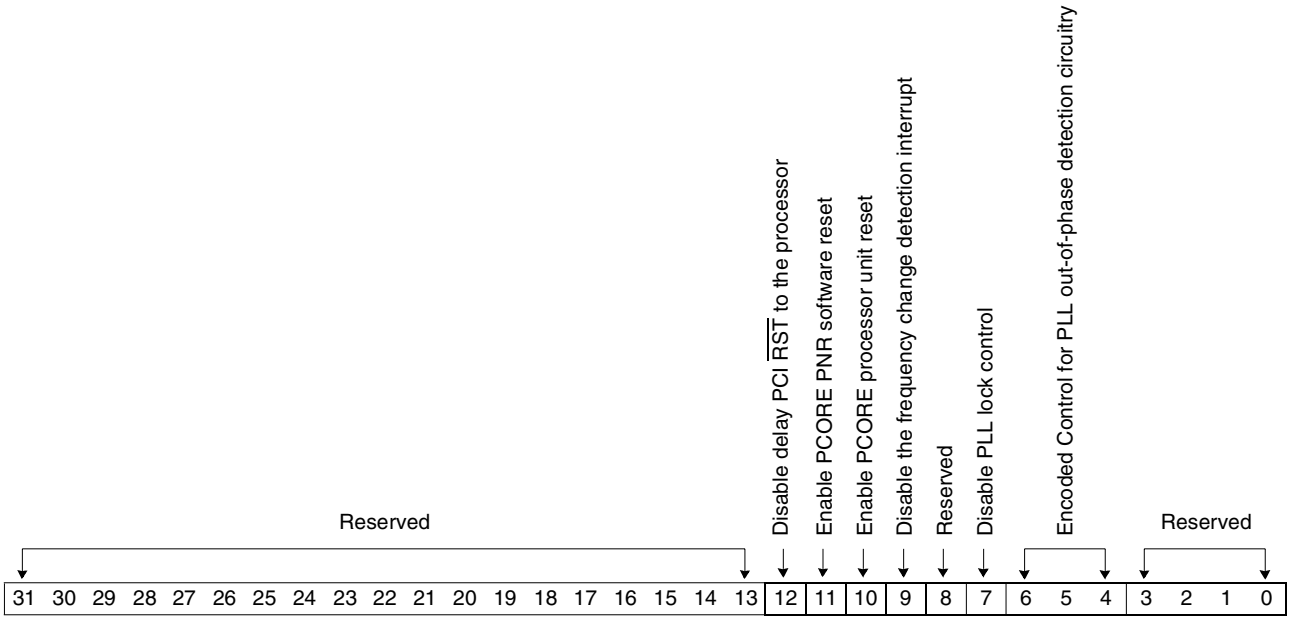
Used to control PCI frequency detection logic.

Length 32 bits

Type Read/Write

Address XXXX 0510

Power On Reset Value x‘0000 0330’



Bit(s)	Name	Description
31-13	Reserved	Reserved.
12	Disable Delay PCI $\overline{RST}$ to the PNR	Setting this bit to a ‘1’ will disable the function that delays a PCI bus reset to the PNR if a serial EPROM is attached and still busy accessing data from the prior reset. By disabling this function, any PCI requirement to tri-state the I/O drivers would be met, but EPROM initialization information would be lost.
11	Enable PCORE PNR Software Reset	Setting this bit to a ‘1’ will enable the PCORE entity to issue a PNR software reset.
10	Enable PCORE Processor Unit Reset	Setting this bit to a ‘1’ will enable the PCORE entity to issue a processor unit reset.
9	Disable the Frequency Change Detection Interrupt	Setting this bit to a ‘1’ will disable using the frequency change detection bit as an interrupt source to INTST.
8	Reserved	Reserved - must be set to a ‘1’. (Engineering note: Setting this bit to a ‘1’ will disable using the out-of-phase detection bit as an interrupt source to INTST.)
7	Disable PLL Lock Control	Setting this bit to a ‘1’ will disable using the PLL lock output to make state transitions in the out-of-phase detection logic.
6-4	Encoded Control for PLL Out-of-Phase Detection Circuitry	These bits determine how much time buffering is allowed before an out-of-phase condition is detected. For a value of ‘000’, a value of about 150 ps buffering is used. For each encoded increment value, an additional 150 ps is added. For example, the default value of three is about 600 ps of buffering.
3-0	Reserved	Reserved.

3.4.7 Clock Control Register

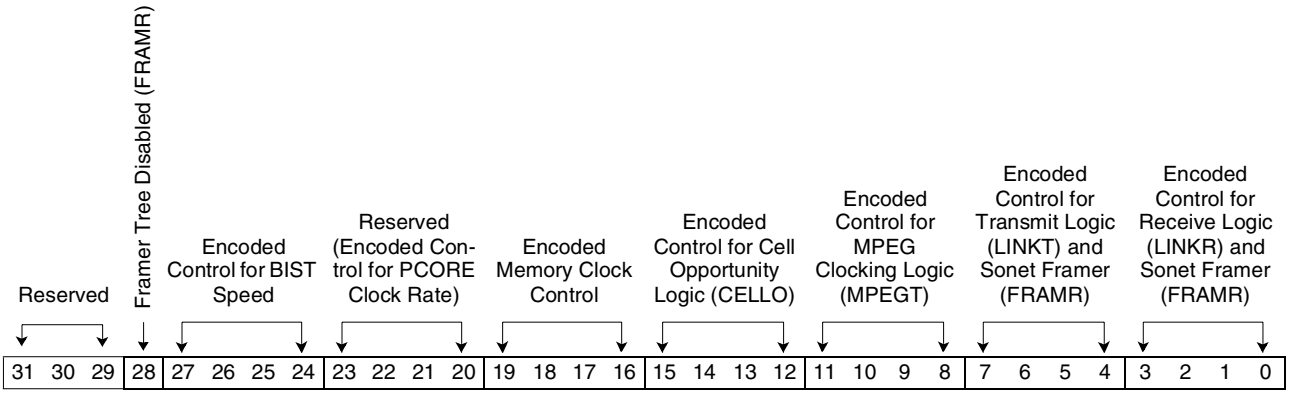
Used to disable clocks for power conservation and provide the Select A Clock function for MPEG and front end support. To change a nibble field in this register, always set it to '0' first, and then to the new value.

Length 32 bits

Type Read/Write

Address XXXX 0520

Power On Reset Value x'060E 5532'



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28	Framer Tree Disabled (FRAMR)	When set, this bit will disable the clock tree to the SONET Framer Logic.
27-24	Reserved (for Encoded Control for BIST Clock Rate)	Reserved.
23-20	Reserved (for Encoded Control for PCORE Clock Rate)	Reserved.
19-16	Memory Clock Control	Encoding of bits: X'D' Use an early version of the clock. X'E' Use a nominal version of the clock. X'F' Use a late version of the clock.
15-12	Encoded Control for Cell Opportunity Logic (CELLO)	Same as bits 3-0.
11-8	Encoded Control for MPEG Clocking Logic (MPEGT)	Same as bits 3-0.
7-4	Encoded Control for Transmit Logic (LINKT) and SONET Framer (FRAMR)	Same as bits 3-0.

Bit(s)	Name	Description
3-0	Encoded Control for Receive Logic (LINKR) and SONET Framer (FRAMR)	Below is the encoded value of the bits that select a given clock. Always refer to *"Select A Clock" Selection Matrix* below for inputs supported for each clock out type. x'0' Turn this clock off. x'1' Use the external MPEG oscillator. x'2' Use the external RX clock. x'3' Use the external TX clock. x'4' Reserved. x'5' Use the internal 15 ns clock. Assumes 33 or 66 MHz PCI clock. x'6' Use the internal 30 ns clock. Assumes 33 or 66 MHz PCI clock. x'7' Use the internal 60 ns clock. Assumes 33 or 66 MHz PCI clock. x'8' Use the internal 120 ns clock. Assumes 33 or 66 MHz PCI clock. x'9' Use the internal 240 ns clock. Assumes 33 or 66 MHz PCI clock. x'A' Use the internal 480 ns clock. Assumes 33 or 66 MHz PCI clock. x'B' Use the differential Receiver clock divided by eight. x'C' Use the differential Transmit clock divided by eight. x'D' Use the differential Receiver clock (chopped). x'E' Use the differential high speed receiver clock (divided by 8 and 50% duty cycle).

Table 13: "Select A Clock" Selection Matrix

Clock Frequency Base	CELLO BCO CCO	MPEGT BMT CMT	LINKT(TX) BTX CTX RTX	LINKR(RX) BRX CRX RRX	Nibble Code
HS RX Rec Diff Osc			X		X'E'
RX Rec Diff Osc				X	X'D'
TX/8 Diff Osc			X		X'C'
RX/8 Diff Osc				X	X'B'
480 ns	X	X	X	X	X'A'
240 ns	X	X	X	X	X'9'
120 ns	X	X	X	X	X'8'
60 ns	X	X	X	X	X'7'
30 ns	X	X	X	X	X'6'
15 ns	X	X	X	X	X'5'
Reserved					X'4'
TX Osc	X	X	X	X	X'3'
RX Osc	X	X	X	X	X'2'
MPEG OSC	X	X	X	X	X'1'
OFF	X	X	X	X	X'0'
Control Bits	15-12	11-8	7-4	3-0	

3.4.8 CBIST PRPG Results

This is the PRPG results register, updated after BIST has run. It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05B0

Power On Reset Value x‘FFFF FFFF’

3.4.9 CBIST MISR Results

This is the MISR results register, updated after BIST has run. It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05B4

Power On Reset Value x‘0000 0000’

3.4.10 CBIST BIST Rate

This register holds a counter value that separates the time between when the A clock and the B clock are launched during BIST. This allows finer tuning to how much power BIST uses versus how much testing gets done within the time allowed. It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05B8

Power On Reset Value x‘0000 0000’

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	A/B Clock Separation	Elapsed time between launch of clock A and clock B.

3.4.11 CBIST PRPG Expected Signature

This is the PRPG signature register, which should be written by the external EPROM code with the expected value of the signature, based on the value in CBIST CYCT Load Value and the clock selected for BIST to run from. It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05C0

Power On Reset Value x‘FFFF FFFF’

3.4.12 CBIST MISR Expected Signature

This is the MISR Signature Register, which should be written by the external EPROM code with the expected value of the signature, based on the value in CBIST CYCT Load Value and the clock selected for BIST to run from. It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05C4

Power On Reset Value x‘0000 0000’

3.4.13 CBIST CYCT Load Value

This register is the loaded value for the CBIST BIST Rate Register. The time for BIST to run can be computed by the following equation: (shift count) * (c30 clock*2) * (cycle time). It is used by the BIST function for chip test.

Length 32 bits

Type Read/Write

Address XXXX 05C8

Power On Reset Value x‘0000 5800’

Bit(s)	Name	Description
31-18	Reserved	Reserved.
17-0	BIST Iteration Count	Loaded value for the CBIST BIST Rate Register.

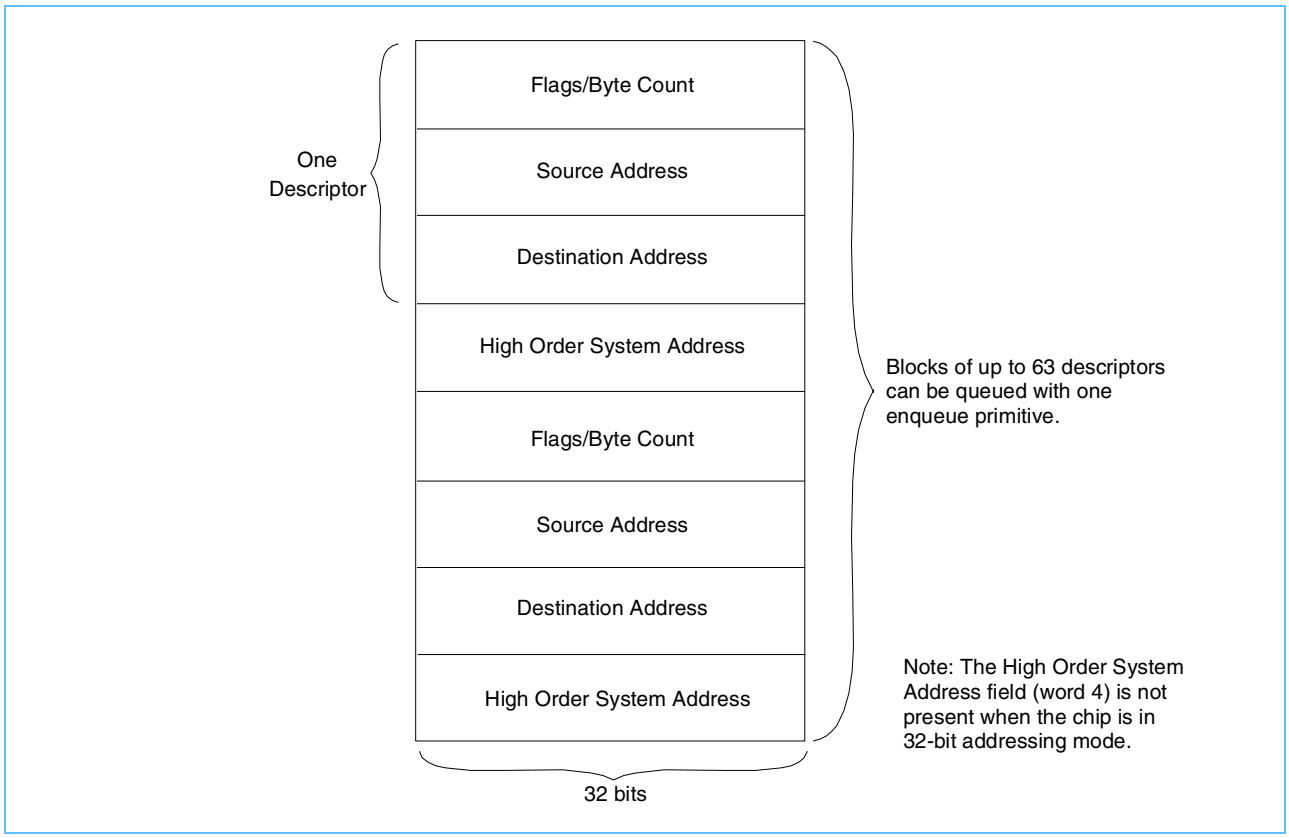
3.5 DMA Queues (DMAQS)

The following sections describe the features of DMAQS, how to set up DMAQS, and some troubleshooting tips.

3.5.1 DMA Descriptors

DMA descriptors can reside in either PCI/system memory space or the PNR memory space. Certain types of descriptors, called cut-through DMA descriptors, must be located in the PNR memory space. DMA descriptors that are located in the PNR memory space are more efficient to process because they do not need to be moved across the PCI bus. However, it is more costly for software to update across the bus. The best option is to mix descriptors in both locations. DMA descriptors that are infrequently changed should reside in the PNR memory, while dynamic descriptors should be placed in system memory. Descriptors located in the PNR memory space must fall in a definable address range. See *3.5.27 DMAQS Local Descriptor Range Registers* on page 134.

Figure 10: DMA Descriptor Layout



3.5.2 DMA Types and Options

The DMA descriptor is very versatile and can perform many actions. The following list shows some examples and possible flags to use. Other combinations are possible: see *3.5.24 DMAQS Transfer Count and Flag Register* on page 130.

Table 14: DMA Types and Flags

Hex Flags	DMA Operation
3000	Clear the current TCP checksum and include this DMA in the TCP checksum.
1000	Include this DMA in the TCP checksum and use previous checksum as seed.
0800	This DMA transfer is done in little endian mode.
0400	Upon completion of this DMA descriptor, the destination address from this descriptor is used as a packet address to be enqueued to transmit.
0100	Queue a DMA complete event when DMA is complete.
0080	Status in the status register is inhibited for this descriptor. This can be useful if ints/polling are being used to track when a particular DMA is complete.
0001	Move system memory to the PNR memory.
0010	Move the PNR memory to system memory.
0012	Move a single PNR register to system memory.
0013	Move PNR memory to system memory and free buffer. Upon DMA completion, the source address is used to free the PNR buffer.
0017	Auto-increment source address and move PNR memory to system memory and free buffer. Upon DMA completion, the source address is used to free the PNR buffer.
0002	Move a single PNR register to PNR memory.
0020	Move PNR memory to a single PNR register.
0021	Move system memory to a single PNR register.
0031	Move system memory to a new PNR buffer. A get buffer operation will be done to fill in the destination address using the low four bits of the destination address as a get pool ID.
0050	Move something to source address of next descriptor. Allows indirection.
0062	Move a single PNR register to destination address of the next descriptor. Allows a get buffer operation in descriptor chain. See the get buff flag for a better option.
0008	Use source address as immediate data. Allows up to four bytes of immediate data in the DMA descriptor.
0004	Auto-increment the source address. The source address picks up where it left off from the previous DMA descriptor.
000C	Auto-increment the source address and use as immediate data. One use is to free a packet after DMAing data. See the free buff flags for better options.
0040	Auto-increment the destination address. The destination address picks up where it left off from the previous DMA descriptor. One use is transmit scatter into an PNR virtual buffer.
2200	Hold the destination address. Useful for freeing a scatter DMA list, or doing a repetitive write to an PNR register.
1200	Hold the source address. Useful for doing a repetitive read from an PNR register.
Note: These are not the only options. Some of the above can be ORed together also.	

Using the above, you can efficiently do TCP check summing, place user events in receive queues, do register reads/writes, free buffers, and get buffers.

3.5.3 Descriptor Based DMAs

This is the recommended approach to processing DMAs. A single descriptor or a descriptor chain is built that describes the actions to take. The descriptor is then enqueued to the proper DMA Queue. The number of descriptors in the DMA chain is placed in the lower six bits of the descriptor address as it is enqueued.

3.5.4 Register Based DMAs

While register based DMAs can be enabled and used, they are not recommended because they are not as efficient and they do not leave a debug trail as the descriptors do in the DMA queue. These should not be used concurrently with descriptor-based DMAs for a particular queue, but register-based and descriptor-based DMAs can be used on different queues. One possible use for register-based DMAs is doing DMAs from the core.

3.5.5 Polling, Interrupts, or Events

There are several choices for handling DMA completion. First, the status register can be polled. While not very efficient, it is the easiest option. Second, you can use interrupts to tell when a DMA is done. Again, not very efficient. However, interrupts should be used to tell when a DMA error has occurred.

One way to deal with DMA completes is to use the RXQUE event mechanism. By generating events, the user can dump in DMA descriptors and clean up at a later time when it is convenient. The user can use the automatic DMA events using the queue on DMA complete flag, or the user can place a user event on an arbitrary queue by writing a DMA descriptor that does an explicit RXQUE enqueue with user data.

3.5.6 Error Detection and Recovery

Ideally, there should not be any errors. Errors are usually user errors in the DMA descriptor which need to be fixed and are not recoverable. Errors on the PCI bus (that is, parity) should not occur in a normal working system, and typically you do not want to recover them. However, if recovery is desired, the current DMA must be recovered in GPDMA. Upon successful completion of the recovered DMA, DMAQS will resume operation.

3.5.7 DMA/Queue Scheduling Options

There are three DMA queues. Queue 0 is higher priority than the other two. This high priority queue is always scheduled to go if the current descriptor is ready. The other two queues (Q1 and Q2) are of equal priority and are scheduled in a round robin fashion when the descriptor is ready. This is meant to provide a transmit DMA queue, receive DMA queue, and a high priority DMA queue. However, these queues can be used for any purpose by setting the routing registers properly.

The queues can be arbitrated after each DMA request length operation, after complete DMA descriptor chains complete, or after a single DMA descriptor in a chain completes. The queues can also be placed in true round robin mode, where all three queues have equal priority.

3.5.8 Address Size

DMAQS can be operated with either 32- or 64-bit System Addresses. See *3.1.21 PCINT 64-bit Control Register* on page 56. All DMAQS address registers are 64 bits wide. In 32-bit addressing mode, the high order portion of address registers are initialized at reset to ‘0’ and cannot be modified. In 32 bit addressing mode, word four of the DMA Buffer Descriptor is ignored.

3.5.9 Data Width

DMAQS recognizes 64 bit writes to 64 bit internal registers. DMAQS internal 64-bit registers may be written either as a 64-bit entity, or by two 32-bit writes. All DMAQS registers are memory mapped on a 64-bit boundary (address bits 2:0 = 0). When in 64-bit addressing mode, an address register is updated with 32 bit writes (atomicity of update cannot be guaranteed). The user should use semaphores to assure the integrity of the operation.

3.5.10 Initialization of DMAQS

DMAQS is very simple to set up by following these steps:

1. Set up each of the three DMA queues.

   To do this, you need to know the size of each queue (see *3.5.12 DMAQS Upper Bound Registers* on page 120 for choices). Given this information, the DMA queue is set up with two register writes in diagnostic mode (see *3.5.19 DMAQS Control Register* on page 126).

   ```
   dmaqs->lowerBound[q] = baseAddress;              // should be aligned with size of queue
   dmaqs->upperBound[q] = encodedSize;              // set encoded size of dma queue
   or dmaqs->bounds[q] = baseAddress + encodedSize; // if 64 bit data is enabled
   ```

   The data structure for the DMA queue is now set up.

2. Set up the queue thresholds if they are being used:

   ```
   dmaqs->threshold[q]=threshold;                   // set threshold size to be interrupted;
                                                       may also need to set int mask
   ```

3. Set up the local DMA descriptor range if local descriptors are being used:

   ```
   dmaqs->localDescriptorLowerBound = localDescriptorBase;// set base addr of local desc in PNR
                                                             memory
   dmaqs->localDescriptorUpperBound = localDescriptorEnd;// set ending addr of local desc in PNR
                                                             memory
   ```

4. Set up any options that are being used in the DMAQS Control Register:

   ```
   dmaqs->control[set] = ENABLE_DMA_QUEUES | CLR_CHECKSUM_TO_FOXES; // set options/modes
   ```

5. Finally, clear the diagnostic bit:

   ```
   dmaqs->control[clr] = DIAG_MODE;                 // clear the diag mode bit
   ```

6. Need to set up memory bank selection if necessary, but normally Control Memory is used.

3.5.11 DMAQS Lower Bound Registers

These registers specify the lower bound of the corresponding DMA queue data structure. The head, tail, and length of the DMA queue are initialized when this register is written. When the DMA queue wraps past the upper bound, it wraps back to the value in the lower bound register, thus implementing the DMA queue as a circular buffer.

When this register is written, the corresponding DMA queue is essentially reset. This is because the head, tail, and length of the queue are all reset.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0604
	Queue 1	XXXX 0684
	Queue 2	XXXX 0704
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. These registers can only be written when the diagnostic bit has been set in the DMAQS Control Register. The alignment should correspond to the size specified in the upper bound register. For example, it should be 4K aligned if the upper bound specifies 4K size. The low order nine bits are not writable and read back ‘0’.	

3.5.12 DMAQS Upper Bound Registers

These registers specify the encoded size/upper bound of the corresponding DMA queue data structure. The actual upper bound is calculated by adding the decoded queue size to the lower bound. When the DMA queue wraps past the upper bound, it wraps back to the lower bound register, thus implementing the DMA queue as a circular buffer.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0600
	Queue 1	XXXX 0680
	Queue 2	XXXX 0700
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. These registers can only be written when the diagnostic bit has been set in the DMAQS Control Register.	

Bit(s)	Name	Description
31-30	Location of Queue	00 Use the location specified in the mode register. 01 Queue located in On Chip Memory. 10 Queue located in Control Memory. 11 Queue located in Packet Memory.
27-24	Descriptor Alignment and Event Type/Location	0000 64 byte aligned, and original 2.5 events 0001 8 byte aligned, new events in lower 3 bits 0010 16 byte aligned, new events in lower 3 bits 0011 32 byte aligned, new events in lower 3 bits 0100 64 byte aligned, new events in lower 3 bits 1000 4 byte aligned, new events in upper nibble 1001 8 byte aligned, new events in upper nibble 1010 16 byte aligned, new events in upper nibble 1011 32 byte aligned, new events in upper nibble 1100 64 byte aligned, new events in upper nibble
2-0	Encode Upper Bound	000 512 bytes of memory 001 1K bytes of memory 010 2K bytes of memory 011 4K bytes of memory 100 8K bytes of memory 101 16K bytes of memory 110 32K bytes of memory 111 64K bytes of memory

The Following are the new 3 bit events mentioned above:

000: TX DMA complete
001: RX DMA complete
010: TX DMA complete with error
011: RX DMA complete with error
100: TX DMA complete with virtual error
101: zero address in dma desc src/dst addr

3.5.13 DMAQS Head Pointer Registers

These registers point to the head element of the corresponding DMA queue. During normal operations, these registers do not need to be read or written; they are used by the PNR to implement the DMA queues. These registers are initialized when the DMAQS Lower Bound Registers for the corresponding DMA queue are written.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0608
	Queue 1	XXXX 0688
	Queue 2	XXXX 0708
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. They can only be written when the diagnostic bit has been set in the DMAQS Control Register. The head pointer registers are 4-byte aligned (low order two bits are always ‘0’). Bits 31-17 are calculated internally and are not writable.	

3.5.14 DMAQS Tail Pointer Registers

These registers point to the next free element of the corresponding DMA queue.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 060C
	Queue 1	XXXX 068C
	Queue 2	XXXX 070C
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. They can only be written when the diagnostic bit has been set in the DMAQS Control Register. The head pointer registers are four-byte aligned (low order two bits are always ‘0’). Bits 31-17 are calculated internally and are not writable.	

3.5.15 DMAQS Length Registers

These registers specify the length in bytes of the corresponding DMA queue. This register is cleared when the corresponding DMAQS Lower Bound Register is written.

Length	32 bits	
Type	Read Only	
Address	Queue 0	XXXX 0614
	Queue 1	XXXX 0694
	Queue 2	XXXX 0714
Power On Reset Value		x‘0000 0000’
Restrictions	The lengths are calculated and cannot be written.	

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Queue Length	Current length of respective queue.

3.5.16 DMAQS Threshold Registers

These registers specify a queue length threshold at which the corresponding status bit is generated.

These registers should be set equal to the queue length that should cause status to be generated. For example, if the value was set to five, then no interrupt would be generated until the queue was length five or more for the corresponding DMA queue. The threshold is level sensitive, so as long as the length is greater than or equal to the threshold, the corresponding status bit is set. When this register is set to ‘0’, no thresholding occurs.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 061C
	Queue 1	XXXX 069C
	Queue 2	XXXX 071C
Power On Reset Value		x‘0000 0000’
Restrictions	Must be a multiple of four.	

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Queue Length Threshold	These bits indicate the minimum number of entries that must be in the respective queue to set that queue’s Threshold Exceeded bit in the *DMAQS Status Register* on page 123.

3.5.17 DMAQS Status Register

This register indicates the source(s) of the interrupt(s) pending.

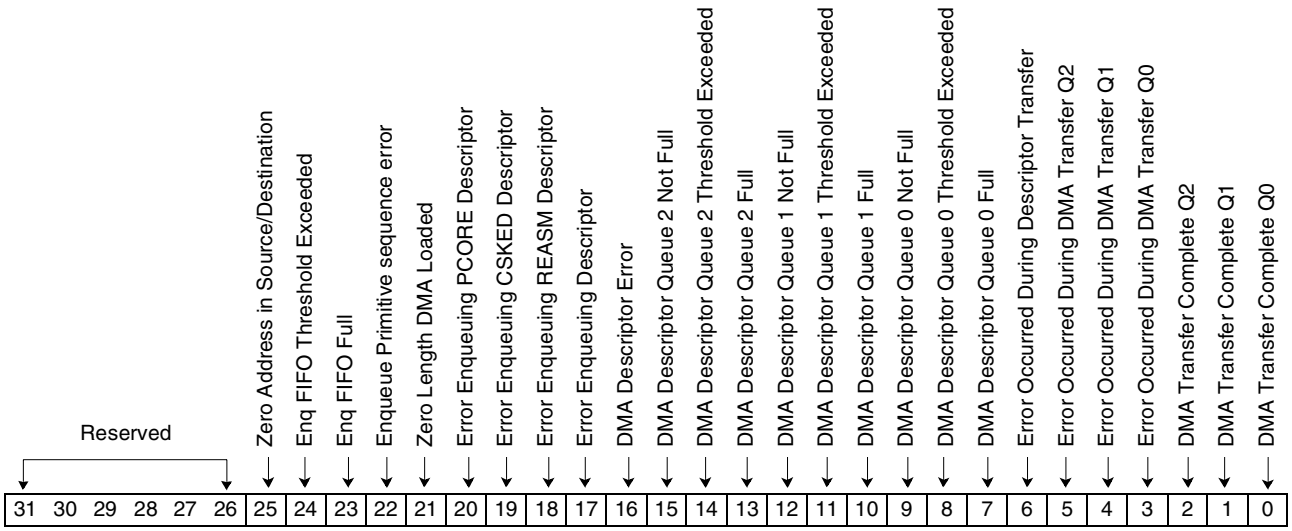
Length 32 bits

Type Set/Clear

Address XXXX 06F0 and 06F4

Power On Reset Value x‘0000 9200’

Restrictions None



Bit(s)	Name	Description
31-26	Reserved	Reserved.
25	Zero Address in Source/Destination	When set, a zero address was detected in the source or destination field of a DMA descriptor. The remainder of the descriptor chain was skipped and an event was enqueued to the DMA complete queue. This may or may not be an error condition. It is not an error if the get buffer mode is being used and no buffer was available. In this case, the descriptor can be retried or discarded by software.
24	Enq FIFO Threshold Exceeded	When set, the DMA enqueue FIFO length threshold has been exceeded.
23	Enq FIFO Full	When set, the DMA enqueue FIFO is full and further enqueues will be held off. This bit is hot and cannot be reset.
22	Enqueue Primitive Sequence Error	This bit is set when an improper sequence is detected for loading the DMAQS Enqueue DMA Descriptor Primitive in 64 bit addressing mode.
21	Zero Length DMA Loaded	A descriptor was loaded that had a DMA length equal to zero. This will not stop the DMA engine, but it is technically a user error.
20	Error Enqueuing PCORE Descriptor	A descriptor was enqueued from PCORE with a chain length of zero.
19	Error Enqueuing CSKED Descriptor	A descriptor was enqueued from CSKED with a chain length of zero.
18	Error Enqueuing REASM Descriptor	A descriptor was enqueued from REASM with a chain length of zero.

Bit(s)	Name	Description
17	Error Enqueuing Descriptor	A descriptor was enqueued with a chain length of zero.
16	DMA Descriptor Error	An invalid transfer was described by the value loaded into the Transfer Count and Flag register.
15	DMA Descriptor Queue 2 Not Full	The DMA descriptor Queue 2 is not full. This bit always contains the status of the queue and is therefore is not writable.
14	DMA Descriptor Queue 2 Threshold Exceeded	The threshold for DMA descriptor Queue 2 has been exceeded.
13	DMA Descriptor Queue 2 Full	The DMA descriptor Queue 2 is full. This bit always contains the status of the queue and is therefore is not writable.
12	DMA Descriptor Queue 1 Not Full	The DMA descriptor Queue 1 is not full. This bit always contains the status of the queue and is therefore is not writable.
11	DMA Descriptor Queue 1 Threshold Exceeded	The threshold for DMA descriptor Queue 1 has been exceeded.
10	DMA Descriptor Queue 1 Full	The DMA descriptor Queue 1 is full. This bit always contains the status of the queue and is therefore is not writable.
9	DMA Descriptor Queue 0 Not Full	The DMA descriptor Queue 0 is not full. This bit always contains the status of the queue and is therefore is not writable.
8	DMA Descriptor Queue 0 Threshold Exceeded	The threshold for DMA descriptor Queue 0 has been exceeded.
7	DMA Descriptor Queue 0 Full	The DMA descriptor Queue 0 is full. This bit always contains the status of the queue and is therefore is not writable.
6	Error Occurred During Descriptor Transfer	Hardware errors occurred transferring the DMA descriptor. The transfer stopped after detecting the error. If the descriptor transfer is finished or is to be terminated, the byte count register must be written to clean up the failed descriptor transfer. Before this bit is reset, the DMA descriptor queue must contain the valid descriptor data.
5	Error Occurred During DMA Transfer Q2	Hardware errors occurred during the last transfer on Queue 2. The transfer stopped after detecting the error. Inspect the GPDMA registers for the actual location of error.
4	Error Occurred During DMA Transfer Q1	Hardware errors occurred during the last transfer on Queue 1. The transfer stopped after detecting the error. Inspect the GPDMA registers for the actual location of error.
3	Error Occurred During DMA Transfer Q0	Hardware errors occurred during the last transfer on Queue 0. The transfer stopped after detecting the error. Inspect the GPDMA registers for the actual location of error.
2	DMA Transfer Complete Q2	The DMA transfer has completed for Queue 2.
1	DMA Transfer Complete Q1	The DMA transfer has completed for Queue 1.
0	DMA Transfer Complete Q0	The DMA transfer has completed for Queue 0.

3.5.18 DMAQS Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *DMAQS Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from DMAQS to INTST if the condition is detected.

Length	32 bits
Type	Set/Clear
Address	XXXX 0670 and 0674
Power On Reset Value	x'0026 0078'
Restrictions	None

3.5.19 DMAQS Control Register

This register is used to set options for DMAQS.

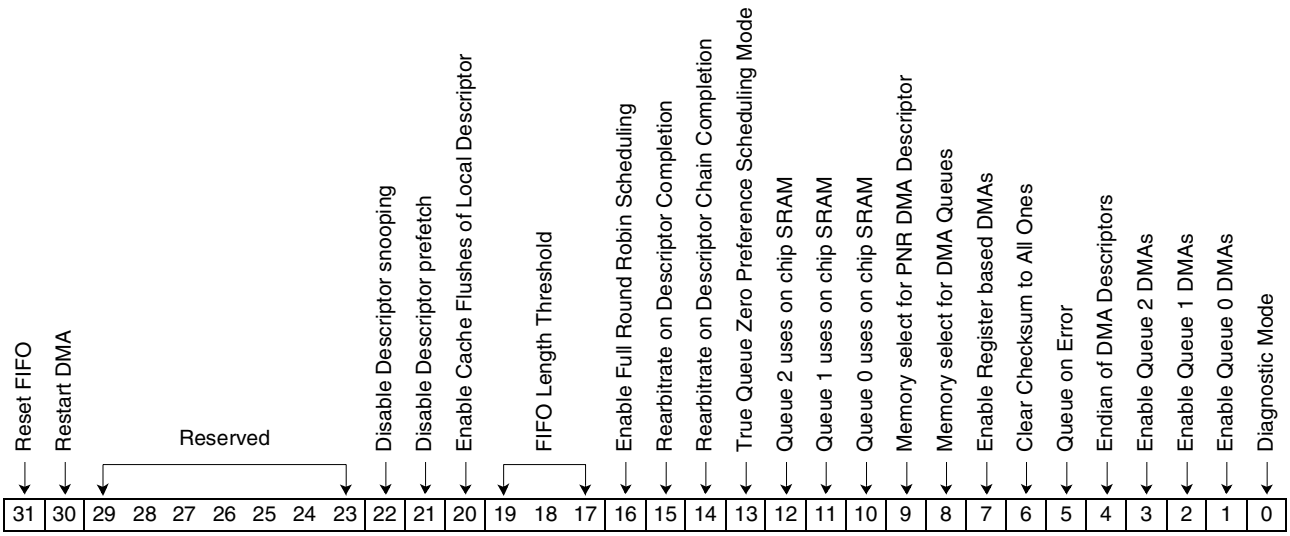
Length 32 bits

Type Set/Clear

Address XXXX 0770 and 0774

Power On Reset Value x‘000C 0001’

Restrictions See bit descriptions.



Bit(s)	Name	Description
31	Reset FIFO	When this bit is set, the internal DMA enqueue FIFO is flushed, and this bit is reset. The result is that this bit will always be read as a ‘0’. This bit can only be set in diagnostic mode.
30	Restart DMA	When this bit is set, the internal DMA state machine restarts the current DMA that is stopped, and this bit is reset. The result is that this bit will always be read as a ‘0’. This bit should only be used at the specific recommendation of an PNR developer.
29-23	Reserved	Reserved.
22	Disable Descriptor snooping	When this bit is set, the DMA descriptor snooping logic is disabled. When this bit is enabled, PNR performance may be enhanced.
21	Disable Descriptor prefetch	When this bit is set, the next descriptor prefetch logic is disabled. Performance may be enhanced by enabling this function.
20	Enable Cache Flushes of Local Descriptor	When this bit is set, all local DMA descriptors are flushed out of BCACH before being used. This only needs to be used if local DMA descriptors are in Packet Memory and are updated via the slave interface. Cut-through descriptors do not fall in this category.
19-17	FIFO Length Threshold	This value is used to set the FIFO length threshold. When this threshold is exceeded, bit 24 of the *DMAQS Status Register* is set.
16	Enable Full Round Robin Schedul-ing	When this bit is set, all three DMA queues are of equal priority. When cleared, Queue 0 is higher priority than queues 1 and 2.

Bit(s)	Name	Description
15	Rearbitrate on Descriptor Completion	When this bit is set, the DMA queues are rearbitrated after each individual DMA descriptor completes.
14	Rearbitrate on Descriptor Chain Completion	When this bit is set, the DMA queues are rearbitrated after full DMA descriptor chains complete. This bit takes precedence over bit 15. When both bits 14 and 15 are cleared, the queues are rearbitrated after each DMA request length operation.
13	True Queue Zero Preference Scheduling Mode	Bit 13 is provided to ensure compatibility with previous chips. In version 2.1 and before, Queue 0 would not be scheduled immediately after itself if queue 1 or queue 2 were ready when a queue 0 DMA completed. This was because it took at least one cycle to reload the queue registers. In the PNR, the queue registers are loaded while the arbitration for the next DMA is being done, if preloading or snooping is enabled. In this case, with bit 17 set, a Queue 0 DMA may be immediately followed by another Queue 0 DMA. With bit 17 reset, the scheduling (with all queues ready) is q0q1q0q2q0q1.... This mode is provided to give Queue 0 scheduling preference without permitting it to lock out the other two queues.
12	Queue 2 Uses On-Chip SRAM	This bit directs queue 2 to fetch all DMA descriptors from the On-Chip SRAM. Bits 63-18 of the system descriptor address will be ignored.
11	Queue 1 Uses On-Chip SRAM	This bit directs queue 1 to fetch all DMA descriptors from the On-Chip SRAM. Bits 63-18 of the system descriptor address will be ignored.
10	Queue 0 Uses On-Chip SRAM	This bit directs queue 0 to fetch all DMA descriptors from the On-Chip SRAM. Bits 63-18 of the system descriptor address will be ignored.
9	Memory Select for PNR DMA Descriptor	When this bit is set, the DMA descriptors that are located in the PNR are located in Packet Memory. Otherwise they are located in Control Memory.
8	Memory Select for DMA Queues	When this bit is set, the DMA Queues are located in Packet Memory. Otherwise they are located in Control Memory.
7	Enable Register Based DMAs	When this bit is set, source, destination, count, and system descriptor address (SDA) registers can be written to start a DMA.
6	Clear Checksum to All Ones	When this bit is set and the DMAQS Checksum Register is cleared, the DMAQS Checksum Register is set to x‘ffff’. When this bit is cleared and the DMAQS Checksum Register is cleared, the DMAQS Checksum Register is set to ‘0’. This option should be used if the TCP/IP checksum should never be set to ‘0’ (x‘ffff’ is ‘0’ also).
5	Queue on Error	When set, this bit causes any DMA error to log an error event.
4	Endian of DMA Descriptors	When set, this bit indicates that DMA descriptors in system memory are in little endian format. The default is big endian.
3	Enable Queue 2 DMAs	This bit enables DMA Queue 2.
2	Enable Queue 1 DMAs	This bit enables DMA Queue 1.
1	Enable Queue 0 DMAs	This bit enables DMA Queue 0.
0	Diagnostic Mode	When this bit is set, DMAQS is in diagnostic mode.

3.5.20 DMAQS Enqueue DMA Descriptor Primitive Register

This register enqueues a DMA descriptor chain to the corresponding DMA queue. The write data is the address of the descriptor chain that describes the DMA transfers. The low six bits contain a count of the number of DMA descriptors in this chain. After the DMA descriptors are enqueued by writing to this register, the chain of descriptors is fetched from system memory and the DMA transfers described by the chain of descriptors are performed. In 32 bit addressing mode, the low-order 32 bits of the register are written, and the high-order 32 bits are reset when the register is loaded.

Length	64 bits	
Type	Write	
Address	Queue 0	XXXX 0620
	Queue 1	XXXX 06A0
	Queue 2	XXXX 0720
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	None	

3.5.21 DMAQS Source Address Register

This register is used to set and keep track of the Source Address during a DMA transfer. This is the source for the current DMA transfer. A bit in the Transfer Count and Flag Register determines whether the source address is internal to the PNR or is a system address. In 32-bit addressing mode, the low-order 32 bits of the register are written, and the high-order 32 bits are reset when the register is loaded.

Length	64 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0638
	Queue 1	XXXX 06B8
	Queue 2	XXXX 0738
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	None	

3.5.22 DMAQS Destination Address Register

This register is used to set and keep track of the destination address during a DMA transfer. This is the Destination address for the current DMA transfer. In 32-bit addressing mode, the low-order 32 bits of the register are written, and the high-order 32 bits are reset when the register is loaded. A bit in the Transfer Count and Flag Register determines whether the destination address is internal to the PNR or is a system address.

Length	64 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0628
	Queue 1	XXXX 06A8
	Queue 2	XXXX 0728
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	None	

3.5.23 DMAQS Buffer Address Register

This register is used to set and keep track of the POOLS Buffer address during a DMA transfer. When the DMA Descriptor directs that a new buffer address be obtained from POOLS, this is the Buffer Address for the current DMA transfer. A bit in the Transfer Count and Flag Register determines whether a buffer address has been obtained for this descriptor. This register can be written to an RXQUE queue. The low-order seven bits should be set to x‘2a’, the event code for Assign Pool Buffer events.

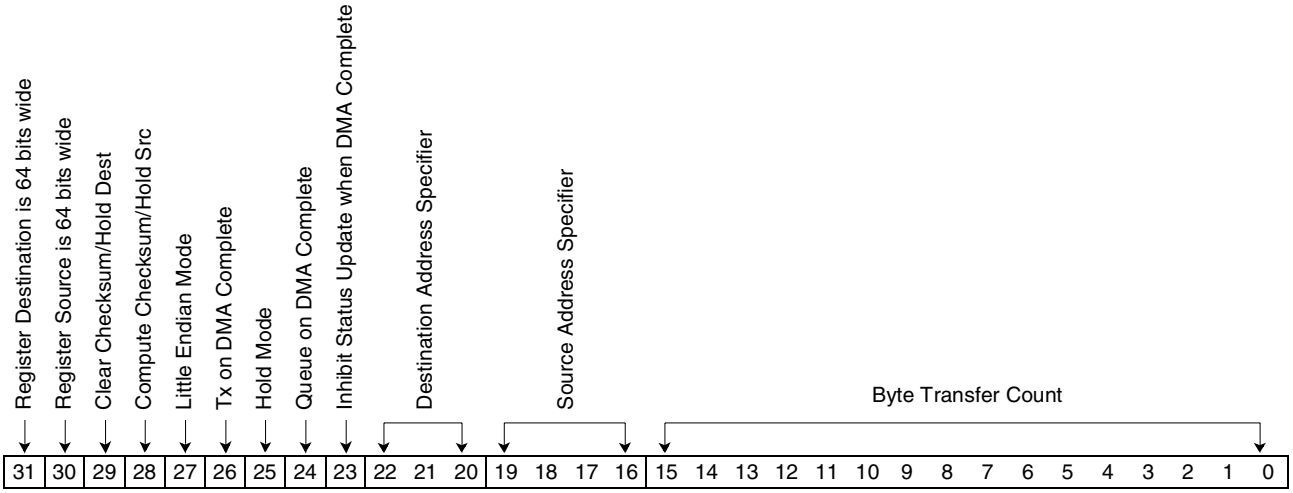
This is the Destination address for the current DMA transfer.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0630
	Queue 1	XXXX 06B0
	Queue 2	XXXX 0730
Power On Reset Value		x‘0000 002A’
Restrictions	These registers should not be written during normal system operation. The low-order 7 bits are set to x‘2A’ and should not be modified. This is the event code for BFA events in RXQUE.	

3.5.24 DMAQS Transfer Count and Flag Register

This register specifies the type and number of bytes transferred during a DMA transfer. The lower 16 bits are a counter of the number of bytes transferred during a DMA transfer. The upper 16 bits specify the type of transfer.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0644
	Queue 1	XXXX 06C4
	Queue 2	XXXX 0744
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31	Register Destination is 64-Bits wide	These bits must be used with bits 25 and 29 (see below).
30	Register Source is 64Bits wide	
29	Clear Checksum/Hold Dest	When this bit is set, the checksum and the alignment state are cleared.
28	Compute Checksum/Hold Src	When this bit is set, a checksum will be computed over this DMA segment.
27	Little Endian Mode	When this bit is written to ‘0’, this DMA channel operates in big endian mode. When set to ‘1’, the channels operate in little endian mode. In little endian mode, both the source and destination must be aligned on four-byte boundaries.
26	Tx on DMA Complete	When set, the destination address is used as the packet address that is to be enqueued to CSKED to be transmitted. The lower bits are set to ‘0’ so the buffer base is used for the CSKED enqueue operation.

Bit(s)	Name	Description
25	Hold Mode	When set, bits 31-28 are redefined to allow the source or destination address to be held instead of incremented. Bit 29 becomes hold destination address and bit 28 becomes hold source address. This allows a single DMA descriptor to do an N-to-1 or 1-to-N transfer. For example, an entire scatter DMA list can be freed to a receive queue enqueue register. The address being held must be a register address. When holding, the maximum length is 252 bytes. When holding, the source or destination is incremented by four when the DMA completes (for auto-increment mode). Bit 31 becomes destination address 64 bits wide. Bit 30 becomes source address 64 bits wide. This destination is required to properly update 64 bit wide registers when hold mode is asserted.
24	Queue on DMA Complete	When this bit is set, the upper 26 bits of the DMAQS System Descriptor Address register will be queued to the DMA event queue when the DMA completes. If descriptors are not being used to set up the DMA, then before starting the DMA, the DMAQS System Descriptor Address register should be loaded before starting the DMA with a value to identify this transfer. If descriptors are being used, the DMAQS System Descriptor Address register will be loaded automatically with the system address of the descriptor block at the time it is processed.
23	Inhibit Status Update when DMA Complete	Normally a bit will be set in the status register when the DMA completes without error. If this bit is set, this update will not be done. This bit is useful when multiple DMAs are to be done and an interrupt is only desired on the last transfer. The DMA error status bits are not affected by this bit.
22-20	Destination Address Specifier	These bits specify how the destination address should be used for this DMA descriptor. The following are the valid patterns: 000 PNR memory address: The destination address specifies an PNR internal memory address. 001 PCI Bus Address: The destination address specifies a PCI bus address. 010 PNR Register Address: The destination address specifies an PNR register address. Only the low 16 bits must be specified. 011 Get PNR Buffer: The low four bits of the destination address specify a pool ID from which to get a buffer. If a buffer is not available, a zero destination address event or appropriate status is raised. Otherwise the buffer address is used as an PNR memory address. 100 Auto Increment Destination Address: The destination address is sourced from the previous DMA instead of the destination address specified in the descriptor. 101 Next Source Address: The destination address is the address of the source address field of the next descriptor in the current DMA chain. Using this feature allows indirection. 110 Next Destination Address: The destination address is the address of the destination address field of the next descriptor in the current DMA chain. Using this feature allows operations like doing a get buffer in the DMA descriptor chain. 111 Offset Destination Address: The Destination Address is a positive offset from the DMAQS Buffer Address Register. Using this feature allows, for example, storing the checksum value in the header of the packet. Others Reserved: Reserved and flagged as errors.

Bit(s)	Name	Description
19-16	Source Address Specifier	These bits specify how the source address should be used for this DMA descriptor. The following are the valid patterns: 0000 PNR Memory Address: The source address specifies an PNR internal memory address. 0001 PCI bus address: The source address specifies a PCI bus address. 0010 PNR Register Address: The source address specifies an PNR register address. Only the low 16 bits must be specified. 0011 PNR Memory Address and Free Buffer when DMA Complete: The source address specifies an PNR internal memory address, and this address will be freed to POOLS when the DMA is complete. -100 Auto Increment Source Address: The source address is sourced from the previous DMA instead of the source address specified in the descriptor. -111 Auto Increment Source Address and Free Buffer when DMA Complete: The source address is sourced from the previous DMA instead of the source address specified in the descriptor. The source address specifies an PNR internal memory address, and this address will be freed to POOLS when the DMA is complete. 1000 Immediate Data: Use the Source Address Field as immediate data. The data is 4 bytes in 32-bit addressing mode or eight bytes when in 64 bit addressing mode. If the count is greater than the data size, the data is repeated. 1011 Immediate Data and Free Buffer when DMA Complete: Use the Source Address Field as immediate data. The data is 4 bytes in 32 bit addressing mode or eight bytes when in 64-bit addressing mode. If the count is greater than the data size, the data is repeated. The source address will be freed to POOLS when the DMA is complete. Others Reserved: Reserved and flagged as errors.
15-0	Byte Transfer Count	These bits indicate the number of bytes to transfer. A non-zero value in this field will start the DMA transfer.

3.5.25 DMAQS System Descriptor Address Register

The upper 57 bits contain the address of the current descriptor block and the lower seven bits contain the number of descriptors in the chain that remain to be processed. When doing register-based DMAs, the low six bits are set to ‘000001’ when the DMAQS Transfer Count and Flag Register is written. If DMA descriptors are used for DMA transfers, this register will contain the system address of the current descriptor block and the number of descriptors that remain to be processed. This address may be queued on DMA completion to correlate DMA transfers with system control blocks. In 32-bit addressing mode, the low-order 32 bits of the register are written, and the high-order 32 bits are reset when the register is loaded.

Length	64 bits	
Type	Read/Write	
Address	Queue 0	XXXX 0648
	Queue 1	XXXX 06C8
	Queue 2	XXXX 0748
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	This register should not be written if descriptors are going to be used to set up DMA transfers. If it is used, it must be written to 0 before descriptors are enqueued.	

3.5.26 DMAQS Checksum Register

This register contains the accumulated checksum value. It can also be used to initialize the checksum with a seed value. The most significant bit contains the alignment state (1 = odd, 0 = even alignment). The alignment state is significant between subsequent checksummed DMAs.

This register can be read at four different addresses. The base address returns the unmodified accumulated checksum. The base address +4 returns the inverted accumulated checksum. The base address + 8 returns the byte-swapped accumulated checksum. The base address + 12 returns the inverted byte-swapped accumulated checksum.

Length	32 bits	
Type	Read/Write	
Address	Q0 Sum	XXXX 0654
	Q0 Inv Sum	XXXX 065C
	Q0 Swapped Sum	XXXX 0664
	Q0 Inv Swapped	XXXX 066C
	Q1 Sum	XXXX 06D4
	Q1 Inv Sum	XXXX 06DC
	Q1 Swapped Sum	XXXX 06E4
	Q1 Inv Swapped	XXXX 06EC
	Q2 Sum	XXXX 0754
	Q2 Inv Sum	XXXX 075C
	Q2 Swapped Sum	XXXX 0764
	Q2 Inv Swapped	XXXX 076C
Power On Reset Value	Q0 Sum	x‘0000 0000’
	Q0 Inv Sum	x‘0000 FFFF’
	Q0 Swapped Sum	x‘0000 0000’
	Q0 Inv Swapped	x‘FFFF 0000’
	Q1 Sum	x‘0000 0000’
	Q1 Inv Sum	x‘0000 FFFF’
	Q1 Swapped Sum	x‘0000 0000’
	Q1 Inv Swapped	x‘FFFF 0000’
	Q2 Sum	x‘0000 0000’
	Q2 Inv Sum	x‘0000 FFFF’
	Q2 Swapped Sum	x‘0000 0000’
	Q2 Inv Swapped	x‘FFFF 0000’
Restrictions	Only the base address accepts write data. All four addresses return read data.	

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16	Checksum Alignment	This bit set to a ‘1’ indicates odd alignment. This bit set to a ‘0’ indicates even alignment.
15-0	Accumulated Checksum	The current value of the checksum being calculated.

3.5.27 DMAQS Local Descriptor Range Registers

These registers specify the lower and upper bounds of the memory range for local DMA descriptors.

These registers contain the address of the lower and upper bound of the memory range of descriptors that are in the PNR. If a descriptor block is enqueued, it is compared to these registers. If it falls within this range, only the descriptor address is placed on the queue. When the descriptor is to be loaded into the DMA registers, and it falls within this range, it will not be taken from the queue but loaded directly from the descriptor address. These registers are 4K aligned. The upper bound register contains the address of the last 4K block in the local descriptor address range.

3.5.27.1 DMAQS Local Descriptor Range Lower Bound Register

Length 64 bits

Type Read/Write

Address XXXX 0798

Power On Reset Value x‘0000 0000 0000 0000’

Restrictions Can be written in diagnostic mode only. The last four addresses in this range are reserved, and should not be used to hold descriptors.

3.5.27.2 DMAQS Local Descriptor Range Upper Bound Register

Length 32 bits

Type Read/Write

Address XXXX 07A4

Power On Reset Value x‘0000 0000’

Restrictions Can be written in diagnostic mode only. Upper bound is 32 bits. The upper 32 bits are internally generated, and are not different from the upper 32 bits of the lower bound register. The last four addresses in this range are reserved, and should not be used to hold descriptors.

3.5.28 DMAQS Event Queue Number Register

This register specifies which DMAQS queue should be used when DMA descriptors are enqueued from CSKED (DMA on transmit comp). This register also indicates the RXQUE Event Queue to which events should be enqueued for each DMAQS queue register.

Length 32 bits

Type Read/Write

Address XXXX 07CC

Power On Reset Value x‘0000 2210’

Restrictions Can be written in diagnostic mode only.

Bit(s)	Name	Description
31-20	Reserved	Reserved.
19	Change CSKED Queue	If this bit is set on a write, the CSKED queue is modified.
18	Change Queue 2 Event Queue Selector	If this bit is set on a write, the Queue 2 Event Queue Selector field is modified.
17	Change Queue 1 Event Queue Selector	If this bit is set on a write, the Queue 1 Event Queue Selector field is modified.
16	Change Queue 0 Event Queue Selector	If this bit is set on a write, the Queue 0 Event Queue Selector field is modified.
13-12	CSKED Queue	Specifies which DMAQS queue should be used when DMA descriptors are enqueued by CSKED. Invalid code is treated as queue 2.
11-8	Queue 2 Event Queue Selection	Specifies the Event Queue to be used for events originating from DMAQS queue 2.
7-4	Queue 1 Event Queue Selection	Specifies the Event Queue to be used for events originating from DMAQS queue 1.
3-0	Queue 0 Event Queue Selection	Specifies the Event Queue to be used for events originating from DMAQS queue 0.

3.5.29 DMAQS DMA Request Size Register

This register specifies the maximum request size for DMA descriptor scheduling.

This is the amount of data that DMAQS will request GPDMA to move in a single request. For example, if a descriptor wants to move 2K of data and the request size is set to 512 bytes, then DMAQS will request 512 bytes to be moved and then rearbitrate the DMA queues. A value of '0' is the same as x'ffff'.

Length 32 bits

Type Read/Write

Address XXXX 07C4

Power On Reset Value x'0000 0000'

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Maximum Request Size	These bits indicate the largest number of bytes DMAQS will request at one time from GPDMA.

3.5.30 DMAQS Enq FIFO Register

This register is for diagnostic use only. It holds DMA descriptors waiting to be placed on a DMA queue. Reading this register is destructive. The oldest entry is read on each read. If it is desired to re-dispatch the dequeued entries, they will have to be re-enqueued.

DMA Descriptors which reside in System Storage are not immediately copied into the queue, but space is reserved in the queue for the descriptors, and a descriptor is built which will copy the descriptor into the queue when needed.

Length 64 bits

Type Read Only

Address XXXX 07F8

Power On Reset Value x'0000 0000 0000 0000'

Restrictions Cannot be written.

3.6 The DRAM Controllers (COMET/PAKIT)

This section describes the function of the COMET/PAKIT entities. COMET is the memory controller for Control Memory, and PAKIT is the memory controller for Packet Memory.

Each controller can support the following types of memory:

- Synchronous DRAMs running at 133 MHz (7.5 ns cycle time) with a CAS latency of two or three and a burst length of two. Memory sizes of 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, and 128 MB are supported. Please note that the cycle time of the SDRAM clock is a constant on the PNR. Any SDRAM part selected must be capable of running at 133 MHz or faster at CAS latency 2 or 3.
- Synchronous SRAM running at 133 MHz (7.5 ns cycle time) with a read latency of two and a write latency of zero or two. Memory sizes of 1 MB, 2 MB, 4 MB, and 8 MB are supported.

Note: For any memory configuration, modules must be selected such that the loading on any memory net (including card wiring) does not exceed 44 pF.

The number of column address lines is programmable, allowing both DRAMs with symmetric address (same number of row and column address lines) and asymmetric address (typically having more row than column address lines).

If using SDRAM, the memory may be operated as having one or two arrays. The arrays are differentiated by their chip selects. If the memory is configured to have two arrays, the memory's address range is split equally between the two arrays.

Memory checking can be enabled/disabled, and the method of checking selected can be either ECC or parity. If ECC is selected, seven data bits are used for ECC over the 32 data bits. If parity is selected, four data bits are used to provide parity over the 32 data bits.

COMET/PAKIT are designed so that memory contents are preserved over a reset. If the PNR is reset while a memory write cycle is in progress, the cycle is completed in an orderly fashion to ensure that valid ECC/parity is written. Memory timings are not violated when reset goes active. Refresh is maintained during the reset.

3.6.1 Memory Reset Sequence

After a reset, onboard ROM or external firmware must properly configure the control registers for COMET/PAKIT.

If using SRAM, the reset sequence is complete. If using SDRAM, bit 3 of the memory controller's SDRAM Command and Status Register must be written to a ‘1’ to initiate forcing the SDRAMs out of the self refresh state and performing the POR sequence. When bits five and four of this register are '00', the SDRAMs are ready for use.

Note: Memory configuration errors occur if an attempt is made to use memory that is configured incorrectly or, if an attempt is made to use SDRAM before the POR sequence is completed.

Accesses to the first x‘20’ bytes of memory (Control or Packet) are not allowed unless bit 26 of the corresponding memory control register is set. With this restriction in place, accesses with zero-valued pointers will cause the zero address error bit in the memory controller’s status register to be set.

3.6.2 COMET/PAKIT Control Register

This register contains the information that controls the functions of the entity. Before this register can be altered, writing it must be enabled in the *COMET/PAKIT Memory Controller Write Enable Register* (described on page 149).

Length 32 bits

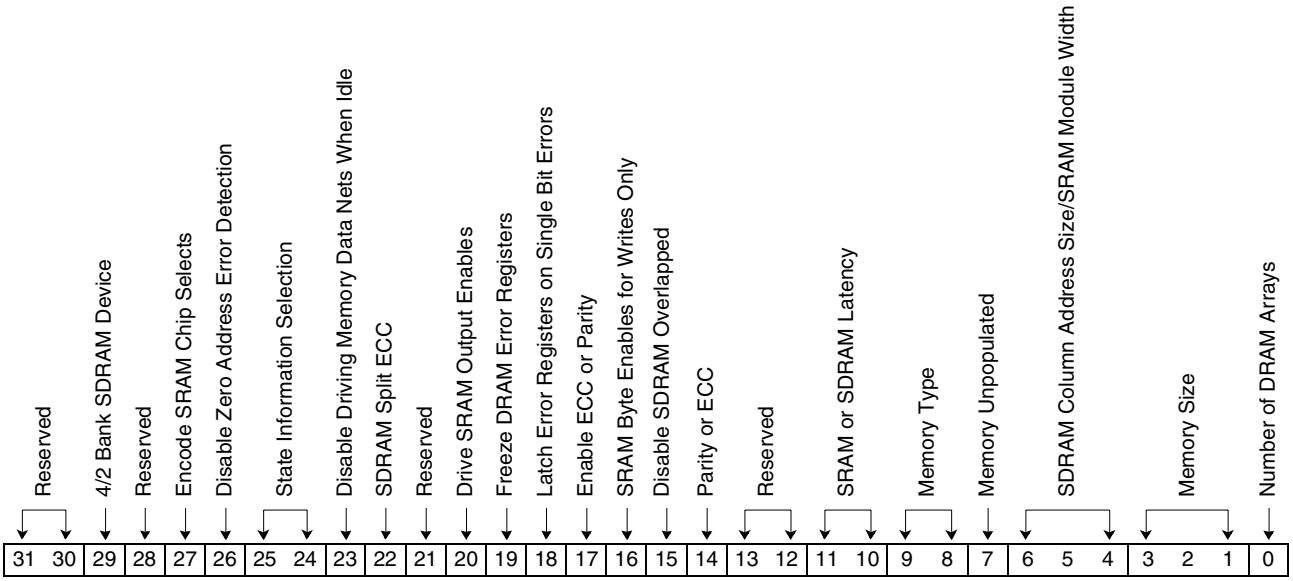
Type Clear/Set

COMET Address XXXX 0900 and 0904

PAKIT Address XXXX 0980 and 0984

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-30	Reserved	Reserved.
29	4/2 Bank SDRAM Device	When this bit is ‘1’, the SDRAMs attached are four-bank devices. When a ‘0’, the SDRAMs are two-bank devices. A ‘0’ setting works for either type device, but four-bank devices provide slightly better performance if this bit is set to ‘1’.
28	Reserved	Reserved.
27	Encode SRAM Chip Selects	When using SRAM, this bit set to a ‘0’ causes the chip select outputs to be direct chip selects. Set to ‘1’, chip selects 2-0 carry an encoded value for one of eight chip selects. Chip select three indicates when chip selects 2-0 are valid.
26	Disable Zero Address Error Detection	When set to ‘1’, this bit disables the detection of zero address errors to memory.
25-24	State Information Selection	These bits control what will be visible on the enstate outputs if COMET/PAKIT are selected for observation on the enstate pins.
23	Disable Driving Memory Data Nets When Idle	When set to ‘1’, this bit disables the memory controller from driving the memory data nets to ‘0’ when the controller is idle.

Bit(s)	Name	Description
22	SDRAM Split ECC	When set to ‘1’, this bit indicates that the ECC/parity for multiple arrays of memory are in separate modules and a slight increase in performance is possible. If this bit is ‘0’, the ECC/parity is in a shared module. If using neither ECC or parity, this bit should be set to ‘1’ for a slight performance increase. This bit applies only when SDRAM is being used.
21	Reserved	Reserved.
20	Drive SRAM Output Enables	When set to ‘1’, this bit allows functional output enables to be driven for SRAMs. When set to ‘0’, the output enables are driven active continuously.
19	Freeze Error Registers	When set to ‘1’, this bit freezes the Memory Address Register and the Syndrome Register when a memory error occurs. When this bit is set to ‘0’, the error registers are updated whenever an error is encountered. For this bit to have any meaning with single bit errors, bit 18 must also be ‘1’.
18	Latch Error Registers on Single Bit Errors	When set to ‘1’, this bit allows error data to be latched into the Memory Error Address Register and the Syndrome Register when a single bit errors occurs. When this bit is set to ‘0’, single bits errors do not latch data into the error registers.
17	Enable ECC or Parity	This bit set to ‘1’ enables ECC detection/correction or parity error detection.
16	SRAM Byte Enables for Writes Only	When set to ‘1’, this bit causes byte enables to only be driven on writes to SRAM. The enables are driven inactive for reads. If the bit is set to ‘0’, the byte enables are valid on both reads and writes.
15	Disable SDRAM Overlapped Bank Accesses/Shorten SRAM Write Duration	When the memory controller is configured for SDRAM, setting this bit to ‘1’ disables the overlapping of bank accesses. When configured for SRAM, setting this bit to ‘1’ shortens the time the PNR drives data on writes.
14	Parity or ECC	When set to ‘1’, this bit causes parity to be generated. This bit set to ‘0’ causes ECC to be generated. ECC is supported for DRAM only.
13-12	Reserved	Reserved.
11-10	SRAM or SDRAM Latency	These bits indicate the delay between performing a read and the memory returning data. The bits are encoded as follows: 00 1 Cycle (SRAM only) 01 2 Cycles 10 3 Cycles (SDRAM only) 11 Reserved
9-8	Memory Type	These bits indicate the type of memory being used for memory. The bits are encoded as follows: 00 SRAM 01 ZBT SRAM 10 Synchronous DRAM (SDRAM) 11 Enhanced Synchronous DRAM (ESDRAM)
7	Memory Unpopulated	If this bit is ‘1’, there is no physical memory connected to this controller.

Bit(s)	Name	Description
6-4	SDRAM Column Address Size/ SRAM Module Width	These bits indicate the number of column address lines. The bits are encoded for SDRAM as follows: ‘000’ 8 column address lines (256 words/row) ‘001’ 9 column address lines (512 words/row) ‘010’ 10 column address lines (1 K words/row) ‘011’ Reserved ‘1XX’ Reserved The bits are encoded for SRAM as follows: ‘000’ 18-bit wide 4 MB SRAM ‘001’ 18-bit wide 8 MB SRAM ‘010’ 18-bit wide 16 MB SRAM ‘011’ 18-bit wide 32 MB SRAM ‘100’ 36-bit wide 4 MB SRAM ‘101’ 36-bit wide 8 MB SRAM ‘110’ 36-bit wide 16 MB SRAM ‘111’ 36-bit wide 32 MB SRAM
3-1	Memory Size	These bits indicate the total amount of memory present, that is, two 64MB SDRAM arrays would result in a value of 128 MB in these bits. The bits are encoded as follows: ‘000’ 1 MB ‘001’ 2 MB ‘010’ 4 MB ‘011’ 8 MB ‘100’ 16 MB ‘101’ 32 MB ‘110’ 64 MB ‘111’ 128 MB - SDRAM Only
0	Number of DRAM Arrays	This bit indicates the number of arrays of DRAM present. This bit set to ‘0’ indicates one array; the bit set to ‘1’ indicates two arrays.

3.6.3 COMET/PAKIT Status Register

This register contains status information for COMET/PAKIT.

Length 32 bits

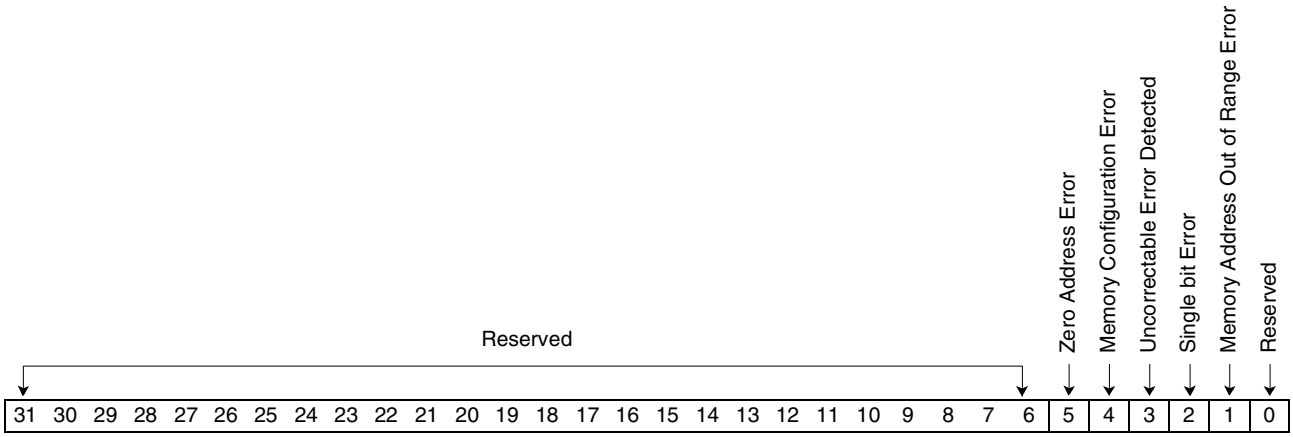
Type Clear/Set

COMET Address XXXX 0908 and 090C

PAKIT Address XXXX 0988 and 098C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-6	Reserved	Reserved.
5	Zero Address Error	This bit is set if COMET/PAKIT is presented an address of zero.
4	Memory Configuration Error	This bit is set if COMET/PAKIT is configured in an invalid combination.
3	Uncorrectable Error Detected	This bit is set if an uncorrectable error is detected.
2	Single Bit Error	This bit is set if a single bit ECC error is detected.
1	Memory Address Out of Range Error	This bit is set if the address presented to the memory controller is out of the defined range.
0	Reserved	Reserved.

3.6.4 COMET/PAKIT Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *COMET/PAKIT Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from COMET/PAKIT to INTST if the condition is detected.

Length 32 bits

Type Clear/Set

COMET Address XXXX 0910 and 0914

PAKIT Address XXXX 0990 and 0994

Power On Reset Value x'0000 003A'

Restrictions None

Bit(s)	Name	Description
31-6	Reserved	Reserved.
5-0	Interrupt Enable	When one of these bits is set to one and the corresponding bit in the *COMET/PAKIT Status Register* is also set, an interrupt is generated.

3.6.5 COMET/PAKIT Lock Enable Register

This register allows the user to selectively allow each of the conditions reported in the *COMET/PAKIT Status Register* to force a memory lock condition in the memory controller. Each bit corresponds to the same bit in the status register and when set to '1' causes a memory lock if the condition is detected.

Length 32 bits

Type Clear/Set

COMET Address XXXX 0918 and 091C

PAKIT Address XXXX 0998 and 099C

Power On Reset Value x'0000 003A'

Restrictions None

Bit(s)	Name	Description
31-6	Reserved	Reserved.
5-0	Lock Memory	When one of these bits is set to one and the corresponding bit in the COMET/PAKIT Status Register is also set, the memory subsystem will lock.

3.6.6 COMET/PAKIT Memory Error Address Register

This register holds the address at which the last memory error occurred.

Length 32 bits

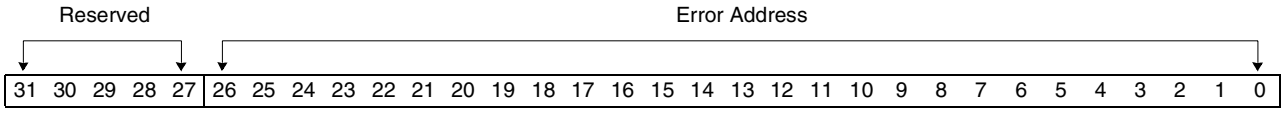
Type Read Only

COMET Address XXXX 0920

PAKIT Address XXXX 09A0

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-27	Reserved	Reserved.
26-0	Error Address	The read address of the last memory error.

3.6.7 COMET/PAKIT SDRAM Command and Status Register

This register is used to issue various commands to and control the timing operation of Synchronous DRAMS when they are attached to the PNR. If the PNR is not configured for SDRAMs, any writes to bits 3-0 of this register are ignored. This register is also used to reflect the status of the Synchronous DRAMs. When a command bit in this register is set (bits 3-0 only), the command executes and resets the bit upon completion. Only one bit (3-0 only) may be set during any write. Software should poll this register to make sure the previous command has completed before issuing another write to this register. If more than one bit at a time is written to this register (3-0 only), the results may be unpredictable.

Length 32 bits

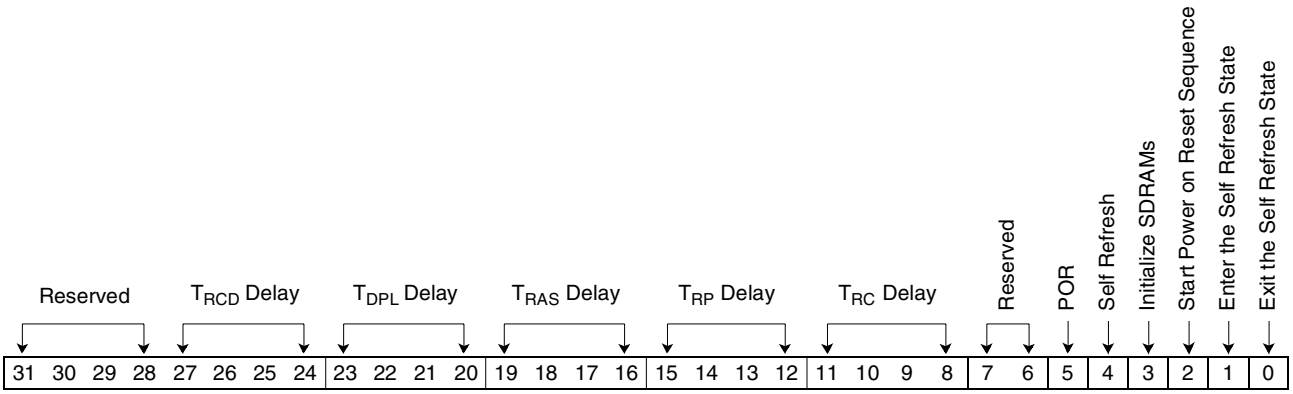
Type Read/Write

COMET Address XXXX 0924

PAKIT Address XXXX 09A4

Power On Reset Value x‘0000 3030’

Restrictions None



Bit(s)	Name	Description
31-28	Reserved	Reserved.
27-24	T_{RCD} Delay	The value of these four bits determine the number of cycles between RAS and CAS. To determine the value needed in these bits, take the T_{RCD} parameter from the specification of the SDRAM part to be used, divide by 7.5 ns, and round up if necessary. Suggested values are: x‘3’ 6.8 ns SDRAM x‘2’ 6 ns ESDRAM x‘2’ 7.5 ns ESDRAM
23-20	T_{DPL} Delay	The value of these four bits determine the number of cycles after writing data before a precharge command may be issued. To determine the value needed in these bits, take the T_{DPL3} (for CAS latency 3) or T_{DPL2} (for CAS latency 2) parameter from the specification of the SDRAM part to be used, divide by 7.5 ns, and round up if necessary. Suggested values are: x‘2’ 6.8 ns SDRAM x‘1’ 6 ns ESDRAM x‘1’ 7.5 ns ESDRAM

Bit(s)	Name	Description
19-16	T_{RAS} Delay	The value of these four bits determine the number of cycles a bank must be active. To determine the value needed in these bits, take the T_{RAS} parameter from the specification of the SDRAM part to be used, divide by 7.5 ns, and round up if necessary. Suggested values are: x‘7’ 6.8 ns SDRAM x‘3’ 6 ns ESDRAM x‘3’ 7.5 ns ESDRAM
15-12	T_{RP} Delay	The value of these four bits determines the number of cycles after a bank precharge starts before the bank may be accessed again. To determine the value needed in these bits, take the T_{RP} parameter from the specification of the SDRAM part to be used, divide by 7.5 ns, and round up if necessary. If T_{DPL} is 2, T_{RP} may need to be increased by one to insure correct operation. Suggested values are: x‘4’ 6.8 ns SDRAM x‘2’ 6 ns ESDRAM x‘2’ 7.5 ns ESDRAM
11-8	T_{RC} Delay	The value of these four bits determine the bank cycle time. To determine the value needed in these bits, take the T_{RC} parameter from the specification of the SDRAM part to be used, divide by 7.5 ns, and round up if necessary. Suggested values are: x‘A’ 6.8 ns SDRAM x‘5’ 6 ns ESDRAM x‘5’ 7.5 ns ESDRAM
7-6	Reserved	Reserved.
5	POR	When set to ‘1’, this bit indicates the POR sequence has not been performed on the SDRAMs. This bit automatically resets to ‘0’ when the POR sequence has been performed.
4	Self Refresh	This bit reads ‘1’ when the SDRAMs are in the self refresh state. This bit reads ‘0’ when the SDRAMs are not in the self refresh state. This bit is ‘1’ after a POR or reset. The exit self refresh operation must be performed before the POR sequence is initiated.
3	Initialize SDRAMs	This bit effectively encapsulates the functions provided by bits 2 and 0. Setting this bit to ‘1’ causes the memory controller to take the SDRAMs out of self refresh and perform the POR sequence on them. This bit clears itself. When the initialization is complete, bits 4 and 5 should be a ‘0’.
2	Start Power on Reset Sequence	When set to ‘1’, this bit causes the DRAM controller to initiate the SDRAM power on sequence. This includes an all-banks precharge, following by a command register write that sets the CAS latency to 3, the wrap type to sequential, and the burst length to 1, followed by two refresh cycles. After this sequence is initiated and completed, bit 5 resets and the SDRAMs are ready for normal use.
1	Enter the Self Refresh State	When set to ‘1’, this bit causes the SDRAM controller to signal the SDRAMs to go into the self refresh state. All memory activity is suspended. Once the SDRAMs have entered the self refresh state, bit 4 will set. This bit will clear itself.
0	Exit the Self Refresh State	When set to ‘1’, this bit causes the SDRAM controller to signal the SDRAMs to exit the self refresh state. Once the SDRAMs have exited the self refresh state, bit 4 will clear. This bit will clear itself.

3.6.8 COMET/PAKIT DRAM Refresh Rate Register

This register holds the value of a counter used to control the rate of refresh for the DRAM.

Length 32 bits

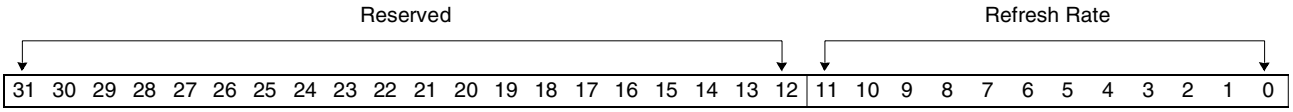
Type Read/Write

COMET Address XXXX 0928

PAKIT Address XXXX 09A8

Power On Reset Value X'0000 0820'

Restrictions None



Bit(s)	Name	Description
31-12	Reserved	Reserved.
11-0	Refresh Rate	The value of these bits multiplied by 7.5 ns gives the refresh rate. The POR value of x'820' yields a refresh rate of 15.6 ms.

3.6.9 COMET/PAKIT Syndrome Register

This register holds the syndrome bits that can be used to isolate the data or check bit in error when ECC is used. When parity is used, this register indicates which of the four bytes of the memory bus had a parity error.

Length 32 bits

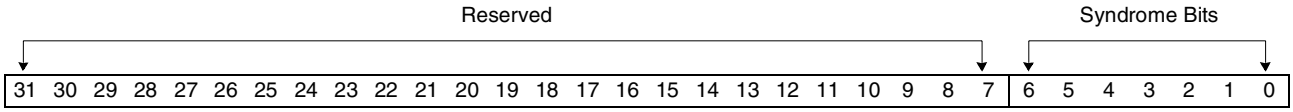
Type Read/Write

COMET Address XXXX 092C

PAKIT Address XXXX 09AC

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Reserved	Reserved.
6-0	Syndrome Bits	When using ECC, a single bit error can be identified by matching the contents of this register to the corresponding bit in the table below. When using parity, only bits 3-0 are valid and are interpreted as follows: 0000 No parity error 0001 Parity error on bits 7-0 0010 Parity error on bits 15-8 0100 Parity error on bits 23-16 1000 Parity error on bits 31-24 Other Reserved

Table 15: ECC Syndrome Bits

Bit in Error	Syndromes	Bit in Error	Syndromes
ECC(6)	‘1000000’	ECC(5)	‘0100000’
ECC(4)	‘0010000’	ECC(3)	‘0001000’
ECC(2)	‘0000100’	ECC(1)	‘0000010’
ECC(0)	‘0000001’	N/A	N/A
DATA(31)	‘0111000’	DATA(30)	‘0110100’
DATA(29)	‘0110010’	DATA(28)	‘0101100’
DATA(27)	‘1110000’	DATA(26)	‘1101000’
DATA(25)	‘1100100’	DATA(24)	‘1100010’
DATA(23)	‘0100101’	DATA(22)	‘0010101’
DATA(21)	‘0001101’	DATA(20)	‘1100001’
DATA(19)	‘0110001’	DATA(18)	‘0101001’
DATA(17)	‘0011001’	DATA(16)	‘1000101’
DATA(15)	‘1010001’	DATA(14)	‘1001100’
DATA(13)	‘1001010’	DATA(12)	‘1000110’

Table 15: ECC Syndrome Bits (Continued)

Bit in Error	Syndromes	Bit in Error	Syndromes
DATA(11)	‘1000011’	DATA(10)	‘1011000’
DATA(09)	‘1010100’	DATA(08)	‘1010010’
DATA(07)	‘0100011’	DATA(06)	‘0010011’
DATA(05)	‘0001011’	DATA(04)	‘0000111’
DATA(03)	‘0011010’	DATA(02)	‘0100110’
DATA(01)	‘0010110’	DATA(00)	‘0001110’

3.6.10 COMET/PAKIT Checkbit Inversion Register

This register can be used for diagnostic purposes to invert the ECC/parity check bits that are written to memory.

Length 32 bits

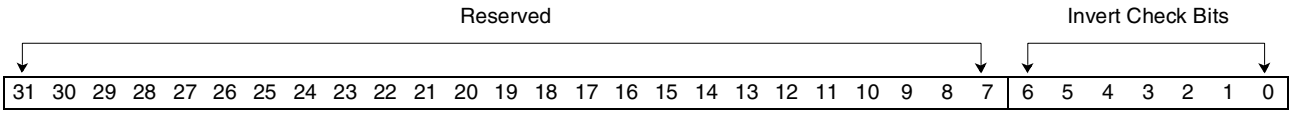
Type Read/Write

COMET Address XXXX 0930

PAKIT Address XXXX 09B0

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Reserved	Reserved.
6-0	Invert Check Bits	Setting any of these bits inverts the corresponding check bit that is written to memory. Only bits 3-0 are valid when parity is used as a checking mechanism.

3.6.11 COMET/PAKIT Memory Controller Write Enable Register

This register must be written to a specific pattern before the Memory Control Register can be written.

Length 32 bits

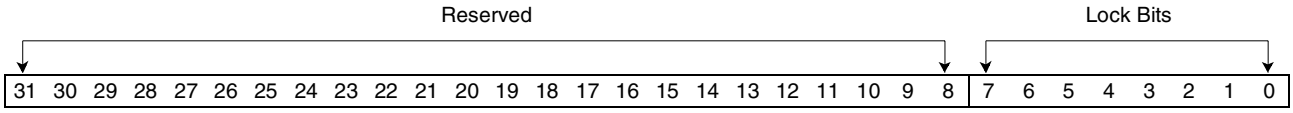
Type Read/Write

COMET Address XXXX 0934

PAKIT Address XXXX 09B4

Power On Reset Value x‘0000 00B4’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Lock Bits	This register must be written to x‘B4’ before the Memory Control Register can be written. This register will POR to x‘B4’, but eprom initialization code may set up the memory controller and clear this register back to x‘0’.

3.6.12 COMET/PAKIT Memory Configuration Error Sense Register

This register can be read to help determine the source of a memory configuration error. The bits in this register reset automatically once the configuration error is resolved.

Length 32 bits

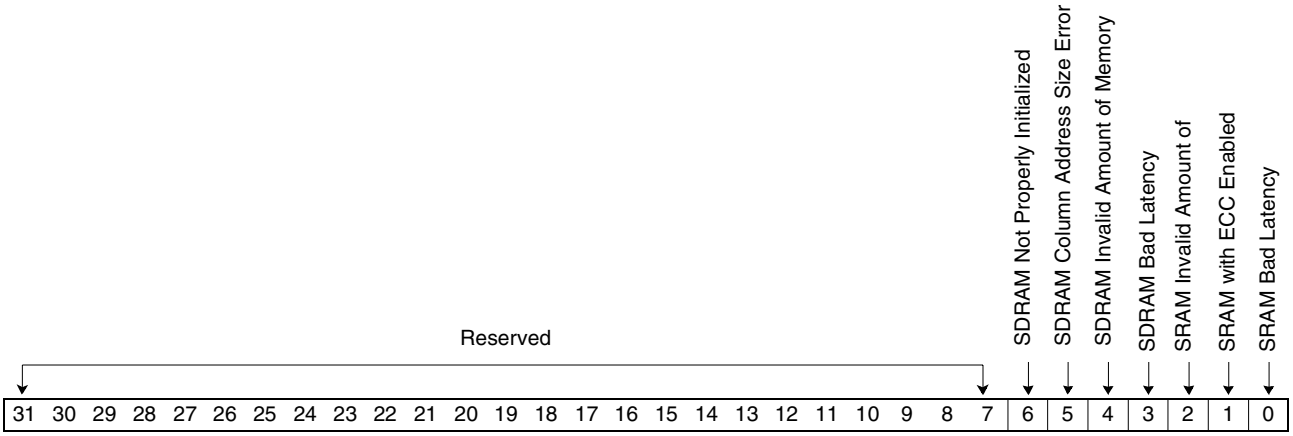
Type Read Only

COMET Address XXXX 0938

PAKIT Address XXXX 09B8

Power On Reset Value x'0000 0000'

Restrictions None



Bit(s)	Name	Description
31-7	Reserved	Reserved.
6	SDRAM Not Properly Initialized	An SDRAM access has been attempted without the SDRAMs being taken out of self refresh and/or the POR sequence being performed.
5	SDRAM Column Address Size Error	Bits 6-4 of the control register have an invalid value.
4	SDRAM Invalid Amount of Memory	Bits 3-2 of the control register indicate less than 4 M of memory.
3	SDRAM Bad Latency	Bits 11-10 of the control register indicate a latency of one or a reserved value.

Bit(s)	Name	Description
2	SRAM Invalid Amount of Memory	Bits 27, 13-12, and 3-1 of the control register indicate an invalid SRAM memory size. Acceptable sizes are: 4 Mbit x18 unmuxed chip selects of sizes 1 M, 2 M, 4 M. 8 Mbit x18 unmuxed chip selects of sizes 2 M, 4 M, 8 M. 16 Mbit x18 unmuxed chip selects of sizes 4 M, 8 M, 16 M. 32 Mbit x18 unmuxed chip selects of sizes 8 M, 16 M, 32 M. 4 Mbit x18 muxed chip selects of sizes 2 M, 4 M, 8 M. 8 Mbit x18 muxed chip selects of sizes 4 M, 8 M, 16 M. 16 Mbit x18 muxed chip selects of sizes 4 M, 16 M, 32 M. 32 Mbit x18 muxed chip selects of sizes 8 M, 32 M, 64 M. 4 Mbit x36 unmuxed chip selects of sizes 1 M, 2 M. 8 Mbit x36 unmuxed chip selects of sizes 1 M, 2 M, 4 M. 16 Mbit x36 unmuxed chip selects of sizes 2 M, 4 M, 8 M. 32 Mbit x36 unmuxed chip selects of sizes 4 M, 8 M, 16 M. 4 Mbit x36 muxed chip selects of sizes 1 M, 2 M, 4 M. 8 Mbit x36 muxed chip selects of sizes 2 M, 4 M, 8 M. 4 Mbit x36 muxed chip selects of sizes 4 M, 8 M, 16 M. 8 Mbit x36 muxed chip selects of sizes 8 M, 16 M, 32 M.
1	SRAM with ECC Enabled	Bits 17, 14, and 9-8 of the control register indicate ECC is enabled with an SRAM configuration. This is invalid.
0	SRAM Bad Latency	Bits 11-10 of the control register indicate a latency of three or a reserved value.

3.7 On-chip Checksum and DRAM Test Support (CHKSM)

3.7.1 Software Use of CHKSM

This section outlines some ways CHKSM can be set up and used.

Test Mode Possible Patterns

In test mode, a 64-bit pattern is written/compared to/with memory. There are several different patterns that can be used:

Constant Test Pattern

When in test mode, and the RP bit is cleared, the CHKSM Ripple Base Register is replicated eight times to form a 64-bit pattern.

Ripple Pattern with increment of 1

When in test mode and the RP bit is set and RP-ADD is set and CHKSM Ripple Limit Register is set to ‘0’, a 64-bit pattern is generated using the CHKSM Ripple Base Register as a base. For example, if the CHKSM Ripple Base Register is set to ‘1’, the following pattern is generated:

```
0102030405060708
0203040506070809
030405060708090A
040506070809A0B
…
```

Ripple Pattern with increment of 8

When in test mode and the RP bit is set and RP-ADD is cleared and CHKSM Ripple Limit Register is set to ‘0’, a 64-bit pattern is generated using the CHKSM Ripple Base Register as a base. For example, if the CHKSM Ripple Base Register is set to ‘1’, the following pattern is generated:

```
0102030405060708
090A0B0C0D0E0F10
1112131415161718
191A1B1C1D1E1F20
…
```

Ripple Pattern with Ripple Limit

Each of the above ripple patterns can also make use of the CHKSM Ripple Limit Register. By setting this register, the user can control when the ripple pattern rolls over to zero. For example, when the CHKSM Ripple Limit Register is set to three in increment-by-one mode the ripple pattern looks like:

```
0102030405060708
0203040506070809
030405060708090A
0001020304050607
0102030405060708
0203040506070809
030405060708090A
…
```

Similarly, when the CHKSM Ripple Limit Register is set to ten, in increment-by-eight mode, the ripple pattern looks like:

```
0102030405060708
090A0B0C0D0E0F10
1112131415161718
0001020304050607
…
```

This section contains descriptions of the registers used by the arbiter logic.

Initializing Packet/Control Memory

The following list shows the steps to use CHKSM to initialize Packet or Control Memory:

- Make sure CHKSM is in diagnostic mode, and other mode bits are reset.
- Set the start address by writing the base address.
- Set up the read/write count with number of bytes to initialize.
- Set up the test pattern register (ripple pattern register) with pattern to use.
- Set up the Control Register to enable test mode, enable checksum entity, and set the memory select bit correctly based on which memory is to be initialized.
- Now busy wait until the operation is done (or set up Interrupt Enable Register and wait for interrupt).

Testing Packet/Control Memory

The following list shows the steps to use CHKSM to test packet or Control Memory:

- First initialize memory with a pattern using above sequence.
- Make sure CHKSM is in diagnostic mode, and other mode bits are reset.
- Set the start address by writing the base address.
- Set up the read/write count with number of bytes to test (same as initialization value).
- The test pattern register (ripple pattern register) already contains the pattern.
- Set up the Control Register to enable test mode, turn on RW bit, enable checksum entity, and set the memory select bit correctly based on which memory is to be initialized.
- Now busy wait until the operation is done (or set up interrupt Enable register and wait for interrupt).
- When done, check the status register for any errors.

Using Ripple Pattern Generation/Checking in Packet/Control Memory

The procedures to use the ripple pattern generation and checking are the same as using test write/read modes. The only difference is that the use ripple pattern mode bit must be set and the ripple pattern base register must be set up.

3.7.2 Running a TCP/IP Checksum in Packet/Control Memory

The following list shows the steps to use CHKSM to generate/verify a TCP/IP checksum:

- Make sure CHKSM is in diagnostic mode (not enabled).
- Set the start address by writing the base address.
- Set up the read/write count with number of bytes to run checksum over, and set the upper two bits of the read/write count register. Writing these upper two bits assumes other mode bits are set correctly (that is, memory bank select).
- Now busy wait until the operation is done (or set up interrupt Enable register and wait for interrupt).

3.7.3 CHKSM Base Address Register

The CHKSM Base Address Register indicates the starting address of a test operation or checksum calculation. The base address can be set up with any alignment and valid address.

This register increments with each read or write to memory. On a test mode error, the register holds the address of the 64-bit word which was read in error.

Length	32 bits
Type	Read/Write
Address	XXXX 0A00
Power On Reset Value	x‘0000 0000’
Restrictions	Can only be written when CHKSM is not enabled (see EE bit in *3.7.10 CHKSM Control Register* on page 161)

3.7.4 CHKSM Read/Write Count Register

The CHKSM Read/Write Count Register indicates the count of remaining bytes of a checksum operation. This register keeps track of how many bytes remain in the current checksum operation and is decremented with each read or write operation.

Any length can be set in the 30 lower significant bits.

The upper two bits of this register can be written when starting a checksum operation instead of writing the control register.

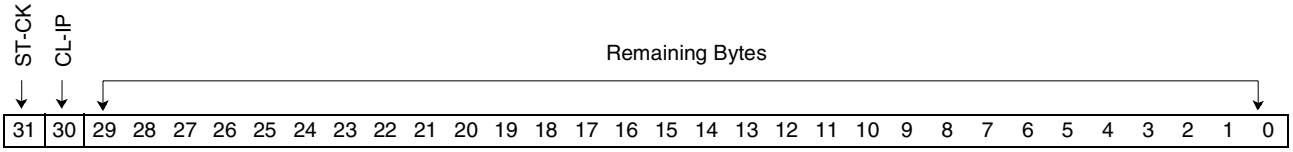
Length 32 bits

Type Read/Write

Address XXXX 0A04

Power On Reset Value x‘0000 0000’

Restrictions Can only be written when CHKSM is not enabled (see EE bit in *3.7.10 CHKSM Control Register* on page 161).



Bit(s)	Name	Description
31	ST-CK	Start a checksum operation. When this bit is written, bits 0 and 1 in the control register are set, and a checksum operation is started. This should only be done when the rest of the control register bits are already set up (i.e., memory select, invert checksum).
30	CL-IP	When this bit is written, it will clear the CHKSM TCP/IP Checksum Data Register. This is the same as writing a ‘1’ to bit 6 of the CHKSM Control Register.
29-0	Remaining Bytes	Bytes remaining in checksum calculation.

3.7.5 CHKSM TCP/IP Checksum Data Register

The CHKSM TCP/IP Checksum Data Register collects the 16-bit, two's complement, end-around-carry sum of the bytes. The source data is zero padded if it starts or ends on an odd byte boundary. It can be seeded with an initial value. If it is not cleared before running a checksum, the previous value will act as a seed. This register can be cleared when starting a checksum operation by writing the CLIP bit in the CHKSM Control Register or by writing upper bits of the CHKSM Read/Write Count Register.

See *3.7.10 CHKSM Control Register* on page 161 for description of how to get/set current checksum alignment.

Length	32 bits	
Type	Read/Write	
Address	Normal sum	XXXX 0A08
	Inverted sum	XXXX 0A0C
	Swapped sum	XXXX 0A34
	Inverted swapped sum	XXXX 0A38
Power On Reset Value		x'0000 0000'
Restrictions	Can only be written when CHKSM is not enabled (see EE bit in *3.7.10 CHKSM Control Register* on page 161).	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Calculated Checksum	As a checksum operation proceeds, the checksum generated is stored here.

3.7.6 CHKSM Ripple Base Register

This register is used as base of a ripple pattern when in test mode. Each consecutive byte will be incremented by one or eight in the pattern. The ripple mode must be set in the Control Register to use this feature. The value of this register will change during the test operation. If a write and compare operation is being performed, this register needs to be set up again for the second operation.

Length 32 bits

Type Read/Write

Address XXXX 0A14

Power On Reset Value x‘0000 0000’

Restrictions Can only be written when CHKSM is not enabled (see EE bit in *3.7.10 CHKSM Control Register* on page 161).

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Ripple Pattern Base	When written prior to a test operation, this register will contain the initial value used to generate the test pattern. During the test operation, this register will be repeatedly updated as the test advances.

3.7.7 CHKSM Ripple Limit Register

This register is used to determine when the ripple base register overflows to zero. This register forms the compare value for the ripple base register. When the value of the ripple base register is greater than or equal to this register, the base register will overflow to zero. For example, when this register is set to four, the ripple base register would count from zero through four if counting by one.

When set to x‘0000 0000’, no overflows to zero occur. For example, when bits 7-0 of the ripple value are x‘FF’, and you are counting by eight, the next value would still be x‘07’. If counting by one, then the next value would be x‘00’.

This register should be written before the ripple base.

Length 32 bits

Type Read/Write

Address XXXX 0A10

Power On Reset Value x‘0000 00FF’

Restrictions Can only be written when CHKSM is not enabled (see EE bit in *3.7.10 CHKSM Control Register* on page 161).

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Ripple Limit	Maximum value for the Ripple Base Register.

3.7.8 CHKSM Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *CHKSM Status Register*. Each bit corresponds to the same bit in the status register and when set to ‘1’ generates an interrupt from CHKSM to INTST if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0A20 and 0A24

Power On Reset Value x‘0000 0FFE’

Restrictions None

3.7.9 CHKSM Status Register

This register is used to relay CHKSM status information.

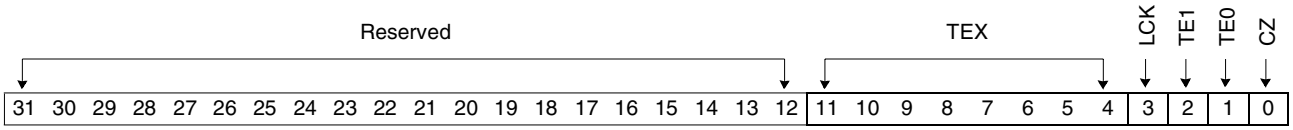
Length 32 bits

Type Clear/Set

Address XXXX 0A18 and 0A1C

Power On Reset Value x‘0000 0001’

Restrictions The count zero bit is not writable.



Bit(s)	Name	Description
31-12	Reserved	Reserved.
11-4	TEX	Test Error in Byte 7-0. When these bits are set, the checksum has determined that a read comparison error was encountered in the corresponding byte. Byte 0 is bits 63-56 in a 64-bit long word.
3	LCK	Comet Lock. When this bit is set, the checksum has determined that COMIT has ceased operation for some reason, or a virtual error was detected.
2	TE1	Test Error MSW. When this bit is set, checksum has determined that a read comparison error was encountered in the most significant 32-bit word.
1	TE0	Test Error LSW. When this bit is set, the checksum has determined that a read comparison error was encountered in the least significant 32-bit word.
0	CZ	Count Zero. This bit is set when the terminal count of an operation is reached.

3.7.10 CHKSM Control Register

The various bits in this register control the mode in which the checksum entity operates.

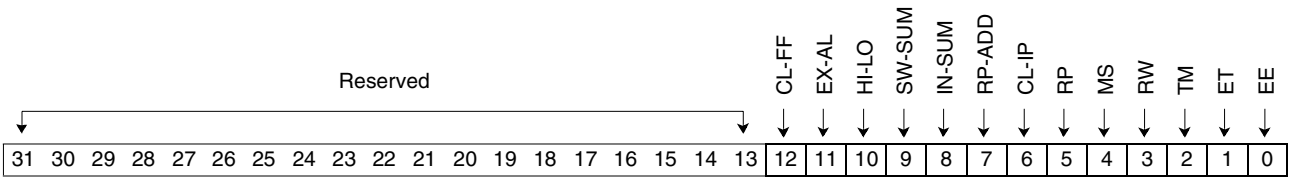
Length 32 bits

Type Clear/Set

Address XXXX 0A28 and 0A2C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-13	Reserved	Reserved.
12	CL-FF	Clear to All Ones. When this bit is set, the CHKSM TCP/IP Checksum Data Register is set to x‘ffff’ when it is cleared. When this bit is cleared, the CHKSM TCP/IP Checksum Data Register is set to ‘0’. This option should be used if the TCP/IP checksum should never be set to ‘0’ (x‘ffff’ is ‘0’ also).
11	EX-AL	Expose Alignment. When this bit is set, the internal checksum alignment is exposed for reading/writing. For writes, bit 16 of the write data is used to set the internal alignment. For reads, the alignment is exposed in bit 16 or bit 0 depending on the value of the HI-LO bit in this register. This can be useful if doing non-consecutive multiple part check sums (need to preserve alignment between chunks). When this bit is cleared, the internal checksum alignment is not exposed. It is always cleared when the CL-IP bit in this register is set. Normally, the internal alignment is calculated and maintained across consecutive check sums.
10	HI-LO	Hi Lo Word. When this bit is set, the checksum data register data is placed in the most significant 16 bits of the 32-bit value read. When this bit is cleared, the checksum data register data is placed in the least significant 16 bits of the 32-bit value read. This bit does not affect how writes to the checksum data register occur; the data from the least significant 16 bits is always used.
9	SW-SUM	Swap Checksum. When this bit is set, the checksum data register data is byte-swapped when read. When this bit is cleared, the checksum data register data is read normally. There are also new checksum data register addresses that can be read that do the same thing as this control bit. This bit is depreciated.
8	IN-SUM	Invert Checksum. When this bit is set, the checksum data register data is inverted when read. When this bit is cleared, the checksum data register data is read normally. There are also new checksum data register addresses that can be read that do the same thing as this control bit. This bit is depreciated.
7	RP-ADD	Ripple Addend. When this bit is set, the ripple base register counts up by one. When this bit is cleared, the ripple base register counts up by eight.
6	CL-IP	Clear IP. When this bit is written, it will clear the CHKSM TCP/IP Checksum Data Register and itself. The result of this will be that this bit will never be read as a ‘1’. The internal alignment is also cleared.

Bit(s)	Name	Description
5	RP	Ripple. When this bit is set, a ripple pattern will be used in both the read and write test modes. The ripple pattern is used instead of the constant test pattern. When this bit is reset, the constant test pattern is used for the test mode data.
4	MS	Memory Select. When this bit is set, all CHKSM memory accesses are to the Control Memory. When this bit is cleared, all CHKSM memory accesses are to the Packet Memory.
3	RW	R/-W Test Mode. When this bit is set, the entity will take the data that is read and compare it to the test/ripple pattern. When this bit is reset, the checksum entity will write data using the test/ripple pattern to the DRAM.
2	TM	Test Mode. When this bit is set, the entity will take the data that is read and compare it to the test/ripple pattern, or will write data using the test/ripple pattern to the DRAM depending on the setting of the RW bit. In both cases, the reading or writing will continue until either an error is encountered or the CHKSM Read/Write Count Register counts down to ‘0’. When this bit is reset, the checksum entity will operate as described by the other bits. Test and CHKSM modes are mutually exclusive, and test mode takes precedence.
1	ET	Enable TCP Checksum Updates. When this bit is set, the entity will collect the TCP checksum in the CHKSM TCP/IP Checksum Data Register. When this bit is reset, the CHKSM TCP/IP Checksum Data Register will not be changed by data that is read from the DRAM. Test and CHKSM modes are mutually exclusive, and test mode takes precedence.
0	EE	Enable Entity CHKSM. When this bit is set, the entity will run as specified. When this bit is reset, the entity will not run.

3.7.11 Debugging Register Access

3.7.11.1 CHKSM Internal State

Internal state of checksum.

Note: This register should not be written unless specifically directed to do so by IBM technical support.

Length 32 bits

Type Read/Write

Address XXXX 0A3C

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	Internal State of Checksum	For use only as specifically directed by IBM Technical Support.

3.8 The PHY Interface (LINKC)

3.8.1 Functional Description

LINKC provides the interface between the PNR and either an ATM PHY device or, when the internal framer is selected, a serializer/deserializer device.

LINKC is composed of three pieces. LINKX, which contains all the registers described below, is clocked with the same clock as other parts of the chip. LINKT, the transmit logic, is clocked on the transmit clock, which is selected via the Clock Control Register (described in *Clock Control Register* on page 111). LINKR, the receive logic, is clocked on the receive clock, which is also selectable via the Clock Control Register. Transmit and receive transfers are synchronized via their respective interface transfer clock. The data path size is 8- or 16-bits wide and is selectable through bit 3 of the control register. The PNR interfaces the following PHY devices:

- PMC SIERRA PM5346 SUNI LITE
- PMC SIERRA PM5351 SUNI TETRA
- PMC SIERRA PM5356 SUNI 622 MAX
- PMC SIERRA PM5357 SUNI 622 POS
- UTOPIA 8- or 16-bit interface
- PMC SIERRA POS-PHY

3.8.2 Multi-Drop

When the PNR is in multi-drop Utopia mode, it supports four external PHY devices. Each port is associated with a configuration register. Four configurations are provided so up to four different types of PHYs can be connected to the PNR. This allows the user to mix cell and POS-PHY devices on the transmit and/or receive interface.

The multi-drop PHY devices supported are Utopia Level 2 (cell based) and PMC Sierra POS-PHY (packet/frame based). The PNR will select which PHY device will transfer data next by polling each of the devices to determine which PHYs can transfer data. A round-robin switching scheme is used to determine which PHY has the priority if more then one wants to transmit/receive data. The PNR will switch to a new drop when a cell has been received/transmitted (for a cell-based PHY) or when 64 bytes or EOP (End of Packet) has been received/transmitted (for POS-PHY PHYs). The transmit and receive sides of LINK are separately configurable for multi-drop mode (bits 1 and 0 of the global control register).

3.8.3 POS-PHY

The POS-PHY interface complies with the PMC Sierra POS-PHY Level 2 Specification. The PNR polls each POS-PHY device to determine its status on both the receive and transmit side. It looks to switch to a different port when 64 bytes or EOP (End of Packet) have been transferred between the POS-PHY and itself. The PNR does not support direct status indication or byte-level transfers. Therefore, the PHY must be programmed to always be able to send/receive at least 64 bytes of information. The RMOD signal will only be looked at when REOP is ‘1’; at all other times it will be ignored. POS-PHY devices should be configured so that they will only signal they are ready for a transfer if they have 64 bytes free in their receive buffer and 64 bytes or EOP in their transmit FIFO.

Table 16: Moving Cells to and from the PNR (Number of cycles to transfer various cells)

Interface	Data Payload	Cell	Cycles for 8-bit Bus	Cycles for 16-bit Bus
Utopia	48	52	52	26
Utopia	48	53	53	27
Utopia	48	54	54	27
Utopia	48	55	55	28
Utopia	48	56	56	28

3.8.4 LINKC Global Control Register

This register contains the information which controls the operation of LINKC. These controls affect all configurations.

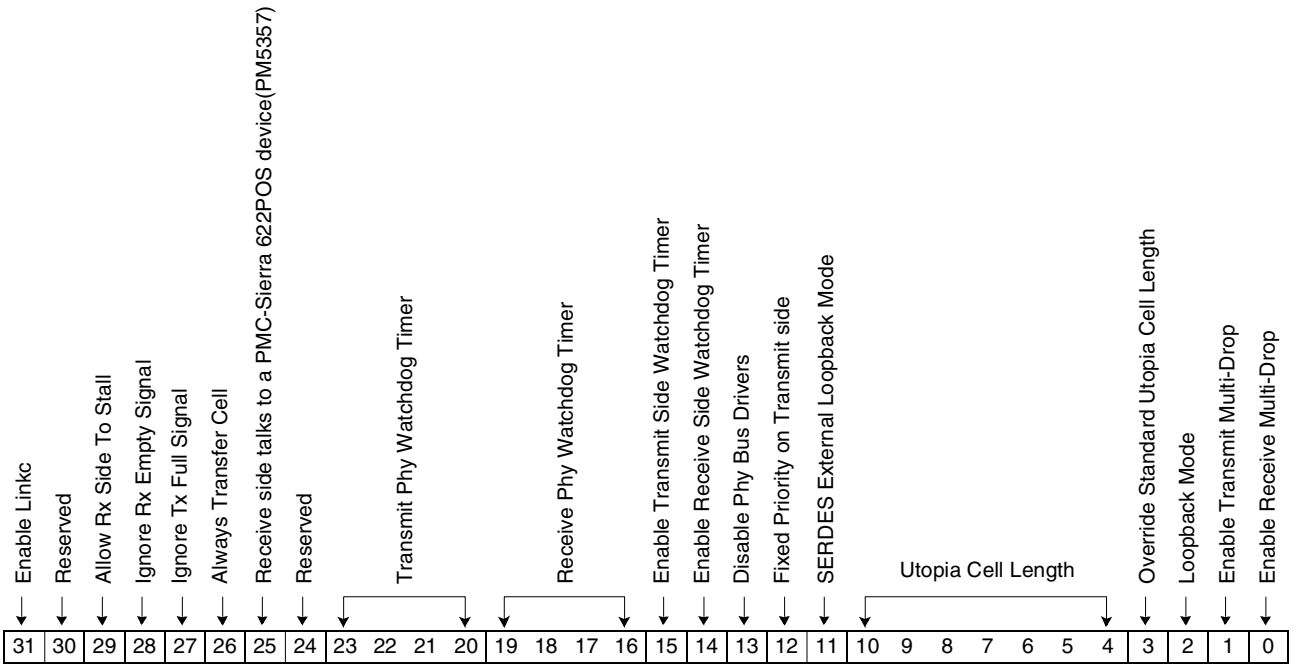
Length 32 bits

Type Clear/Set

Address XXXX 0B30 and 0B34

Power On Reset Value x‘C000 0344’

Restrictions None



Bit(s)	Name	Description
31	Enable LINKC	This bit, when set to ’1’, enables LINKC. The default for this bit is ’1’.
30	Reserved	Reserved.
29	Allow RX Side to Stall	When this bit is set, the Receive side is allowed to stall, allowing the PNR to park on a port until the port has data for the PNR. This bit should be set when the PNR is being run in multi-drop mode and is interfacing with a single drop POS-PHY device that doesn’t have address pins.
28	Ignore RX Empty Signal	When this bit is set to ‘1’, the EMPTY signal is ignored and the PNR always assumes that the PHY has data. The default for this bit is ’0’.
27	Ignore TX Full Signal	When this bit is set the Full signal will be ignored and it is always assumed the PHY has room. The default for this bit is ‘0’.
26	Always Transfer Cell	When this bit is set to ‘1’, the TCA (transmit cell available) is ignored until the current transfer ends. This mode is recommended when talking to a single-drop Utopia device. The default for this bit is ‘0’.
25	Receive Side Talks to a PMC-Sierra 622POS Device(PM5357)	This bit must be set to ‘1’ when the receive side of the PNR is communicating to a PMC-Sierra 622-POS device(PM5357). Setting this bit will cause the PNR to raise FYRENB one cycle before the receive side FIFO overruns.
24	Reserved	Reserved.
23-20	Transmit PHY WatchDog Timer	These four bits are the number of transmit clock cycles the transmit side (LINKT) will wait before switching to another PHY. If the timer times out, a status bit in the LINKC Interrupt/ Status Register will be set for the offending PHY.
19-16	Receive PHY WatchDog Timer	These four bits are the number of receive clock cycles the receive side (LINKR) will wait before switching to another PHY. If the timer times out, a status bit in the LINKC Interrupt/ Status Register will be set for the offending PHY.
15	Enable Transmit Side WatchDog Timer	This bit, when set to ‘1’, causes LINKT to time out if the PHY has started to take data but is now unable to take data for the number of cycles determined by the Transmit PHY Watchdog Timer (bits 23-20). The Timer is only valid if the transmit side is in multi-drop mode.
14	Enable Receive Side WatchDog Timer	This bit, when set to ‘1’, causes LINKR to time out if the PHY is receiving data and is unable to provide data for the number of cycles determined by the Receive PHY watch-dog timer (bits 19-16). The timer is only valid if the receive side of LINKC is in multi-drop mode and the PHY is a Utopia device.
13	Disable PHY Bus Drivers	This bit, when set to ‘1’, tri-states the drivers of the PHY bus. When set to ‘0’, the drivers are enabled.
12	Fixed Priority on Transmit Side	When this bit is set to '1', the transmit side will have a fixed priority instead of a round robin priority. When the fixed priority is used port 0 will have the highest priority and port 3 will have the lowest. The default for this bit is '0'.
11	SERDES External Loopback Mode	When this bit is set to ‘1’, the Receive Side SERDES input is routed to the Transmit Side SERDES output.
10-4	Utopia Cell Length	These seven bits define what the Utopia cell length (in bytes) will be if the override stan-dard Utopia cell length bit (bit 3) is set to ‘1’. The upper limit of this register is 64 and the lower limit is one. The default value of these bits is x‘0110100’.
3	Override Standard Utopia Cell Length	When this bit is set to ‘1’, the standard Utopia cell length (52 or 53 bytes) is replaced by the value in bits 10-4. This bit has no effect on PHYs that aren't Utopia and it disables the HEC generation for any Utopia PHY.

Bit(s)	Name	Description
2	Loop Back Mode	This bit set to '1' places the PNR in an internal loop back mode. The PHY interface will be disabled. The clocks to LINKT and LINKR should be set to the same source in the Clock Control Register. This bit is flushed to a '1' after POR. For loopback to work in multi-drop mode the transmit and receive configurations must be the same. When a configuration is set up for Utopia Cell-based transmission the receive and transmit sides should be identical in all ways. These include odd/even parity, data path length, 52-byte cell mode, null cell generation, and HEC generation of null cells. The additional header bytes should be set to '00' when in loopback mode. See Table 17: *Legal Loopback Configurations* on page 168.
1	Enable Transmit Multi-Drop	Setting this bit to '1' puts the transmit side into multi-drop mode. In multi-drop mode the PNR supports four configurations and four unique ports. This bit should not be set if the transmit side is connected to the Internal SONET Framer. Configuration 0 Transmit Control Register will control the transmit interface. If this bit is not set, the PNR is in single drop mode.
0	Enable Receive Multi-Drop	Setting this bit to '1' puts the receive side into multi-drop mode. In multi-drop mode, the PNR supports four configurations and four unique PHY ports. This bit should not be set if the receive side is connected to the Internal SONET Framer. Configuration 0 Receive Control Register will control the receive interface. If this bit is not set, the PNR receive side is in single drop mode.

Table 17: Legal Loopback Configurations

Configuration 0		Configuration 1		Configuration 2		Configuration 3	
Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive
SONET	SONET	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
Utopia Cell	Utopia Cell	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
Not Used	Not Used	Utopia Cell	Utopia Cell	Not Used	Not Used	Not Used	Not Used
Not Used	Not Used	Not Used	Not Used	Utopia Cell	Utopia Cell	Not Used	Not Used
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Utopia Cell	Utopia Cell
Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell
POS-PHY	POS-PHY	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used
Not Used	Not Used	POS-PHY	POS-PHY	Not Used	Not Used	Not Used	Not Used
Not Used	Not Used	Not Used	Not Used	POS-PHY	POS-PHY	Not Used	Not Used
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	POS-PHY	POS-PHY
POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY
Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY
POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	POS-PHY	POS-PHY
POS-PHY	POS-PHY	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY
POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell
Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	POS-PHY	POS-PHY
Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY
Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell
POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY

Table 17: Legal Loopback Configurations (Continued)

Configuration 0		Configuration 1		Configuration 2		Configuration 3	
Transmit	Receive	Transmit	Receive	Transmit	Receive	Transmit	Receive
POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell
POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell
Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell
Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY	Utopia Cell	Utopia Cell
Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	Utopia Cell	POS-PHY	POS-PHY

3.8.5 LINKC Additional Transmit Control Register

This register contains additional information for controlling the operation of the transmit side of Link.

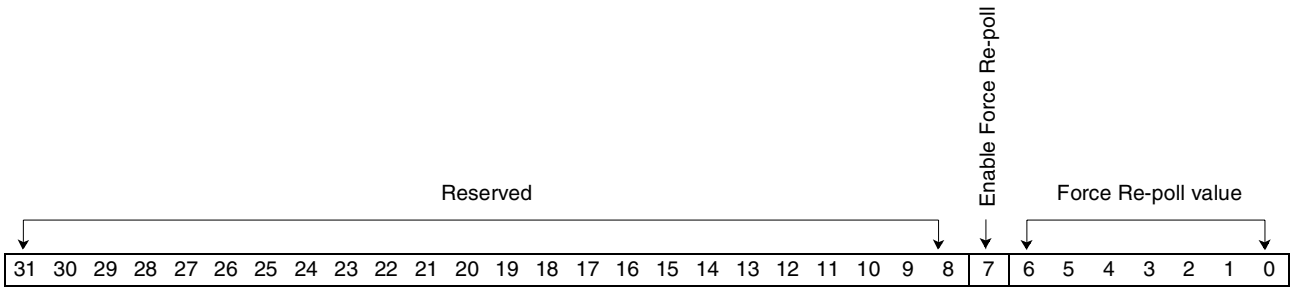
Length 32 bits

Type Clear/Set

Address XXXX 0B88 and 0B8C

Power On Reset Value x‘0000 000C’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7	Enable Force Re-poll	When bit 7 is a logical ’1’ the transmit side will never transmit to the port it is currently transmitting to, until that port has been repolled. Setting this bit to a ‘1’ and setting the Force Re-poll value to x'00' will insure that the transmission of back to back cells/packets to the same port will not happen without a repolling of that port between the ending of the first transfer and the start of the next. When the Enable Force Repoll bit is set to a ‘0’ the transmit side will always use the result of the last poll of the port it is currently transmitting to.
6-0	Force Re-poll Value	When the hex value of bits 6-0 equals the number of bytes left that the transmit side still has to send and force re-poll bit (bit 7) is on then the transmit side forces a repolling of the port to which it is currently transmitting data. If a data transfer is less, then the value of the Force Repoll register then the port will need to be repolled before the transmit side of Charm will transfer another cell/packet to that port. Due to pipelining in the transmit logic and unknown pipelining in the Phys not all values are useful.

3.8.6 LINKC Configuration 0 Transmit & Receive Control Register

This register contains the information that controls the operation of Configuration 0 on the transmit and receive.

Length 32 bits

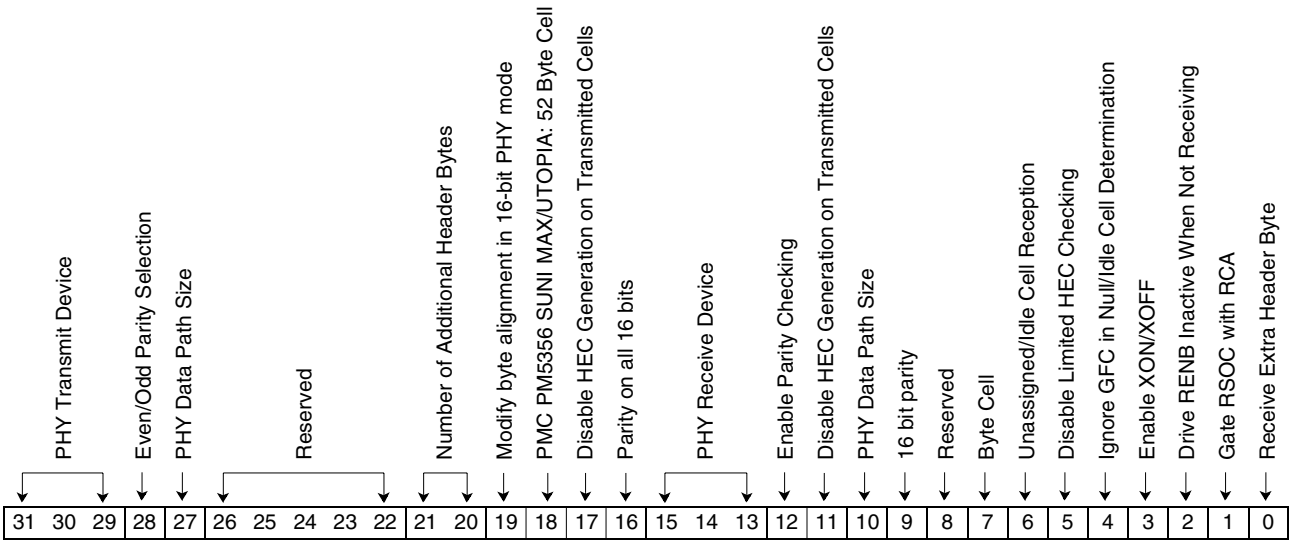
Type Clear/Set

Address XXXX 0B50 and 0B54

Power On Reset Value x‘7801 6E00’

Restrictions Bits 18-16 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA is selected (bits 31-29 = ‘011’). If any other device is chosen, these bits will be ignored.

Bits 7-0 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA is selected (bits 15-13 = ‘011’). Otherwise, they are ignored. Bits 2-0 are used to make adjustments to the Utopia interface for compatibility with the Suni-PHD PHY.



Bit(s)	Name	Description
31-29	PHY Transmit Device	These bits indicate to which PHY the PNR’s Transmit Config 0 will interface. If the configuration’s port address is all ‘1’s, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame-based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Internal SONET(sts-3c)/SDH(STM-1) Framer with SERDES (Serial interface) 111 Reserved
28	Even/Odd Parity Selection	This bit when set to ‘0’, selects even parity. The default value is ‘1’ for odd parity. Parity will always be generated when the PNR is transmitting data. If the PHY does not check parity, do not connect the lines.

Bit(s)	Name	Description
27	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY is eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Receive PHY device but not as the Transmit PHY device. In this case, '1' on this bit allows FYTDAT(1 - 13) to be used for the 16-bit external Transmit PHY device, while a '0' allows FYTDAT(15-13) to be used for the Receive HDLC controller. This implies that it is not possible to use the internal receive framer, the Receive HDLC interface, and an external 16-bit transmit framer at the same time.
26-22	Reserved	Reserved.
21-20	Number of Additional Header Bytes	These bits indicate the number of additional header bytes that will be read from SEGBF and added to the beginning of each cell as each is transmitted to the PHY. The bytes are meant to be used for additional routing information. These control bits have no effect in IBM 25 Mb/s PHY mode, and should be set to '0's when in internal SONET/SDH framer mode. If used in conjunction with 52-byte mode, the byte normally containing the cell HEC will not be transmitted and the total number of cells transmitted will be the value of this field plus 52. If 16-bit PHY mode is selected, by default, the byte alignment will follow that of normal 52- or 53-byte 16-bit mode, with the additional header bytes contiguously prepended. As a result, a mode with three additional header bytes cannot be obtained in 53-byte, 16-bit mode (LSB is normally padded with zeros so MSB gets truncated). Bit 3 of this register is therefore provided to adjust the alignment in 16-bit, 53-byte mode so all five header bytes will be transmitted with up to three additional router bytes prepended.
19	Modify Byte Alignment in 16-Bit PHY Mode	When set to '1', this bit changes the default byte alignment in 16-bit PHY mode if this register also contains a non-zero value in bits 21-20. See the description of those bits for further details.
18	52 Byte Cell	When set, the cell sent to the PHY will be 52 bytes. No HEC byte will be sent.
17	Disable HEC Generation on Transmitted Cells	When this bit is set to '1', x'00' will be placed in the HEC byte of Utopia cells. If bit 17 is set to '0', the value of the LINKC Transmitted HEC Control byte will be sent. If bit 18 is set to '1', then no HEC will be sent and this bit will be ignored.
16	Parity on All 16 Bits	When set, this bit enables the PNR to produce a single parity bit across the 16-bit transmit data bus. When set to '0', the PNR produces two parity bits, one across generation and the lower half of the 16 bits (parity bit 0) and one against the upper (parity bit 1). The default for this bit is '1'.
15-13	PHY Receive Device	These bits indicate to which PHY the PNR's Receive Config 0 will interface. If the configuration's port address is all '1's, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame-based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Internal SONET (sts-3c)/SDH(STM-1) Framer with SERDES (Serial Interface) 111 Reserved
12	Enable Parity Checking	When set to '1', this bit enables checking of parity on data from the receive path. When set to '0' (default), parity checking is disabled. The upper bit of the transmit parity is not valid when the internal SONET/SDH Framer has been selected as the receive PHY device. The upper bit of the receive parity is also not valid when the internal SONET/SDH Framer has been selected as the transmit PHY device. This is only a concern if a combination of the internal framer and an external PHY is being used and that external PHY has a 16-bit data interface. In this case, parity cannot be checked or generated on the upper byte.
11	Even/Odd Parity Selection	When this bit is set to '0', even parity is selected. When this bit is set to '1' (default), odd parity is selected.

Bit(s)	Name	Description
10	PHY Data Path Size	This bit, when set to ‘0’, selects a 16-bit wide data path to the PHY device. When set to ‘1’, this bit selects an 8-bit wide data path to the PHY device. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Receive PHY device but not as the Transmit PHY device. In this case, a ‘1’ on this bit allows FYTDAT(15-13) to be used for the 16-bit external Transmit PHY device, while a zero allows FYTDAT(15-13) to be used for the Receive HDLC controller. This implies that it is not possible to use the internal receive framer, the Receive HDLC interface, and an external 16-bit transmit framer at the same time.
9	16 Bit Parity	When this bit is set to ‘1’ in 16-bit mode, parity will be calculated across all 16 bits and checked against FYRPAR(1). When this bit is set to ‘0’ in 8-bit mode, the parity will be checked against FYRPAR(1). This bit has no effect if receive device is POS-PHY. The default setting of this bit is ‘1’.
8	Reserved	Reserved.
7	Byte Cell	When this bit is set to ‘1’, the cell received from the PHY will be 52 bytes. No HEC byte will be received.
6	Unassigned/Idle Cell Reception	When set to ‘1’, this bit will enable unassigned/idle cell reception. This should be set to ‘0’ when using the internal SONET Framer.
5	Disable Limited HEC Checking on Received Idle/Unassigned Cells	When this bit is set to ‘1’, the receive logic ignores the HEC byte of the header of idle and unassigned cells. Idle is defined as a header of x‘0000 0001’ and unassigned is defined as a header of x‘0000 000n’ where n is ‘xxx0’. If bit 6 is set to enable unassigned/idle cell reception, all cells will be passed to REASM regardless of how this bit is set. If bit 6 is set to disable unassigned/idle cell reception and this bit is set to ’0’, the HEC byte of cells with an apparent idle header is completely checked before deciding whether or not to pass the cell to REASM. If a cell appears to have an unassigned header, HEC bits 7, 6, and 0 are checked because they are a constant, regardless of the value of bits 3, 2, and 1 of the header. If other HEC bits are bad, REASM detects the HEC error and discards the cell. If there is a correctable HEC error and the cell is indeed unassigned, an out of range error occurs in REASM.
4	Ignore GFC in Null/Idle Cell Determination	This bit, when set to ‘1’, causes the receive logic to ignore the first four bits of the ATM header in determining whether a cell being received is a null or idle cell.
3	Enable XON/XOFF	This bit, when set to ‘1’, allows the XON/XOFF bit of the header of a received cell to suspend or continue transmission from the PNR’s transmit logic for all ports associated with Config 0.
2	Drive RENB Inactive When Not Receiving	This bit, when set to ‘1’, forces the receive logic to deactivate RENB when in the idle state.
1	Gate RSOC with RCA	This bit, when set to ’1’, forces the receive logic to see both RSOC and RCA before considering RSOC valid.
0	Receive Extra Header Byte	This bit, when set to ’1’, allows an extra header byte to be accepted at the start of a cell by the receive logic. The extra byte is discarded.

3.8.7 LINKC Configuration 1 Transmit & Receive Control Register

This register contains the information which controls the operation of Configuration 1 on the transmit and receive.

Length 32 bits

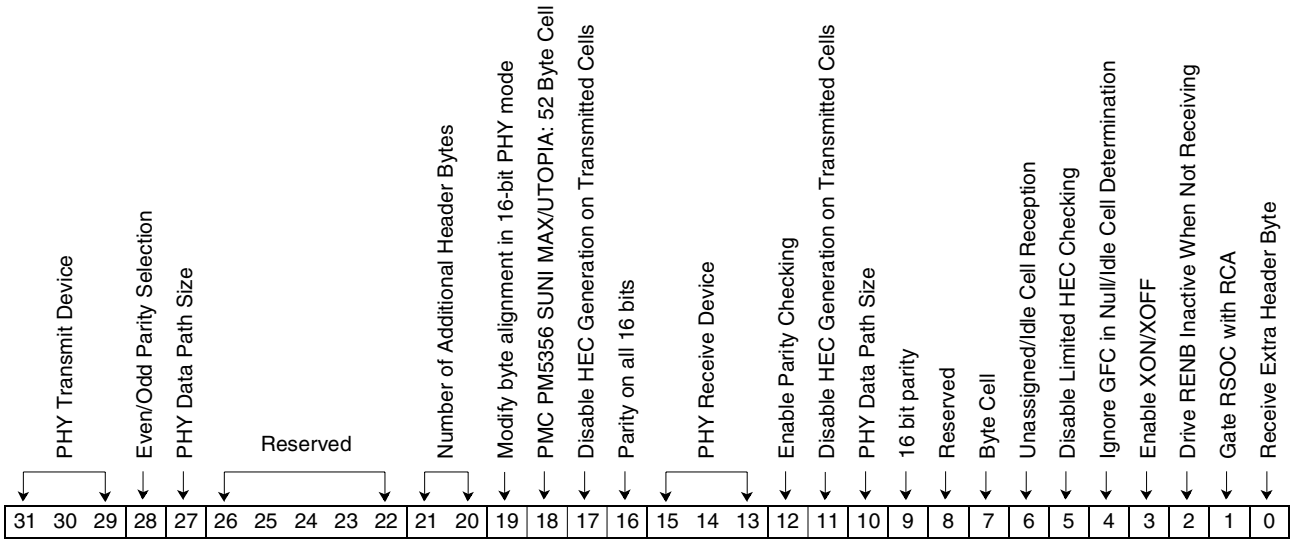
Type Clear/Set

Address XXXX 0B58 and 0B5C

Power On Reset Value x‘7801 6E00’

Restrictions Bits 18-16 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 31-29 = ‘011’) is selected. If any other device is chosen these bits will be ignored.

Bits 7-0 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 15-13 = ‘011’) is selected. Otherwise, these bits will be ignored. Bits 2-0 are used to make adjustments to the Utopia interface for compatibility with the Suni-PHD PHY.



Bit(s)	Name	Description
31-29	PHY Transmit Device	Bits 31, 30, and 29 indicate to which PHY the PNR’s Transmit Config 1 will be interfacing. If the configuration’s port address is all ‘1’s, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
28	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for odd parity. Parity will always be generated when the PNR is transmitting data. If the PHY does not check parity, do not connect the lines.

Bit(s)	Name	Description
27	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY will be eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit will allow FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero will allow FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
26-22	Reserved	Reserved.
21-20	Number of Additional Header Bytes	The value of bits 21-20 indicates the number of additional header bytes that will be read from SEGBF and added to the beginning of each cell as each is transmitted to the PHY. The bytes are meant to be used for additional routing information. These control bits have no effect in IBM 25 Mb/s PHY mode, and should be set to '0's when in internal SONET/SDH framer mode. If used in conjunction with 52-byte mode, the byte normally containing the cell HEC will not be transmitted and the total number of cells transmitted will be the value of this field plus 52. If 16-bit PHY mode is selected, by default, the byte alignment will follow that of normal 52- or 53-byte 16-bit mode, with the additional header bytes contiguously prepended. As a result, a mode with three additional header bytes cannot be obtained in 53-byte, 16-bit mode (LSB is normally padded with zeros so MSB gets truncated). Bit 3 of this register is therefore provided to adjust the alignment in 16-bit, 53-byte mode so all five header bytes will be transmitted with up to three additional router bytes prepended.
19	Modify Byte Alignment in 16-Bit PHY Mode	When set to '1', this bit changes the default byte alignment in 16-bit PHY mode if this register also contains a non-zero value in bits 21-20. See the description of those bits for further details.
18	52 Byte Cell	When set, the cell sent to the PHY will be 52 bytes. No HEC byte will be sent.
17	Disable HEC Generation on Transmitted Cells	If bit 17 is set to '1', x'00' will be placed in the HEC byte of Utopia cells. If bit 17 is set to '0', the value of LINKC Transmitted HEC Control byte will be sent. If bit 18 is set to '1', then no HEC will be sent and this bit will be ignored.
16	Parity on All 16 Bits	When set, this bit enables the PNR to produce a single parity bit across the 16-bit transmit data bus. When set to '0', the PNR produces two parity bits, one across generation and the lower half of the 16 bits (parity bit zero) and one against the upper (parity bit 1). The default for this bit is '1'.
15-13	PHY Receive Device	Bits 15, 14, and 13 indicate which PHY the PNR's Receive Config 1 will be interfacing. If the configuration's port address is all '1's, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
12	Enable Parity Checking	When set, this bit enables checking of parity on data from the receive path. The default is that parity checking is disabled. The upper bit of the transmit parity is not valid when the internal SONET/SDH Framer has been selected as the receive PHY device. The upper bit of the receive parity is also not valid when the internal SONET/SDH Framer has been selected as the transmit PHY device. This is only a concern if a combination of the internal framer and an external PHY is being used and that external PHY has a 16-bit data interface. In this case, parity cannot be checked/generated on the upper byte.
11	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for odd parity.

Bit(s)	Name	Description
10	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY is eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit will allow FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero will allow FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
9	16 Bit Parity	When this bit is set to '1' and it is in 16-bit mode, parity will be calculated across all 16 bits and checked against FYRPAR(1). When in eight-bit mode with bit 9 set to '0', the parity will be compared against FYRPAR(1). This bit has no effect if the receive device is POS-PHY. The default setting of this bit is '1'.
8	Reserved	Reserved.
7	52 Byte Cell	When set, the cell received from the PHY is 52 bytes. No HEC byte will be received.
6	Unassigned/Idle Cell Reception	When set to '1', this bit will enable unassigned/idle cell reception. This should be set to '0' when using the internal SONET Framer.
5	Disable Limited HEC Checking on Received Idle/Unassigned Cells	If bit 5 is set to '1', the receive logic will ignore the HEC byte of the header of idle and unassigned cells. Idle is defined as a header of x'0000 0001' and unassigned is defined as a header of x'0000 000N' where N is 'XXX0'. If bit 6 is set to enable unassigned/idle cell reception, all cells are passed to REASM regardless of how this bit is set. If bit 6 is set to disable unassigned/idle cell reception and this bit is set to '0', the HEC byte of cells with an apparent idle header will be completely checked before deciding whether or not to pass the cell to REASM. If a cell appears to have an unassigned header, HEC bits seven, six, and zero will be checked because they are a constant regardless of the value of bits 3-1 of the header. If other HEC bits are bad, REASM will detect the HEC error and discard the cell. If there is a correctable HEC error and the cell is indeed unassigned, an out of range error will occur in REASM.
4	Ignore GFC in Null/Idle Cell Determination	Bit 4, when set, will cause the receive logic to ignore the first four bits of the ATM header in determining whether a cell being received is a null or idle cell.
3	Enable XON/XOFF	Bit 3, when set, will allow the XON/XOFF bit of the header of a received cell to suspend/continue transmission from the PNR's transmit logic for all ports associated with Config 1.
2	Drive RENB Inactive When Not Receiving	When set to '1', this bit forces the receive logic to deactivate RENB when in the idle state.
1	Gate RSOC with RCA	When set to '1', this bit forces the receive logic to see both RSOC and RCA before considering RSOC valid.
0	Receive Extra Header Byte	When set to '1', this bit allows an extra header byte to be accepted at the start of a cell by the receive logic. The extra byte is discarded.

3.8.8 LINKC Configuration 2 Transmit & Receive Control Register

This register contains the information that controls the operation of configuration 2 on the transmit and receive.

Length 32 bits

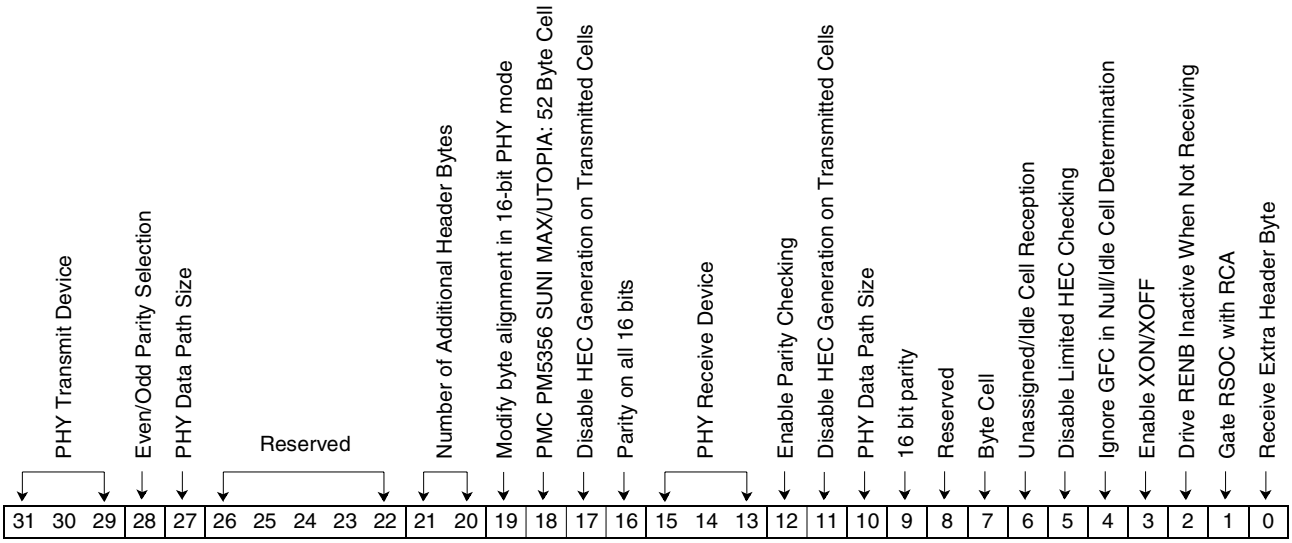
Type Clear/Set

Address XXXX 0B60 and 0B64

Power On Reset Value x‘7801 6E00’

Restrictions Bits 18-16 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 31-29 = ‘011’) is selected. If any other device is chosen these bits will be ignored.

Bits 7-0 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 15-13 = ‘011’) is selected. If any other device is chosen, these bits are ignored. Bits two through zero are used to make adjustments to the Utopia interface for compatibility with the Suni-PHD PHY.



Bit(s)	Name	Description
31-29	PHY Transmit Device	Bits 31, 30, and 29 indicate which PHY the PNR’s Transmit Config 2 will be interfacing. If the configuration’s port address is all 1s, the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
28	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for odd parity. Parity will always be generated when the PNR is transmitting data. If the PHY does not check parity, do not connect the lines.

Bit(s)	Name	Description
27	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY will be eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit allows FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero allows FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
26-22	Reserved	Reserved.
21-20	Number of Additional Header Bytes	The value of bits 21-20 indicate the number of additional header bytes that will be read from SEGBF and added to the beginning of each cell as each is transmitted to the PHY. The bytes are meant to be used for additional routing information. These control bits have no effect in IBM 25 Mb/s PHY mode, and should be set to '0's when in internal SONET/SDH framer mode. If used in conjunction with 52-byte mode, the byte normally containing the cell HEC will not be transmitted and the total number of cells transmitted will be the value of this field plus 52. If 16-bit PHY mode is selected, by default, the byte alignment will follow that of normal 52- or 53-byte 16-bit mode, with the additional header bytes contiguously prepended. As a result, a mode with three additional header bytes cannot be obtained in 53-byte, 16-bit mode (LSB is normally padded with zeros so MSB gets truncated). Bit 3 of this register is therefore provided to adjust the alignment in 16-bit, 53-byte mode so all five header bytes will be transmitted with up to three additional router bytes prepended.
19	Modify Byte Alignment in 16-Bit PHY Mode	When set to '1', this bit changes the default byte alignment in 16-bit PHY mode if this register also contains a non-zero value in bits 21-20. See the description of those bits for further details.
18	52 Byte Cell	When set, the cell sent to the PHY is 52 bytes. No HEC byte will be sent.
17	Disable HEC Generation on Transmitted Cells	If bit 17 is set to '1', x'00' will be placed in the HEC byte of Utopia cells. If bit 17 is set to '0', the value of LINKC Transmitted HEC Control byte will be sent. If bit 18 is set to '1', then no HEC is sent and this bit will be ignored.
16	Parity on All 16 Bits	When set, this bit enables the PNR to produce a single parity bit across the 16-bit transmit data bus. When set to '0', the PNR will produce two parity bits, one across generation and the lower half of the 16 bits (parity bit zero) and one against the upper (parity bit 1). The default for this bit is '1'.
15-13	PHY Receive Device	Bits 15, 14, and 13 indicate which PHY the PNR's Receive Config 2 will be interfacing. If the configuration's port address is all ones, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
12	Enable Parity Checking	When set, this bit will enable checking of parity on data from the receive path. The default parity checking is disabled. The upper bit of the transmit parity is not valid when the internal SONET/SDH Framer has been selected as the receive PHY device. The upper bit of the receive parity is also not valid when the internal SONET/SDH Framer has been selected as the transmit PHY device. This is only a concern if a combination of the internal framer and an external PHY is being used and that external PHY has a 16-bit data interface. In this case, parity cannot be checked/generated on the upper byte.
11	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for odd parity.

Bit(s)	Name	Description
10	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY will be eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit will allow FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero allows FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
9	16 Bit Parity	When this bit is set to '1' and it is in 16-bit mode, that parity will be calculated across all 16 bits and check against FYRPAR(1). When in eight-bit mode with bit 9 set to '0', the parity will be compared against FYRPAR(1). This bit has no effect if receive device is POS-PHY. The default setting of this bit is '1'.
8	Reserved	Reserved.
7	52 Byte Cell	When set, the cell received from the PHY is 52 bytes. No HEC byte is received.
6	Unassigned/Idle Cell Reception	When set to '1', this bit will enable unassigned/idle cell reception. This should be set to '0' when using the internal SONET Framer.
5	Disable Limited HEC Checking on Received Idle/Unassigned Cells	If bit 5 is set to '1', the receive logic will ignore the HEC byte of the header of idle and unassigned cells. Idle is defined as a header of x'0000 0001' and unassigned is defined as a header of x'0000 000N' where n is 'XXX0'. If bit 6 is set to enable unassigned/idle cell reception, all cells are passed to REASM regardless of how this bit is set. If bit 6 is set to disable unassigned/idle cell reception and this bit is set to '0', the HEC byte of cells with an apparent idle header will be completely checked before deciding whether or not to pass the cell to REASM. If a cell appears to have an unassigned header, HEC bits seven, six, and zero will be checked because they are a constant regardless of the value of bits 3-1 of the header. If other HEC bits are bad, REASM will detect the HEC error and discard the cell. If there is a correctable HEC error and the cell is indeed unassigned, an out of range error will occur in REASM.
4	Ignore GFC in Null/Idle Cell Determination	Bit 4, when set, causes the receive logic to ignore the first four bits of the ATM header in determining whether a cell being received is a null or idle cell.
3	Enable XON/XOFF	Bit 3, when set, allows the XON/XOFF bit of the header of a received cell to suspend/continue transmission from the PNR's transmit logic for all ports associated with Config 2.
2	Drive RENB Inactive When Not Receiving	When set to '1', this bit forces the receive logic to deactivate RENB when in the idle state.
1	Gate RSOC with RCA	When set to '1', this bit forces the receive logic to see both RSOC and RCA before considering RSOC valid.
0	Receive Extra Header Byte	When set to '1', this bit allows an extra header byte to be accepted at the start of a cell by the receive logic. The extra byte is discarded.

3.8.9 LINKC Configuration 3 Transmit & Receive Control Register

This register contains the information which controls the operation of configuration 3 on the transmit and receive.

Length 32 bits

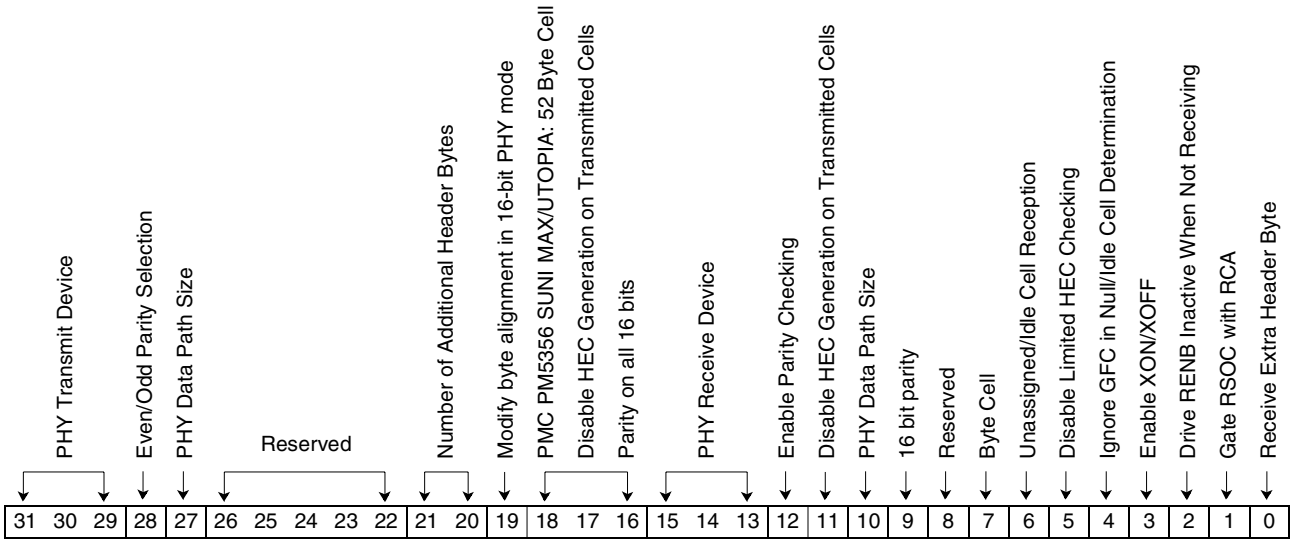
Type Clear/Set

Address XXXX 0B68 and 0B6C

Power On Reset Value x‘7801 6E00’

Restrictions Bits 18-16 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 31-29 = ‘011’) is selected. If any other device is chosen these bits will be ignored.

Bits 7-0 only have meaning if a PMC PM5356 SUNI MAX/UTOPIA (bits 15-13 = ‘011’) is selected. If any other device is chosen, these bits are ignored. Bits 2-0 are used to make adjustments to the Utopia interface for compatibility with the Suni-PHD PHY.



Bit(s)	Name	Description
31-29	PHY Transmit Device	Bits 31, 30, and 29 indicate to which PHY the PNR’s Transmit Config 3 will be interfacing. If the configuration’s port address is all ‘1’s, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
28	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for Odd parity. Parity will always be generated when the PNR is transmitting data. If the PHY does not check parity, do not connect the lines.

Bit(s)	Name	Description
27	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY will be eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit will allow FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero will allow FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
26-22	Reserved	Reserved.
21-20	Number of Additional Header Bytes	The value of bits 21-20 indicate the number of additional header bytes that will be read from SEGBF and added to the beginning of each cell as each is transmitted to the PHY. The bytes are meant to be used for additional routing information. These control bits have no effect in IBM 25 Mb/s PHY mode, and should be set to '0's when in internal SONET/SDH framer mode. If used in conjunction with 52-byte mode, the byte normally containing the cell HEC will not be transmitted and the total number of cells transmitted will be the value of this field plus 52. If 16-bit PHY mode is selected, by default, the byte alignment will follow that of normal 52- or 53-byte 16-bit mode, with the additional header bytes contiguously prepended. As a result, a mode with three additional header bytes cannot be obtained in 53-byte, 16-bit mode (LSB is normally padded with zeros so MSB gets truncated). Bit 3 of this register is therefore provided to adjust the alignment in 16-bit, 53-byte mode so all five header bytes will be transmitted with up to three additional router bytes prepended.
19	Modify Byte Alignment in 16-Bit PHY Mode	When set to '1', this bit changes the default byte alignment in 16-bit PHY mode if this register also contains a non-zero value in bits 21-20. See the description of those bits for further details.
18	52 Byte Cell	When set, the cell sent to the PHY is 52 bytes. No HEC byte will be sent.
17	Disable HEC Generation on Transmitted Cells	If bit 17 is set to '1', x'00' will be placed in the HEC byte of Utopia cells. If bit 17 is set to '0', the value of LINKC Transmitted HEC Control byte will be sent. If bit 18 is set to '1', no HEC is sent and this bit will be ignored.
16	Parity on All 16 Bits	When set, this bit enables the PNR to produce a single parity bit across the 16-bit transmit data bus. When set, the PNR produces two parity bits, one across generation and the lower half of the 16 bits (parity bit 0) and one against the upper (parity bit 1). The default for this bit is '1'.
15-13	PHY Receive Device	Bits 15, 14, and 13 indicate to which PHY the PNR's Receive Config 3 will be interfacing. If the configuration's port address is all ones, then the configuration is unused and the value of these bits does not matter. 000 Reserved 001 PMC POS-PHY (Frame based Utopia) 010 Reserved 011 PMC PM5356 SUNI MAX/UTOPIA interface (STS-3c/STM-1 OR STS-1) 100 Reserved 101 Reserved 111 Reserved
12	Enable Parity Checking	When set, this bit enables checking of parity on data from the receive path. The default is that parity checking is disabled. The upper bit of the transmit parity is not valid when the internal SONET/SDH Framer has been selected as the receive PHY device. The upper bit of the receive parity is also not valid when the internal SONET/SDH Framer has been selected as the transmit PHY device. This is only a concern if a combination of the internal framer and an external PHY is being used and that external PHY has a 16-bit data interface. In this case, parity cannot be checked/generated on the upper byte.
11	Even/Odd Parity Selection	Even parity is selected when this bit is cleared. The default value is for odd parity.

Bit(s)	Name	Description
10	PHY Data Path Size	This bit, when set to '0', selects a 16-bit wide data path to the PHY device. When set to '1', the data path width to the PHY will be eight bits. This bit has no effect on the internal SONET/SDH framer except if the internal framer has been selected as the Rx PHY device but not as the Tx PHY device. In this case, a '1' on this bit will allow FYTDAT(15-13) to be used for the 16-bit external Tx PHY device, while a zero will allow FYTDAT(15-13) to be used for the Rx HDLC controller. This implies that it is not possible to use the internal RX framer, the RX HDLC interface, and an external 16-bit TX framer at the same time.
9	16 Bit Parity	When this bit is set to '1' and it is in 16-bit mode, parity will be calculated across all 16 bits and checked against FYRPAR(1). When in eight-bit mode with bit 9 set to '0', the parity is compared against FYRPAR(1). This bit has no effect if receive device is POS-PHY. The default setting of this bit is '1'.
8	Reserved	Reserved.
7	52 Byte Cell	When set, the cell received from the PHY is 52 bytes. No HEC byte will be received.
6	Unassigned/Idle Cell Reception	When set to '1', this bit will enable unassigned/idle cell reception. This should be set to '0' when using the internal SONET Framer.
5	Disable Limited HEC Checking on Received Idle/Unassigned Cells	If bit 5 is set to '1', the receive logic will ignore the HEC byte of the header of idle and unassigned cells. Idle is defined as a header of x'0000 0001' and unassigned is defined as a header of x'0000 000N' where N is B'XXX0'. If bit 6 is set to enable unassigned/idle cell reception, all cells are passed to REASM regardless of how this bit is set. If bit 6 is set to disable unassigned/idle cell reception and this bit is set to '0', the HEC byte of cells with an apparent idle header will be completely checked before deciding whether or not to pass the cell to REASM. If a cell appears to have an unassigned header, HEC bits 7, 6, and 0 are checked because they are a constant regardless of the value of bits 3-1 of the header. If other HEC bits are bad, REASM detects the HEC error and discards the cell. If there is a correctable HEC error and the cell is indeed unassigned, an out of range error occurs in REASM.
4	Ignore GFC in Null/Idle Cell Determination	Bit 4, when set, causes the receive logic to ignore the first four bits of the ATM header in determining whether a cell being received is a null or idle cell.
3	Enable XON/XOFF	Bit 3, when set, allows the XON/XOFF bit of the header of a received cell to suspend/continue transmission from the PNR's transmit logic for all ports associated with Config 3.
2	Drive RENB Inactive When Not Receiving	When set to '1', this bit forces the receive logic to deactivate RENB when in the idle state.
1	Gate RSOC with RCA	When set to '1', this bit forces the receive logic to see both RSOC and RCA before considering RSOC valid.
0	Receive Extra Header Byte	When set to '1', this bit allows an extra header byte to be accepted at the start of a cell by the receive logic. The extra byte is discarded.

3.8.10 LINKC Map Transmit Configurations to Port Addresses

This register contains the port address for each of the transmit configurations. If the port address is ‘11111’ then the configuration is unused.

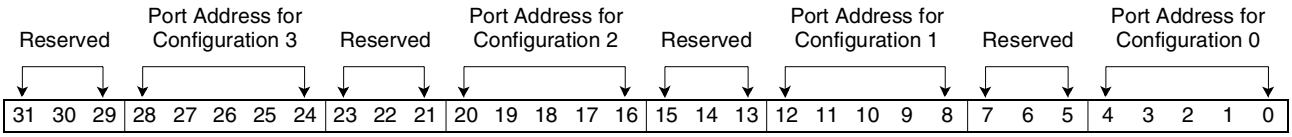
Length 32 bits

Type Clear/Set

Address XXXX 0B70 and 0B74

Power On Reset Value x‘1F1F 1F1F’

Restrictions None



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28-24	Port Address for Configuration 3	Port Address for Configuration 3.
23-21	Reserved	Reserved.
20-16	Port Address for Configuration 2	Port Address for Configuration 2.
15-13	Reserved	Reserved.
12-8	Port Address for Configuration 1	Port Address for Configuration 1.
7-5	Reserved	Reserved.
4-0	Port Address for Configuration 0	Port Address for Configuration 0.

3.8.11 LINKC Map Receive Configurations to Port Addresses

This register contains the port address for each of the receive configurations. If the port address is '11111' then the configuration is unused.

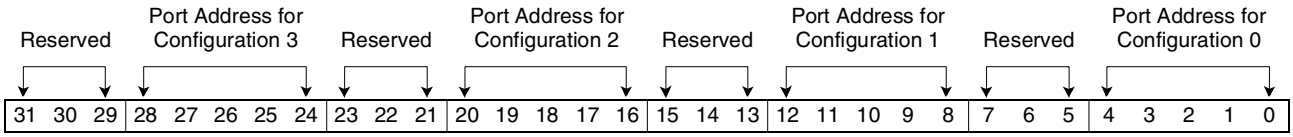
Length 32 bits

Type Clear/Set

Address XXXX 0B80 and 0B84

Power On Reset Value x'1F1F 1F1F'

Restrictions None



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28-24	Port Address for Configuration 3	Port Address for Configuration 3.
23-21	Reserved	Reserved.
20-16	Port Address for Configuration 2	Port Address for Configuration 2.
15-13	Reserved	Reserved.
12-8	Port Address for Configuration 1	Port Address for Configuration 1.
7-5	Reserved	Reserved.
4-0	Port Address for Configuration 0	Port Address for Configuration 0.

3.8.12 LINKC Transmitted HEC Control Byte

When the PNR is transmitting to a 53-byte Utopia PHY the HEC byte (byte five of the ATM header) will be sent as x‘00’, if bit 17 of the transmitting configuration is a ‘1’. Otherwise the value of the LINKC Transmitted HEC Control Byte Register will be sent.

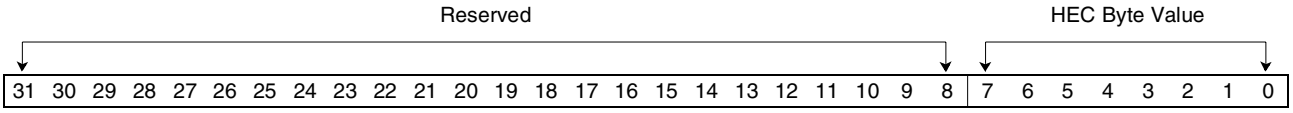
Length 32 bits

Type Read/Write

Address XXXX 0B04

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	HEC Byte Value	Value of the HEC byte to be sent when talking to a 53-byte Utopia PHY.

3.8.13 LINKC Interrupt/Status Register

This register reports the status of LINKC.

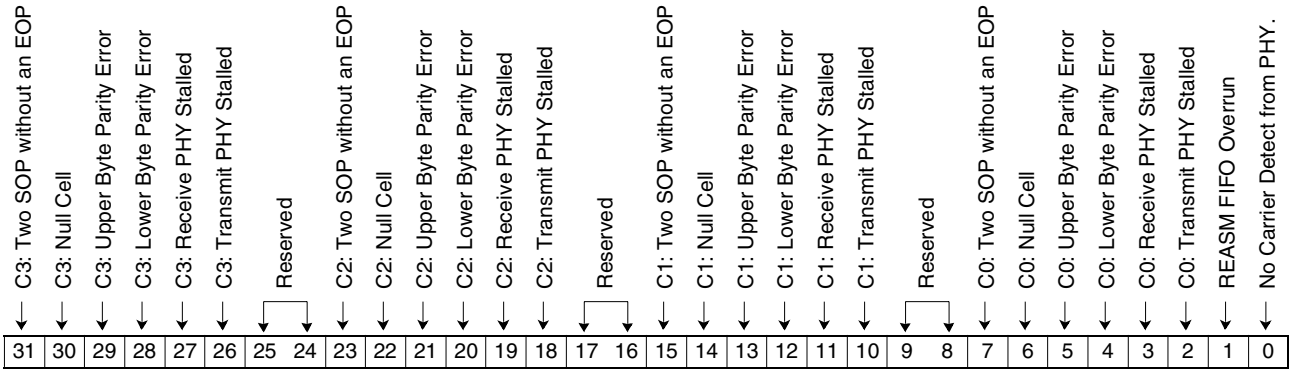
Length 32 bits

Type Clear/Set

Address XXXX 0B10 and 0B14

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31	C3: Two SOP without an EOP	Indicates that Config 3 has seen two SOPs in a 64-byte boundary without an EOP. Multiple SOPs outside the 64-byte boundary will be passed up, and it is up to the higher levels to deal with this case.
30	C3: Null Cell	Indicates that Config 3 has received a null cell.
29	C3: Upper Byte Parity Error	Indicates a parity error on the upper byte of receive data from the Config 3 PHY.
28	C3: Lower Byte Parity Error	Indicates a parity error on the lower byte of receive data from the Config 3 PHY.
27	C3: Receive PHY Stalled	Indicates Config 3’s receive PHY has stalled out.
26	C3: Transmit PHY Stalled	Indicates Config 3’s transmit PHY has stalled out.
25-24	Reserved	Reserved.
23	C2: Two SOP without an EOP	Indicates that Config 2 has seen two SOPs in a 64-byte boundary without an EOP. Multiple SOPs outside the 64-byte boundary will be passed up, and it is up to the higher levels to deal with this case.
22	C2: Null Cell	Indicates that Config 2 has received a null cell.
21	C2: Upper Byte Parity Error	Indicates a parity error on the upper byte of receive data from the Config 2 PHY.
20	C2: Lower Byte Parity Error	Indicates a parity error on the lower byte of receive data from the Config 2 PHY.
19	C2: Receive PHY Stalled	Indicates Config 2’s receive PHY has stalled out.
18	C2: Transmit PHY Stalled	Indicates Config 2’s transmit PHY has stalled out.
17-16	Reserved	Reserved.
15	C1: Two SOP without an EOP	Indicates that Config 1 has seen two SOPs in a 64-byte boundary without an EOP. Multiple SOPs outside the 64-byte boundary will be passed up, and it is up to the higher levels to deal with this case.

Bit(s)	Name	Description
14	C1: Null Cell	Indicates that Config 1 has received a null cell.
13	C1: Upper Byte Parity Error	Indicates a parity error on the upper byte of receive data from the Config 1 PHY.
12	C1: Lower Byte Parity Error	Indicates a parity error on the lower byte of receive data from the Config 1 PHY.
11	C1: Receive PHY Stalled	Indicates Config 1's receive PHY has stalled out.
10	C1: Transmit PHY Stalled	Indicates Config 1's transmit PHY has stalled out.
9-8	Reserved	Reserved.
7	C0: Two SOP without an EOP	Indicates that Config 0 has seen two SOPs in a 64-byte boundary without an EOP. Multiple SOPs outside the 64-byte boundary will be passed up, and it is up to the higher levels to deal with this case.
6	C0: Null Cell	Indicates that Config 0 has received a null cell.
5	C0: Upper Byte Parity Error	Indicates a parity error on the upper byte of receive data from the Config 0 PHY.
4	C0: Lower Byte Parity Error	Indicates a parity error on the lower byte of receive data from the Config 0 PHY.
3	C0: Receive PHY Stalled	Indicates Config 0's receive PHY has stalled out.
2	C0: Transmit PHY Stalled	Indicates Config 0's transmit PHY has stalled out.
1	REASM FIFO Overrun	REASM FIFO has been overrun.
0	No Carrier Detect from PHY	No carrier detect from the PHY.

3.8.14 LINKC Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *LINKC Interrupt/ Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from LINKC to INTST when the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0B18 and 0B1C

Power On Reset Value x'0000 0000'

Restrictions None

3.8.15 LINKC Prioritized Interrupts

Used to access the prioritized encoding of LINKC interrupts. Reading this location will give a decimal number that is the prioritized encoding of bits 7-0 in the *LINKC Interrupt/Status Register* (seven being the most significant bit) assuming the corresponding enable bit is on.

Length 32 bits

Type Read Only

Address XXXX 0B2C

Power On Reset Value x'0000 0000'

Restrictions None

Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Prioritize Interrupts	Prioritized encoding of bits 7-0 in COMET/PAKIT Status Register.

3.8.16 LINKC Transmit State Machine Register

This register indicates the state of the transmit sequencer.

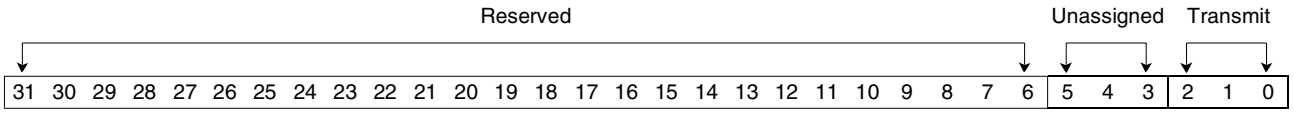
Length 32 bits

Type Read/Write

Address XXXX 0B24

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-6	Reserved	Reserved.
5-3	Cell State Machine	Unassigned cell state machine.
2-0	Transmit State Machine	Transmit state machine.

3.8.17 LINKC Receive State Machine Register

This register indicates the state of the receiver sequencer.

Length 32 bits

Type Read/Write

Address XXXX 0B28

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-2	Reserved	Reserved.
1-0	Receive State Machine	Receive state machine.

3.8.18 LINKC LAN Address Register

If using an IBM built adapter that utilizes external EPROM, this register contains the ROM level in bits 63-48 and the LAN address of the adapter in bits 47-0. The lower address selects bits 63-32 and the higher address selects bits 31-0.

Length 64 bits

Type Read/Write

Address XXXX 0B38 and 0B3C

Power On Reset Value x‘AAAA 5555 5555 AAAA’

Restrictions None

3.8.19 LINKC Canonical LAN Address Register

This register contains the same data as the LINKC LAN Address Register except each byte is bit reversed. This allows the user to obtain the LAN address in canonical format.

Length 64 bits

Type Read Only

Address XXXX 0B08 and 0B0C

Power On Reset Value x‘5555 AAAA AAAA 5555’

Restrictions None

3.8.20 LINKC Passed TX Data Register

The bits in this register are passed over PHY transmit data I/O 15-8 when using an 8-bit wide PHY data bus. This allows these I/Os to be used to control other devices that are external to the PNR.

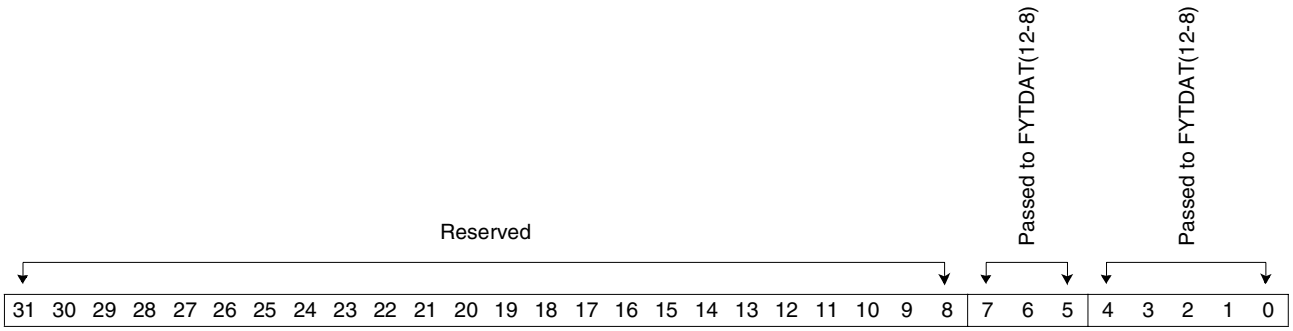
Length 32 bits

Type Read/Write

Address XXXX 0B40

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-5	Passed to the PNR FYTDAT(15-13)	Passed to PNR FYTDAT(15-13), except in the case of the internal SONET/SDH framer. When the internal SONET/SDH framer is selected as the Rx PHY device, signals FYTDAT(15-13) are used as the Rx HDLC interface, unless a 16-bit wide external Tx PHY is also selected. Then they are used as data lines.
4-0	Passed to the PNR FYTDAT(12-8)	Passed to PNR FYTDAT(12-8).

3.9 Virtual Memory Logic (VIMEM)

All addresses can be categorized into three distinct types, based entirely upon the location of the requested address with respect to the three base registers defined in this entity. The three types of addresses are referred to as control, real packet, and virtual packet addresses.

All memory requests arriving on the Control Memory bus are handled as Control Memory accesses, and have the contents of the Control Memory Base Register subtracted from them before being passed on to the Control Memory Entity. When the processor accesses memory, the cache controller compares the requested address to the Real Packet Memory Base Register and if the address is less than the base register, the request is routed to the Control Memory bus; otherwise it is routed to the Packet Memory bus. All requests arriving on the Packet Memory bus are compared to the Virtual Memory Base Address Register. If the address of the request is less than the base register, the contents of the Real Packet Memory Base Register are subtracted from the address and this address is passed on to the Packet Memory Control Entity. If the requested address is greater than or equal to the base register, a more complex, but flexible scheme is used to determine the real address to provide to the Packet Memory Control Entity. For a detailed explanation of the virtual address generation scheme refer to *3.17.4 Virtual Memory Overview* on page 396 and the accompanying figures.

3.9.1 VIMEM Virtual Memory Base Address

This register defines the starting address of the virtual address space used to manage incoming and outgoing frames. Any time an access is made to Virtual Memory that falls within the defined bounds of Virtual Memory, the contents of this register are subtracted from the virtual address to derive the true offset into Virtual Memory. This true offset, along with the known length of all virtual buffers, allows the index of the specific virtual buffer to be derived by the Virtual Memory access hardware. This index can then be used to access the real buffer map associated with this virtual buffer.

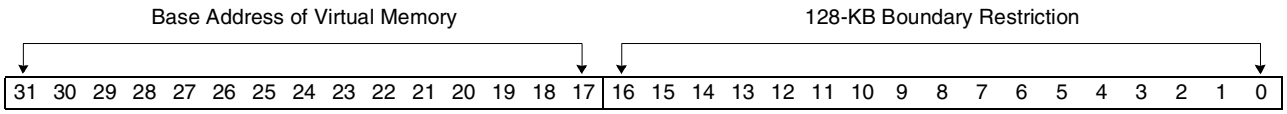
Length 32 bits

Type Read/Write

Address XXXX 0D10

Power On Reset Value x‘0040 0000’

Restrictions The start of virtual address space must begin on a 128-KB boundary. For this reason, the lowest 17 bits of this register are forced to ‘0’ and are not implemented. Writes of any value to the low 17 bits of this register are ignored, and a read always returns ‘0’ for the low 17 bits.



Bit(s)	Name	Description
31-17	Virtual Memory Base Address	These bits contain the upper 15 bits of the base address of Virtual Memory.
16-0	Reserved	These bits are forced to ‘0’ because the Virtual Memory base address must start on a 128-KB boundary.

3.9.2 VIMEM On-Chip Memory Base Address

This register is used by various entities to generate the base address of the On-Chip Memory (OCM).

Length 32 bits

Type Read/Write

Address XXXX 0D9C

Power On Reset Value x‘0010 0000'

Restrictions The start OCM address space must begin on a 128-KB boundary. For this reason, the lowest 17 bits of this register are forced to ‘0’ and are not implemented. Writes of any value to the low 17 bits of this register are ignored, and a read always returns ‘0’ for the low 17 bits.

Bit(s)	Name	Description
31-17	OCM Base Address	These bits contain the upper 15 bits of the base address of On-Chip Memory.
16-0	Reserved	Reserved.

3.9.3 VIMEM Control Memory Base Address

This register defines the starting address of the Control Memory address space. Any time an access is made to Control Memory, the contents of this register are subtracted from the address before an access to memory occurs.

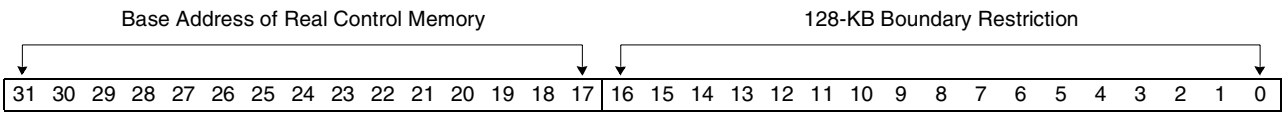
Length 32 bits

Type Read/Write

Address XXXX 0D14

Power On Reset Value x‘0000 0000’

Restrictions The start of real control address space must begin on a 128-KB boundary. For this reason, the lowest 17 bits of this register are forced to ‘0’ and are not implemented. Writes of any value to the low 17 bits of this register are ignored, and a read always returns ‘0’ for the low 17 bits.



Bit(s)	Name	Description
31-17	Control Memory Base Address	These bits contain the upper 15 bits of the base address of real Control Memory.
16-0	Reserved	These bits are forced to ‘0’ because the real Control Memory base address must start on a 128-KB boundary.

3.9.4 VIMEM Packet Memory Base Address

This register defines the starting address of the Packet Memory address space. Any time an access is made to Packet Memory, the contents of this register are subtracted from the address before an access to memory occurs.

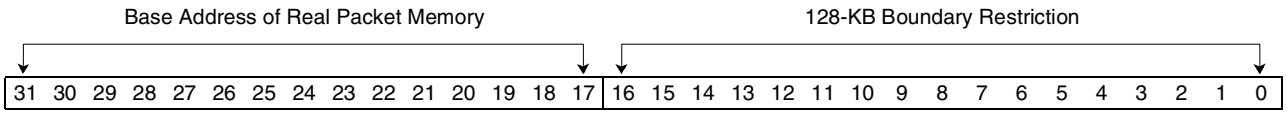
Length 32 bits

Type Read/Write

Address XXXX 0D18

Power On Reset Value x‘0020 0000’

Restrictions The start of real packet address space must begin on a 128-KB boundary. For this reason, the lowest 17 bits of this register are forced to ‘0’ and are not implemented. Writes of any value to the low 17 bits of this register are ignored, and a read always returns ‘0’ for the low 17 bits. This register must also be set up before any of the Real Buffer Base Registers, or the Virtual Buffer Map Registers are written.



Bit(s)	Name	Description
31-17	Packet Memory Base Address	These bits contain the upper 15 bits of the base address of real Packet Memory.
16-0	Reserved	These bits will be forced to ‘0’ because the real Packet Memory base address must start on a 128-KB boundary.

3.9.5 VIMEM Virtual Memory Total Bytes

This register defines the total number of bytes in the address space being allocated for Virtual Memory. The contents of this register, divided by the configured size of virtual buffers, yields the total number of virtual buffer indices that should be used to initialize POOLS. The value of the indices should range from this calculated value minus one, down to zero. If an address is determined to be above or equal to the Virtual Memory Base Register, it is assumed to be a virtual access. If the virtual buffer index derived from the requested address indicates that the virtual buffer space being accessed is above the limit defined by this register, an error is generated.

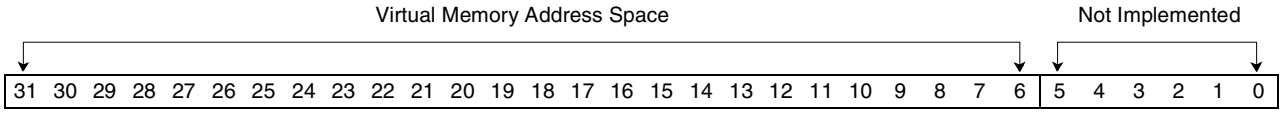
Length 32 bits

Type Read/Write

Address XXXX 0D0C

Power On Reset Value x‘0001 0000’

Restrictions The maximum value that should be set in this register is (65535 * virtual buffer size). For example, if 64-byte virtual buffers are configured, the maximum value that should be loaded into this register is x‘3F FFC0’.



Bit(s)	Name	Description
31-6	Amount of Virtual Memory	These bits contain the upper 26 bits of the total number of bytes of address space being reserved for Virtual Memory.
5-0	Reserved	These bits are not implemented and are forced to ‘0’ because the Virtual Memory block can only be allocated in increments of the current virtual buffer size (minimum size is 64 bytes).

3.9.6 VIMEM Virtual/Real Memory Buffer Size

This register defines the total number of bytes to be occupied by each of the virtual or real buffers as well as the spacing from one buffer to the next.

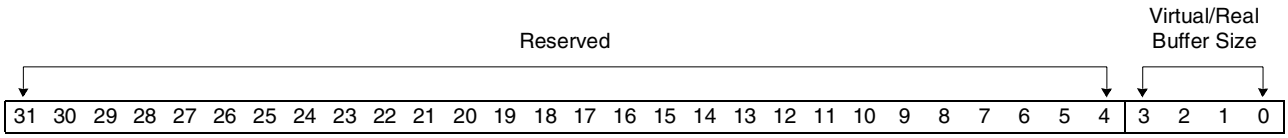
Length 32 bits

Type Read/Write

Address XXXX 0D04

Power On Reset Value x‘0000 0002’

Restrictions Care must be taken to set this register to a large enough value to contain the entire frame being sent as well as certain control information that the hardware stores in the buffer header. For example, if the maximum frame being sent or received is 1024 bytes long, then this register should be set to indicate 2048-byte frames to allow sufficient room for the buffer header information added by the hardware.



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Buffer Size	These bits contain the encoded four-bit value that defines the virtual/real buffer size. The encoding is as follows: 0000 64 bytes 0001 128 bytes 0010 256 bytes 0011 512 bytes 0100 1024 bytes 0101 2048 bytes 0110 4096 bytes 0111 8192 bytes 1000 16384 bytes 1001 32768 bytes 1010 65536 bytes 1011 131072 bytes 1100 -1111 Reserved

3.9.7 VIMEM Packet Memory Offset

This register contains the number that will be added by the VIMEM access logic to all accesses of real Packet Memory that occur. In a high performance configuration (separate control and packet store), this register should be written to all zeros to indicate that all accesses of real Packet Memory do not require any additional offset to be added. In a medium performance configuration (combined control and packet store), this register should be loaded with a value that indicates the logical partitioning between control and packet storage. If for instance, a single bank of 2 M was configured and this register was loaded with x‘0010 0000’ (1 M), then all accesses to real Packet Memory would be forced into the 1-meg to 2-meg range.

Length	32 bits
Type	Read/Write
Address	XXXX 0D3C
Power On Reset Value	x‘0000 0000’
Restrictions	This register should only be loaded with a non-zero value if a medium performance configuration (combined control and packet store) exists. The value loaded must be between zero and the maximum of the total amount of memory in the single bank, and it must be on a 128-KB boundary. Any time the value in this register is changed, the related base registers must be reloaded because the value loaded into them is affected by the contents of this register during the load operation. The related registers are the Virtual Buffer Map Base Address Register and all five real buffer base registers.

3.9.8 VIMEM Maximum Buffer Size

This register is used by the Virtual Memory logic to determine if an access to a virtual buffer falls into the region of the buffer that can be accessed. If a virtual buffer read or write accesses an offset in a virtual buffer that is greater than the contents of this register, the Virtual Memory logic can be configured to halt and generate an interrupt. The power up value of all '1's causes this check to be disabled. This register is intended to provide the user with a means of providing additional protection to accesses of the virtual buffers. For example, if this register is loaded with x'FF8', all memory access up to and including the byte at address x'FFF' are allowed. Any access of offset x'1000' or above will cause an exception.

Length 32 bits

Type Read/Write

Address XXXX 0D34

Power On Reset Value x'0001 FFF8'

Restrictions All address logic based on this register only recognizes 8-byte words in memory. For this reason, the low 3 bits of this register are not implemented and are always forced to '0'.

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Maximum Buffer Size	Maximum virtual buffer size. The maximum value written into these bits would yield a buffer size of 128KB - 8 bytes.

3.9.9 VIMEM Control Register

The bits in this register control the configurable features of the Virtual Memory logic.

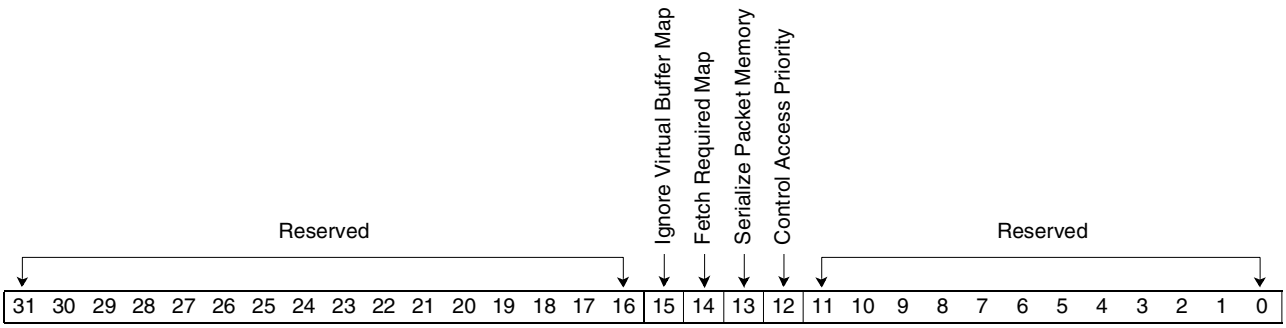
Length 32 bits

Type Clear/Set

Address XXXX 0D80 and 0D84

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15	Ignore Virtual Buffer Map Validity	When set, this bit forces the Virtual Memory logic to ignore the virtual buffer map validity indication, and force all maps to appear valid.
14	Always Fetch Map Information	When set, this bit forces the Virtual Memory logic to fetch the required map entry from storage on every new virtual access. If a Virtual Memory map is updated by the software for any reason, this bit should be toggled on and off after the map is updated and before any virtual access happens to ensure that the Virtual Memory logic is not using stale cached map segments. There is no hardware provided to make sure that the map entry required by the Virtual Memory logic is not contained in one of the BCACH lines. It is the responsibility of the software to ensure that all modified lines are flushed from the cache before the Virtual Memory logic needs them.
13	Serialize Packet Memory Accesses	When set, this bit forces all accesses to Packet Memory to be serialized.
12	Force Control Access Priority in Single Bank Mode	When set, this bit causes control accesses to always have priority over packet accesses in a single memory bank configuration. When reset, priority will toggle every time an access is initiated.
11-0	Reserved	Reserved.

3.9.10 VIMEM Status Register

This register contains information regarding the current status of the Virtual Memory logic mainly with respect to detected error access conditions.

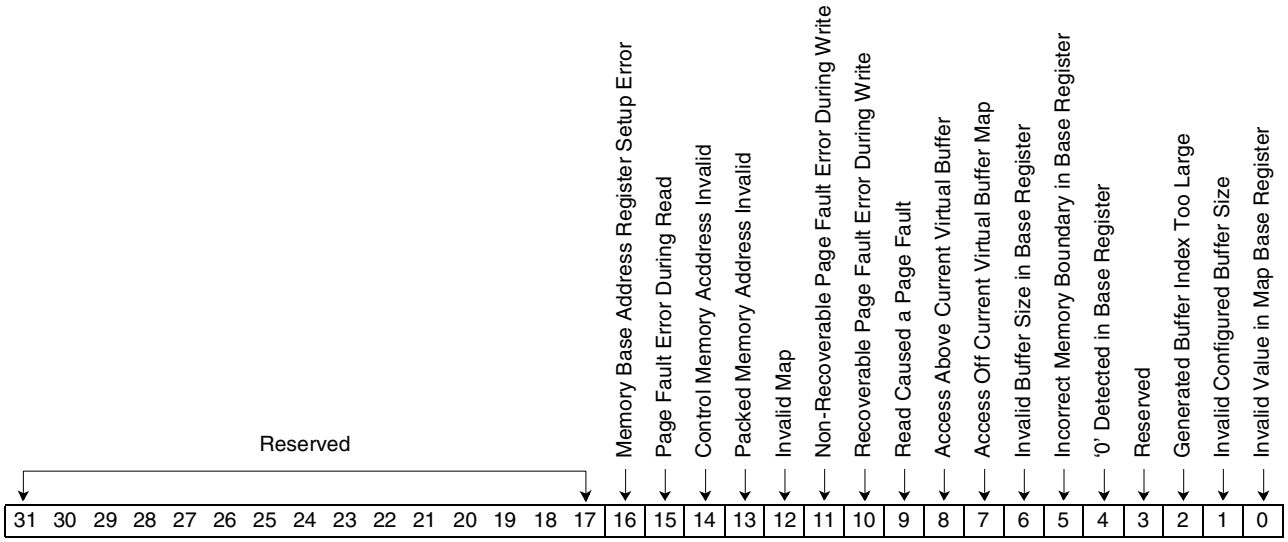
Length 32 bits

Type Clear/Set

Address XXXX 0D60 and 0D64

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-17	Reserved	Reserved.
16	Memory Base Address Register Setup Error	When set, this bit indicates that the required conditions for the control, packet, and virtual base address registers has not been satisfied. The required conditions are: control base address < packet base address < virtual base address.
15	Page Fault During Read	When set, this bit indicates that the Virtual Memory logic has detected a page fault error when attempting to read memory. This indicates that no real buffer was available to map into the virtual address space when required. All virtual reads that fail during a page fault regardless of the requesting entity will cause this bit to be set. If the corresponding bit is reset in the lock register, the read operation will complete, but with invalid data.
14	Control Memory Address Invalid	When set, this bit indicates that a Control Memory access was detected that was above the value contained in the Packet Memory Offset Register for single bank configurations, or in a multiple bank configuration in which the high address bits 31-27 were not ‘0’.
13	Packet Memory Address Invalid	When set, this bit indicates that a Packet Memory access of address zero was detected in single bank mode, or that a packet address was detected that contained an address out of range (high five bits non-zero).

Bit(s)	Name	Description
12	Invalid Map	When set, this bit indicates that the Virtual Memory logic has detected a Virtual Memory operation that attempted to access a map that was not marked as valid. A virtual buffer map is marked valid by the POOLS entity when the buffer is originally acquired, and is marked as invalid when the buffer is freed back to POOLS. Receiving this error indication typically means that the software is trying to use a buffer that has not been acquired through the normal means, or is trying to use a buffer that has already been freed, or that memory has been corrupted. The valid indication that is checked by the hardware is the value x‘?656’ in the first 16 bits of the eight-byte map entry being accessed. To determine the failing address, the memory control entity can be locked on this type of failure, and the information saved by the memory controller, along with the base registers in this entity can be used to determine which map was being accessed at the time of failure.
11	Non-Recoverable Page Fault Error During Write	When set, this bit indicates that the Virtual Memory logic has detected a non-recoverable page fault error when attempting to write memory. This indicates that no real buffer was available to map into the virtual address space when required. All virtual writes that fail during a page fault, with the exception of BCACH and REASM operations, cause this bit to be set.
10	Recoverable Page Fault Error During Write	When set, this bit indicates that the Virtual Memory logic has detected a recoverable page fault error when attempting to write memory. This indicates that no real buffer was available to map into the virtual address space when required. Operations from BCACH and REASM cause this bit to be set instead of the non-recoverable bit because the software can recover from these failures. If a BCACH write to Virtual Memory fails in this manner, the packet header of the frame being updated is updated to indicate the failure. Software can check the field in the packet header to ensure that the DMA operation completed successfully. If such a packet is enqueued to CSKED, the packet header is checked and will prevent the frame from being passed on to the segmentation logic. When CSKED encounters a frame that has had this type of failure, there are several possible ways in which it can be configured (via the CSKED control register) to handle the situation. It can be configured to ignore the error and attempt to transmit the frame anyway (probably not a good way), or the buffer can be freed back to POOLS, or an event can be generated to allow the software to deal with the situation. If a REASM write to Virtual Memory fails in this manner, the packet currently being received is dropped; it is up to the software to perform any recovery operations that are required.
9	Read Caused a Page Fault	When set, this bit indicates that the Virtual Memory logic has detected a read operation that caused a page fault. This is an invalid condition because the data required for a read operation should have been previously initialized by a write operation, so no page fault should ever occur on a read operation. If the corresponding bit in the lock register is reset, a page is mapped into the current virtual buffer segment and the data that previously was written in that page is returned. This bit can come on in several situations that are not really errors. In these cases, the associated interrupt and lock bits can be reset so that this error does not cause the adapter to halt normal operation. Several of these conditions are: When predictive fill is enabled, a read from the end of a buffer may cause a predictive read that crosses a virtual segment boundary and causes this bit to be set. If a small buffer (fits entirely in the cache) is copied from one PNR buffer to another PNR buffer, a subsequent read of the last bytes written causes this bit to be set if the cache hasn’t been flushed between the write and the read, and the last write cycle did not write all four bytes, and the address that is being written/read is within the first x‘20’ bytes of a virtual segment.
8	Access Above Current Virtual Buffer	When set, this bit indicates that the Virtual Memory logic has detected an access of a virtual buffer that falls above the limit set by the buffer maximum size register.
7	Access Off Current Virtual Buffer Map	When set, this bit indicates that the Virtual Memory logic has detected an access that does not fall in one of the currently mapped buffer segments based upon the currently-configured virtual buffer map size.
6	Invalid Buffer Size in Base Register	When set, this bit indicates that a virtual access has been detected that used a base register that had an invalid associated buffer size configured in the low order bits.
5	Incorrect Memory Boundary in Base Register	When set, this bit indicates that a virtual access has been detected that used a base register that was not on the correct memory boundary. For example, if a base register is set up to use 2 KB buffers, the base register must be set up on a 2 KB boundary.
4	‘0’ Detected in Base Register	When set, this bit indicates that a virtual access has been detected that used a base register that contained a value of ‘0’.

Bit(s)	Name	Description
3	Reserved	Reserved.
2	Generated Buffer Index Too Large	When set, this bit indicates that the Virtual Memory logic has detected a memory access that resulted in the generation of a buffer index that was greater than the currently configured maximum derived from the VIMEM Virtual Memory total bytes register.
1	Invalid Configured Buffer Size	When set, this bit indicates that the currently configured size of buffers is invalid.
0	Invalid Value in Map Base Register	When set, this bit indicates that the map base register contains an invalid value. Two possible causes are that bits 5-2 are not '0' or bits 31-6 are '0'.

3.9.11 VIMEM Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *VIMEM Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from VIMEM to INTST if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0D68 and 0D6C

Power On Reset Value x'0001 FFFF'

Restrictions None

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Interrupt Enables	When one of these bits is on and the corresponding bit in the *VIMEM Status Register* is on, an interrupt is generated.

3.9.12 VIMEM Memory Lock Enable Register

This register allows the user to selectively allow each of the conditions reported in the *VIMEM Status Register* to force a memory lock condition in the memory controller. Each bit corresponds to the same bit in the status register and when set to ‘1’ causes a memory lock if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 0D70 and 0D74

Power On Reset Value x‘0001 FFFF’

Restrictions None

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Lock Enables	When one of these bits is on and the corresponding bit in the ’VIMEM Status Register” on page 199 is on, the memory subsystem will lock.

3.9.13 VIMEM State Machine Current State

This register provides feedback to the user regarding the current status of the state machines in VIMEM. One use of this register is to make sure that the required initialization time has expired after loading the segment size register. This is accomplished by reading this register repeatedly until the initialization state machine is in the idle state.

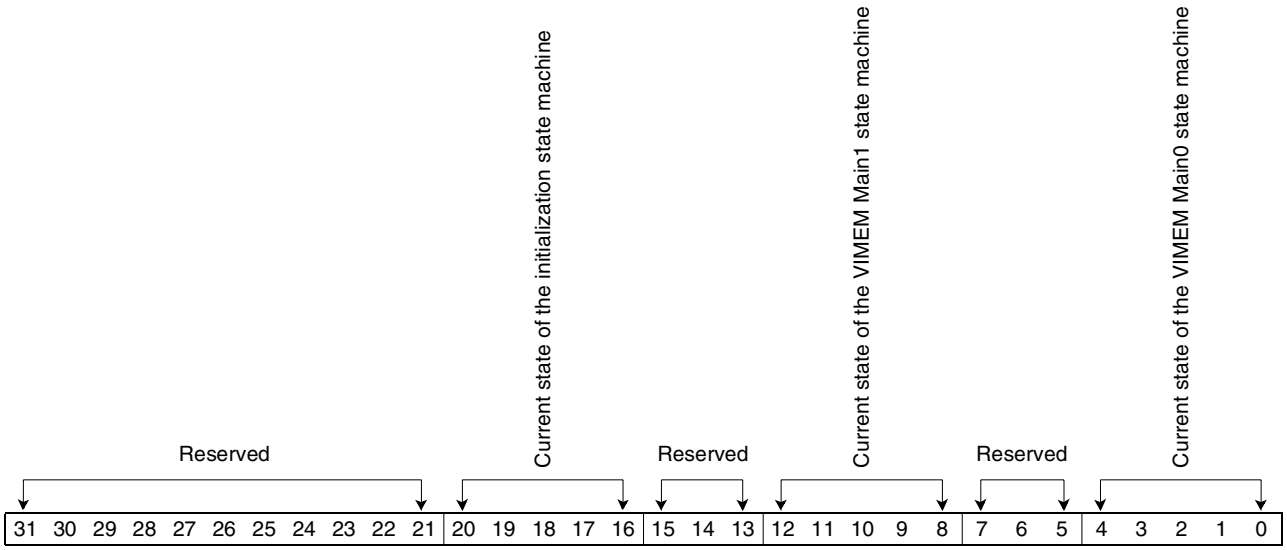
Length 32 bits

Type Read Only

Address XXXX 0D78

Power On Reset Value x‘001D 0000’

Restrictions None



Bit(s)	Name	Description
31-21	Reserved	Reserved.
20-16	Current state of the initialization state machine	These bits contain the current state of the initialization state machine. A value of “1----” indicates that the state machine is in the idle state.
15-13	Reserved	Reserved.
12-8	Current state of the VIMEM Main 1 state machine	These bits contain the current state of the VIMEM Main1 state machine. A value of “00000” indicates that the state machine is in the idle state.
7-5	Reserved	Reserved.
4-0	Current state of the VIMEM Main 0 state machine	These bits contain the current state of the VIMEM Main0 state machine. A value of “00000” indicates that the state machine is in the idle state.

3.9.14 VIMEM Last Processor Read Real Address Address

This register provides information to the user about the last read access of virtual Packet Memory by the processor. If a virtual address was accessed, this register contains the real address generated by the Virtual Memory logic that can be used to access the same location. This register is intended mainly as an aid in debugging to make virtual address translation easier. To perform the translation, the processor must read from the desired virtual address: after the read is complete, this register contains the real address that was accessed. The address contained in this register is an offset from the beginning of physical Packet Memory.

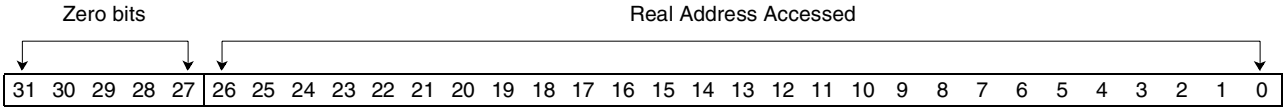
Length 32 bits

Type Read Only

Address XXXX 0D7C

Power On Reset Value x‘0000 0000’

Restrictions None

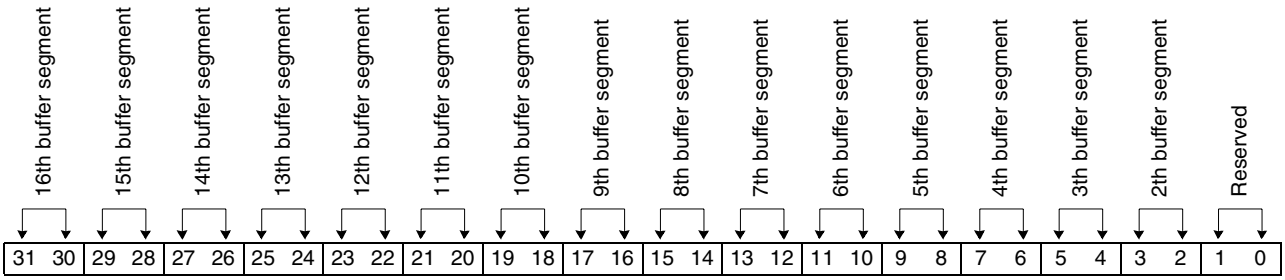


Bit(s)	Name	Description
31-27	Reserved	Reserved. These bits will always read as ‘0’.
26-0	Read Address Accessed	After any read operation from the processor to Packet Memory, these bits will contain the real address that was accessed.

3.9.15 VIMEM Virtual Buffer Segment Size Register

This register, along with the lower four bits of the real buffer base registers, defines the size of the second through 16th real buffers that are concatenated to make up a virtual buffer. Two bits of this register are associated with each real buffer segment and indicate one out of four possible associations. The associative possibilities are shown in the bit table below. Every two bits defines the connection between a particular buffer segment and the real buffer base registers.

Length	32 bits
Type	Read/Write
Address	XXXX 0D00
Power On Reset Value	x‘0000 0000’
Restrictions	Care must be used when setting up this register to ensure that only values that correspond to real buffer sizes that POOLS has also been set up to provide are loaded. A write to this register causes the Virtual Memory logic to calculate the different real buffer boundaries within a virtual buffer. This calculation requires information from the real buffer base registers to determine the size of the different segments making up the virtual buffer. For this reason, it is required that this register be written after the real buffer base registers have been initialized. After writing this register, the software must wait at least 2 ms before accessing Virtual Memory.



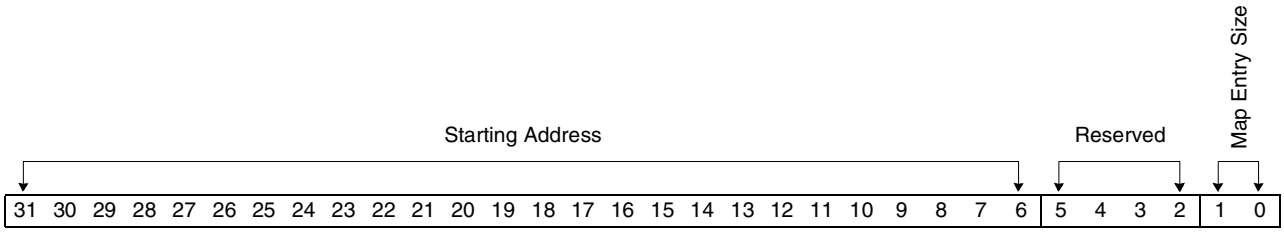
Bit(s)	Description	Bit Association
31-30	Defines the 16th buffer segment's connection.	
29-28	Defines the 15th buffer segment's connection.	
27-26	Defines the 14th buffer segment's connection.	
25-24	Defines the 13th buffer segment's connection.	
23-22	Defines the 12th buffer segment's connection.	
21-20	Defines the 11th buffer segment's connection.	
19-18	Defines the 10th buffer segment's connection.	00 Associates this real buffer segment with Real Buffer Base Register 0
17-16	Defines the 9th buffer segment's connection.	01 Associates this real buffer segment with Real Buffer Base Register 1
15-14	Defines the 8th buffer segment's connection.	10 Associates this real buffer segment with Real Buffer Base Register 2
13-12	Defines the 7th buffer segment's connection.	11 Associates this real buffer segment with Real Buffer Base Register 3
11-10	Defines the 6th buffer segment's connection.	
9-8	Defines the 5th buffer segment's connection.	
7-6	Defines the 4th buffer segment's connection.	
5-4	Defines the 3rd buffer segment's connection.	
3-2	Defines the 2nd buffer segment's connection.	
1-0	Reserved. The first real buffer is implicitly associated with the virtual buffer, these bits will always be read as '0'.	

3.9.16 VIMEM Buffer Map Base Address Register

This register contains the address in Packet Memory at which the buffer map table starts. The buffer map table consists of a variable number of eight-byte entries for each buffer that is allocated in the system. The first 16 bits of each eight-byte entry contains the POOL ID and various status flags associated with this buffer, thus this base register is used in both real and Virtual Memory modes.

In Virtual Memory mode, each of the three subsequent 16 bits contains an index which is associated with a buffer size base register using the Buffer Segment Limit Register. The index and buffer size base register are used to determine a real buffer address. If the map size is set to eight bytes, only one eight-byte entry is used for each buffer. If the map size is set to 16 bytes, two eight-byte entries are used for each buffer. If the map size is set to 32 bytes, four eight-byte entries are used for each buffer. If the map size is set to 64 bytes, five eight-byte entries are used for each buffer, and the remaining 24 bytes of the map are unused by the hardware.

Length	32 bits
Type	Read/Write
Address	XXXX 0D08
Power On Reset Value	x‘0020 0000’ (This value is actually the power up contents of the Packet Memory Real Base Register added to the power up contents of this register x‘0000 0000’) due to the automatic address adjustment explained below.)
Restrictions	The base address for the buffer map must begin on a 64-byte boundary. When a base register is written, the hardware performs an automatic adjustment to the address using the contents of the Packet Memory Real Base Register, and the Packet Memory Offset Register. This results in the actual value being stored, not being the value that is written by the program. This is done to make the virtual accesses that use the base register execute more quickly. The reverse adjustment is made when the read operation is performed, so that it appears to the program no different than a normal operation. Care must be taken, however, to ensure that both the Packet Memory Real Base Register and the Packet Memory Offset Register are set-up before any of the base registers are written. If the Packet Memory Base Register or the Packet Memory Offset Register are changed, Packet Memory should not be accessed until all the base registers have been written again.



Bit(s)	Name	Description
31-6	Starting Address	Defines the starting address of the buffer map.
5-2	Reserved	Reserved, should be written with '0'.
1-0	Map Entry Size	Defines the size of each map entry: 00 8 bytes 01 16 bytes 10 32 bytes 11 64 bytes

3.9.17 VIMEM Real Buffer Base Address Registers

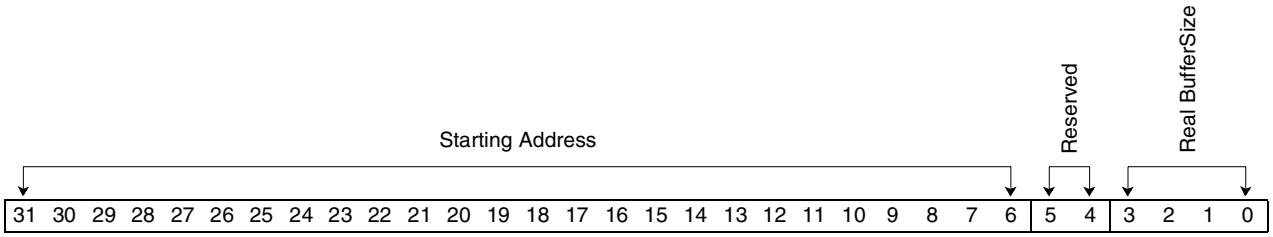
These registers contain the address in Packet Memory at which a block of memory begins that is used to provide a given size buffer. In general, the block allocated must be large enough to contain as many buffers as will be freed to POOLS on initialization. However, for Real Buffer Base 4, the size of the block reserved must be large enough so that one buffer is available for each of the virtual buffers freed to POOLS. These buffers must not be freed to POOLS because they are implicitly used as the first real buffer segment for each of the virtual buffers. If a given base register (and associated buffer size) is not used, the low four bits of the register should be set to x'F' to ensure that accesses of this buffer size are detected and flagged as an error. When using real memory mode (controlled in POOLS), all of these base registers are unused with the exception of base register zero, which contains the base address for all real memory buffers. In real mode, the low four bits of base register zero are of no significance. The size of the real buffers is controlled through the Buffer Size Register.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 0D20
	Buffer Size 1	XXXX 0D24
	Buffer Size 2	XXXX 0D28
	Buffer Size 3	XXXX 0D2C
	Buffer Size 4 (implicit)	XXXX 0D30
Power On Reset Value		x'0020 000F'

Restrictions

The base address for any given buffer size must begin on a boundary that is equal to the buffer size. For example, the base address for 128-byte buffers must be on a 128-byte boundary, and the base address for 4096-byte buffers must be on a 4096-byte boundary.

When a base register is written, the hardware performs an automatic adjustment to the address using the contents of the Packet Memory real base register and the Packet Memory offset register. This results in the actual value being stored, not being the value that is written by the program. This is done to make the memory accesses that use the base register execute quicker. The reverse adjustment is made when the read operation is performed, so that it appears to the program no different than a normal operation. Care must be taken, however, to ensure that the Packet Memory Real Base Register and the Packet Memory Offset Register are set-up before any of the base registers are written. If the Packet Memory Base Register or the Packet Memory Offset Register is changed, Packet Memory should not be accessed until all the base registers have been written again. The power on reset value of these registers is actually the power on reset value of the Packet Memory Real Base Register added to the contents of the Packet Memory Offset Register added to the original contents of these registers (x'0000 000F').



Bit(s)	Name	Description
31-6	Starting Address	Defines the starting address in Packet Memory of the memory block used to provide real buffers of defined size.
5-4	Reserved	Reserved (User should write zeros and ignore read value).
3-0	Real Buffer Size	Defines the size of the real buffers in this block of memory with the following encoding: 0000 64 bytes 0001 128 bytes 0010 256 bytes 0011 512 bytes 0100 1024 bytes 0101 2048 bytes 0110 4096 bytes 0111 8192 bytes 1000 16384 bytes 1001 32768 bytes 1010 65536 bytes 1011 131072 bytes 1100 -1111Reserved

3.10 Memory Arbitration Logic (ARBIT)

This section contains descriptions of the registers used by the arbiter logic.

3.10.1 ARBIT Control Priority Resolution Register High

The bits in this register define the priority of requesting entities to Control Memory.

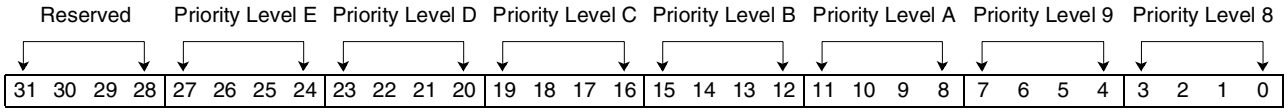
Length 32 bits

Type Read/Write

Address XXXX 0E00

Power On Reset Value x‘0EDC BA98’

Restrictions None



Bit(s)	Name	Description
31-28	Reserved	Reserved.
27-24	Priority Level E	The value loaded into these bits defines which entity will be requesting at priority level E (lowest priority). Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: TXLCD D: PCORE LO 5: RXLCD C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: RXXLT 1: BCACH HI 8: RXQUE 0: POOLS HI
23-20	Priority Level D	The value loaded into these bits defines which entity will request at priority level D. Value encoding is as listed in the description of bits 27-24.
19-16	Priority Level C	The value loaded into these bits defines which entity will request at priority level C. Value encoding is as listed in the description of bits 27-24.
15-12	Priority Level B	The value loaded into these bits defines which entity will request at priority level B. Value encoding is as listed in the description of bits 27-24.
11-8	Priority Level A	The value loaded into these bits defines which entity will request at priority level A. Value encoding is as listed in the description of bits 27-24.
7-4	Priority Level 9	The value loaded into these bits defines which entity will request at priority level 9. Value encoding is as listed in the description of bits 27-24.
3-0	Priority Level 8	The value loaded into these bits defines which entity will request at priority level 8. Value encoding is as listed in the description of bits 27-24.

3.10.2 ARBIT Control Priority Resolution Register Low

The bits in this register define the priority of requesting entities to Control Memory.

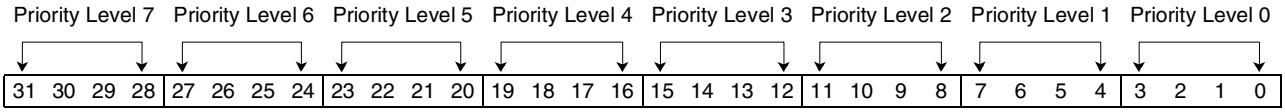
Length 32 bits

Type Read/Write

Address XXXX 0E04

Power On Reset Value x‘7654 3210’

Restrictions None



Bit(s)	Name	Description
31-28	Priority Level 7	The value loaded into these bits defines which entity will request at priority level 7. Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: TXLCD D: PCORE LO 5: RXLCD C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: RXXLT 1: BCACH HI 8: RXQUE 0: POOLS HI
27-24	Priority Level 6	The value loaded into these bits defines which entity will request at priority level 6. For value encoding, see the description of bits 31-28.
23-20	Priority Level 5	The value loaded into these bits defines which entity will request at priority level 5. For value encoding, see the description of bits 31-28.
19-16	Priority Level 4	The value loaded into these bits defines which entity will request at priority level 4. For value encoding, see the description of bits 31-28.
15-12	Priority Level 3	The value loaded into these bits defines which entity will request at priority level 3. For value encoding, see the description of bits 31-28.
11-8	Priority Level 2	The value loaded into these bits defines which entity will request at priority level 2. For value encoding, see the description of bits 31-28.
7-4	Priority Level 1	The value loaded into these bits defines which entity will request at priority level 1. For value encoding, see the description of bits 31-28.
3-0	Priority Level 0	The value loaded into these bits defines which entity will request at priority level 0 (highest priority). For value encoding, see the description of bits 31-28.

3.10.3 ARBIT Control Error Mask Register

The bits in this register control whether ARBIT-detected error conditions on an entity's interface will lock the Control Memory subsystem. Bits in this register also control the locking of the Control Memory subsystem based on Control Memory, Packet Memory, Virtual Memory, and BCACH-detected error conditions. Resetting the appropriate bit will force errors from that source to be ignored.

Length 32 bits

Type Clear/Set

Address XXXX 0E08 and 0E0C

Power On Reset Value x'000F FFFF'

Restrictions None

Bit(s)	Name	Description
31-19	Reserved	Reserved.
18	ARBIT Packet Memory Error	When this bit is set, ARBIT detected Packet Memory errors will lock Control Memory.
17	PCORE Error	When this bit is set, an error from PCORE will lock Control Memory.
16	POOLS Error	When this bit is set, an error from POOLS will lock Control Memory.
15	BCACH Error	When this bit is set, an error from BCACH will lock Control Memory.
14	VIMEM Error	When this bit is set, an error from VIMEM will lock Control Memory.
13	PAKIT Error	When this bit is set, an error from PAKIT will lock Control Memory.
12	COMET Error	When this bit is set, an error from COMET will lock Control Memory.
11	CHKSM	When set, an error on the Control Memory interface between CHKSM and ARBIT will lock Control Memory.
10	PCORE	When set, an error on the Control Memory interface between PCORE and ARBIT will lock Control Memory.
9	BCACH	When set, an error on the Control Memory interface between BCACH and ARBIT will lock Control Memory.
8	POOLS	When set, an error on the Control Memory interface between POOLS and ARBIT will lock Control Memory.
7	CSKED	CWhen set, an error on the Control Memory interface between CSKED and ARBIT will lock Control Memory.
6	RXXLT	When set, an error on the Control Memory interface between RXXLT and ARBIT will lock Control Memory.
5	RXQUE	When set, an error on the Control Memory interface between RXQUE and ARBIT will lock Control Memory. RXQUE
4	SEGBF	When set, an error on the Control Memory interface between SEGBF and ARBIT will lock Control Memory.
3	TXLCD	When set, an error on the Control Memory interface between TXLCD and ARBIT will lock Control Memory.
2	RXLCD	When set, an error on the Control Memory interface between RXLCD and ARBIT will lock Control Memory.

Bit(s)	Name	Description
1	GPDMA	When set, an error on the Control Memory interface between GPDMA and ARBIT will lock Control Memory.
0	DMAQS	When set, an error on the Control Memory interface between DMAQS and ARBIT will lock Control Memory.

3.10.4 ARBIT Control Error Source Register

The bits in this register provide feedback to indicate the source of errors that have been detected by the memory subsystem.

Length 32 bits

Type Clear/Set

Address XXXX 0E18 and 0E1C

Power On Reset Value x‘0000 0000’

Restrictions Bits 17 through 12 are driven from external entities and cannot be set or reset in this register. They must be set or reset in the entity of origin.

Bit(s)	Name	Description
31-19	Reserved	Reserved.
18	ARBIT Packet Memory Error	ARBIT detected a Packet Memory error.
17	PCORE Error	PCORE indicated an error condition.
16	POOLS Error	POOLS indicated an error condition.
15	BCACH Error	BCACH indicated an error condition.
14	VIMEM Error	VIMEMindicated an error condition.
13	PAKIT Error	PAKIT indicated an error condition.
12	COMET Error	COMET indicated an error condition.
11	CHKSM	An error was detected on the Control Memory interface from CHKSM.
10	PCORE	An error was detected on the Control Memory interface from PCORE.
9	BCACH	An error was detected on the Control Memory interface from BCACH.
8	POOLS	An error was detected on the Control Memory interface from POOLS.
7	CSKED	An error was detected on the Control Memory interface from CSKED.
6	RXXLT	An error was detected on the Control Memory interface from RXXLT.
5	RXQUE	An error was detected on the Control Memory interface from RXQUE.
4	SEGBF	An error was detected on the Control Memory interface from SEGBF.
3	TXLCD	An error was detected on the Control Memory interface from TXLCD.
2	RXLCD	An error was detected on the Control Memory interface from RXLCD.
1	GPDMA	An error was detected on the Control Memory interface from GPDMA.
0	DMAQS	An error was detected on the Control Memory interface from DMAQS.

3.10.5 ARBIT Control Winner Register

The bits in this register indicate which entity currently owns Control Memory.

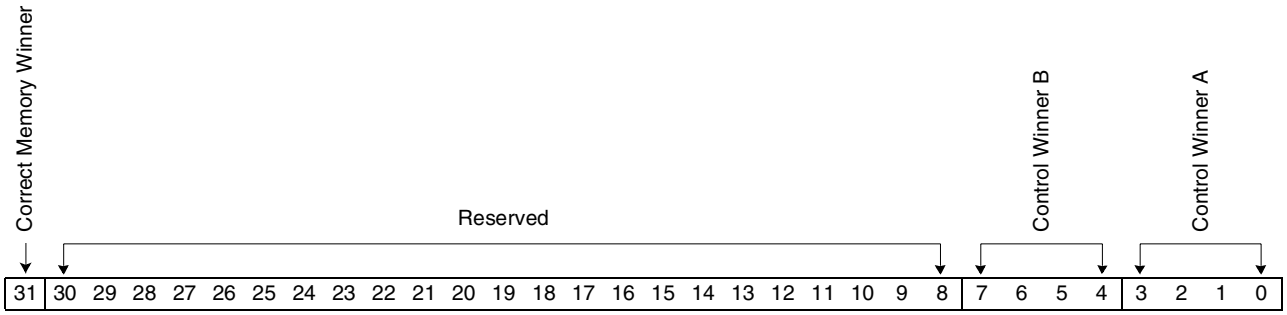
Length 32 bits

Type Read Only

Address XXXX 0E2C

Power On Reset Value x‘0000 000F’

Restrictions None



Bit(s)	Name	Description
31	Correct Memory Winner	For performance reasons, two sets of operational latches (bank A and bank B) exist in the arbiter for Control Memory. When set, this bit indicates that the B latches are active, and when reset indicates that the A latches are active. When this bit is set and memory is locked, bits 7-4 of this register contain a value that indicates the entity that most recently was accessing memory. If this bit is reset and memory is locked, bits 3-0 of this register contain a value that indicates the entity that was accessing memory most recently.
30-8	Reserved	Reserved. Will read ‘0’.
7-4	Control Winner B	Control winner B. F: Reserved 7: SEGBF E: CHKSM 6: TXLCD D: PCORE LO 5: RXLCD C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: RXXLT 1: BCACH HI 8: RXQUE 0: POOLS HI
3-0	Control Winner A	Control winner A. F: Reserved 7: SEGBF E: CHKSM 6: TXLCD D: PCORE LO 5: RXLCD C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: RXXLT 1: BCACH HI 8: RXQUE 0: POOLS HI

3.10.6 ARBIT Control Address Register A

If latch bank A is active, the bits in this register indicate the last address that was used to access Control Memory.

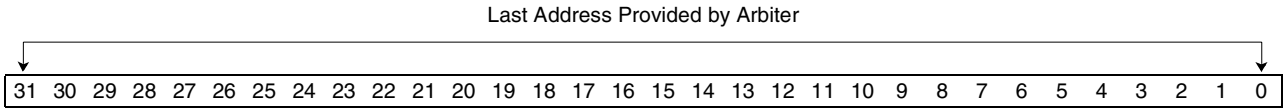
Length 32 bits

Type Read Only

Address XXXX 0E10

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Last Address Bank A	These bits contain the last address provided by the arbiter to the Control Memory controller.

3.10.7 ARBIT Control Address Register B

If latch bank B is active, the bits in this register indicate the last address that was used to access Control Memory.

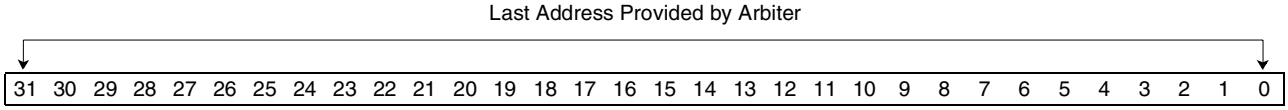
Length 32 bits

Type Read Only

Address XXXX 0E20

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Last Address Bank B	These bits contain the last address provided by the arbiter to the Control Memory controller.

3.10.8 ARBIT Control Length Register

The bits in this register indicate the last length used to access Control Memory.

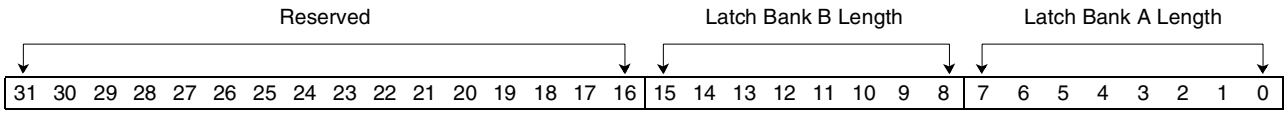
Length 32 bits

Type Read Only

Address XXXX 0E14

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	Length Bank B	These bits contain the length used to access Control Memory through latch bank B.
7-0	Length Bank A	These bits contain the length used to access Control Memory through latch bank A.

3.10.9 ARBIT Control Lock Entity Enable Register

The value programmed in this register controls which entity, if any, has access to Control Memory immediately after memory has locked. This register powers up to a value that will not allow any entity to access memory after a lock condition until the lock condition has been properly cleared.

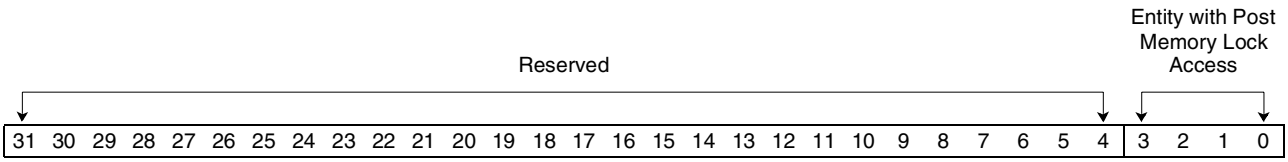
Length 32 bits

Type Read/Write

Address XXXX 0E28

Power On Reset Value x‘0000 000F’

Restrictions None



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Entity with Post Memory Lock Access	The value in these bits map to the following entities: F: Reserved 7: SEGBF E: CHKSM 6: TXLCD D: PCORE LO 5: RXLCD C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: RXXLT 1: BCACH HI 8: RXQUE 0: POOLS HI

3.10.10 ARBIT Control Config Register

The bits in this register control the operation of the Control Memory arbiter.

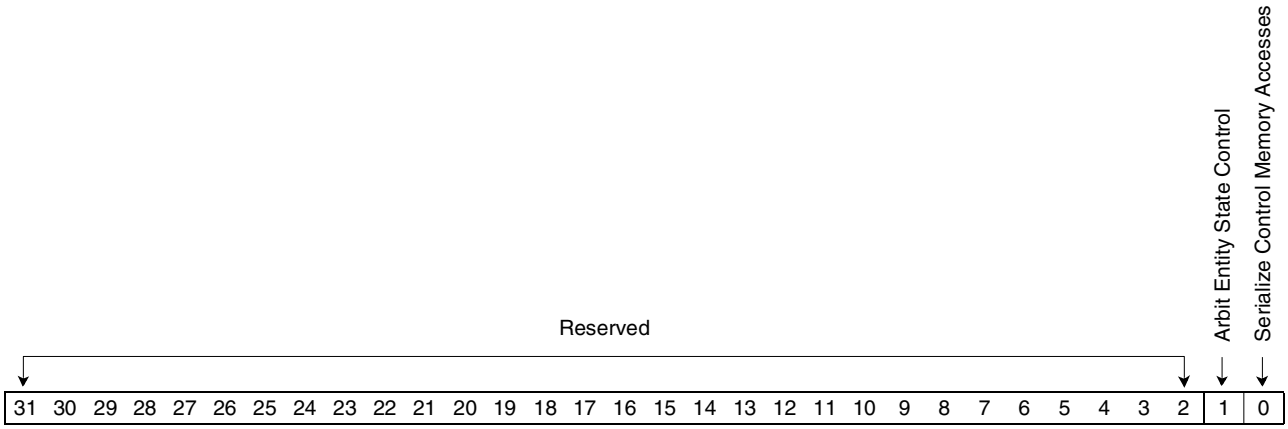
Length 32 bits

Type Clear/Set

Address XXXX 0E38 and 0E3C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-2	Reserved	Reserved.
1	Arbit Entity State Control	This bit controls the ARBIT entity state debug mux. When set, the incoming entity requests and outgoing acknowledges are routed to the entity state pins. When reset, the internal state information is routed to the entity state pins.
0	Serialize Control Memory Accesses	When set, this bit forces all operations to Control Memory to be serialized. An operation from one entity must be entirely complete before an operation from another entity will be started. When reset, if the memory operation in process can be overlapped, a second operation will be started before the first operation is complete.

3.10.11 ARBIT Packet Priority Resolution Register High

The bits in this register define the priority of requesting entities to Packet Memory.

Length 32 bits

Type Read/Write

Address XXXX 0E80

Power On Reset Value x‘0EDC BA98’

Restrictions None

Bit(s)	Name	Description
31-28	Reserved	Reserved.
27-24	Priority Level E	The value loads into these bits defines which entity will request at priority level E (lowest priority). Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: Reserved D: PCORE LO 5: RXAAL C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: Reserved 1: BCACH HI 8: RXQUE 0: POOLS HI
23-20	Priority Level D	The value loaded into these bits defines which entity will request at priority level D. For value encoding, see the description of bits 27-24.
19-16	Priority Level C	The value loaded into these bits defines which entity will request at priority level C. For value encoding, see the description of bits 27-24.
15-12	Priority Level B	The value loaded into these bits defines which entity will request at priority level B. For value encoding, see the description of bits 27-24.
11-8	Priority Level A	The value loaded into these bits defines which entity will request at priority level A. For value encoding, see the description of bits 27-24.
7-4	Priority Level 9	The value loaded into these bits defines which entity will request at priority level 9. For value encoding, see the description of bits 27-24.
3-0	Priority Level 8	The value loaded into these bits defines which entity will request at priority level 8. For value encoding, see the description of bits 27-24.

3.10.12 ARBIT Packet Priority Resolution Register Low

The bits in this register define the priority of requesting entities to Packet Memory.

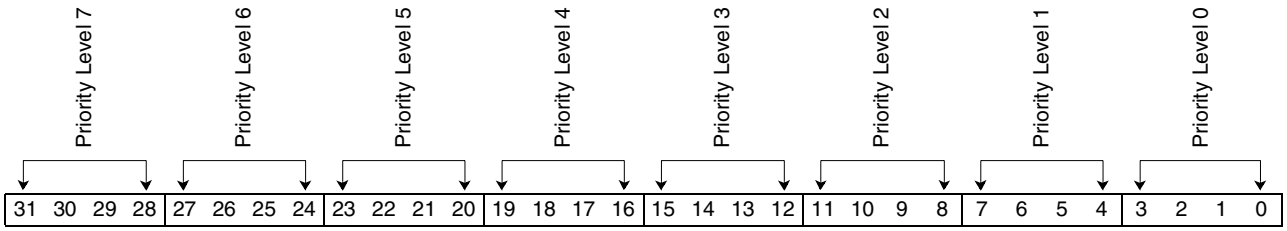
Length 32 bits

Type Read/Write

Address XXXX 0E84

Power On Reset Value x‘7654 3210’

Restrictions None



Bit(s)	Name	Description
31-28	Priority Level 7	The value loaded into these bits define which entity will be requesting at priority level 7. Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: Reserved D: PCORE LO 5: RXAAL C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: Reserved 1: BCACH HI 8: RXQUE 0: POOLS HI
27-24	Priority Level 6	The value loaded into these bits defines which entity will request at priority level 6. For value encoding, see the description of bits 31-28 above.
23-20	Priority Level 5	The value loaded into these bits defines which entity will request at priority level 5. For value encoding, see the description of bits 31-28 above.
19-16	Priority Level 4	The value loaded into these bits defines which entity will request at priority level 4. For value encoding, see the description of bits 31-28 above.
15-12	Priority Level 3	The value loaded into these bits defines which entity will request at priority level 3. For value encoding, see the description of bits 31-28 above.
11-8	Priority Level 2	The value loaded into these bits defines which entity will request at priority level 2. For value encoding, see the description of bits 31-28 above.
7-4	Priority Level 1	The value loaded into these bits defines which entity will request at priority level 1. For value encoding, see the description of bits 31-28 above.
3-0	Priority Level 0	The value loaded into these bits defines which entity will request at priority level 0 (highest priority). For value encoding, see the description of bits 31-28 above.

3.10.13 ARBIT Packet Entity Error Mask Register

The bits in this register control whether ARBIT-detected error conditions on an entity's interface will lock the Packet Memory subsystem. Bits in this register also control the locking of the Packet Memory subsystem based on Control Memory, Packet Memory, Virtual Memory, and BCACH-detected error conditions. Resetting the appropriate bit will force errors from that source to be ignored.

Length 32 bits

Type Clear/Set

Address XXXX 0E88 and 0E8C

Power On Reset Value x'000F FFFF'

Restrictions None

Bit(s)	Name	Description
31-20	Reserved	Reserved.
19	Rearbitration Failure	When this bit is set, a rearbitrationf failure will lock Packet Memory.
18	ARBIT Control Memory Error	When this bit is set, ARBIT detected Control Memory errors will lock Packet Memory.
17	PCORE Error	When this bit is set, an error from PCORE will lock Packet Memory.
16	POOLS Error	When this bit is set, an error from POOLS will lock Packet Memory.
15	BCACH Error	When this bit is set, an error from BCACH will lock Packet Memory.
14	VIMEM Error	When this bit is set, an error from VIMEM will lock Packet Memory.
13	PAKIT Error	When this bit is set, an error from PAKIT will lock Packet Memory.
12	COMET Error	When this bit is set, an error from COMET will lock Packet Memory.
11	CHKSM	When set, an error on the Packet Memory interface between CHKSM and ARBIT will lock Packet Memory.
10	PCORE	When set, an error on Packet Memory interface between PCORE and ARBIT will lock Packet Memory.
9	BCACH	When set, an error on the Packet Memory interface between BCACH and ARBIT will lock Packet Memory.
8	POOLS	When set, an error on the Packet Memory interface between POOLS and ARBIT will lock Packet Memory.
7	CSKED	When set, an error on the Packet Memory interface between CSKED and ARBIT will lock Packet Memory.
6	Reserved	Reserved.
5	RXQUE	When set, an error on the Packet Memory interface between RXQUE and ARBIT will lock Packet Memory.
4	SEGBF	When set, an error on the Packet Memory interface between SEGBF and ARBIT will lock Packet Memory.
3	Reserved	Reserved.
2	RXAAL	When set, an error on the Packet Memory interface between RXAAL and ARBIT will lock Packet Memory.

Bit(s)	Name	Description
1	GPDMA	When set, an error on the Packet Memory interface between GPDMA and ARBIT will lock Packet Memory.
0	DMAQS	When set, an error on the Packet Memory interface between DMAQS and ARBIT will lock Packet Memory.

3.10.14 ARBIT Packet Error Source Register

The bits in this register provide feedback to indicate the source of errors that have been detected by the memory subsystem.

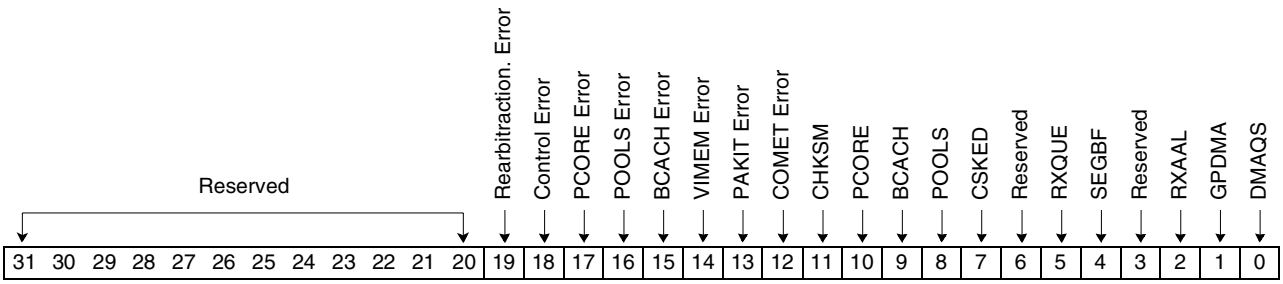
Length 32 bits

Type Clear/Set

Address XXXX 0E98 and 0E9C

Power On Reset Value x‘0000 0000’

Restrictions Bits 17, 16, and 11 through 14 are driven from external entities and can not be set/reset in this register. They must be set/reset in the entity of origin.



Bit(s)	Name	Description
31-20	Reserved	Reserved.
19	Rearbitration Failure.	Rearbitration detected while already handling rearbitration condition. This condition would indicate that the priorities programmed in the priority resolution logic were incorrectly programmed and POOLS HIGH was not given the highest priority.
18	ARBIT Control Memory Error	ARBIT detected control errors.
17	PCORE Error	PCORE indicated an error condition.
16	POOLS Error	POOLS indicated an error condition.
15	BCACH Error	BCACH indicated an error condition.
14	VIMEM Error	VIMEM indicated an error condition.
13	PAKIT Error	PAKIT indicated an error condition.
12	COMET Error	COMET indicated an error condition.
11	CHKSM	An error was detected on the Packet Memory interface from CHKSM.
10	PCORE	An error was detected on the Packet Memory interface from PCORE.
9	BCACH	An error was detected on the Packet Memory interface from BCACH.
8	POOLS	An error was detected on the Packet Memory interface from POOLS.
7	CSKED	An error was detected on the Packet Memory interface from CSKED.
6	Reserved	Reserved.
5	RXQUE	An error was detected on the Packet Memory interface from RXQUE.
4	SEGBF	An error was detected on the Packet Memory interface from SEGBF.
3	Reserved	Reserved.

Bit(s)	Name	Description
2	RXAAL	An error was detected on the Packet Memory interface from RXAAL.
1	GPDMA	An error was detected on the Packet Memory interface from GPDMA.
0	DMAQS	An error was detected on the Packet Memory interface from DMAQS.

3.10.15 ARBIT Packet Winner Register

The bits in this register indicate which entity currently owns Packet Memory.

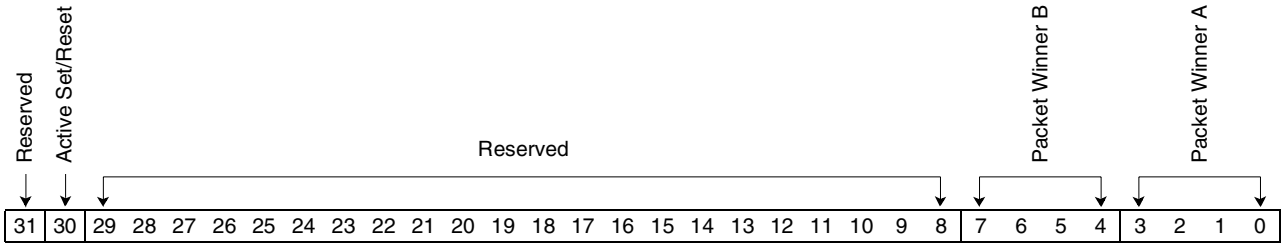
Length 32 bits

Type Read Only

Address XXXX 0EAC

Power On Reset Value x‘0000 000F’

Restrictions None



Bit(s)	Name	Description
31	Reserved	Reserved.
30	Active Set/Reset	For performance reasons, two sets of operational latches (bank A and bank B) exist in the arbiter for Packet Memory. When set, this bit indicates that the B latches are active, and when reset it indicates that the A latches are active. When this bit is set and memory is locked, bits 7-4 of this register contain a value that indicates the entity that most recently was accessing memory. If this bit is reset and memory is locked, bits 3-0 of this register contain a value that indicates the entity that was accessing memory most recently.
29-8	Reserved	Reserved. Will read ‘0’.
7-4	Packet Winner B	Packet winner B.
3-0	Packet Winner A	Packet winner A. Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: Reserved D: PCORE LO 5: RXAAL C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: Reserved 1: BCACH HI 8: RXQUE 0: POOLS HI

3.10.16 ARBIT Packet Address Register A

If latch bank A is active, the bits in this register indicate the last address used to access Packet Memory.

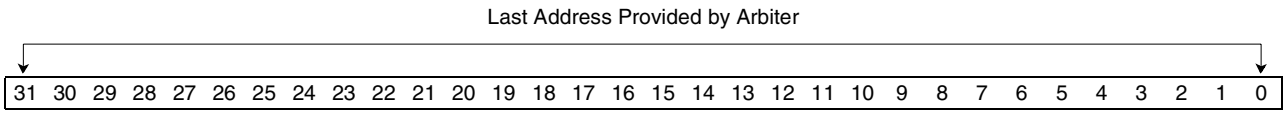
Length 32 bits

Type Read Only

Address XXXX 0E90

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Last Address Bank A	These bits contain the last address provided by the arbiter to the Packet Memory controller.

3.10.17 ARBIT Packet Address Register B

If latch bank B is active, the bits in this register indicate the last address used to access Packet Memory.

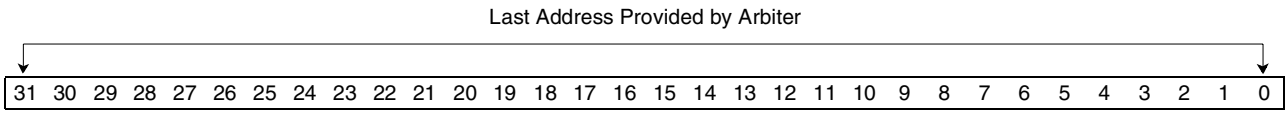
Length 32 bits

Type Read Only

Address XXXX 0EA0

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Last Address Bank B	These bits contain the last address provided by the arbiter to the Packet Memory controller.

3.10.18 ARBIT Packet Length Register

The bits in this register indicate the last length used to access Packet Memory.

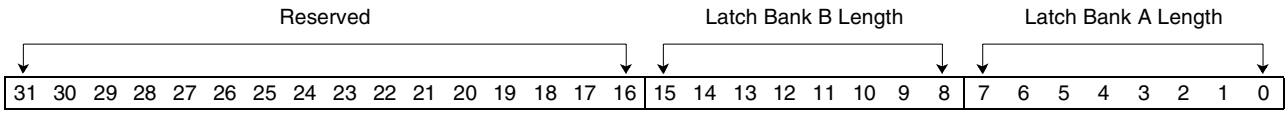
Length 32 bits

Type Read Only

Address XXXX 0E94

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	Bank B Length	These bits contain the length used to access Packet Memory through Latch Bank B.
7-0	Bank A Length	These bits contain the length used to access Packet Memory through Latch Bank A.

3.10.19 ARBIT Packet Lock Entity Enable Register

The value programmed in this register controls which entity, if any, has access to Packet Memory immediately after memory has locked. This register powers up to a value that will not allow any entity to access memory after a lock condition until the lock condition has been properly cleared.

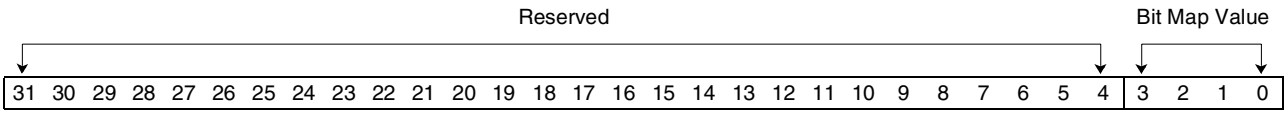
Length 32 bits

Type Read/Write

Address XXXX 0EA8

Power On Reset Value x‘0000 000F’

Restrictions None



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Entity with Post Memory Lock Access	The value in these bits map to the following entities: Value encoding is: F: Reserved 7: SEGBF E: CHKSM 6: Reserved D: PCORE LO 5: RXAAL C: BCACH LO 4: GPDMA B: POOLS LO 3: DMAQS A: CSKED 2: PCORE HI 9: Reserved 1: BCACH HI 8: RXQUE 0: POOLS HI

3.10.20 ARBIT Packet Config Register

The bits in this register control the operation of the Packet Memory arbiter.

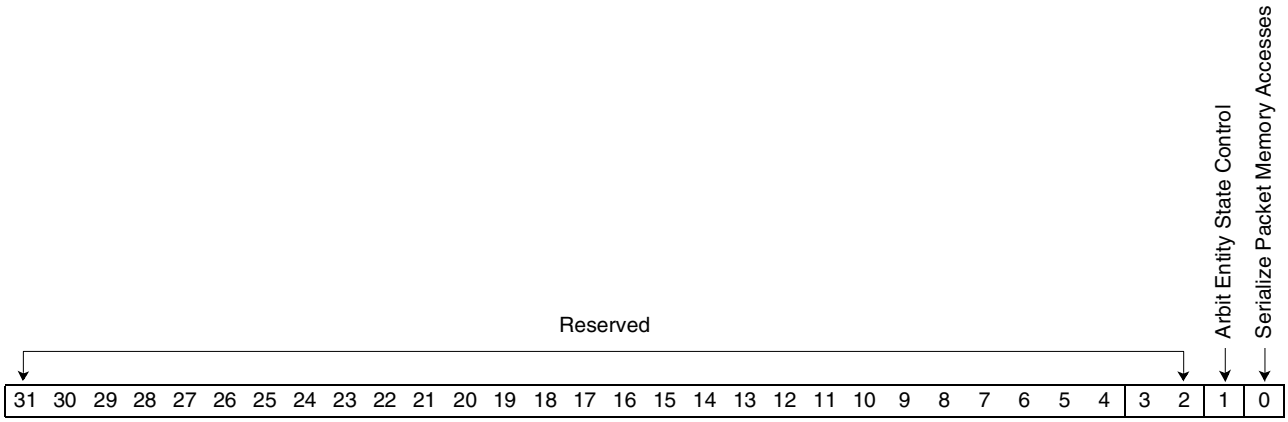
Length 32 bits

Type Clear/Set

Address XXXX 0EB8 and 0EBC

Power On Reset Value x‘0000 0000’

Restrictions None

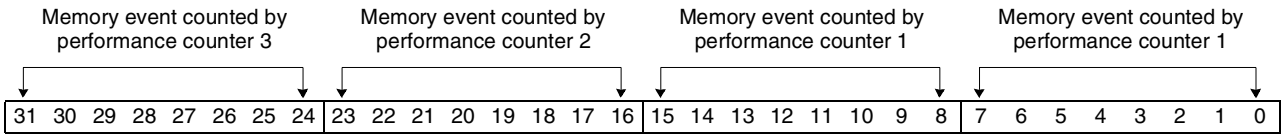


Bit(s)	Name	Description
31-2	Reserved	Reserved.
1	Arbit Entity State Control	This bit controls the ARBIT entity state debug mux. When set, the incoming entity requests and outgoing acknowledges are routed to the entity state pins. When reset, the internal state information is routed to the entity state pins.
0	Serialize Packet Memory Accesses	When set, this bit forces all operations to Packet Memory to be serialized. An operation from one entity must be entirely complete before an operation from another entity will be started. When reset, if the memory operation in process can be overlapped, a second operation will be started before the first operation is complete.

3.10.21 ARBIT Performance Counter Control

The bits in this register determine what events are counted by the memory performance counters. This 32-bit register is divided into four 8-bit values, one value for each of the counters. The eight bits determine what memory event is counted by the associated counter.

Length	32 bits
Type	Read/Write
Address	XXXX 0EB4
Power On Reset Value	x'9F1E 8000'
Restrictions	None

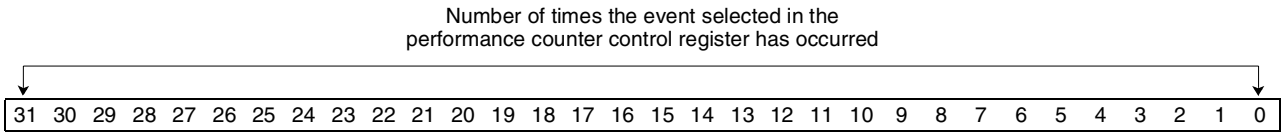


Bit(s)	Name	Description
31-24	Event Counter 3 Control	The value loaded into these bits defines what memory event is counted by performance counter 3. These bits are defined as follows: Bit 7: When reset, Control Memory events are counted, when set, Packet Memory events are counted by the associated counter. Bit 6: Reset the associated counter to 0. This bit will be reset by the hardware, during the same cycle that the counter is being reset. Bit 5: Reserved Bits 4-0: Cycle type, encoded as: 00000 Any Request 00001 Any Request between 0 and 4 bytes 00010 Any Request between 5 and 8 bytes 00011 Any Request between 9 and 16 bytes 00100 Any Request between 17 and 32 bytes 00101 Any Request between 33 and 64 bytes 00110 Any Request between 65 and 128 bytes 00111 Reserved 01000 Any Read Request 01001 Any Read Request between 0 and 4 bytes 01010 Any Read Request between 5 and 8 bytes 01011 Any Read Request between 9 and 16 bytes 01100 Any Read Request between 17 and 32 bytes 01101 Any Read Request between 33 and 64 bytes 01110 Any Read Request between 65 and 128 bytes 01111 Reserved 10000 Any Write Request 10001 Any Write Request between 0 and 4 bytes 10010 Any Write Request between 5 and 8 bytes 10011 Any Write Request between 9 and 16 bytes 10100 Any Write Request between 17 and 32 bytes 10101 Any Write Request between 33 and 64 bytes 10110 Any Write Request between 65 and 128 bytes 10111 Reserved 11000 Read op latency 11001 Write op latency 11010 Reserved 11011 Reserved 11100 Reserved 11101 Reserved 11110 Hold Current Count 11111 Every Cycle
23-16	Event Counter 2 Control	The value loaded into these bits define what memory event is counted by performance counter 2.
15-8	Event Counter 1 Control	The value loaded into these bits define what memory event is counted by performance counter 1.
7-0	Event Counter 0 Control	The value loaded into these bits define what memory event is counted by performance counter 0.

3.10.22 ARBIT Memory Performance Counter

These registers count memory events as defined in the ARBIT performance counter control register.

Length	32 bits	
Type	Read/Write	
Address	Counter 0	XXXX 0EC0
	Counter 1	XXXX 0EC4
	Counter 2	XXXX 0EC8
	Counter 3	XXXX 0ECC
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-0	Event Count	These bits count the number of times that the event selected in the performance counter control register has occurred.

3.11 The Bus DRAM Cache Controller (BCACH)

The array is organized in four logically separate cache lines, any of which can be used for processor accesses or master/slave DMA accesses. The cache is accessible on byte boundaries on the Control Processor side; access of this entity to PAKIT is performed on 64-bit (word) boundaries. The address tags of each of the four 32-byte cache lines are compared to the requesting address to select the bank to be used to satisfy the Control Processor bus operation.

Streaming accesses of the cache use a predictive look-ahead scheme to fill the cache for read operations from Packet Memory. Under normal conditions, a single cache miss will be expected at the start of each DMA read operation. This cache miss will initiate a read operation from Packet Memory to fetch the requested data and enough additional data to fill the remainder of the cache line. If the requested data is in the last N bytes (N is programmable via the BCACH control register) of the cache line, the read operation to PAKIT will be extended to fill the next cache line with sequential data as well. This same programmable value is used to determine when to initiate the next sequential cache line fill operation during a DMA read operation. During non-aligned write operations to Packet Memory, BCACH will perform read/modify/write cycles to PAKIT.

Processor accesses operate without predictive caching. When a cache miss occurs, a COMET read operation will be initiated to fetch the 32-byte block of data that contains the requested data. The data read from PAKIT will be loaded into the “Least Recently Used” cache line.

This section contains descriptions of the registers used by the Bus Cache logic Transmit Data Path entities.

3.11.1 BCACH Control Register

The bits in this register control the various functions provided by the cache logic.

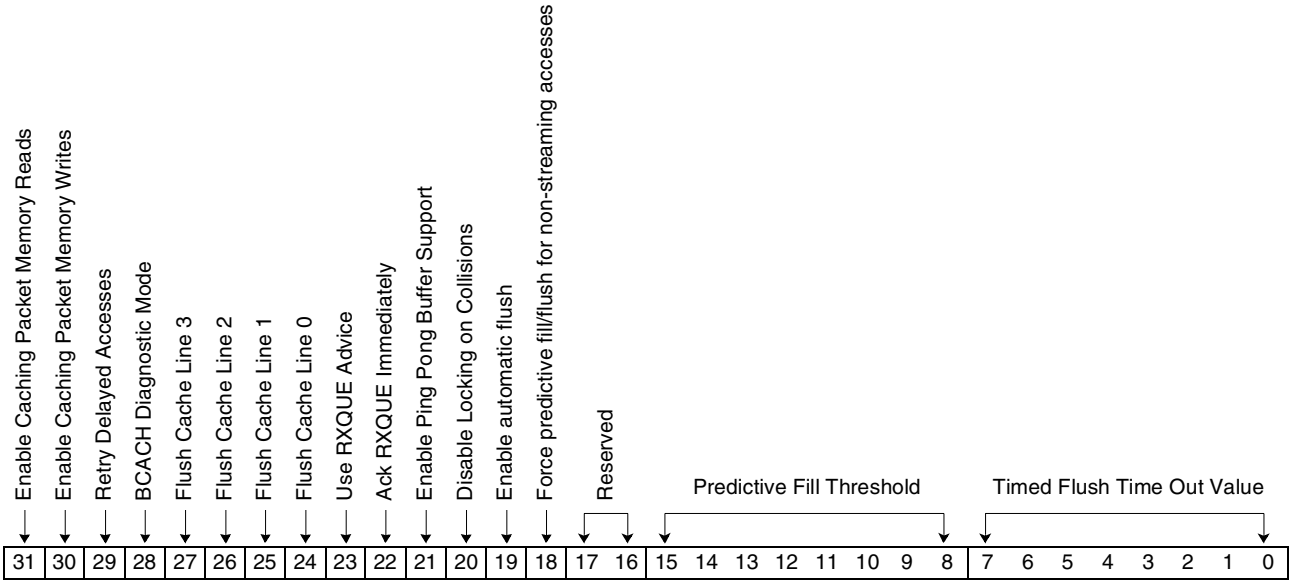
Length 32 bits

Type Clear/Set

Address XXXX 1000 and 1004

Power On Reset Value x‘2000 0000’

Restrictions None



Bit(s)	Name	Description
31	Enable Caching Packet Memory Reads	When this bit is set, reads of Packet Memory will be cached.
30	Enable Caching Packet Memory Writes	When this bit is set, writes to Packet Memory will be cached.
29	Retry Delayed Accesses	When this bit is set, and the cache is enabled, any access of Packet Memory that cannot be satisfied within one cycle will be terminated by the cache with a retry indication. The accessing device is expected to allow competing devices a chance to gain access to the bus and then retry the same operation.
28	BCACH Diagnostic Mode	When this bit is set, diagnostic mode is enabled and reads and writes of the BCACH array from the processor are enabled. When reset, reads from the processor will return x‘BADD BADD’ and writes will have no affect. Care must be taken when performing writes from the processor: if a cache line fill operation is in process and a write is performed from the processor that writes to the same address in the array as is being written from the fill operation, results are indeterminate.
27	Flush Cache Line 3	Setting this bit forces a flush of cache line 3 if it is dirty. This bit is reset by the hardware when the flush completes.
26	Flush Cache Line 2	Setting this bit forces a flush of cache line 2 if it is dirty. This bit is reset by the hardware when the flush completes.

Bit(s)	Name	Description
25	Flush Cache Line 1	Setting this bit forces a flush of cache line 1 if it is dirty. This bit will be reset by the hardware when the flush completes.
24	Flush Cache Line 0	Setting this bit forces a flush of cache line 0 if it is dirty. This bit will be reset by the hardware when the flush completes.
23	Use RXQUE Advice	When set, advice from the receive queue entity causes the cache logic to fill a line with the data from the start of the buffer that was just dequeued by the software. This should improve performance by having the receive data available when the processor accesses the buffer after the dequeue. To make best use of this feature, the code should access the receive data shortly after the dequeue to avoid the data in the cache line from becoming stale and being invalidated due to other cache functions. When reset, advice from the receive queue entity will be ignored.
22	Ack RXQUE Immediately	When reset, advice from the receive queue entity is acknowledged immediately even if the cache is not able to perform the requested data fetch. In this case, the advice is lost, and the cache will not fetch the data until the processor requests it again. When set, the advice from the receive queue entity is not acknowledged until the cache has actually latched the advice information. This guarantees that the advice will be used, but may cause delays in the Receive Queue entity's processing.
21	Enable Ping Pong Buffer Support	When reset, this bit disables the two-line ping pong feature associated with consistent sequential cache accesses. When set, a series of sequential accesses to Packet Memory that would normally require more than two cache lines to be satisfied is limited to only two cache lines, regardless of the length of the transfer. This feature is intended to improve cache performance by preventing cache lines that contain the most recently used processor data from being flushed due to a long streaming access.
20	Disable Locking on Collisions	When set, this bit prevents detected collisions from locking up the memory control entity.
19	Enable Automatic Flush	When set, this bit enables the automatic flush feature of the cache. The auto flush feature forces a flush of a cache line to be performed if a sequential write of the last two locations in the cache line is detected.
18	Force Predictive Fill/Flush for Non-Streaming Accesses	When set, this bit forces the predictive fill/flush logic to operate on all accesses of the cache rather than just streaming accesses. When reset, the predictive fill logic will only be activated for streaming accesses in the cache.
17-16	Reserved	Reserved.
15-8	Predictive Fill Threshold	These bits set the threshold at which a predictive fill will be initiated. If all of these bits are set to '1', a predictive fill will be initiated on the first streaming access of a cache line, regardless of which byte in the line is accessed. If this field is set to x'3F' a predictive fill will be initiated on any streaming access of bytes at offset x'2' through x'7' in the cache line. If this field is set to x'03' a predictive fill will be initiated on any streaming access of bytes at offset x'6' or x'7' in the cache line. Setting the field to all '0's will disable predictive fills.
7-0	Timed Flush Time Out Value	These bits control the time-out value used to monitor dirty cache lines for inactivity. The value loaded into these eight bits is the number of 240 ns ticks that can occur without any activity in a dirty cache line before the cache logic will force a flush of the line to main memory. Setting these bits to all '0's disables the timed flush feature.

3.11.2 BCACH Status Register

The bits in this register reflect the current status of the cache.

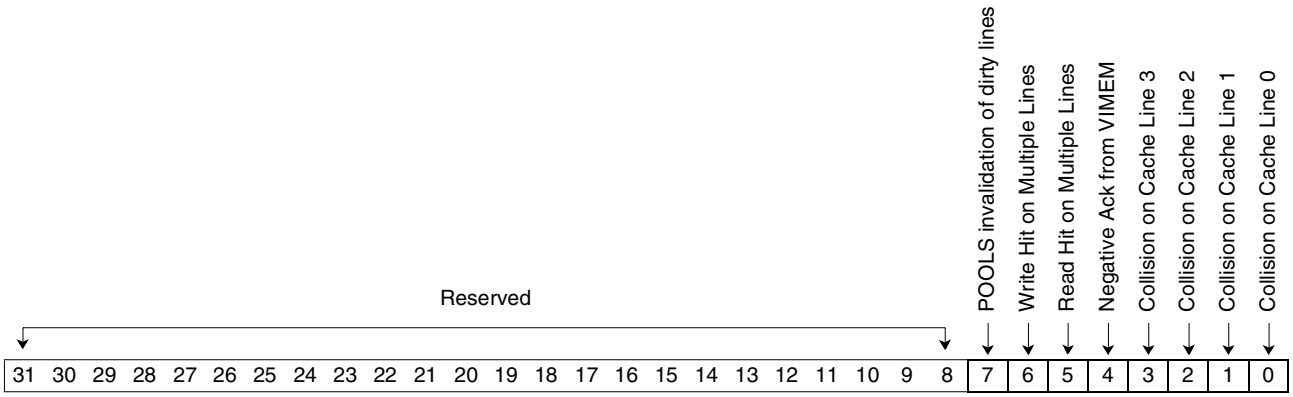
Length 32 bits

Type Clear/Set

Address XXXX 1008 and 100C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7	POOLS Invalidation of Dirty Lines	When this bit is set, it indicates that POOLS requested that the cache logic invalidate a line that was dirty. This is usually an indication that a buffer was freed by the software before data written out to the buffer had been flushed to memory. This may or may not be an error condition.
6	Write Hit on Multiple Lines	When this bit is set, the cache logic has detected a write hit to multiple lines. This indicates an internal logic error in the cache.
5	Read Hit on Multiple Lines	When this bit is set, the cache logic has detected a read hit to multiple lines. This indicates an internal logic error in the cache.
4	Negative Ack from VIMEM	When set, the cache logic has detected a negative acknowledgment from the Virtual Memory Logic entity. This indicates that a virtual buffer boundary was crossed and a new real buffer was needed to map the requested address space into, but no real buffer was available. In addition to setting this status bit, the cache logic writes the pattern x‘ZZZZ ZBAD’ into the header of the packet at offset x‘C’ where ZZZZZ is the offset of the failing write into the packet.
3	Collision on Cache Line 3	When this bit is set, the cache logic has detected a collision in cache line 3. This is a situation where another entity in the PNR was accessing an area of memory that was contained in one of the cache lines that was dirty. Further information for problem diagnosis is latched in the memory controller logic when this condition is detected.
2	Collision on Cache Line 2	When this bit is set, the cache logic has detected a collision in cache line 2.
1	Collision on Cache Line 1	When this bit is set, the cache logic has detected a collision in cache line 1.
0	Collision on Cache Line 0	When this bit is set, the cache logic has detected a collision in cache line 0.

3.11.3 BCACH Interrupt Enable Register

Bits 7-0 in this register allow the user to selectively determine which bits in the *BCACH Status Register* will cause processor interrupts. A ‘0’ in a bit position masks interrupts from the corresponding bit location in the *BCACH Status Register*. A ‘1’ in a bit position allows interrupts for the corresponding bit in the *BCACH Status Register*.

Bits 15-8 in this register allow the user to selectively determine which bits in the *BCACH Status Register* will lock the cache. Bits 15-8 correspond to bits 7-0 of the *BCACH Status Register* with regard to determining an enabled lock condition. A ‘1’ in any bit position forces the cache to lock if the corresponding bit is set in the *BCACH Status Register*. If the cache locks, all status regarding the cache lines is maintained until the cache enable bits in the control register are turned off.

Length 32 bits

Type Clear/Set

Address XXXX 1010 and 1014

Power On Reset Value x‘0000 FFFF’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	Lock Enables	Bits 15-8 correspond to bits 7-0 in the *BCACH Status Register* on page 236. If a lock enable bit and the corresponding status register bit are set, the cache will lock.
7-0	Interrupt Enables	Bits 7-0 correspond to bits 7-0 in the *BCACH Status Register* on page 236. If an interrupt enable bit and the corresponding status register bit are set, an interrupt is generated.

3.11.4 BCACH High Priority Timer Value

This register defines the number of 15 ns cycles that will pass from the time a valid PCI bus request is raised to BCACH until BCACH will raise its high priority request to the memory controllers. A value of ‘0’ in this register disables this function completely.

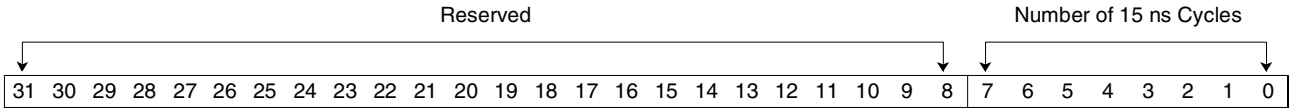
Length 32 bits

Type Read/Write

Address XXXX 1040

Power On Reset Value x‘0000 0040’

Restrictions None

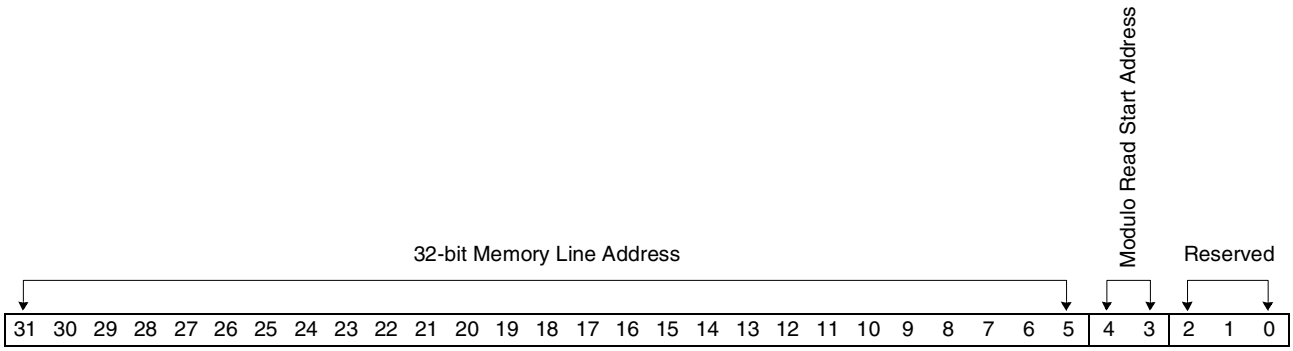


Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Number of 15 ns Cycles	Specifies the number of 15 ns cycles before a high priority request. For example, if bit 3 is set to ‘1’ and all others are set to ‘0’, then 6 cycles (120 ns) will pass between receipt of request and sending request to controllers.

3.11.5 BCACH Line Tag Registers

These registers are useful only in diagnostic testing of the cache logic. Each register will contain the tag value for the data contained in that particular cache line.

Length	32 bits	
Type	Read Only	
Address	Tag Number 0	XXXX 1080
	Tag Number 1	XXXX 10A0
	Tag Number 2	XXXX 10C0
	Tag Number 3	XXXX 10E0
Power On Reset Value		x‘0000 0000’
Restrictions	None	

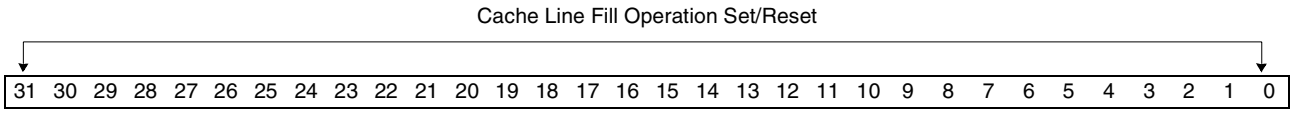


Bit(s)	Name	Description
31-5	32-byte Memory Line Address	These bits contain the address of the 32-byte line of memory contained in the cache line.
4-3	Modulo Read Start Address	In an attempt to provide the fastest possible access to data in memory, the 8-byte word in memory that contains the requested read data is accessed first and all other entries in the cache line are filled by wrapping back to the beginning of the cache line if required. These two bits contain the starting address for the modulo read fill operation. They will also contain the least significant address bits when a cache line is initially written to.
2-0	Reserved	Will always be returned as ‘0’.

3.11.6 BCACH Line Valid Bytes Register

These registers are useful only in diagnostic testing of the cache logic. Each register will contain a bit significant flag indicating which bytes in the 32-byte cache line are valid. All of these bits will be active after a cache line fill operation has occurred, but any combination of these bits can be valid after the processor has performed a write operation to memory.

Length	32 bits	
Type	Read Only	
Address	Tag Number 0	XXXX 1084
	Tag Number 1	XXXX 10A4
	Tag Number 2	XXXX 10C4
	Tag Number 3	XXXX 10E4
Power On Reset Value		x‘0000 0000’
Restrictions	None	

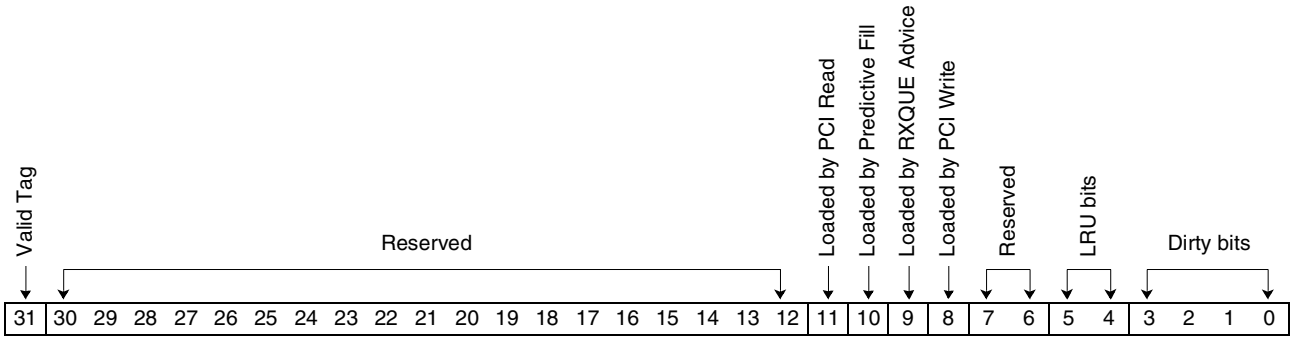


Bit(s)	Name	Description
31-0	Valid Bytes in Cache Line	Each bit indicates whether the associated byte in the cache line contains valid data. If the bit is set, the cache line contains valid data and a fetch from main storage is not required to fulfill a request for a read from this location. If the bit is reset, a read of the associated location will require a cache line fill operation before the request can complete.

3.11.7 BCACH Line Status Register

These registers are useful only in diagnostic testing of the cache logic. Each register will contain a bit significant flag indicating the current status of the associated cache line.

Length	32 bits	
Type	Read Only	
Address	Tag Number 0	XXXX 1088
	Tag Number 1	XXXX 10A8
	Tag Number 2	XXXX 10C8
	Tag Number 3	XXXX 10E8
Power On Reset Value	Tag Number 0	x‘0000 0000’
	Tag Number 1	x‘0000 0010’
	Tag Number 2	x‘0000 0020’
	Tag Number 3	x‘0000 0030’
Restrictions	None	



Bit(s)	Name	Description
31	Valid Tag	When set, this indicates that the associated tag register contains a valid tag.
30-12	Reserved	Reserved.
11	Loaded by PCI Read	When set, this bit indicates that the associated tag register was loaded due to a read request from the PCI bus.
10	Loaded by Predictive Fill	When set, this bit indicates that the associated tag register was loaded due to a predictive fill request.
9	Loaded by RXQUE Advice	When set, this bit indicates that the associated tag register was loaded due to advice from the receive queue entity.
8	Loaded by PCI Write	When set, this bit indicates that the associated tag register was loaded due to a write request from the PCI bus.
7-6	Reserved	Reserved.

Bit(s)	Name	Description
5-4	LRU Bits	These bits indicate the cache lines current position with respect to the least recently used algorithm. A value of ‘0’ indicates it is the most recently used while a value of ‘3’ indicates the least recently used.
3-0	Dirty Bits	These bits, when set, indicate that the associated 8-byte word of the cache line is dirty. This information is used on cache line flushes, to lower memory utilization, by eliminating non-dirty word flushes from the cache line flush operation. For example, if these bits contain x‘1’, only the 8-byte word at offset zero in the cache line is dirty, so the flush operation will only write this one word to memory, saving three memory access cycles. If these bits contain x‘C’, only the two 8-byte words starting at offset x‘10’ in the cache line are dirty.

3.11.8 BCACH Cache Line Array

This array is divided into four 32-byte buffers used as cache lines 0, 1, 2, and 3.

Length 16 Words x 64 bits

Type Read/Write

Address XXXX 1100 - 117F

Restrictions This array can only be accessed when the diagnostic mode bit in the control register is set.

Bit(s)	Name	Description
—	Cache Lines	The four cache lines start at the following offsets into the array: Line 0 Offset x‘00’ Line 1 Offset x‘20’ Line 2 Offset x‘40’ Line 3 Offset x‘60’

3.12 Transmit Scheduler (CSKED)

The logic consists of timers and counters for determining transmit opportunities and interfaces to ARBIT (for accessing the timing data and descriptors), PCINT (for register accesses), RXQUE (for queuing events), POOLS (for returning buffers when finished transmitting), SEGBF (for getting the data from memory to transmit) and TXLCD (for caching the LCDs).

3.12.1 Scheduling Overview

This entity provides traffic shaping to ensure that traffic sent by the PNR conforms to the Quality of Service (QoS) parameters as defined by the ATM Forum. CSKED provides support for the following QoS parameters:

- Peak Cell Rate (PCR). The maximum number of cells per second that the connection can transfer into the network.
- Sustained Cell Rate (SCR). The average number of cells per second that the connection can transfer into the network. The burst tolerance determines the length of time over which the network measures this average.
- Burst Tolerance.The maximum length of time that the user can transfer at the peak cell rate. Burst Tolerance can be measured in number of cells, a measurement known as maximum burst size (MBS).

CSKED will send out cells at the SCR. If transmit opportunities are missed, as is the case when there is no data to send, the actual rate will become less than SCR. When data becomes available to send, CSKED will transmit up to MBS cells at the PCR, until the transmit rate returns to SCR.

3.12.2 Operational Description

3.12.2.1 LCD Initialization

A Logical Channel Data Structure (LCD) containing scheduling parameters for the circuit must be initialized before segmentation can be started. The parameters that are important to the operation of this entity are:

average_interval	This field contains the minimum average spacing allowed between cells transmitted on this connection. It is the reciprocal of the SCR, as specified in the ATM Forum Traffic Management Specification. The value for this field is expressed in slot times. The length of time for a slot is defined by the Timeslot Prescaler Register and should normally be set to one cell time.
peak_interval	This field contains the minimum spacing allowed between consecutive cells on this connection. It is the reciprocal of the PCR as specified in the ATM Forum Traffic Management Specification. This spacing is also expressed in slot times. A connection that can transmit every slot time would have a value of ‘1’ for this field.
max_burst_value and max_burst_mult	The values in these fields are used to limit the number of cells that can be transferred at the peak rate. The max_burst_value will be multiplied by four to the power of the max_burst_mult to yield the maximum credit time. This time is expressed in slot times and represents the time it would take to acquire the maximum number of cell credits. This maximum credit time should equal the average interval minus the peak interval, multiplied by the maximum number of cells (MBS) that can be transferred at the peak rate.

transmit_priority	This field specifies the priority of transmission on this connection. Three levels of priority are available. Connections needing the highest quality of service, such as a CBR connection, should use the highest priority. Connections with the lowest quality of service requirements, such as a UBR connection, should use the lowest priority.
drop	Data can be sent on up to four physical drops. This field specifies the drop for this connection.
max_resolution	If this bit is set, the lower eight bits of the average interval and peak interval parameters contain a fractional component. This allows a finer resolution for scheduling. For example, for a peak interval of 1.5 time units, the value written to the peak_interval field should be x'0180'. If this bit is set, the initial value of time-stamp should contain the current timeslot counter shifted 16 bits to the left.

See *7.3 Transmit LCD Data Structures* on page 678 for further information.

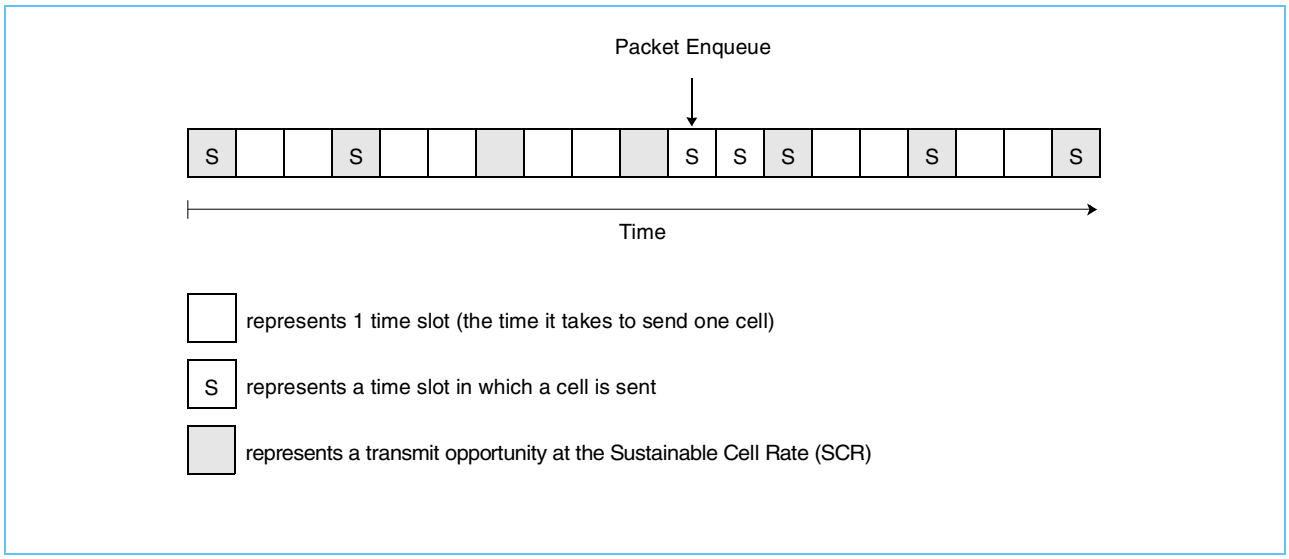
3.12.2.2 A Scheduling Example

If a connection is to have an SCR of 50 Mbps and a PCR at the line rate of 150 Mbps and a MBS of 10 cells, the LCD needs to be initialized as follows:

- average_interval = 150 Mbps/50 Mbps = 3
- peak_interval = 150 Mbps/150 Mbps = 1
- max_burst_value = 10*(3-1) = 20

The following example uses a timeline to show how a connection with these parameters is scheduled. Cells are sent every third slot while there is data to send. After the first two cells are sent there is no more data to send until another packet is enqueued. For each missed transmit opportunity, a cell can be sent at the peak interval, which is one. In the 15 timeslots after the first cell, five cells are sent for an SCR of 50 Mbps. The burst size is three, which is less than MBS. The unfilled slots can be used by other connections.

Figure 11: Timeline Example of Scheduling



3.12.2.3 CSKED Initialization

Before packets are enqueued for transmission, in addition to initializing the above scheduling parameters in the LCD, the following registers need to be set up.

- Timeslot Prescaler Register - The amount of time for one timeslot is defined by this register. It defaults to 707 ns which is one cell time on a 622 Mbps Sonet interface.
- CSKED Control Register - Additional scheduling options, such as number of priorities, need to be set in this register.

3.12.2.4 Packet Initialization

Packets to be segmented are written to Packet Memory, which has been allocated by POOLS. The address of the LCD describing the channel that this packet is to be transmitted on must be written to the header of the packet. Packet segmentation is started by issuing the transmit enqueue primitive to this entity. This entity will schedule segmentation of the packet according to the parameters set up in the LCD.

3.12.3 Scheduling Options

3.12.3.1 ABR Scheduling

CSKED has logic to assist in the processing of ABR connections. If the connection is ABR, the LCD will have a different configuration, as specified in *7.3 Transmit LCD Data Structures* on page 678. The following fields need to be initialized before the packets are sent on the connection.

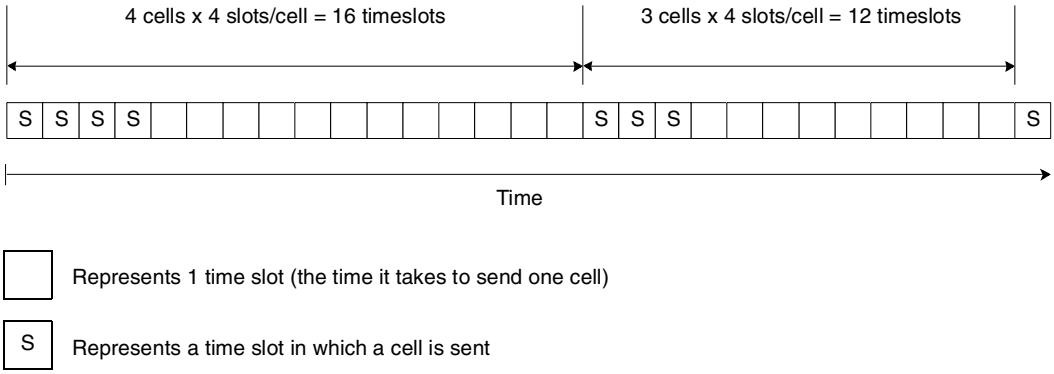
- **Scheduling type**. This field must be set to the value specifying an ABR connection.
- **Nrm.** This field should specify the maximum number of cells a source may send for each forward RM-cell. Number of cells = $(2^{Nrm})+1$.
- **Trm**. This field provides an upper bound on the time between forward RM-cells for an active source. Time = $100*(2^{-Trm})$ msec.
- **ADTF**. The ACR Decrease Time Factor is the time permitted between sending RM-cells before the rate is decreased to ICR. Time = ADTF* 0.01 msec.
- All other ABR fields should be initialized to ‘0’.

3.12.3.2 Frame Scheduling

CSKED has logic to support frame-based scheduling. It is enabled whenever the PHY type is configured for POS-PHY in LINKC. In frame-based scheduling the packet is sent out at the line rate, but the start time of the next frame is determined by multiplying the peak interval by the number of 64-byte blocks in the packet. The average portion of the bandwidth used by a connection will be 1/(peak interval). In frame-based scheduling, the average interval in the LCD should be set equal to the peak interval times the maximum packet size divided by 64.

For example, if a connection is to use 1/4 of the bandwidth, the peak interval should be set to four. The frames will be sent out at line rate, but the spacing between the start of each frame will be four timeslots for each cell sent from the packet. On average, 1/4 of the bandwidth will be used by the connection. The following timeline example depicts sending two packets, the first contains four cells and the second contains three cells. The unfilled slots can be used by other connections.

Figure 12: Timeline Example of Frame Scheduling



The above example assumes that one slot time is initialized to the time it takes to send 64 bytes out on the line. The term “cells” was used in this example to mean a 64-byte block of packet data. In frame mode, the ATM header is not prepended to the data being sent.

Weighted fair queueing on a frame basis is supported on the low priority queue by setting bit 17 in the CSKED Control Register. When using frame-based scheduling and weighted fair queuing together, the average interval will be used to limit the spacing between packets, not cells.

3.12.3.3 Path Scheduling

CSKED has logic to support sharing scheduling parameters between multiple connections. In path scheduling, an LPD is set up to contain the scheduling parameters for the group of connections in the same way it is done for LCDs. All connections that wish to share this bandwidth set the alter_sched field in their LCD to indicate this VC is on a VP, and initialize the lpd_pointer field to point to the LPD. The segmentation portion of the LPD is not used since the segmentation parameters are taken from the LCD. The scheduling parameters in the LCDs are not used as they are in the LPD. The bandwidth is shared on a packet or cell basis depending the value of the alter_sched field in the LCD. Since both the LPD and LCD need to be fetched for each transmit opportunity, this scheduling method should not be used where the performance boundaries are being pushed, as in 622 Mbps. See *7.3 Transmit LCD Data Structures* on page 678 for further information on LPD descriptors.

3.12.4 Primitives

3.12.4.1 Enqueue

After a packet has been written to memory and the packet header updated with the offset and length of the data and the LCD address of the connection, an enqueue primitive needs to be issued to the Transmit Enqueue Primitive address.

3.12.4.2 Close Connection

When no more traffic is to be sent on a connection, this primitive can be executed to cause an event to be generated when segmentation has stopped on this connection. Segmentation will be stopped immediately, or stopped after all packets on this connection have been transmitted as specified in the CSKED Control Register.

3.12.4.3 Transmit Enqueue Primitive

Enqueues a buffer for transmission. When read, will return the address of the last packet enqueued.

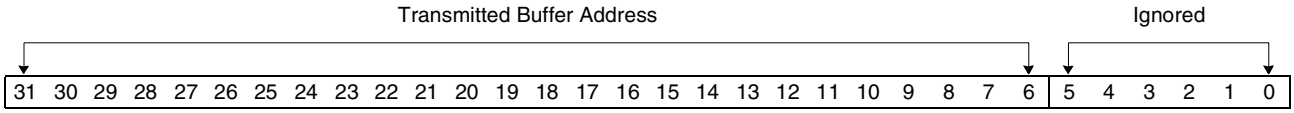
Length 32 bits

Type Read/Write

Address XXXX 1200

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-6	Transmitted Buffer Address	This must contain the address of the buffer to be transmitted. Buffers must be aligned on at least 64-byte boundaries. The lower six bits are ignored.
5-0	Ignored	Ignored.

3.12.4.4 Resume Transmission Primitive

Resumes transmission on an ABR connection that has been suspended. On an ABR connection, ADTF, CRM, and CCR=0 events will cause the transmission to be suspended until a rate conversion is completed, normally by the internal processor. This primitive will resume transmission on those connections, once the rate conversion is completed.

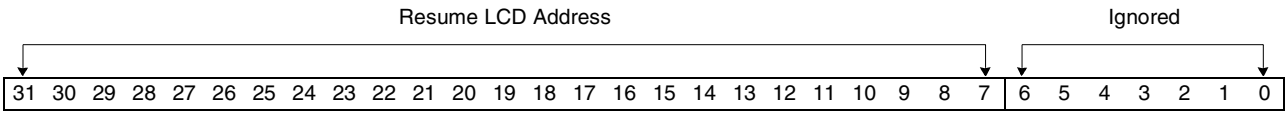
Length 32 bits

Type Read/Write

Address XXXX 1204

Power On Reset Value x‘0000 0000’

Restrictions This address should be written with care. This primitive should only be used on connections that have been suspended.



Bit(s)	Name	Description
31-7	Resume LCD Address	This must contain the address of the LCD that is to resume transmission. The lower seven bits are ignored.
6-0	Ignored	Ignored.

3.12.4.5 Start/Stop Timer Primitive

Start or stop a timer with the parameters in the specified LCD address. When this primitive is executed, a timer whose parameters are contained in the specified LCD is started or stopped. Bit 0 specifies whether to start (0) or stop (1) the timer. When the timer pops, a DMA descriptor specified in the LCD will be executed.

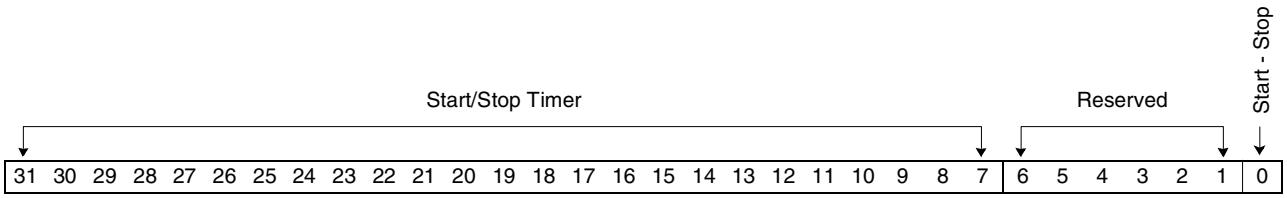
Length 32 bits

Type Read/Write

Address XXXX 1208

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Start/Stop Timer	This must contain the address of the LCD that contains the timer parameters.
6-1	Reserved	Reserved.
0	Start - Stop	This bit specifies whether the timer is to be started (0) or stopped (1).

3.12.4.6 Close Connection Primitive

Transmission is complete on a connection specified by an LCD address. When no more traffic is to be sent on a connection, this primitive can be executed to cause an event to be generated when segmentation has stopped on this connection. Segmentation will be stopped immediately, or stopped after all packets on this connection have been transmitted, as specified in the CSKED Control Register.

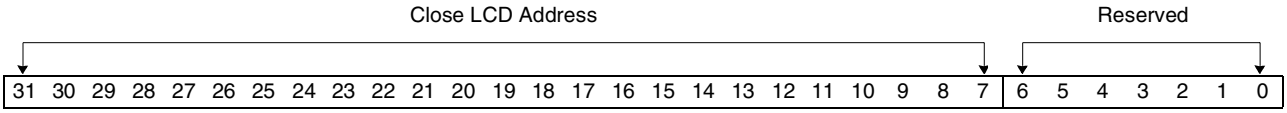
Length 32 bits

Type Read/Write

Address XXXX 120C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Close LCD Address	This must contain the address of the LCD that is to be closed. The lower seven bits are ignored.
6-0	Reserved	Reserved.

3.12.4.7 Timeslot Prescaler Register

This register determines the length of time for one timeslot. This controls the rate that the cell scheduling counters are incremented. Each clock cycle, the value in this register is added to a 24-bit counter. When the upper bit of the counter changes state, the Current Timeslot Counter is incremented. This should normally be set to the time it takes to transmit one cell. It will be initialized to the cell time for a 622 Mb/s SONET connection (599.04 Mb/s payload). The following formula should be used to determine the value to load in this register: Timeslot Prescaler = (clock interval/timeslot interval) x 2^{23}.

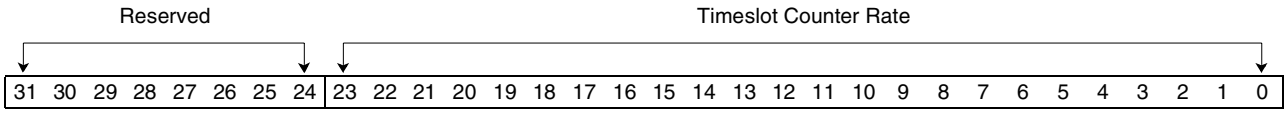
Length 32 bits

Type Read/Write

Address XXXX 1210

Power On Reset Value x‘0002 B67C’

Restrictions This register should be written only at initialization time.



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	Timeslot Counter Rate	This value will determine the rate at which the Current Timeslot Counter is advanced.

3.12.4.8 Current Timeslot Counter

This counter contains a count of how many prescaled intervals have elapsed. It is used to determine if it is time to send data from a connection.

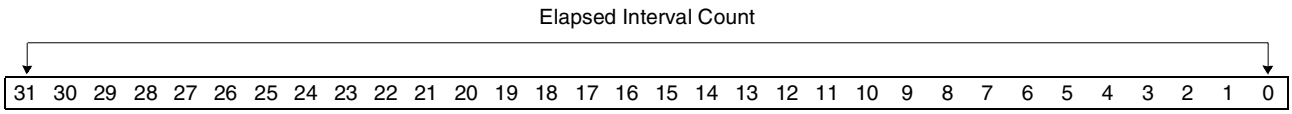
Length 32 bits

Type Read/Write

Address XXXX 1218

Power On Reset Value x‘0000 0000’

Restrictions This register is meant to be read only. It is writable for diagnostic purposes only.



Bit(s)	Name	Description
31-0	Elapsed Interval Count	This value represents how many expirations have occurred since the counter rolled over.

3.12.5 CSKED Control Register

This register is used to control the actions of CSKED.

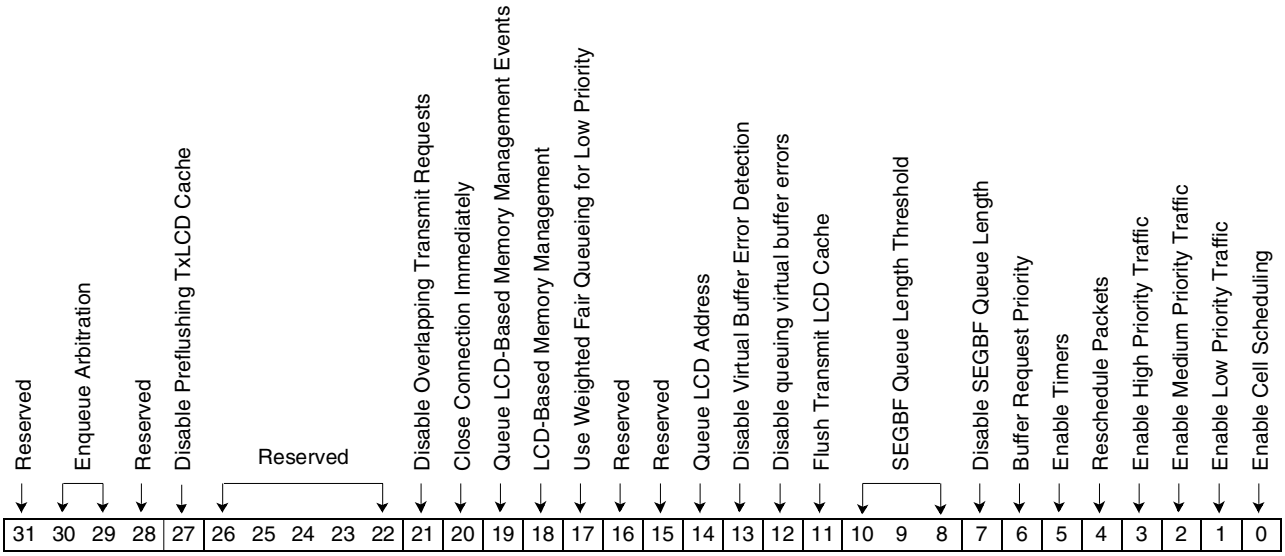
Length 32 bits

Type Clear/Set

Address XXXX 1220 and 1224

Power On Reset Value x‘0000 0759’

Restrictions None



Bit(s)	Name	Description
31	Reserved	Reserved.
30-29	Enqueue Arbitration	There can be three sources of an enqueue request. These bits control the order in which the requestoring entities will be serviced if more than one is active. 00 Round robin 01 PCINT, DMAQS, REASM 10 DMAQS, REASM, PCINT 11 REASM, PCINT, DMAQS
28	Reserved	Reserved.
27	Disable preflushing TXLCD cache	This bit disables automatically, flushing a cache line when all lines are dirty.
26-22	Reserved	Reserved.
21	Disable overlapping transmit requests	This bit is meant for debug purposes only. It will disable the ability of CSKED to overlap requests to SEGBF.
20	Close connection immediately	Setting this bit to ‘1’ causes segmentation to stop immediately on any connection that has been issued a close connection primitive. When this bit is set to ‘0’, an event will be generated after all traffic queued to this connection has been sent.

Bit(s)	Name	Description
19	Queue LCD-based memory management events	Setting this bit to '1' causes LCD-based memory management events to be queued to the Transmit Complete Queue, if enabled by bit 18 of this control register. If LCD-based memory management is enabled and this bit is off, the receive pool ID associated with this connection will be updated when a threshold is crossed.
18	LCD-based memory management	Setting this bit to '1' enables LCD-based memory management for received packets. See *Figure 69: Definition of LCD-Based Memory Management of Transmit LCD* on page 686 for further information on this function.
17	Use weighted fair queueing for low priority	Setting this bit to '1' causes low priority traffic to be scheduled using weighted fair queueing. The peak interval in the LCD is used to provide a relative weight in determining the amount of bandwidth the connection will use. For example, a peak interval of one will use twice the bandwidth as a connection with a peak interval of two. The average interval specifies the maximum rate that the connection can use. For example if the average interval is set to two, the maximum rate at which it can send a cell is every two timeslot times (as defined in the Timeslot Prescaler Register).
16-15	Reserved	Reserved.
14	Queue the LCD address if freeing and queueing	Setting this bit to '1' causes the LCD address, instead of the packet address, to be queued if both freeing and queueing on transmit are complete.
13	Disable virtual buffer error detection	Setting this bit to '1' causes the buffer enqueue logic to ignore virtual buffer errors.
12	Disable queuing virtual buffer errors	If virtual buffer error detection is not disabled, detected errors will be queued. When this bit is set to '1', this queueing is disabled and the buffer will be freed.
11	Flush Transmit LCD Cache	When this bit is set to '1', the transmit LCD cache will be flushed. This bit resets after the cache has been flushed. Flushing the cache should not be needed in normal operation.
10-8	SEGBF Queue Length Threshold	Cells can be queued in SEGBF up to the number specified in this register. The default is seven which is more than the actual buffers available. Writing these bits to '000' also disables this function.
7	Disable SEGBF Queue Length in Scheduling	CSKED will normally include SEGBFs queue length in the calculations when rescheduling a cell. Setting this bit to '1' disables this function, and the cell will be scheduled as if the cells were transferred when SEGBF accepted them.
6	Priority of buffer requests	When this bit is set to '0', scheduling requests have a higher priority than buffer enqueue requests. When this bit is set this priority is reversed. It should be '1' if a significant percentage of packets are only a few cells long.
5	Enable timers	Timer descriptors can be enqueued to this entity that will cause a DMA descriptor to be executed on expiration. If these timers are used, this bit must be set to '1'. If they are not used, this bit should be set to '0' (default).
4	Reschedule Packets in the Slow Queue to the Fast Queue	If the average or peak interval is greater than 255, the cells will be scheduled in the slow queue. The slow queues will be serviced every 64 pre-scaler time units. This means that a jitter of up to 64 pre-scaler time units should be expected for slow traffic. If this bit is set, packets in the slow queue will be rescheduled at the appropriate time to the fast queue. This will decrease the variation in the scheduling but may cause some performance degradation if traffic is heavy.
3	Enable High Priority Traffic	Enable High priority Traffic.
2	Enable Medium Priority Traffic	Enable Medium Priority Traffic.
1	Enable Low Priority Traffic	Enable Low Priority Traffic.
0	Enable Cell Scheduling	When this bit is set to '0', no primitives will be handled and no cells will be scheduled.

3.12.6 Transmit Segmentation Throttle Register

This register contains the number of cycles to wait between successive requests to transmit a cell. Its purpose is to slow segmentation on all VCIs if it is determined by software that the network cannot handle the generated load. The value in this register will be loaded into the Transmit Segmentation Counter each time a cell is accepted for transmission. For normal operation, the value in this register should be ‘0’.

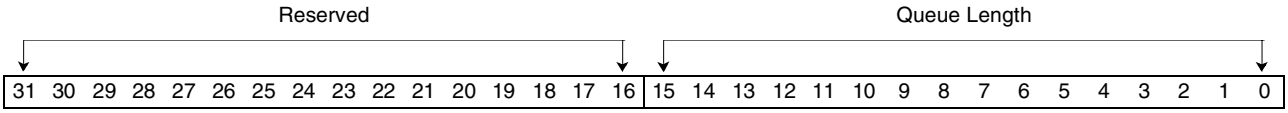
Length 32 bits

Type Read/Write

Address XXXX 1230

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Queue Length	When the transmit complete queue length reaches this value an interrupt will be generated.

3.12.7 Transmit Segmentation Throttle Counter

This register is loaded with the value in the Transmit Segmentation Throttle Register after each cell is accepted for transmission and counts down until it reaches ‘0’. A new cell transmission will not be requested until this counter reaches ‘0’.

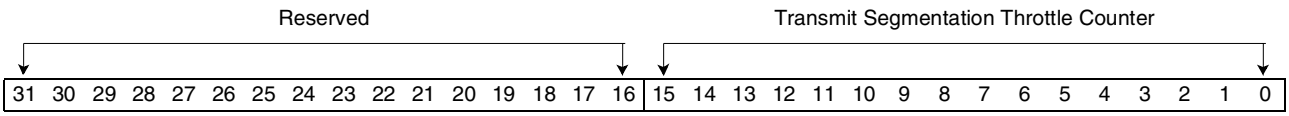
Length 32 bits

Type Read Only

Address XXXX 1234

Power On Reset Value x‘0000 0000’

Restrictions Read Only



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Transmit Segmentation Throttle Counter	When this counter reaches ‘0’, a new cell can be transmitted.

3.12.8 MPEG Conversion Register

This register is used to convert MPEG time units into timeslot time units. If MPEG traffic is configured in the LCD, the data stream will be monitored for PCRs. If a PCR is detected, it will be scheduled at the time specified in the PCR. A conversion factor needs to be written into this register to convert the MPEG time units into timeslot units. It will be initialized to a value that converts the MPEG time units (90 KHz) into the timeslot units (353.2 KHz, assuming one timeslot is the time it takes to send one cell over a SONET connection). The lower 12 bits of this register contain the fractional portion of this conversion factor.

```
Example: 353.2076 KHz / 90 KHz = 3.924528 = 3.ECB hex
```

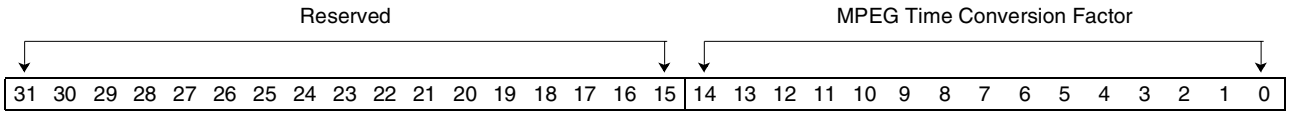
Length 32 bits

Type Read/Write

Address XXXX 125C

Power On Reset Value x‘0000 3ECB’

Restrictions None



Bit(s)	Name	Description
31-15	Reserved	Reserved.
14-0	MPEG Time Conversion Factor	Contains the conversion factor.

3.12.9 ABR Timer Prescaler Register

This register determines the length of time for a tick of the RM Cell Timer. This controls the rate the cell scheduling counters are incremented. Each clock cycle, the value in this register is added to a 24-bit counter. When the upper bit of the counter changes state, the RM Cell Timer is incremented. This should be set to value of 0.78 ms. It will be initialized to 0.78 ms assuming a 15-ns clock (as set up in SCLCK). The following formula should be used to determine the value to load in this register:

ABR Timer Prescaler = (clock interval/0.78 ms) x 2^{23}.

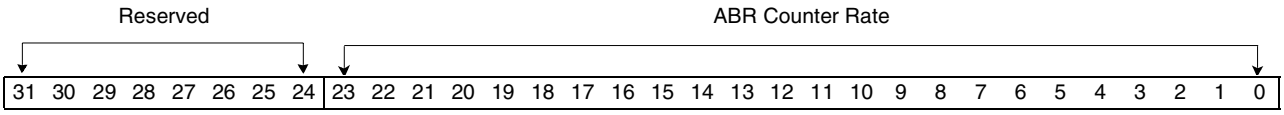
Length 32 bits

Type Read/Write

Address XXXX 127C

Power On Reset Value x‘0000 00A2’

Restrictions This register should be written only at initialization time.



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	ABR Counter Rate	This value will determine the rate at which the ABR counter is advanced.

3.12.10 RM Cell Timer

This register is used to keep track of the last time that an ABR RM cell was sent. Its period should be 0.78 ms.

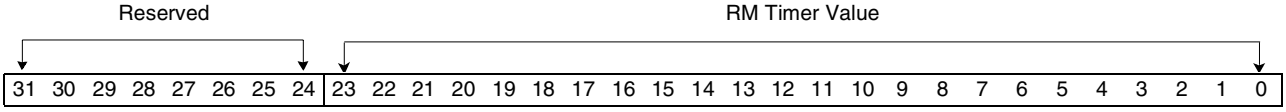
Length 32 bits

Type Read/Write

Address XXXX 126C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	RM Timer Value	Timer value.

3.12.11 CSKED LCD Update Data Registers

Used to specify data to write into the LCD on the update LC operation. These registers contain the data used in the LC Update Operation. See *3.12.14 CSKED LCD Read Operation Register* on page 259.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update1	XXXX 1300
	Update2	XXXX 130C
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.12.12 CSKED LCD Update Mask Registers

Used to specify data to write into the LCD on the update LC operation. These registers contain the mask used in the LC Update Operation. See *CSKED LCD Read Operation Register*.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update1	XXXX 1304
	Update2	XXXX 1310
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.12.13 CSKED LCD Update Operation Registers

Used to specify the LCD word to update. This operation is used to update a portion of an LCD. If this operation is not used, software or PNR updates of the LCD may be lost because the LCD is cached in the PNR while cells are being processed.

This register is written with the address of the LCD word to update. Once this register is written the update operation starts. All subsequent reads or writes to the data, mask, or update registers are held off until the operation completes. A read-modify-write will occur to update the portion specified by the mask with the masked value in the data register.

Normally this register would not be read. However, if it is read then the low order bit is read as ‘0’ and the next lowest order bit (bit 1) is read as the busy bit. This signifies whether an operation is still going on. If an operation is still going on, then a new write to any of the data, mask, or update operation registers is held off until the original operation is complete.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update1	XXXX 1308
	Update2	XXXX 1314
Power On Reset Value		x‘0000 0000’
Restrictions	The low order two bits are not writable.	

3.12.14 CSKED LCD Read Operation Register

This operation is used to specify the LCD word to read.

This register is written with the adddress of the LCD word to read. Once this register is written, the read operation starts. It uses the Update2 register of the *CSKED LCD Update Data Registers* on page 257. All subsequent reads or writes to the CSKED data, mask, or update registers are held off until the operation completes.

The lowest order bit (bit 0) of this register is read as the busy bit. This signifies whether an operation is still going on. The read data will be valid in the Update2 register of the *CSKED LCD Update Data Registerss* after the busy bit is turned off. If an operation is still going on, then a new write to any of the data, mask, or update operation registers is held off until the original operation is complete.

Length	32 bits
Type	Read
Address	XXXX1354
Power On Reset Value	x‘0000 0000’
Restrictions	The low order two bits are not writable.

3.12.15 Drop Access Control Register

Each drop (4) has registers that can be used for debugging purposes and bandwidth limiting. To conserve address space, this register determines the drop for the register access. These registers are Fast Serviced Counters, Slow Serviced Counters, and Priority Bandwidth Limit Registers. This register must be rewritten whenever values for a different drop need to be read or written.

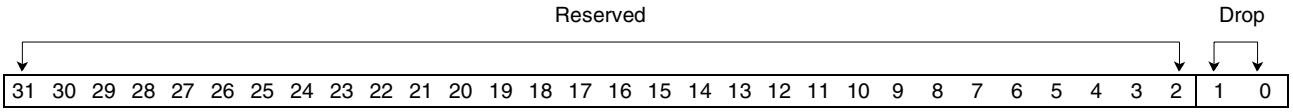
Length 32 bits

Type Read/Write

Address XXXX 1288

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-2	Reserved	Reserved.
1-0	Drop	This value represents the drop number or the above registers that will be accessed.

3.12.16 Performance Registers

This section contains registers that are for performance purposes.

3.12.16.1 High Priority Bandwidth Limit Register

This register can be used to limit the bandwidth used by high priority connections. Bits 15-8 of this register specify the number of high priority cells that can be sent in a window specified by bits 7-0 of this register. If no data needs to be sent by lower priority connections, high priority connections will not be limited.

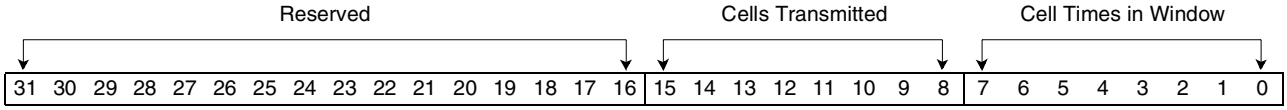
Length 32 bits

Type Read/Write

Address XXXX 1270

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	High Priority Cells per Time Window	This value specifies the number of cells that can be transmitted from high priority connections in one time window.
7-0	Cell Times per Time Window	This value specifies the number of cell times in the window.

3.12.16.2 Medium Priority Bandwidth Limit Register

This register can be used to limit the bandwidth used by medium priority connections. The upper eight bits of this register specify the number of medium priority cells that can be sent in a window specified by the lower eight bits of this register. If no data needs to be sent by low priority connections, medium priority connections will not be limited.

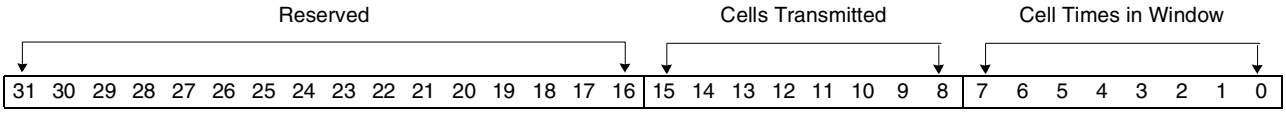
Length 32 bits

Type Read/Write

Address XXXX 1274

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	Medium Priority Cells per Time Window	This value specifies the number of cells that can be transmitted from medium priority connections in one time window.
7-0	Cell Times per Time Window	This value specifies the number of cell times in the window.

3.12.16.3 Low Priority Bandwidth Limit Register

This register can be used to limit the bandwidth used by low priority connections. The upper eight bits of this register specify the number of low priority cells that can be sent in a window specified by the lower eight bits of this register.

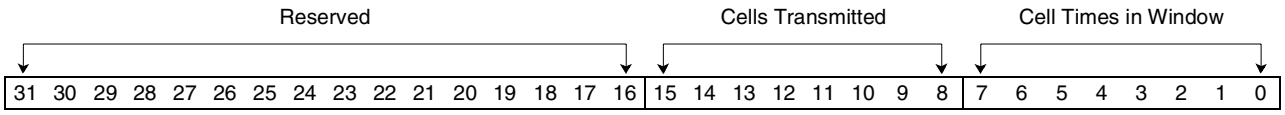
Length 32 bits

Type Read/Write

Address XXXX 1278

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-8	Low Priority Cells per Time Window	This value specifies the number of cells that can be transmitted from low priority connections in one time window.
7-0	Cell Times per Time Window	This value specifies the number of cell times in the window.

3.12.16.4 High Priority Cells Transmitted Counter

This register contains the number of cells transmitted from high priority connections.

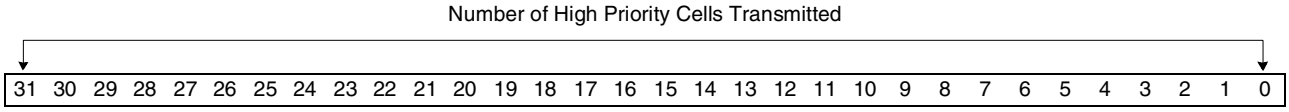
Length 32 bits

Type Read/Write

Address XXXX 1260

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	High Priority Cells Transmitted	This value represents the number of cells transmitted from high priority connections.

3.12.16.5 Medium Priority Cells Transmitted Counter

This register contains the number of cells transmitted from medium priority connections.

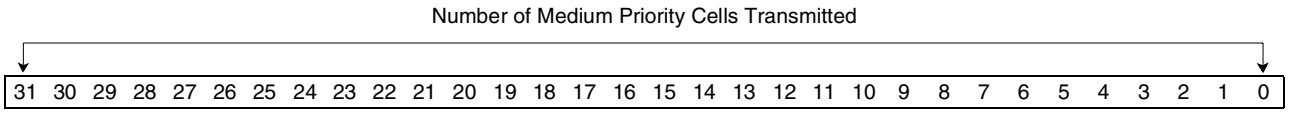
Length 32 bits

Type Read/Write

Address XXXX 1264

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Medium Priority Cells Transmitted	This value represents the number of cells transmitted from medium priority connections.

3.12.16.6 Low Priority Cells Transmitted Counter

This register contains the number of cells transmitted from low priority connections.

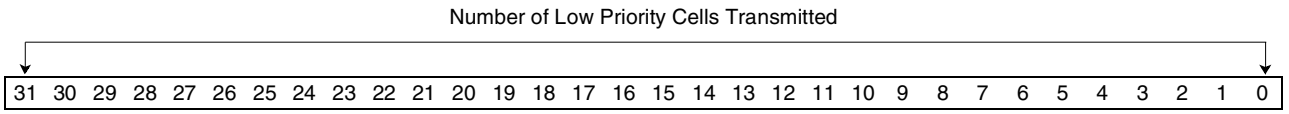
Length 32 bits

Type Read/Write

Address XXXX 1268

Power On Reset Value x‘0000 0000’

Restrictions None

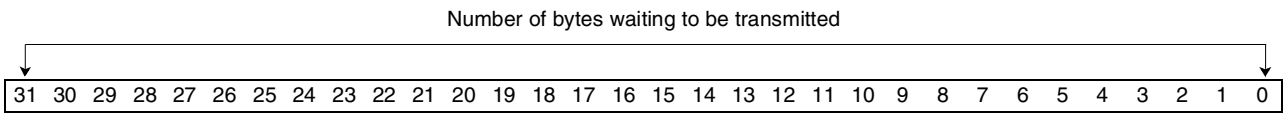


Bit(s)	Name	Description
31-0	Low Priority Cells Transmitted	This value represents the number of cells transmitted from low priority connections.

3.12.16.7 Bytes Queued Counters

These registers (12) contain the number of bytes queued for transmission for each priority (3) on each drop (4). The addresses are assigned to the range in the following order:

Length	32 bits	
Type	Read/Write	
Address	High priority, Port 0	XXXX 1290
	High priority, Port 1	XXXX 1294
	High priority, Port 2	XXXX 1298
	High priority, Port 3	XXXX 129C
	Medium priority, Port 0	XXXX 12A0
	Medium priority, Port 1	XXXX 12A4
	Medium priority, Port 2	XXXX 12A8
	Medium priority, Port 3	XXXX 12AC
	Low priority, Port 0	XXXX 12B0
	Low priority, Port 1	XXXX 12B4
	Low priority, Port 2	XXXX 12B8
	Low priority, Port 3	XXXX 12BC
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-0	Bytes Queued	This value represents the number of bytes waiting to be transmitted for each priority on each drop.

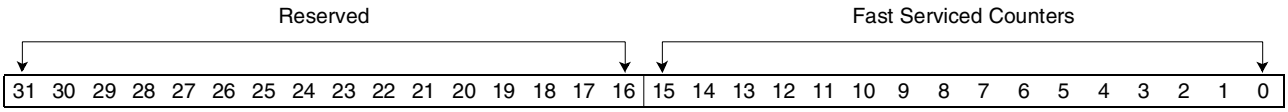
3.12.17 Debugging Register Access

This section contains registers that are for debug purposes only. These registers need not be written or read during normal operations.

3.12.17.1 Fast Serviced Counters

There are three fast serviced counters, one for each transmit priority: high, medium, and low. These registers contain the value of the last fast time slot that has been serviced. When this count differs from the current timeslot count, at least one fast slot needs servicing. Each time the fast slot is serviced, this counter will increment.

Length	32 bits	
Type	Read/Write	
Address	High Priority	XXXX 1240
	Medium Priority	XXXX 1244
	Low Priority	XXXX 1248
Power On Reset Value		x‘0000 0000’
Restrictions	These registers are meant to be read only. They are writable for diagnostic purposes only.	

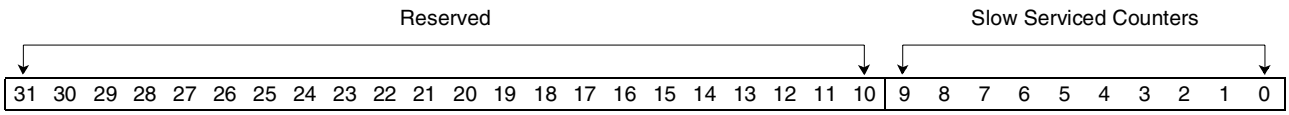


Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Fast Serviced Counters	This value represents how many times this time wheel has been serviced since the counter rolled over.

3.12.17.2 Slow Serviced Counters

There are three slow serviced counters, one for each transmit priority: high, medium, and low. These registers contain the value of the last slow time slot that has been serviced. When this count differs from the current timeslot count, at least one slow slot needs servicing. Each time the slow slot is serviced, this counter will increment.

Length	32 bits	
Type	Read/Write	
Address	High Priority	XXXX 124C
	Medium Priority	XXXX 1250
	Low Priority	XXXX 1254
Power On Reset Value		x‘0000 0000’
Restrictions	These registers are meant to be read only. They are writable for diagnostic purposes only.	



Bit(s)	Name	Description
32-10	Reserved	Reserved.
9-0	Slow Serviced Counters	This value represents how many times this slow wheel has been serviced since the counter rolled over.

3.12.17.3 Timer Serviced Counters

In addition to the counters above, there is an additional counter for processing timer requests. These registers contain the value of the last timer slot serviced. When this count differs from the current timeslot count (bits 22-15), at least one slow slot needs servicing. Each time a timer slot is serviced, this counter will increment.

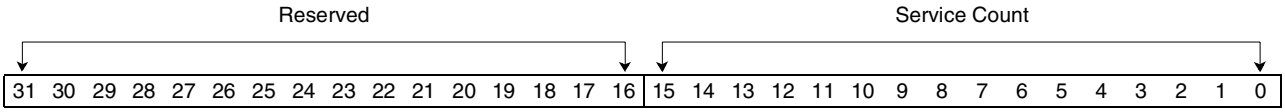
Length 32 bits

Type Read/Write

Address XXXX 1280

Power On Reset Value x‘0000 0000’

Restrictions This register is meant to be read only. It is writable for diagnostic purposes only.



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Service Count	This value represents how many times this timer wheel has been serviced since the counter rolled over.

3.12.17.4 CSKED Status Register

This register is used to indicate status for CSKED.

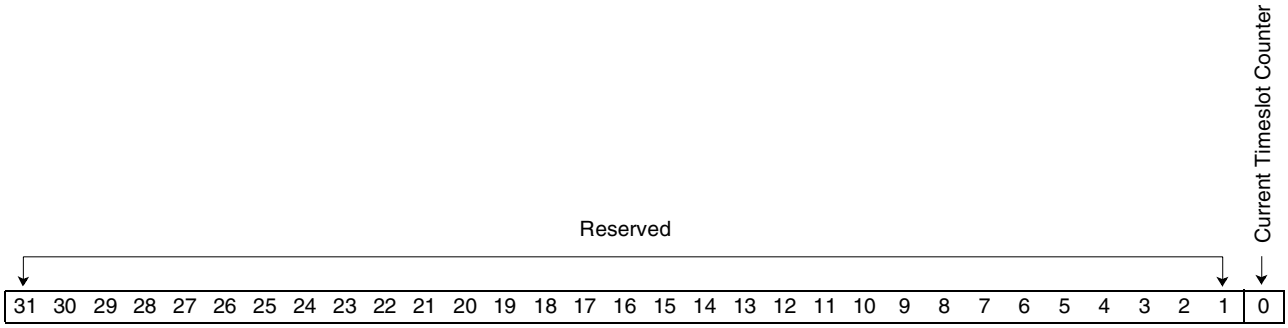
Length 32 bit

Type Clear/Set

Address XXXX 1228 and 122C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-1	Reserved	Reserved.
0	Current Timeslot Counter	Current timeslot counter has wrapped. If this bit is on, the timeslot counter has wrapped.

3.12.17.5 CSKED Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *CSKED Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from CSKED to INTST if the condition is detected.

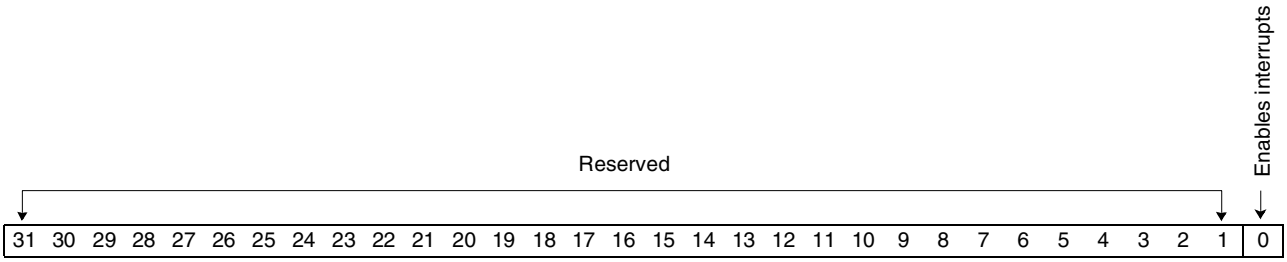
Length 32 bit

Type Clear/Set

Address XXXX 1238 and 123C

Power On Reset Value x'0000 0000'

Restrictions None



Bit(s)	Name	Description
31-1	Reserved	Reserved.
0	Interrupt Enable	When this bit is on and the corresponding bit in the *CSKED Status Register* is on, an interrupt is generated.

3.12.17.6 CSKED Timing Data Array Pointer

The CSKED Timing Data Array contains data relevant to scheduling cells. It contains 96 32-bit words. It should only be written for diagnostic purposes to test the array. It will power up to all zeros and should be rewritten to zeros after the array has been tested. This register points to an offset in the CSKED timing data array for accesses from the PCI bus. This register must be loaded with the correct offset before the desired data can be read from the CSKED timing data array data register. This register will auto-increment after each access to the associated data register. When the last address is accessed, this register wraps to zero.

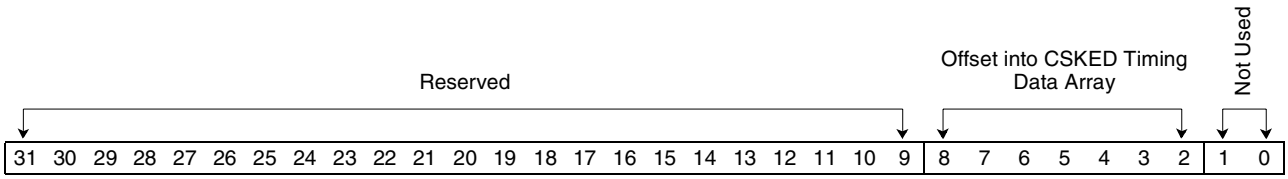
Length 32 bits

Type Read/Write

Address XXXX 12C0

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-9	Reserved	Reserved.
8-2	Array Offset	These bits provide an offset into the CSKED cell staging array for accesses from the PCI bus. These bits provide access to the 256 unique four-byte locations in the array. Accessing the last location in the array will cause the address to wrap back around to the beginning of the array.
1-0	Not used	These bits are not implemented. They cannot be written and will always return ‘0’ when read.

3.12.17.7 CSKED Timing Data Array Data

This register is used to access the array pointed to by the CSKED Timing Data Array Pointer.

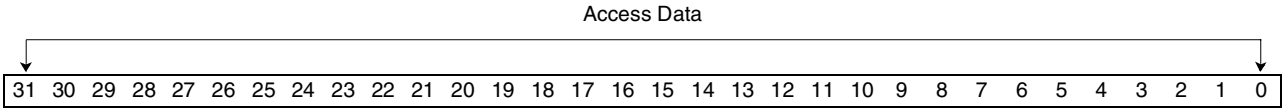
Length 32 bits

Type Read/Write

Address XXXX 12C4

Power On Reset Value

Restrictions Should be written for diagnostic use only. Initialize back to ‘0’s when through testing.



Bit(s)	Name	Description
31-0	Array Data	Array data.

3.12.17.8 CSKED Time Wheel Array Pointer

The CSKED Time Wheel Array contains data relevant to scheduling cells. It contains 16 K 19-bit words. It should only be written for diagnostic purposes to test the array. It will power up to all zeros and should be rewritten to zeros after the array has been tested. This register points to an offset in the CSKED time wheel array for accesses from the PCI bus. This register must be loaded with the correct offset before the desired data can be read from the CSKED Time Wheel Array Data register. This register will auto-increment after each access to the associated data register. When the last address is accessed, this register wraps to zero.

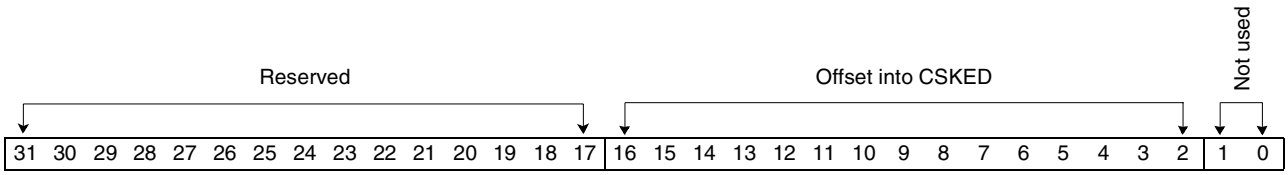
Length 32 bits

Type Read/Write

Address XXXX 12C8

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-2	Array Offset	These bits provide an offset into the CSKED cell staging array for accesses from the PCI bus. These bits provide access to the 16 K unique 19-bit locations in the array. Accessing the last location in the array will cause the address to wrap back around to the beginning of the array.
1-0	Not used	These bits are not implemented, they cannot be written and will always return ‘0’ when read.

3.12.17.9 CSKED Time Wheel Array Data

This register is used to access the array pointed to by the CSKED Time Wheel Array Pointer.

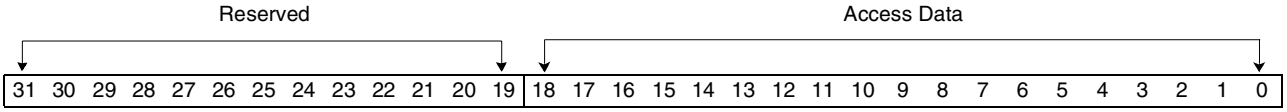
Length 32 bits

Type Read/Write

Address XXXX 12CC

Power On Reset Value

Restrictions Should be written for diagnostic use only. Initialize back to zeros when through testing.



Bit(s)	Name	Description
31-19	Reserved	Reserved.
18-0	Array Data	Array data.

3.12.17.10 CSKED LCD Cache Array Pointer

The CSKED LCD Cache Array contains the transmit portion of LCDs used by CSKED and SEGBF. It contains 160 32-bit words. It should only be written for diagnostic purposes to test the array. It will power up to all zeros and should be rewritten to zeros after the array has been tested. This register points to an offset in the LCD Cache array for accesses from the PCI bus. This register must be loaded with the correct offset before the desired data can be read from the LCD Cache Array Data register. This register will auto-increment after each access to the associated data register. When the last address is accessed, this register wraps to zero.

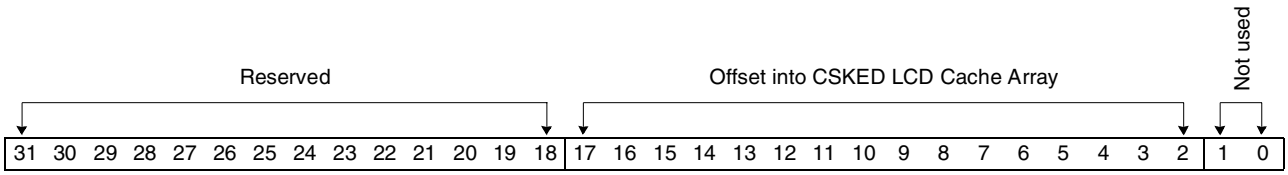
Length 32 bits

Type Read/Write

Address XXXX 1318

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-18	Reserved	Reserved.
17-2	Array Offset	These bits provide an offset into the CSKED cell staging array for accesses from the PCI bus. These bits provide access to the 160 unique 32-bit locations in the array. Accessing the last location in the array will cause the address to wrap back around to the beginning of the array.
1-0	Not used	These bits are not implemented. They cannot be written and will always return ‘0’ when read.

3.12.17.11 CSKED LCD Cache Array Data

This register is used to access the array pointed to by the CSKED LCD Cache Array Pointer.

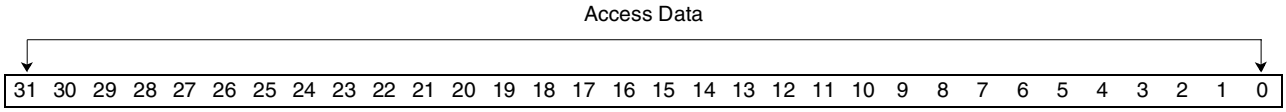
Length 32 bits

Type Read/Write

Address XXXX 131C

Power On Reset Value

Restrictions Should be written for diagnostic use only. Initialize back to zeros when through testing.



Bit(s)	Name	Description
31-0	Array Data	Array data.

3.12.17.12 CSKED State Machine Variables Register

This register contains the current state of the three main state machines in this entity.

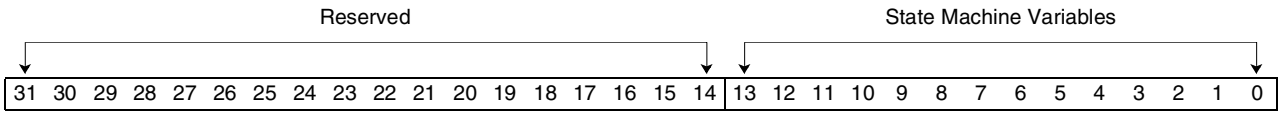
Length 32 bits

Type Read Only

Address XXXX 1258

Power On Reset Value x‘0000 0000’

Restrictions None

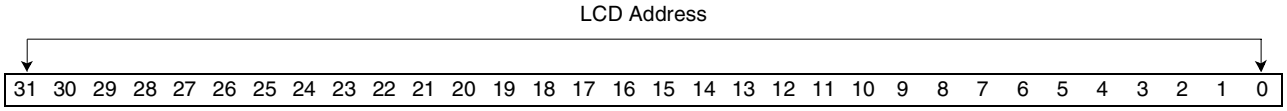


Bit(s)	Name	Description
31-14	Reserved	Reserved.
13-0	State Machine Information	Value of state machine variables.

3.12.17.13 LCD Cache LCD Address Registers

These registers contain the addresses of the LCDs that are currently available in the LCD cache.

Length	32 bits	
Type	Read Only	
Address	Line 0	XXXX 1330
	Line 1	XXXX 1334
	Line 2	XXXX 1338
	Line 3	XXXX 133C
	Line 4	XXXX 1340
	Line 5	XXXX 1344
	Line 6	XXXX 1348
	Line 7	XXXX 134C
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-0	LCD Address	The address of the LCD currently stored in the corresponding LCD cache line. Since LCDs are 128 byte aligned, bits 6-0 will always read ‘0000000’.

3.12.17.14 LCD Cache State Machine Variables Register

This register contains state information about the LCD cache.

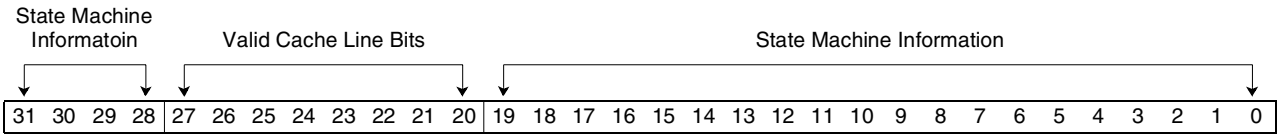
Length 32 bits

Type Read Only

Address XXXX 1320

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-28	State Machine Information	Value of state machine variables.
27-20	Valid Cache Line Bits	These bits indicate which of the LCD cache lines are valid. Bit 27 corresponds to line 7, bit 26 to line 6, etc.
19-0	State Machine Information	Value of state machine variables.

3.12.17.15 LCD Cache LRU State Register

This register contains information about the LRU status of the 8 lines of the LCD cache. Each nibble contains the encoded value of a cache line number. The highest nibble will indicate which cache line was least recently used while the lowest nibble will indicate which cache line was the most recently used.

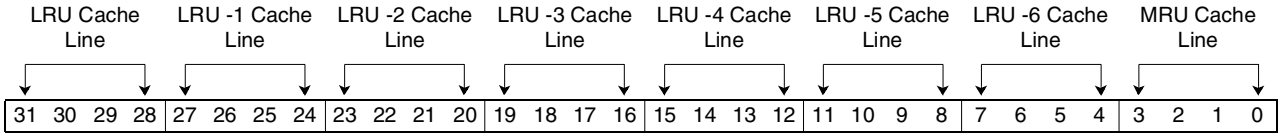
Length 32 bits

Type Read Only

Address XXXX 1324

Power On Reset Value x‘0000 0000’

Restrictions None

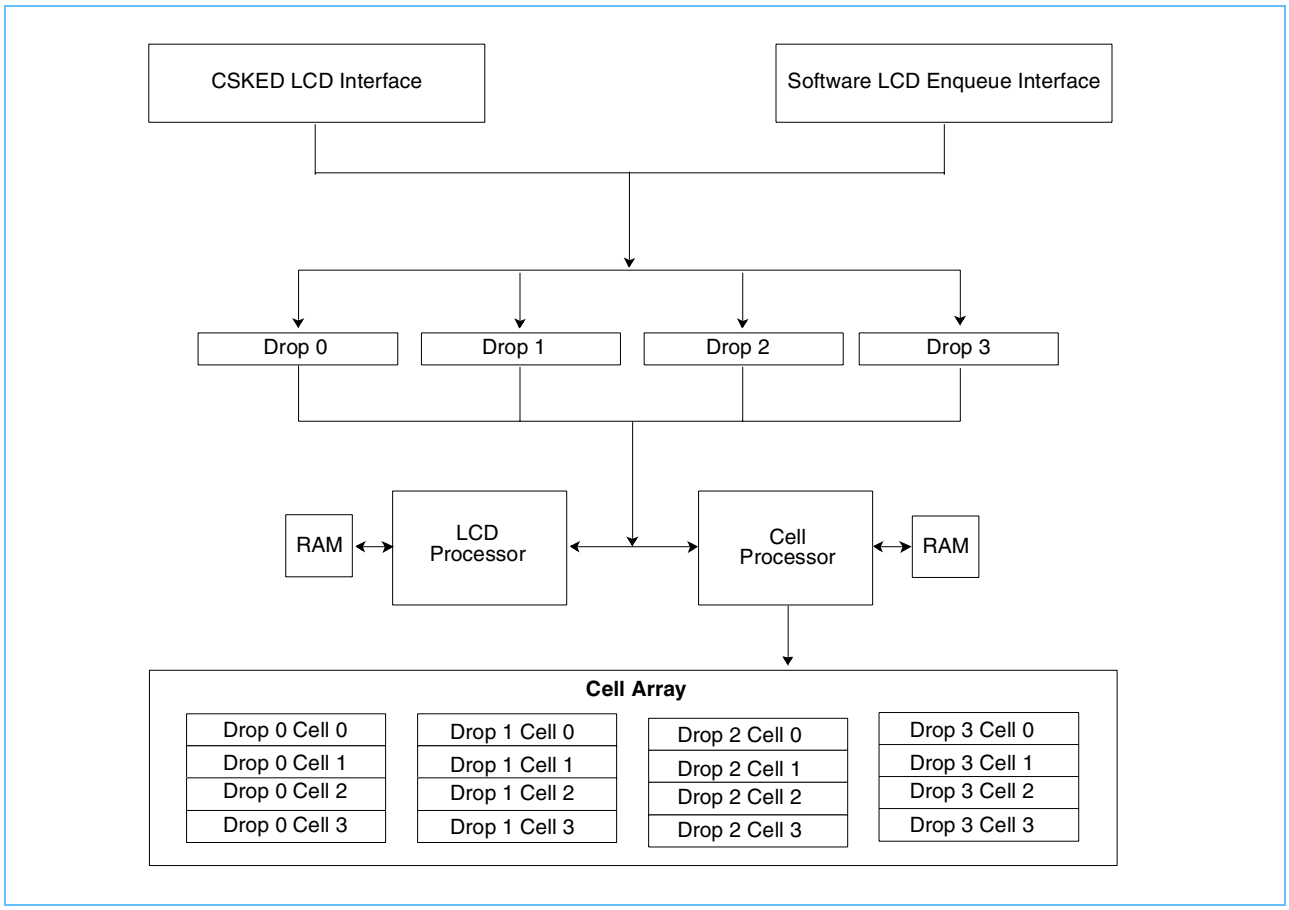


Bit(s)	Name	Description
31-28	LRU Cache Line	Least recently used LCD cache line.
27-24	LRU -1 Cache Line	LRU -1 cache line.
23-20	LRU -2 Cache Line	LRU - 2 cache line.
19-16	LRU -3 Cache Line	LRU - 3 cache line.
15-12	LRU - 4 Cache Line	LRU - 4 cache line.
11-8	LRU - 5 Cache Line	LRU - 5 cache line.
7-4	LRU - 6 Cache Line	LRU - 6 cache line.
3-0	MRU Cache Line	Most recently used cache line.

3.13 Transmit Buffer Segmentation (SEGBF)

The SEGBF logic consists of four input LCD address latches, two specialized processors and the associated ROM/RAM for each, a 16-cell array buffer, and various support logic. The input latches and cell buffers are logically divided into four different drops, with each drop consisting of an input latch and four cell buffers. Under normal operation (CSKED providing LCD), the drop is defined by the drop field in the transmit LCD. When an LCD is enqueued by software, data bits five and six of the enqueued address define with which drop the enqueued LCD is associated. The four logical drops in SEGBF can be mapped to any of the physical link level addresses via registers in LINKC (LINKC Map Transmit Ports to Configuration). The processors fetch instructions from ROM/RAM and handle normal segmentation activity such as LCD update operations and cell generation functions. The type of cell that is generated by the segmentation logic is determined by the initial instruction pointer that is contained in the LCD structure. For example, software can enqueue an LCD that has the initial instruction pointer field set for normal AAL5 cells, and SEGBF will generate a single AAL5 cell as a result of the enqueue operation. If, however, software enqueues an LCD that has the initial instruction pointer field set for POS-PHY operation, then SEGBF will continue to generate buffers to pass to the link level until all the data has been exhausted. For a more complete description of the segmentation entry points, refer to the seg_prc_Entry_point field in *7.3 Transmit LCD Data Structures* on page 678. After the buffers/cells are built in a 16-by-64 byte array, they are marked as available to the link level layer (LINKT) in the PNR. A simplified block diagram is shown below.

Figure 13: SEGBF Block Diagram



The sequence of events that happens when an AAL5 frame is enqueued to SEGBF is as follows:

1. An initial check is made to determine if there is space available in the cell buffer. If no space is available, processing stops for this drop until a cell buffer is freed by the link logic (LINKT).
2. When buffer space becomes available, the enqueued LCD address is requested from the transmit LCD cache (there are four entries in the LCD cache). The segmentation logic waits for a valid indication from the cache; at this time all LCD information is available to the segmentation logic on the LCD cache interface.
3. The initial instruction pointer (IP) is fetched from the LCD and loaded for both of the segmentation processors. Software controls what type of cells are generated by the segmentation logic by initializing this field in the LCD to the entry points defined for different types of cell generation. For a more complete description of the segmentation entry points, refer to the seg_prc_Entry_point field in *7.3 Transmit LCD Data Structures* on page 678.
4. Assuming an AAL5 entry point is setup in the LCD, the segmentation logic will first initiate a memory fetch of the data required to build the cell.
5. While the data fetch is in process, the segmentation processors will update various fields in the LCD including statistics and the next segmentation pointer. Cell construction will be started using the ATM header from the LCD.
6. When the payload data is available from memory, it is written to the cell buffer following the header.
7. If the segmentation logic determines that the current cell being assembled will be the last cell of this frame, the AAL5 trailer is appended to the cell buffer, with any unused bytes being padded with zeros.
8. If the current cell is not the last of the frame, the partial CRC is written back out to the LCD.
9. After the cell has been completed, it is marked as available to the link level logic.

3.13.1 SEGBF Software LCD Enqueue

This register provides a mechanism for software to transmit a single cell or a group of cells making up a buffer that can contain any user-defined data at any time. To cause a cell/buffer to be transmitted, the software must write the address of a valid LCD control block to this register. The segmentation hardware will then construct a cell to match the AAL type defined in the LCD control block, using the segmentation pointer contained in the LCD to fetch data and present this cell to the next lower level of hardware to transmit. This method of cell transmission bypasses the cell scheduler completely, so it is the responsibility of the software to ensure that peak and average rates are not violated. When the segmentation logic has completed building the cell/frame and queued it for transmission, the LCD address will be loaded into the software LCD complete register. This method of cell transmission is not designed for high performance and, as such, there is only a single level of queueing underneath the complete register. It is recommended that only a single software LCD be queued to the segmentation logic at any one time to prevent hanging the segmentation logic as it attempts to queue a complete software LCD to the complete queue.

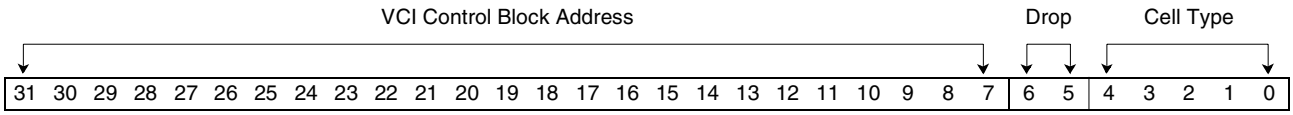
Length 32 bits

Type Read/Write

Address XXXX 1400

Power On Reset Value x‘0000 0000’

Restrictions Before enqueuing a VCI, software must ensure that the previous software enqueue has been handled by the hardware. This is accomplished by reading this register before an enqueue is attempted. If a value of ‘0’ is returned, the segmentation hardware is ready to accept an enqueue operation. If a non-zero value is returned, it will be the address of the previous VCI that was enqueued and this indicates that the segmentation hardware has not been able to enqueue the VCI to it’s internal VCI buffer segmentation queue. If this mechanism shows that this interface is busy and unable to accept new VCI addresses for any appreciable amount of time (tens of µs), it is likely that a condition exists which is preventing the hardware below the segmentation logic from accepting cells for transmission, and the segmentation logics input buffer is full. This mechanism also adds the restriction that a VCI control block should never exist at address ‘0’.



Bit(s)	Name	Description
31-7	VCI Control Block Address	These bits contain the upper 25 bits of the address of the VCI control block.
6-5	Drop	These bits define with which drop this enqueue operation will be associated.
4-0	Cell Type	These bits control what type of cell will be built by the segmentation logic. There are currently only two valid values for these bits. If these bits are all ‘0’, a normal cell as defined by the LCD will be built. If these bits have a value of ‘0x1F’, an ABR cell will be built using fields defined in the LCD.

3.13.2 SEGBF Control Register

This register provides a mechanism to control the various programmable features of SEGBF.

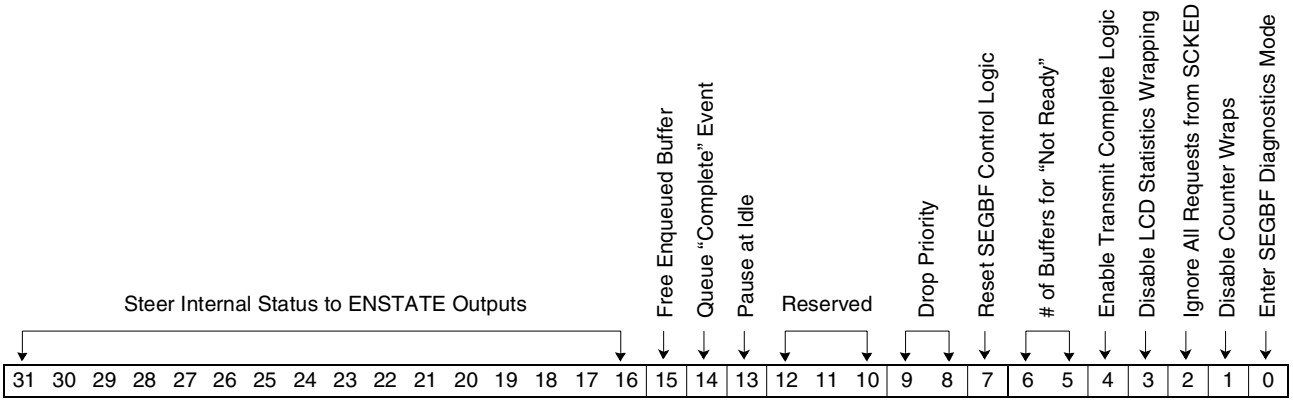
Length 32 bits

Type Clear/Set

Address XXXX 1408 and 140C

Power On Reset Value x‘9840 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Steer Internal Status to ENSTATE Outputs	These bits are used to steer internal SEGBF status to the ENSTATE outputs.
15	Free Enqueued Buffer	This bit, when set, will cause the segmentation processors to free a software enqueued buffer after the last cell has been generated.
14	Queue “Complete” Event	This bit, when set, will cause the segmentation processors to queue a transmit complete event after the last cell has been generated for a software enqueued frame.
13	Pause at Idle	This bit, when set, will cause the segmentation logic to pause when it reaches the idle state. Segmentation will not be continued until this bit has been reset. Care must be taken to leave this bit set for a very short duration so that segmentation throughput will not be adversely affected.
12-10	Reserved	Reserved.
9-8	Drop Priority	These two bits define the prioritization scheme used by the segmentation logic to determine for which drop to build a cell when running in frame mode. A value of ‘00’ will provide for equal priority among all drops: the drops will be processed in order from zero to three as long as data is available to segment and space is available in the cell buffer for the drop. A value of ‘01’ will provide descending priority from drop 0 to drop 3. If data exists and a cell buffer is available for drop 0, a drop 0 cell will always be built regardless of the situation on any other drops. In this mode, a cell will only be built on drop three if all other drops either have no data or no cell buffer available.
7	Reset SEGBF Control Logic	This bit, when set, will reset all control logic in the entity. After being set, this bit must be reset before the segmentation logic will function properly. This bit must remain set for at least one microsecond to reset the segmentation logic properly.

Bit(s)	Name	Description
6-5	Number of Buffers for “Not Ready”	These two bits define the number of cell buffers that can be filled on a given drop before a not ready condition is returned to the cell scheduler. This addresses latency issues caused by multiple cells waiting for transmission by the lower link level. A value of ‘00’ allows all four cell buffers to be used at any time; a value of ‘01’ allows one cell buffer to be used; a value of ‘10’ allows two cell buffers to be used, and a value of ‘11’ allows three buffers to be used.
4	Enable Transmit Complete Logic	This bit, when set, enables the transmit complete event modification logic in the segmentation processors. This logic will retrieve two bits from the xmit_comp_evnt_mod field in the LCD and logically OR them with bits eight down to seven of the buffer address being enqueued to RXQUE. This logic only functions when buffer addresses are being queued; it will not modify the event if LCD addresses are being enqueued. This also adds the restriction that all buffer addresses must start on a 512-byte boundary or greater.
3	Disable LCD Statistics Wrapping	This bit, when set, disables the LCD statistics wrap events.
2	Ignore All Requests from CSKED	This bit, when set, will cause all requests from the cell scheduler to be ignored. This allows complete program control of all cells being sent out on the external interface.
1	Disable Counter Wraps	This bit, when set, disables the programmable counter wrap events.
0	Enter SEGBF Diagnostics Mode	This bit, when set, causes the SEGBF entity to enter diagnostic mode. This bit must be set in order to access the internal array. When accessing the array, care must be taken that normal entity reads and writes of the array are not happening at the same time or the results will be indeterminate.

3.13.3 SEGBF Status Register

This register provides feedback to the user on the current status of SEGBF.

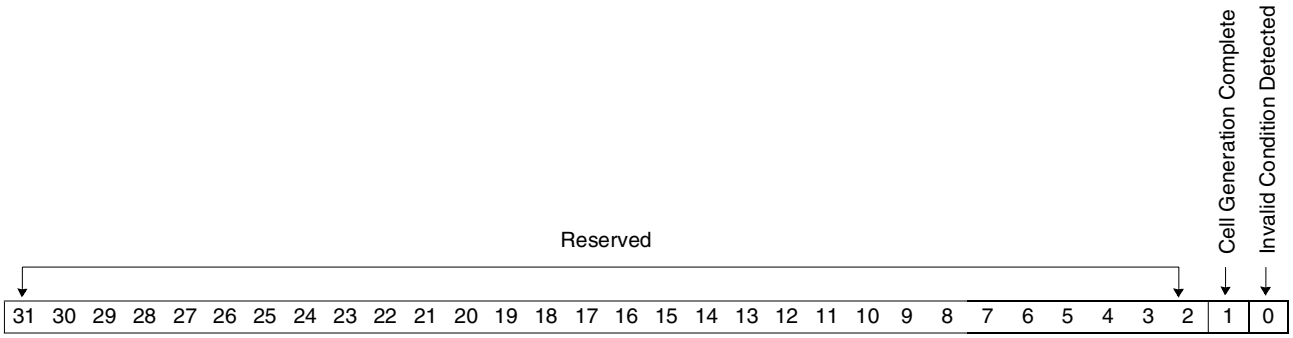
Length 32 bits

Type Clear/Set

Address XXXX 1410 and 1414

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-2	Reserved	Reserved.
1	Cell Generation Complete	This bit, when set, indicates that the segmentation logic has completed cell generation for an LCD that was enqueued by the software to the software LCD enqueue register.
0	Invalid Condition Detected	This bit, when set, indicates that the segmentation logic has detected an invalid condition in one of the LCDs that it was processing. The address of the LCD in error is contained in the Invalid LCD register. Any invalid LCDs detected are not processed further by the segmentation logic, so the program must do something to clear this condition.

3.13.4 SEGBF Invalid LCD Register

This register provides feedback to the program when the segmentation logic detects an invalid LCD. If multiple invalid LCDs are being processed, this register will contain the address of the last one that was processed by the segmentation logic. There are several invalid LCD situations for which the segmentation logic checks. The first is the LCD address not being on the correct boundary. For example, if the chip is configured to have all LCDs on 128-byte boundaries and an LCD is encountered that is not on a 128-byte boundary it is an invalid LCD situation. Another invalid condition is when the transmit length configured in the LCD plus the offset in the LCD when added together exceed the maximum overall packet size configured in the chip. It is up to the program to determine which of the possible conditions caused the error to be reported.

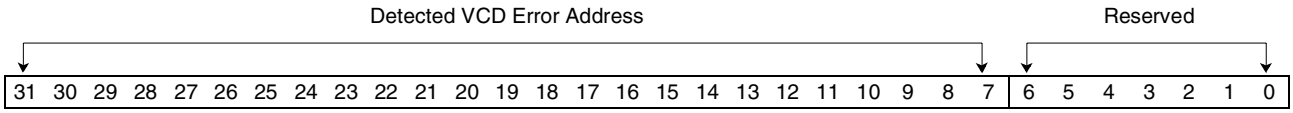
Length 32 bits

Type Read/Write

Address XXXX 1418

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Detected VCD Error Address	These bits contain the 32-bit address of the LCD detected to be in error.
6-0	Reserved	Reserved. Always read as ‘0’.

3.13.5 SEGBF Software LCD Complete

This register provides feedback to the program when the segmentation logic completes cell generation for an LCD that was enqueued by the software. After the segmentation logic has updated the LCD, the address of the LCD is copied into this register providing any previous LCD addresses written to this register have been read by the software. If multiple software queued LCDs are outstanding to the segmentation logic at any time, the segmentation process can be delayed when multiple software enqueued LCDs complete without the software getting a chance to read the LCD addresses from this register. To guarantee that the segmentation logic never has to wait for the software to read this register, it is recommended that only one software LCD be enqueued at any one time.

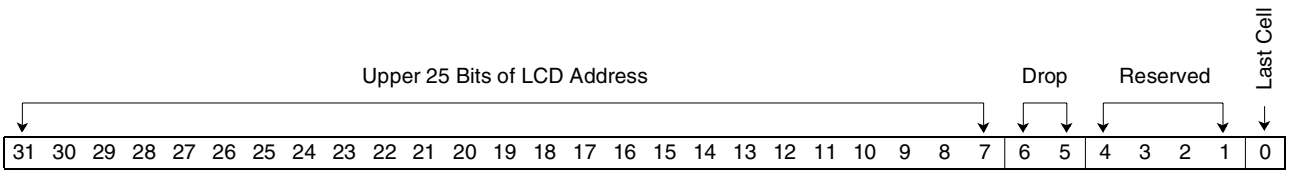
Length 32 bits

Type Read/Write

Address XXXX 141C

Power On Reset Value x‘0000 0000’

Restrictions Bits 4-1 are not implemented and will always return to ‘0’. To maintain future compatibility, ‘0’s should be written to these bits.



Bit(s)	Name	Description
31-7	Upper 25 Bits of LCD Address	These bits contain the upper 25 bits of the LCD address that the segmentation logic has finished processing.
6-5	Drop	These bits indicate the drop on which the cell was sent.
4-1	Reserved	Reserved. These bits will read back as ‘0’.
0	Last Cell	This bit will be set when the cell that was built was the last cell of a frame and reset if the cell that was built was not the last cell of a frame.

3.13.6 SEGBF Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *SEGBF Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt from SEGBF to INTST if the condition is detected.

Length 32 bits

Type Clear/Set

Address XXXX 1420 and 1424

Power On Reset Value x'0000 0000'

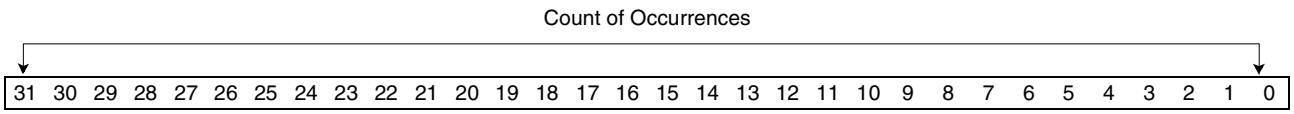
Restrictions None

Bit(s)	Name	Description
31-2	Reserved	Reserved.
1-0	Interrupt Enables	When one of these bits is on and the corresponding bit in the *SEGBF Status Register* on page 286 is on, an interrupt is generated.

3.13.7 SEGBF Programmable Counters

This register provides the user with feedback on the number of times that a particular event or condition has occurred in the segmentation logic. The event or condition that causes this counter to increment is defined by the associated SEGBF Programmable Counter Source Specification register. When the counter wraps, an event is generated.

Length	32 bits	
Type	Read/Write	
Address	Counter 0	XXXX 1430
	Counter 1	XXXX 1434
	Counter 2	XXXX 1438
	Counter 3	XXXX 143C
	Counter 4	XXXX 1440
	Counter 5	XXXX 1444
	Counter 6	XXXX 1448
	Counter 7	XXXX 144C
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-0	Event Count	These bits contain a count of the occurrences of the desired event or condition.

3.13.8 SEGBF Transmit LCD Size

This register should be loaded with the number of 8-byte words that are needed for the maximum-sized LCD that will be setup by software. Refer to the previous section describing LCD layout to determine the number of words required to support the different modes. The minimum value is six. This is the correct value when running only AAL5 mode; it includes three words of scheduling information, two words shared between CSKED and SEGBF, and one word for SEGBF to maintain statistics. Setting this register to a value that is too small will likely cause the chip to function improperly. Setting this register to a value that is too large will adversely affect performance.

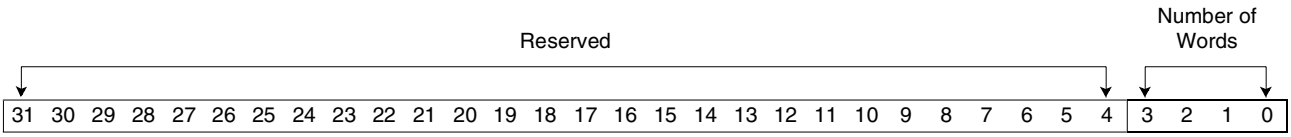
Length 32 bits

Type Read/Write

Address XXXX 1488

Power On Reset Value x‘0000 0006’ (This is the correct value when running AAL5 with statistics.)

Restrictions Minimum is x‘6’, maximum is x‘A’



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Transmit LCD Size	These bits contain the number of 8-byte words in the LCD to be used by the transmit logic.

3.13.9 SEGBF Cell Queue Status

This register indicates the number of cells queued up for transmission over the media. SEGBF can have a maximum of 16 cells queued up for transmission: four cells on each of four drops. When a bit is set to '1', the corresponding cell buffer contains a cell that has not been completely processed by the link logic.

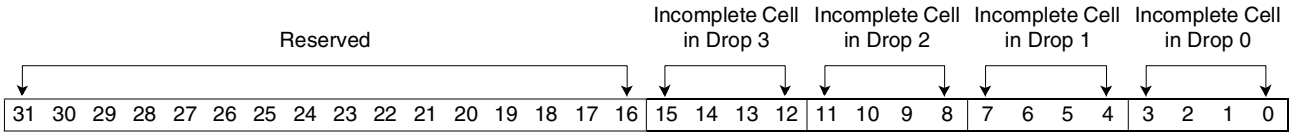
Length 32 bits

Type Read Only

Address XXXX 148C

Power On Reset Value x'0000 0000'

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-12	Cells Pending on Drop 3	These bits indicate which cell buffers contain cells that have not been processed by the link level for drop 3.
11-8	Cells Pending on Drop 2	These bits indicate which cell buffers contain cells that have not been processed by the link level for drop 2.
7-4	Cells Pending on Drop 1	These bits indicate which cell buffers contain cells that have not been processed by the link level for drop 1.
3-0	Cells Pending on Drop 0	These bits indicate which cell buffers contain cells that have not been processed by the link level for drop 0.

3.13.10 SEGBF Processor 1 Control/Status

Reading this register provides feedback to the user on the current state of segmentation processor 1. Writing the appropriate bits in this register causes processor 1 to begin executing at a new location specified in the data that was written.

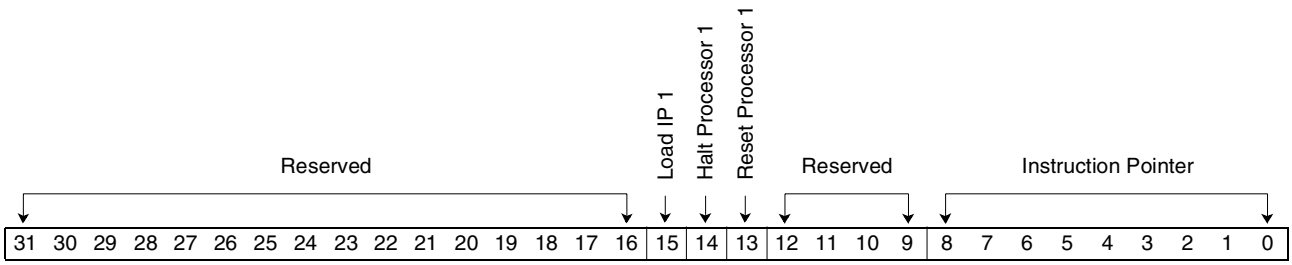
Length 32 bits

Type Read/Write

Address XXXX 14A0

Power On Reset Value x‘0000 C000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15	Load IP 1	Writing ‘0’ to this bit causes the instruction pointer (IP) for processor 1 to be loaded with the data in bits 8-0. This bit will immediately be set back to ‘1’ after the IP load completes.
14	Halt Processor 1	Writing ‘0’ to this bit halts processor 1. Writing ‘1’ makes the processor fetch and execute instructions.
13	Reset Processor 1	Setting this bit to ‘1’ resets processor 1.
12-9	Reserved	Reserved.
8-0	Instruction Pointer	When written, these 9 bits contain the new IP for processor 1. When read, these bits reflect the current IP for processor 1.

3.13.11 SEGBF Processor 2 Control/Status

Reading this register provides feedback to the user on the current state of segmentation processor 2. Writing the appropriate bits in this register causes processor 2 to begin executing at a new location specified in the data that was written.

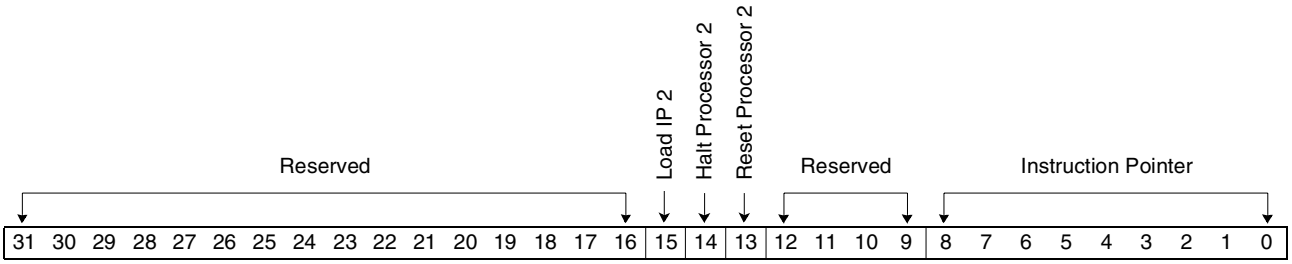
Length 32 bits

Type Read/Write

Address XXXX 14A4

Power On Reset Value x‘0000 C000’

Restrictions None

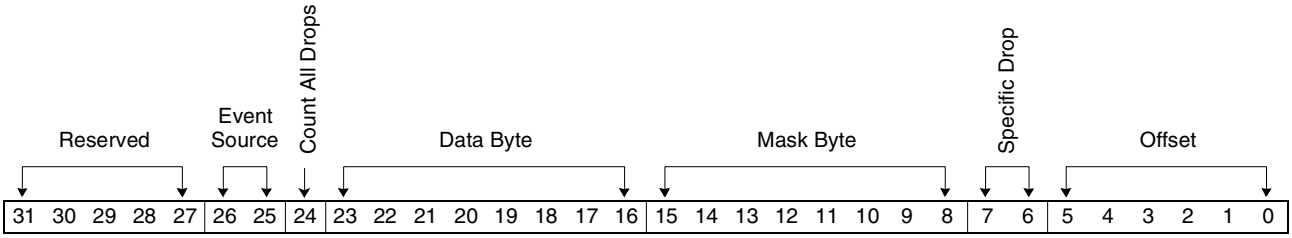


Bit(s)	Name	Description
31-16	Reserved	Reserved.
15	Load IP 2	Writing a ‘1’ to this bit will cause the instruction pointer (IP) for processor 2 to be loaded with the data in bits 8-0. This bit will immediately be set back to a ‘1’ after the IP load completes.
14	Halt Processor 2	Writing a ‘0’ to this bit will halt processor 2; writing a ‘1’ will make the processor fetch and execute instructions.
13	Reset Processor 2	Setting this bit to a ‘1’ will reset processor 2.
12-9	Reserved	Reserved.
8-0	Instruction Pointer	When written, these nine bits contain the new IP for processor 2. When read, these bits reflect the current IP for processor 2.

3.13.12 SEGBF Programmable Counter Source Specification

This register determines what event or condition will cause the associated counter to increment.

Length	32 bits	
Type	Read/Write	
Address	Counter 0	XXXX 14B0
	Counter 1	XXXX 14B4
	Counter 2	XXXX 14B8
	Counter 3	XXXX 14BC
	Counter 4	XXXX 1450
	Counter 5	XXXX 1454
	Counter 6	XXXX 1458
	Counter 7	XXXX 145C
Power On Reset Value	Counter 0	x‘0000 0803’
	Counter 1	x‘0000 0903’
	Counter 2	x‘0008 0803’
	Counter 3	x‘0002 0203’
	Counter 4	x‘0000 0000’
	Counter 5	x‘0000 0000’
	Counter 6	x‘0000 0000’
	Counter 7	x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-27	Reserved	Reserved.
26-25	Event Source	These bits select the source of the event to be counted. 00 Selects the cell events that are further defined in bits 23-0 of this register. 01 Selects the number of bytes transmitted on a given drop. 10 Selects the number of frames transmitted on a given drop. The drop is selected by bits seven and six, or all drops can be included by setting bit 24.
24	Count All Drops	This bit, when set, causes the counter to count the specified event for all drops, not just the drop specified in bits seven and six.
23-16	Data Byte	These bits define the data byte that is compared to the result of logically ANDing the data byte being written to the cell array at the offset specified in bits 5-0 with the mask in bits 15-8. If there is an exact match, the counter will increment.
15-8	Mask Byte	These bits define the mask byte to be logically ANDed with the data byte being written to the cell array.
7-6	Specific Drop	These bits determine with which drop this counter is associated.
5-0	Offset	These bits define a byte offset into the cell being built in the segmentation cell array. Zero corresponds to the first byte in the cell and 63 corresponds to the last byte in the cell. When the segmentation logic copies a byte of data into the cell array at this offset, the logic compares the byte defined in bits 23-16 to the logical AND of the data being written and the mask defined in bits 15-8 of this register. If an exact match is detected, the counter will be incremented.

3.13.13 SEGBF Cell Staging Array Pointer

This register points to an offset in the SEGBF cell staging array for accesses from the PCI bus. This register must be loaded with the correct offset before the desired data can be read from the SEGBF Cell Staging Array Data Register. This register will auto-increment after each access to the associated data register. When the last address is accessed, this register wraps to zero.

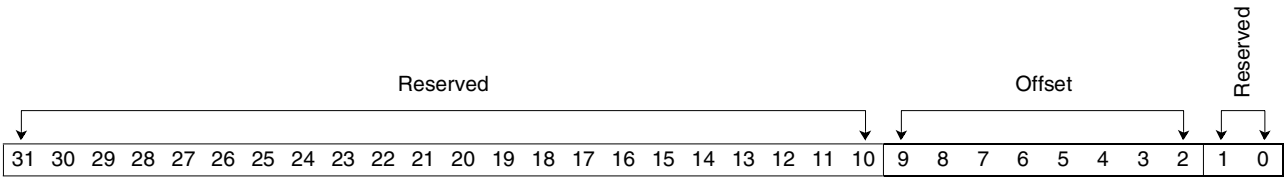
Length 32 bits

Type Read/Write

Address XXXX 14C0

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-10	Reserved	Reserved.
9-2	Offset	These bits provide an offset into the SEGBF cell staging array for accesses from the PCI bus. These bits provide access to the 256 unique four-byte locations in the array. Accessing the last location in the array will cause the address to wrap back around to the beginning of the array.
1-0	Reserved	Reserved. These bits are not implemented, they cannot be written and will always return ‘0’ when read.

3.13.14 SEGBF Cell Staging Array Data

This array is divided into 16 64-byte buffers used to assemble cells that are ready for transmission on the physical interface.

Length 32 bits

Type Read/Write

Address XXXX 14C4

Power On Reset Value Undefined

Restrictions This array can only be accessed when the diagnostic mode bit in the control register is set. Accesses attempted when not in diagnostic mode will return x‘BADD BADD’.

3.13.15 SEGBF Instruction SRAM Pointer

This register points to an offset in the SEGBF SRAM that is used to store processor instructions. This register must be loaded with the correct offset before the desired data can be read/written from/to the SEGBF instruction SRAM data register. This register will auto-increment after each access to the associated data register. When the last address is accessed, this register wraps to zero. The first 256 locations in the array should be loaded with the instructions for processor 1, and the second 256 locations should be loaded with the instructions for processor 2.

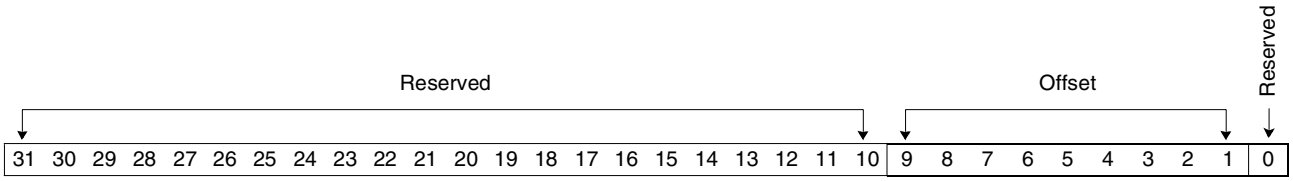
Length 32 bits

Type Read/Write

Address XXXX 14C8

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-10	Reserved	Reserved.
9-1	Offset	These bits provide an offset into the SEGBF instruction SRAM for accesses from the PCI bus. These bits provide access to the 512 unique two-byte locations in the array. Accessing the last location in the array will cause the address to wrap back around to the beginning of the array.
0	Reserved	Reserved. This bit is not implemented; it cannot be written and will always return ‘0’ when read.

3.13.16 SEGBF Instruction SRAM Data

This register address can be used to read/write the instruction data that is needed by the segmentation processors. All instructions must be written before the processors can be brought out of the halt state.

Length 32 bits

Type Read/Write

Address XXXX 14CC

Power On Reset Value Undefined

Restrictions This array can only be accessed when the processors are in the halt state. Reads attempted when the processor is in run mode will return invalid data. Writes attempted when the processor is in run mode will be ignored.

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Instruction Data	SEGBF Processor Instructions.

3.13.17 SEGBF MPEG-2 PCR Increment Register

Each tick of the time base will add the contents of this register to the MPEG PCR Reference Register. This register contains a fixed point number with 27 bits of fraction and five bits of units. This means that the external reference clock can range in speed from 22.5 Khz to the maximum speed of this entity which is 66 MHz. Assuming that the entity will run with a 50 Mhz clock, the conversion to 720 Khz can be done with an accuracy of 1.1 parts in two million. (A clock of 19.4 Mhz will give a conversion accuracy of one part in 4.9 million.) If the input clock is 19.4 Mhz, the value to put in the increment register is (720,000 / 19,400,000) * 2^{27} or 4,981,277. If the input clock is 33 Mhz, the value to put in the increment register is (720,000 / 16,666,666) * 2^{27} or 5,798,206.

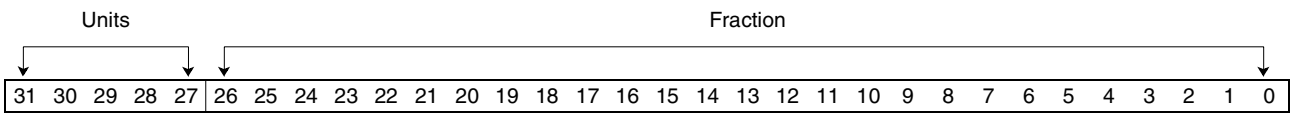
Length 32 bits

Type Read/Write

Address XXXX 1468

Power On Reset Value x‘002C 3C9F’ (33 Mhz)

Restrictions None



Bit(s)	Name	Description
31-27	Integer Increment Value	These bits contain the whole part of the increment value.
26-0	Fractional Increment Value	These bits contain the fractional part of the increment value.

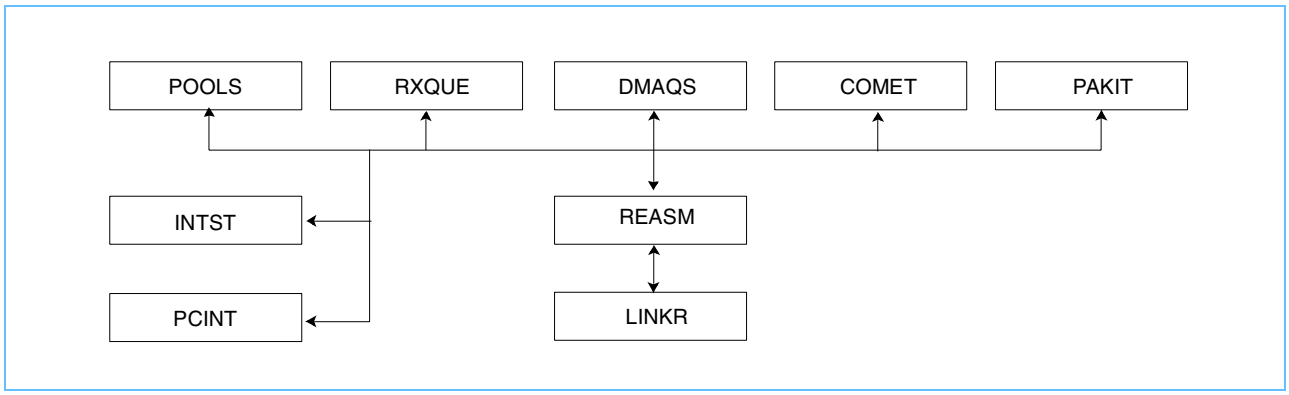
3.14 Cell/Packet Reassembly (REASM)

REASM is the top level receive entity that encapsulates all of the receive sub-entities.

Note: The receive portion of the PNR is very different from previous versions of the processor. REASM no longer does HEC correction or detection, since everything to which it interfaces already performs this function.

The following figure shows how REASM interacts with the other entities.

Figure 14: REASM Entity Interfaces



REASM is made up of a number of sub-entities that provide the overall receive functionality. REASM contains the following sub-entities:

RXBUF Provides receive cell/packet buffering between LINKC and REASM. Also defines the port configurations and mappings.

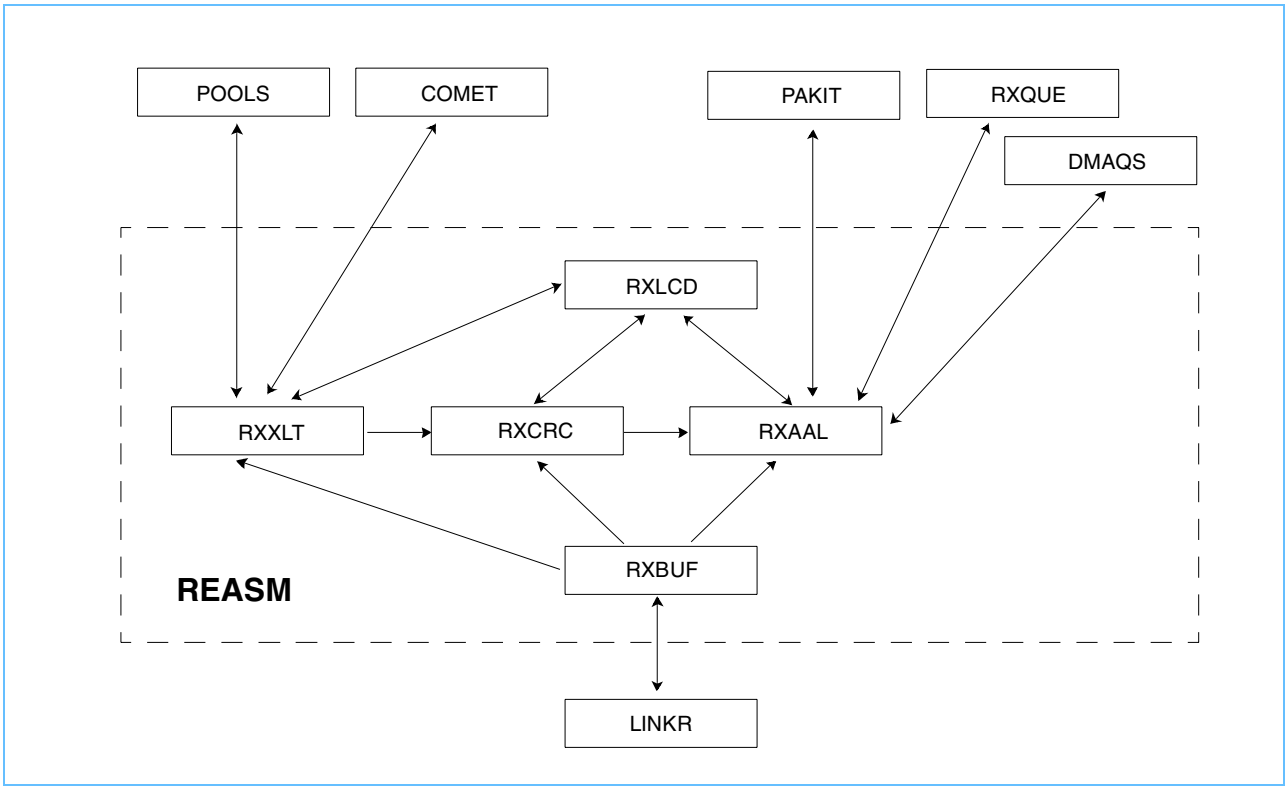
RXXLT Provides general LCD translation facilities.

RXCRC Provides CRC facilities.

RXAAL Performs the Cell and Packet Reassembly functions including AAL processing and all Cell and Packet Post-Processing functions.

RXLCD Provides RX LCD caching for the REASM sub-entities.

Figure 15: REASM Sub-Entity Block Diagram



RXXLT, RXCRC, and RXAAL form a cell processing pipeline. Each stage is allowed up to a cell time to process the cell it is currently working on. This means each cell has the potential to have a three-cell time latency through the REASM entity. The overall performance should be at its maximum since a single cell completes processing every cell time. The stages are allowed to run faster if there is no blocking condition. The only blocking condition is the latency of memory accesses and the total length of the nano-program that needs to run.

The following sections provide a brief description of each sub-entity and the function it provides.

3.14.1 Miscellaneous Reassembly Functions

3.14.1.1 ATM OAM Cell Processing

When processing an ATM data stream, OAM cell processing may be necessary. This function is enabled when bits 11-8 of the *REASM Reassembly Modes Register* are set, and it can be optionally enabled on a per port basis. As cells arrive for processing, the nanocode works together with some dedicated logic to discriminate among different types of OAM cell traffic. Each type that is discriminated produces a different event when traffic is surfaced to a receive queue. In *Table 18: OAM Cell Processing and Handling*, the first column lists the types that are discriminated, and the second column lists the event that is produced when traffic is surfaced to a receive queue.

The RXCRC and RXAAL nanocode understand and process OAM traffic in different ways when enabled. Control bits in the receive LCD allow the user to specify on a per connection basis how the OAM traffic should be handled: with either a routed connection or a terminated one.

- A routed connection is a raw LCD that is fast forwarded, including raw mode with early packet discard. When OAM traffic is processed on a routed connection, the OAM traffic can be fast forwarded or dropped based on the discrimination configuration bits in the receive LCD. A mask value of ‘0’ fast forwards the cell, and a mask value of ‘1’ drops the cell.
- A terminated connection is any connection that terminates either cells or packets, including AAL5 and packet LCDs that are fast forwarded (because they are terminated before they are fast forwarded). When OAM traffic is processed on a terminated connection, the OAM traffic can be terminated or dropped based on the discrimination configuration bits in the receive LCD. A mask value of ‘0’ terminates the cell, and a mask value of ‘1’ drops the cell.

Whenever possible, a mask bit specific to the sub-type is used. For example, an F5 Segment Pm Cell will use the “Segment Pm Cell” mask bit. If one of the sub-types does not match, then a basic type mask bit is used (such as F4 End to End). There is a 16 bit OAM mask field in the receive LCD. The mask bit assignments are listed in the third column of Table 18.

When an OAM cell is processed, the configuration information from the *RXAAL OAM LCD Information Register* is used to make reassembly decisions such as which buffer pool or receive queue to use. The fourth column of Table 18 contains the event that is generated for each type of OAM cell.

Table 18: OAM Cell Processing and Handling

Type of OAM Cell	Configuration Information from the *RXAAL OAM LCD Information Register*	Bit in the oamMask Field of the Receive LCD (see *Receive LCD Data Structure and Modes* on page 692)	Event Produced when traffic is surfaced to a receive queue
Reserved	Reserved	15	
F4 Segment	VCI = 0003	14	x‘48
F4 End to End	VCI = 0004	13	x‘49’
F5 Segment	Not F4 and PTI field = 100	12	x‘4A’
F5 End To End	Not F4 and PTI field = 100	11	x‘4B’
Rm Forward Cell	PTI = 110 and DIR = 0	10	x‘4C’
Rm Backward Cell	PTI = 110 and DIR = 1	9	x‘4D’

Table 18: OAM Cell Processing and Handling (Continued)

Type of OAM Cell	Configuration Information from the *RXAAL OAM LCD Information Register*	Bit in the oamMask Field of the Receive LCD (see *Receive LCD Data Structure and Modes* on page 692)	Event Produced when traffic is surfaced to a receive queue
Pti Reserved Cell	PTI field = 111	8	x‘4E’
End to End Alarm	End to End and OAM type = 0001 func = 0000 or 0001	7	x‘4F’
Segment Alarm	Segment and OAM type = 0001 func = 0000 or 0001	6	x‘4F’
End to End Loopback	End to End and OAM type = 0001 func = 1000	5	x‘4F’
Segment Loopback	Segment and OAM type = 0001 func = 1000	4	x‘4F’
End to End Pm Cell	End to End and OAM type = 0010	3	x‘4F’
Segment Pm Cell	Segment and OAM type = 0010	2	x‘4F’
End to End Activate/Deactivate Cell	End to End and OAM type = 1000	1	x‘4F’
Segment Activate/Deactivate Cell	Segment and OAM type = 1000	0	x‘4F’

3.14.1.2 TCP/IP Receive Checksum Verification

When enabled, the PNR is able to perform verification of the IP header checksum and the associated protocol checksum for the user. The final checksum status is raised to the user in the packet header flags. This function is accomplished by the RXCRC entity using the CRC nano-program.

To enable and use the function, two things must be done:

- TCP/IP checksum function must be enabled in the *REASM Mode Register*. This enables the overall function and includes the checksum state words in the receive portion of the LCD.
- Specify a frame type in the frameType field of the receive LCD. This field specifies an entry point into the checksum verification nano-code. The entry point points to a piece of code that understands how to locate the IP header based on the current frame type. For example, a connection might be native IP over ATM or LAN Emulation.

  Note: Other frame types can be added if needed.

Once properly enabled, TCP/IP checksums are verified as packets arrive. The status is raised to the user in the packet header using four bits of status (two bits for IP and two bits for protocol). The format and meanings of the bits are specified in section *7.1: Packet Header* on page 673. For connections that have mixed traffic, the checksum operation is only run on packets that are recognized as TCP/IP. For example, on a LANE ETH connection packets of different protocols can be interleaved.

3.14.1.3 Scatter/Cut Through Receive Processing

The scatter/cut through support is very versatile and easy to use. Scatter typically refers to scattering pages from a contiguous PNR buffer into multiple non-contiguous host pages. Cut through refers to moving contiguous data from PNR buffers into contiguous storage in host memory. The functions are similar, and the terms

scatter and cut through may be interchanged in the following text since cut through is really a special case of scatter. The correct term is used when context requires it.

The scatter processing is performed by RXAAL along with RXQUE and DMAQS. The following items need to be set up:

- Set up DMAQS.
- Set up RXQUE. Each queue used should have the proper event size selected, the direction set correctly, and timestamps and BCACH advice disabled.
- Place page buffers or descriptors on the configured receive queues.
- Set the scatter configurations in the RXAAL Scatter/Cut Through Info Registers.
- Set the scatter flags in the RXAAL Scatter/Cut Through Flag Registers.
- Set the ppMode field for each LCD that uses scatter to do scatter.
- Select a scatter configuration for each connection by setting the cutThruSel field in the receive LCD.

Once set up, the scatter mechanism is performed by RXAAL for the user. There is user intervention required to process the packets when the scatter is complete, and for page recovery in error scenarios.

There are many options when setting up scatter, and the selection of the type of scatter processing to perform depends on the user's environment. The basic scatter mechanism will be described followed by a discussion of the different options that can be used.

When packets are received and scattered, the following structure shows the main components of the received packet:

Figure 16: General Layout of a Received Packet in Scatter Mode

```
struct ScatterRxPacket {
     packetHeader;                          // Charm packet header
     dmaList;                               // Scatter dma list
     padbytes;                              // Pad out to receive offset from lcd
     packetData;                            // Actual receive packet
  };
```

The DMA list is maintained immediately after the PNR packet header, and before the receive packet data. For this reason, the user should allocate enough space between the packet header and the packet data to accommodate a maximum-sized DMA list based on the maximum number of pages that could be DMAed. The rxOffset field in the receive LCD is where this offset is specified. The maximum receive offset is 256 bytes, which is specified with an rxOffset value of '0'. The following is the layout of the DMA list:

Figure 17: General Layout of a Scatter DMA List

```
struct dmaList {
     bit16  numHeadbytes;                  // number of bytes included with header dma
     bit16  numTailbytes;                  // number of bytes in last dma page

     bit1   deqLocked;                     // error status
     bit1   deqInvalid;                    // "
     bit1   headerTruncated;               // "
     bit1   badDmaList;                    // "
     bit4   DeqLockedQueueNum;             // "
     bit16  reserved;
     bit2   cutThruSel;                    // copy of cutThruSel used from receive lcd
     bit6   numPages;                      // number of page entries that follow (max=63)

     bit32  pageList[N];                   // Actual dma descriptors or page addresses
                                           // Note: each entry can be 32, 64, or 128
                                           // bits wide
  };
```

The first eight bytes are always present and are filled in when the packet is complete or when an error occurs. The actual page list is filled in as the data is DMAed. The first location is initially skipped and is filled in later when the header is DMAed. The second and subsequent entries are filled as each page is DMAed. Each page list entry contains either physical page addresses, PNR-based DMA descriptor addresses, or user data. Whether a physical page address or DMA descriptor address is present depends on the cut through configuration. From here on, the terms “page address” and “DMA descriptor” are used interchangeably as either is valid based on the configuration, but the correct term is used when the context requires it.

A page list entry can contain one or two pieces of information. Each page list entry can be 32, 64, or 128 bits long. If using 32 bit addresses, then the entry is 32 or 64 bits. If using 64-bit addresses, then the entry is 64 or 128 bits. The first piece is always the page address or the DMA descriptor address. Each cut through configuration allows the user to specify an optional second dequeue operation from the receive queue being used. This allows the user to place user information associated with the particular page address in the receive queue and the page list. Thus, the corresponding virtual address of a page could be surfaced along with the physical page address. It is very important to enqueue information to the receive queue in the proper order if using this mode. The physical page address is first, followed by the user information.

As the receive packet data is being received, it is DMAed as soon as a page crossing occurs if there is a DMA descriptor available on the receive queue being used. If no descriptor is available, then no DMA takes place until the next receive cell is received, at which time the receive queue availability is checked again. This catch-up process continues until the packet is complete. When the packet is complete, all DMAs are scheduled if page addresses are available. If a page address is not available, then a “no DMA descriptor available” is surfaced to the user so the packet can be used and the DMA list recovered.

As each data page is DMAed to the user, a DMA descriptor is formed and enqueued to the DMAQS DMA queue specified in the cut through configuration. The DMA descriptor is formed based on if page addresses or DMA descriptor are provided on the receive queue being used. If PNR-based DMA descriptors are being used, then the receive queue contains DMA descriptor chains where the low order bits of the DMA descriptor address specify how many descriptors are in the chain. Typically, this chain length is one, but more can be used. The first descriptor in the chain provides the destination address (page address) which is filled in by the user. The source address, the length, and the flags are filled in by the PNR for the first descriptor in the chain. The source address is filled in with the beginning address of the page within the current receive buffer. The length is filled in with either the page size (if a full page is present) or the number of bytes in the last page for the last page. The flags are filled in using the flags from the appropriate RXAAL - Scatter/Cut Through Flag

Registers. If physical page addresses are contained in the receive queue, then a single DMA descriptor is formed by DMAQS directly in DMA queue storage using the page address and the same information that would have been filled into the DMA descriptor. Generally, using page addresses performs better but is less versatile. Normally no DMA event is generated in the flags when pages are DMAed.

When the last cell of a packet is received, and all the data pages have been DMAed, the packet header and DMA list are updated and DMAed into a header buffer. The mechanism and configuration of the header buffer is similar to the pages, but separate configuration is usually necessary for correct functionality. For example, different flags are normally used in order to get an event for the header DMA so the user can process the packet. The header DMA normally frees the PNR buffer; another difference is the page (or buffer) size used for headers is normally different than the normal page size. Some of the optional features described later also drive having different configuration for the header DMAs.

Once the user gets the event for the header DMA, the user processes the received packet using the DMA list and the packet header. Once the packet has been processed, the pages or descriptors need to be returned to the proper receive queue when the pages can be reused, thus completing the scatter processing.

There are several ways of getting that important event to start the receive processing. Usually the event is generated when the last header DMA is complete. If DMA descriptors are being used, then there are two choices. First, the normal DMA flag that generates an event can be used. This generates an event with the DMA descriptor address in the significant bits. While this works and may be desirable in some environments, the DMA descriptor needs to be read in order to get access to the host header buffer address. The second way to generate an event when using descriptors is to provide a second DMA descriptor in the DMA descriptor chain that enqueues the header buffer address and a user-defined event in the lower order bits. Generating an event in this manner provides the user with the buffer address; the header DMA descriptor address is available in the header buffer as part of the DMA list.

When using page addresses, the event source in the cut through configuration should be set to use the destination address as the event data. When this is done, the event data contains the header buffer address as in the second case above.

Error Recovery

There are two types of error that need to be handled. First, if there is no error on the receive packet and a page address was not available, then the packet is surfaced to the user with a “no DMA descriptor available” event in the event type field and the PNR buffer address in the event information field. The user has a choice at this point. The packet is good so it can be used or freed by the user. In either case, the DMA list in the packet header must be recovered. So if the DMA list in the header is not used, it should be recovered by returning it to the proper receive queues. The event surfaced specifies which type of page address failed so the user can parse the DMA list properly. The event will specify whether a normal page descriptor, optional header descriptor, or packet header descriptor was received. The same descriptor recovery must be performed when an error event is surfaced (that is, CRC error). When there is an error event, no packet header DMA is performed so no packet header descriptor is in the DMA list.

Scatter Options

Most of the optional scatter features have to do with the header bytes and how the header DMA is performed. The numHeadbytes field in the DMA header specifies the number of header bytes that are available. The location of the header bytes in the DMA buffers can be configured. The default is that they are kept with the packet header and DMA list in the packet header buffer. For this case, the user should be sure the packet header buffer size is large enough to contain all of this data.

Alternatively, the header bytes can be placed in a separate buffer. To do this, split header mode should be enabled in the cut through configuration. This buffer is referred to as the optional header page and uses its own page size and receive queue to allow for better storage utilization. When enabled, the second entry in the DMA list becomes the optional header page entry, and should be treated accordingly for page recovery. In split header mode, the header bytes are DMAed as soon as they are all received. This mode is useful if the user environment requires the header bytes to be in a separate buffer from the packet header and DMA list.

Another optional feature is to DMA the header only. This feature is enabled in the cut through configuration. When enabled, only the packet header, DMA list, and header bytes are DMAed. Either a single DMA or two DMAs occur based on if the optional header feature is enabled. This feature can be useful when a routing decision needs to be made for a packet and the entire packet does not need to be brought into host storage. Another possible scenario is the header bytes may determine how the user wants to DMA the packet data to the host.

For smaller packet sizes, such as less than 2 KB, it may be more efficient to perform a single DMA and keep the packet header, DMA list, and packet data in a single buffer. To do this, single page mode should be enabled in the cut through configuration. When enabled, the header page size is used to determine the DMA behavior. If a packet completes and the total length of the packet and headers will fit in the header page size, then a single DMA is performed. If the data length exceeds the single page size as it is being received, the data is scattered using the normal options (might need to catch up). This feature can be useful for optimizing user processing for small packets. Head Bytes

There are two ways to set the number of head bytes. They are set on a per connection basis in the receive LCD using the numHeadbytes and useCrcNumHead fields. When the useCrcNumHead field is set to ‘0’, the numHeadbytes field provides a fixed number of bytes that is used as the number of header bytes. When use-CrcNumHead field is set to ‘1’, then the RXCRC nano code will calculate the number of header bytes using the frameType field to index an IP procedure. Currently, RXCRC will only set the number of header bytes for recognized TCP/IP headers. Other headers can be recognized. Contact IBM technical support to discuss requirements.

3.14.2 REASM

3.14.2.1 REASM Logical Channel Descriptor Base Register

The REASM Logical Channel Descriptor Base Register indicates the starting address of the logical channel descriptor table. This register defines where the Logical Channel Descriptors are located.

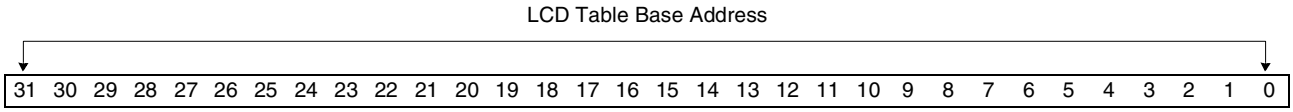
Length 32 bits

Type Read/Write

Address XXXX 1618

Power On Reset Value x‘0000 8000’

Restrictions The value must be in the range of the physical memory allocated for Control Memory.



Bit(s)	Name	Description
31-0	LCD Table Base Address	These bits define where the Logical Channel Descriptors are located.

3.14.2.2 REASM Mode Register

This register is used to set the REASM and sub-entity modes and contains the mode bits that specify how REASM is to operate.

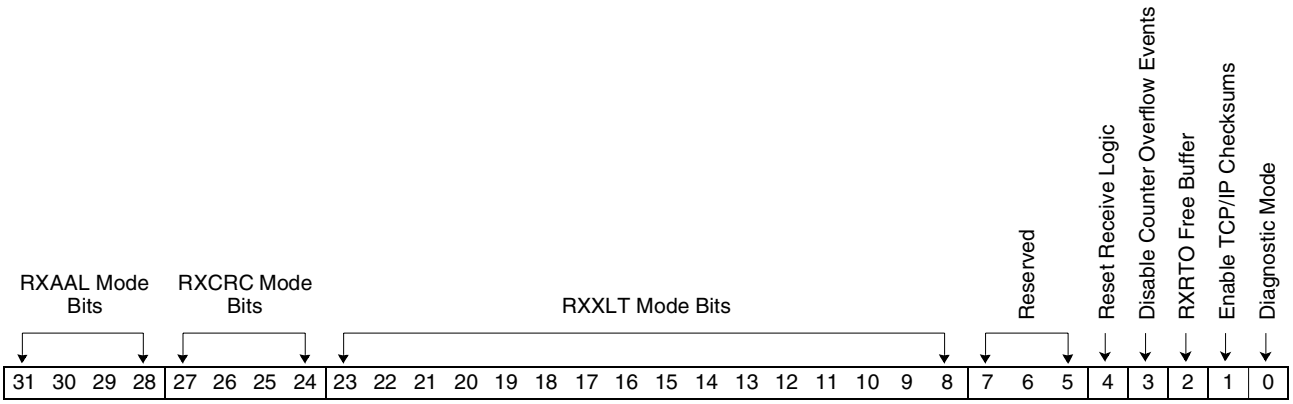
Length 32 bits

Type Clear/Set

Address XXXX 1610 and 1614

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-28	RXAAL Mode Bits	RXAAL code specific mode bits.
27-24	RXCRC Mode Bits	RXCRC code specific mode bits.
23-8	RXXLT Mode Bits	RXXLT code specific mode bits. Each nibble is for a port. Bits 23-20 are RXXLT mode bits 3-0 for port 3, bits 19-16 are RXXLT mode bits 3-0 for port 2, bits 15-12 are for port 1, and bits 11-8 are for port 0.
7-5	Reserved	Reserved.
4	Reset Receive Logic	Reset receive logic.
3	Disable Counter Overflow Events	Disable counter overflow events.
2	RXRTO Free Buffer	When set, a buffer that times out is freed and the event will contain the LCD address instead.
1	Enable TCP/IP Checksums	When set, TCP/IP checksum verification is enabled. When enabled, the receive LCD data structure includes the IP state.
0	Diagnostic Mode	When set, REASM is placed in diagnostic mode.

3.14.2.3 REASM Reassembly Modes Register

This register contains the mode bits that specify different reassembly modes.

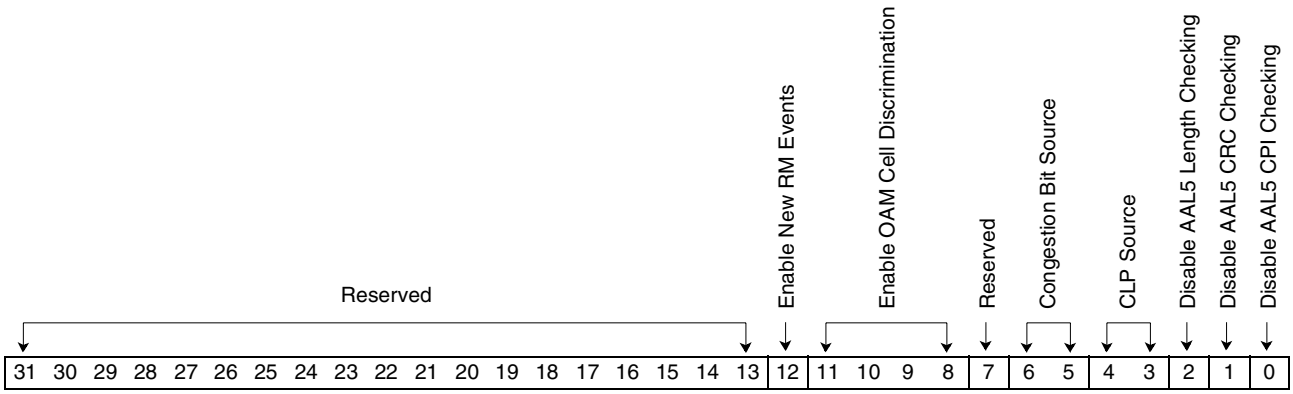
Length 32 bits

Type Clear/Set

Address XXXX 1630 and 1634

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-13	Reserved	Reserved.
12	Enable New RM Events	When set, the new RM cell events are enabled, and the ABR event routing register is ignored. This allows separate events for forward and backward RM cells, but routes the events to the general OAM cell receive queue.
11-8	Enable OAM Cell Discrimination	When set, the OAM processing is enabled for ports 0-3. When cleared, OAM cells are NOT discriminated.
7	Reserved	Reserved.
6-5	Congestion Bit Source	Specify which congestion bit source to use if doing routing. Values are: 00 Use value from LCD routed LCD ptr field 01 Use ORed congestion value (or last in case of cell) 10 Use value from last cell
4-3	CLP Source	Specify which CLP source to use if doing routing. Values are: 00 Use value from LCD routed LCD ptr field 01 Use ORed CLP value (or last in case of cell) 10 Use value from last cell.
2	Disable AAL5 Length Checking	When set, the AAL5 trailer length field is not checked.
1	Disable AAL5 CRC Checking	When set, the AAL5 trailer CRC is not checked.
0	Disable AAL5 CPI Checking	When set, the AAL5 trailer CPI bytes are not checked against zero.

3.14.2.4 REASM Status Register

This register contains the status bits for the REASM sub-entities. It is used to surface REASM and sub-entity status.

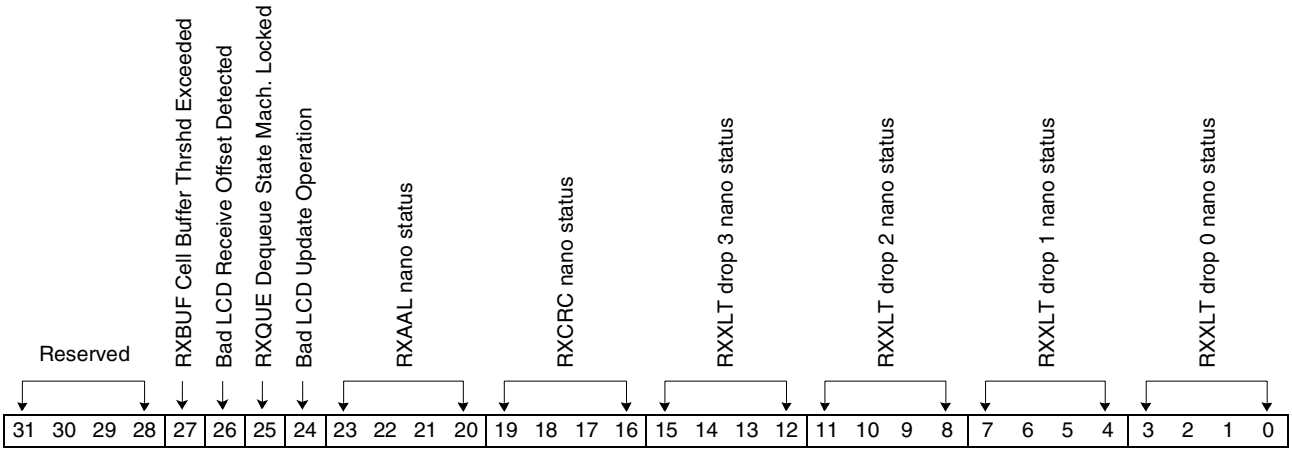
Length 32 bits

Type Clear/Set

Address XXXX 1600 and 1604

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-28	Reserved	Reserved.
27	RXBUF Cell Buffer Threshold Exceeded.	This bit is set when the number of receive cell buffers exceeds the threshold set in the RXBUF Receive Buffer Threshold. This bit is persistent and must be reset by software after being set.
26	Bad LCD Receive Offset Detected	This bit is set when a receive LCD is used that does not have a good receive offset. Either the receive offset does not allow enough room for the configured packet header, or there is not enough room for the DMA list entry that would have been written.
25	RXQUE Dequeue State Machine Locked	This bit is set when an RXQUE dequeue operation is attempted in order to get a piece of user data for the DMA list and there is no data available. When using two pieces of data in a DMA list entry, both must be available.
24	Bad LCD Update Operation	This bit is set when a receive LCD update was attempted on an offset that falls in the transmit portion of the LCD, or when an LCD that is out of range is updated.
23-20	RXAAL Nano Status	These bits can be set from the RXAAL nano code.
19-16	RXCRC Nano Status	These bits can be set from the RXCRC nano code.
15-12	RXXLT Drop 3 Nano Status	These bits can be set from the RXXLT nano code for drop 3.
11-8	RXXLT Drop 2 Nano Status	These bits can be set from the RXXLT nano code for drop 2.
7-4	RXXLT Drop 1 Nano Status	These bits can be set from the RXXLT nano code for drop 1.
3-0	RXXLT Drop 0 Nano Status	These bits can be set from the RXXLT nano code for drop 0.

3.14.2.5 REASM Interrupt Enable Register

This register is used to enable interrupts for REASM status conditions. When set, the corresponding status condition generates an interrupt from REASM to INTST.

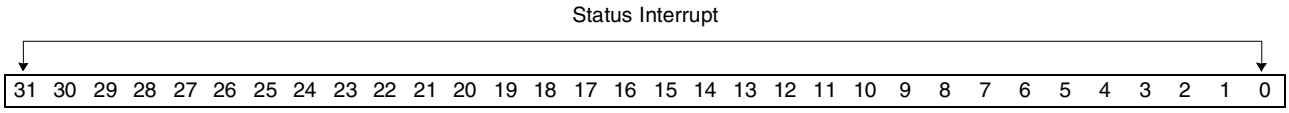
Length 32 bits

Type Clear/Set

Address XXXX 1608 and 160C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Interrupt Enables	When one of these bits is on and the corresponding bit in the *REASM Status Register* on page 312 is on, an interrupt is generated.

3.14.2.6 REASM DEBUG State Selector Register

This register selects which entity states are surfaced. Use this register only under the advice of IBM technical support.

Length 2 x 32 bits

Type Read/Write

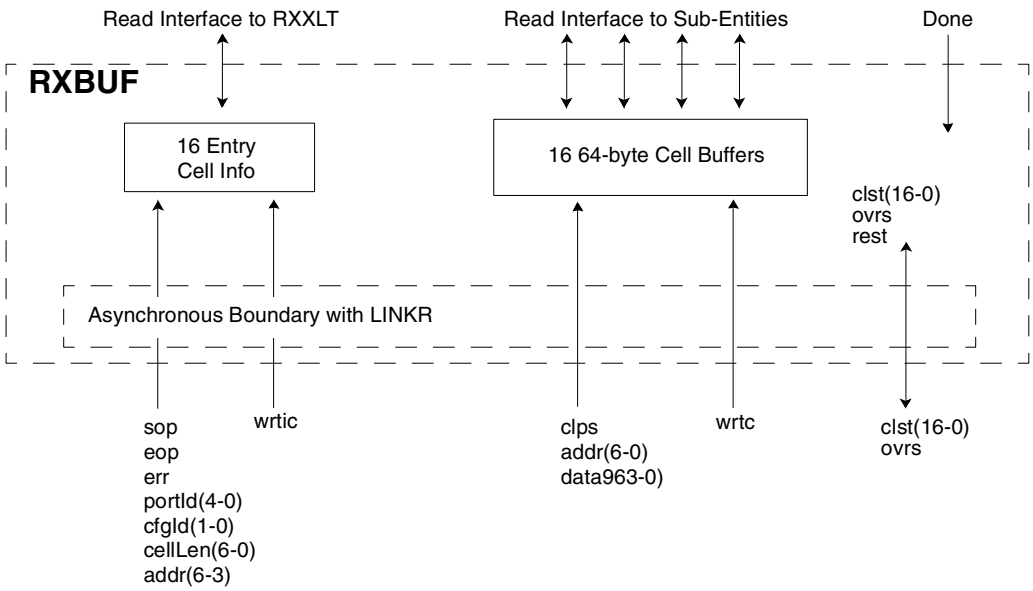
Address XXXX 1620-1624

Power On Reset Value x‘0000 0000’

Restrictions None

3.14.3 RXBUF

Figure 18: RXBUF Block Diagram



3.14.3.1 RXBUF Functional Description

RXBUF provides the cell/packet buffering mechanism between LINKR and the rest of REASM. The buffering provides enough storage for sixteen 64-byte cells and the associated control information for each cell buffer. LINKR writes the cell/packet data and control information into the buffers. The buffering mechanism is then exposed to the remainder of the REASM sub-entities for reading.

The cell buffers are sequenced in order regardless of on which port the received cells arrive. Thus, a total of 16 cells of buffering exists and is used as a shared 16-cell FIFO.

3.14.3.2 RXBUF Cell Data Buffer Address

This register provides the read/write address for accessing the cell data buffer. When the RXBUF Cell Data Buffer Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 1640

Power On Reset Value x‘0000 0000’

Restrictions Low two bits are always zero.

Bit(s)	Name	Description
31-11	Reserved	Reserved.
10-0	Cell Data Buffer Address	Auto-incremented when the RXBUF Cell Data Buffer Port is read or written. Rolls over to zero when the last address is read or written.

3.14.3.3 RXBUF Cell Data Buffer Read/Write Port

This register provides read/write access to the receive cell data buffer. The array is divided into sixteen 64-byte buffers used to buffer/assemble cells received from the line. When this register is read/written, the address provided by the RXBUF Cell Data Buffer Address register is used to select the array word to be accessed. The RXBUF Cell Data Buffer Address is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 256 words x 32 bits

Type Read/Write

Address XXXX 1648

Power On Reset Value x‘0000 0000’

Restrictions The array can only be accessed in diagnostic mode. If not in diagnostic mode, zero is returned on reads and writes are silently ignored.

3.14.3.4 RXBUF Cell Info Buffer Address

This register provides the read/write address for accessing the cell information buffer. When the RXBUF Cell Info Buffer Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 1644

Power On Reset Value x‘0000 0000’

Restrictions Low two bits are always zero.

Bit(s)	Name	Description
31-6	Reserved	Reserved.
5-0	Cell Information Buffer Address	Auto-incremented when the RXBUF Cell Information Buffer Read/Write Port is read or written. Rolls over to zero when the last address is read or written.

3.14.3.5 RXBUF Cell Info Buffer Read/Write Port

This register provides read/write access to the Receive Cell Info Buffer. The array is divided into 16 areas used to provide information about each received cell from LINKR. When this register is read/written, the address provided by the RXBUF Cell Info Buffer Address is used to select the array word to be accessed. The RXBUF Cell Info Buffer Address is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 16 words x 32 bits

Type Read/Write

Address XXXX 1650

Power On Reset Value x‘0000 0000’

Restrictions The array can only be accessed in diagnostic mode. If not in diagnostic mode, zero is returned on reads and writes are silently ignored.

3.14.3.6 RXBUF Receive Buffer Threshold

This register provides a method to monitor the number of cell buffers in use. The value of this register compared against the number of active cell buffers. When this threshold is exceeded, the status is raised in the REASM status register.

Length 32 bits

Type Read/Write

Address XXXX 1660

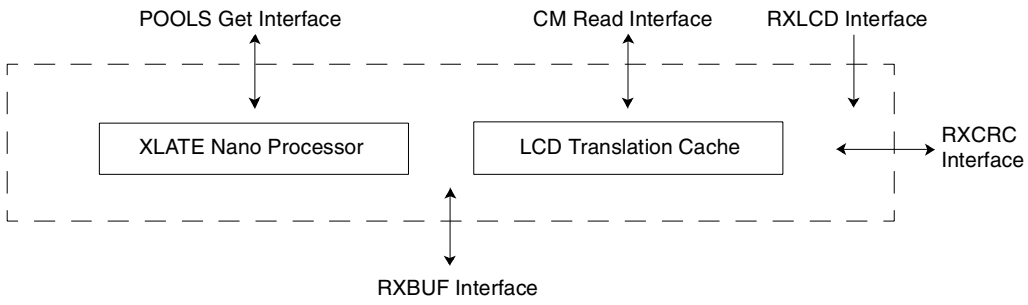
Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-5	Reserved	Reserved.
4-0	Receive Buffer Threshold	Compared to the number of active cell buffers. When the number of active cell buffers is greater than the value in this field, bit 27 in the *REASM Status Register* on page 312 is set.

3.14.4 RXXLT

Figure 19: RXXLT Block Diagram



3.14.4.1 RXXLT Functional Description

RXXLT is the first stage in the cell processing pipeline. RXXLT provides general LCD translation facilities and link level statistics. These are provided via a nano-processor and nano-programs.

Up to four unique drops/ports can be supported, each with a unique configuration. Each port is able to run a unique nano-program to do LCD address translation. For example, one port may be a packet-based PHY using 64-byte segments with PPP LCD translation, and another port may be an ATM cell based PHY. The drop/config number (0-3) along with the port id is passed to RXXLT from RXBUF/LINKR. The drop number (0-3) is used to specify which nano-program is executed by RXXLT to translate cell/packet information into an LCD address. This is different from previous versions of the processor which had a fixed LCD translation mechanism. RXXLT instruction formats are not defined here and are IBM Confidential.

RXXLT uses the resulting LCD address to load the LCD cache for the next stage of the pipeline. The LCD address and cell buffer address are passed to RXCRC upon completion of processing.

There are a number of degrees of freedom in the LCD translation. Generally, the nano program performs the following steps:

- Gathers bytes from the cell buffer.
- Checks errors and the fields of the default LCD.
- Selects and shifts appropriate bits to form an LCD translate table index
- Reads the LCD translate table to access an LCD index
- Generates the LCD address from the LCD index and the LCD base address

There are eight general purpose registers per PHY drop and four drops. These eight registers contain values that the nano-code uses, and are available on a per port basis. For example, the LCD translate table addresses would reside in these registers (this is different from previous versions of the processor where these registers were at fixed addresses). Other items that might reside in these registers are default/error LCD addresses, compare values, and masks. Because these are general purpose registers, multiple LCD tables or multiple default LCDs can be specified. One quarter of the total registers are available to each port, so there can be an LCD translate table (etc.) for each port.

The total LCD translate tables and LCD table sizes are only limited in size by the amount of memory that is available to the PNR. The LCD indexes are limited to 16 bits, and LCD addresses are always 128-byte aligned.

The LCD translation code must execute in one cell time in order to run at full bandwidth. The only variable portion of the code execution time is the reads to PNR memory when reading the LCD translation table. Thus, while a double lookup is possible, it may not meet the time constraints of running at full bandwidth.

The following pseudo code shows some of the types of LCD translations that are possible using the nano-processor.

Note: The following do not imply types/numbers of instructions needed, but the different variable names imply different general purpose registers are being used, so variables are specified on a per port basis.

In the following code there are shift, mask, and compare values that are not specified. These are values that would be customizable at run time. These will be customized via the general purpose registers.

The following code uses nomenclature that matches the PNR (zero-based big endian). So bit(1) in a comm spec might be bit(0) in the following code. The comments use spec nomenclature so the two can be matched.

Figure 20: Standard ATM

```
atmH = read 4 bytes from rxbuf at offset 0 -- read the atm header from cell

if non_user_data {                         -- non-user data as specified in pti
    lcdAddr = defaultLcd                   -- field is handled by the deafult lcd
    return
}

tblIndex  =  (atmH and vciMask) >> 4       -- gather pertinent vci bits
tblIndex |= ((atmH and vpiMask) >> X)      -- gather pertinent vpi bits
                                           -- X depends on num of vci bits used
if non-masked bits on {                    -- check for out of range
    out of range counter++                 -- update counter
    if mode(X) {                           -- if configured to flush out of
        flush cell                         -- range cells flush and we are done
    }
    else {
        lcdAddr = errorLcdAddr
    }
    return
}

if tblIndex == 0 {                         -- check for zero id
    zero id counter++                      -- update counter
    if mode(X) {                           -- if configured to flush zero id
        flush cell                         -- cells flush and we are done
    }
    else {
        lcdAddr = errorLcdAddr
    }
    return
}

lcdIndex = Lookup(lcdTable, tblIndex)      -- read index from cm using tableIndex
lcdAddr = lcdBase + lcdIndex*128           -- calc lcd addr from index
```

Figure 21: PPP

```
label = read 4 bytes from rxbuf at offset 0
if label == 0xff030021 {
    read 1 bytes from rxbuf at offset 4       -- read the ip header version (5th byte)
    if IPVER_HEADERLGT == 0x45 {
        tblIndex = read byte from offset 5    -- read QOS field (6th byte)
        lcdIndex = Lookup(lcdTable, tblIndex) -- read index from cm using tableIndex
        lcdAddr = lcdBase + lcdIndex*128      -- calc lcd addr from index
    }
    else {
        lcdAddr = defaultPortLcd              -- use port default lcd
    }
}
else {
    lcdAddr = defaultPortLcd                  -- use port default lcd
}
```

Figure 22: Q.922 2 Byte Addressing

```
head = read 2 bytes from rxbuf at offset 0    -- read the header (network bytes 0-1)
if (bit(0) == 1) && (bit(8) == 0) {           -- EA bits indicate two byte addr
                                              -- byte 0 bit 1 == 0 && byte 1 bit 1 == 1
    tblIndex  =  (head and dlciMask0) >> X    -- gather 6 of 10 dlci bits from byte 0
    tblIndex |= ((head and dlciMask1) >> X)   -- gather 4 of 10 dlci bits from byte 1
    lcdIndex = Lookup(lcdTable, tblIndex)     -- read index from cm using tableIndex
    lcdAddr = lcdBase + lcdIndex*128          -- calc lcd addr from index
}
else {
    lcdAddr = errorLcdAddr                    -- not a two byte addr
}
```

Figure 23: Q.922 4 Byte Addressing

```
head = read 4 bytes from rxbuf at offset 0    -- read the header (network bytes 0-3)
if  (bit(0)  == 1) && (bit(8)  == 0) &&       -- EA bits indicate four byte addr
    (bit(16) == 0) && (bit(24) == 0) {        -- byte 0 bit 1 == 0 && byte 1 bit 1 == 0 &&
                                              -- byte 2 bit 1 == 0 && byte 3 bit 1 == 1
    if dcBit == 1 {                           -- check for dc bit being set
        lcdAddr = defaultPortLcd              -- and surface on default port lcd
    }
    else {                                    -- gather 16 least significant dlci bits
        tblIndex  =  (head and dlciMask1) >> X-- gather 3 dlci bits from byte 1
        tblIndex |= ((head and dlciMask2) >> X)-- gather 7 dlci bits from byte 2
        tblIndex |= ((head and dlciMask3) >> X)-- gather 6 dlci bits from byte 3
        lcdIndex = Lookup(lcdTable, tblIndex) -- read index from cm using tableIndex
        lcdAddr = lcdBase + lcdIndex*128      -- calc lcd addr from index
    }
}
else {
    lcdAddr = errorLcdAddr                    -- not a four byte addr
}
```

Figure 24: FUNI 2.0 2 Byte Addressing

```
head = read 2 bytes from rxbuf at offset 0    -- read the header (network bytes 0-1)
if (bit(0) == 1) && (bit(8) == 0) {           -- EA bits indicate two byte addr
                                              -- byte 0 bit 1 == 0 && byte 1 bit 1 == 1
    if (bit(2) == 0) && (bit(9) == 0) {       -- FID1 & FID2 == 0 (byte 0 bit 2 & byte 1 bit 3)
        tblIndex  =  (head and faMask1) >> X  -- gather 6 of 10 FA bits from byte 0
        tblIndex |= ((head and faMask0) >> X) -- gather 4 of 10 FA bits from byte 1
        lcdIndex = Lookup(lcdTable, tblIndex) -- read index from cm using tableIndex
        lcdAddr = lcdBase + lcdIndex*128      -- calc lcd addr from index
    }
    else {
        lcdAddr = defaultPortLcd              -- otherwise surface on port default lcd
    }
}
else {
    lcdAddr = errorLcdAddr                    -- not a two byte addr
}
```

Figure 25: FUNI 2.0 4 Byte Addressing

```
head = read 4 bytes from rxbuf at offset 0    -- read the header (network bytes 0-3)
if  (bit(0)  == 1) && (bit(8)  == 0) &&       -- EA bits indicate four byte addr
    (bit(16) == 0) && (bit(24) == 0) {        -- byte 0 bit 1 == 0 && byte 1 bit 1 == 0 &&
                                              -- byte 2 bit 1 == 0 && byte 3 bit 1 == 1
    if (bit(18) == 0) && (bit(25) == 0) {     -- FID1 & FID2 == 0 (byte 0 bit 2 & byte 1 bit 3)
                                              -- gather 16 vpi/vci bits
        tblIndex  =  (head and vciMask0) >> 1 -- gather X vci bits from byte 3
        tblIndex  =  (head and vciMask1) >> X -- gather X vci bits from byte 2
        tblIndex  =  (head and vciMask2) >> X -- gather X vci/vpi bits from byte 1
        tblIndex  =  (head and vpiMask3) >> X -- gather X vpi bits from byte 0
        lcdIndex = Lookup(lcdTable, tblIndex) -- read index from cm using tableIndex
        lcdAddr = lcdBase + lcdIndex*128      -- calc lcd addr from index
    }
    else {
        lcdAddr = defaultPortLcd              -- otherwise surface on port default lcd
    }
}
else {
    lcdAddr = errorLcdAddr                    -- not a four byte addr
}
```

3.14.4.2 RXXLT Register Array Address Port

This register provides the read/write address for accessing register array. When the RXXLT Register Array Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 1680

Power On Reset Value x‘0000 0000’

Restrictions Low two bits are always zero.

Bit(s)	Name	Description
31-7	Reserved	Reserved.
6-0	Register Array Address	Auto-incremented when the RXXLT Register Array Read/Write port is read or written. Rolls over to zero when the last address is read or written.

3.14.4.3 RXXLT Register Array Read/Write Port

This register provides read/write access to the register array. The array is divided into four groups of eight registers. Each group is associated with a receive port (0-3). So each nano-program has eight registers available. These registers have intended uses and also serve as the link level counters, so they are not general purpose registers.

When this register is read/written, the address provided by RXXLT Register Array Address Port is used to select the array word to be accessed. RXXLT Register Array Address Port is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 32 words x 32 bits

Type Read/Write

Address XXXX 1688

Power On Reset Value x‘0000 0000’

Restrictions None

3.14.4.4 RXXLT Processor State Selector

This register allows the user to select which data should be accessed with the RXXLT Processor State Read/Write Port. An encoded selector is provided for accessing internal processor registers and state via reads/writes to the RXXLT Processor State Read/Write Port.

Length 32 bits

Type Read/Write

Address XXXX 1698

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	State Information Selector	The following are the meanings of the encoded values: 0000 Accumulator register 0001 Header register 0010 LCD index register 0011 Reserved 0100 Reserved 0101 Flags 0110 Reserved 1111 Instruction ptr

3.14.4.5 RXXLT Processor State Read/Write Port

This register provides read/write access to the internal state of the processor. The internal processor state is externalized for debug and testing reasons. See the description of *3.14.4.4: RXXLT Processor State Selector* on page 323 for definitions of the addresses.

Length 32 bits

Type Read/Write

Address XXXX 169C

Power On Reset Value x‘0000 0000’

Restrictions Processor state can only be set in diagnostic mode.

3.14.4.6 RXXLT Instruction Array Address Port

This register provides the read/write address for accessing the instruction array. When the RXXLT Instruction Array Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 1684

Power On Reset Value x‘0000 0000’

Restrictions Low two bits are always zero.

Bit(s)	Name	Description
31-9	Reserved	Reserved.
8-0	Instruction Array Address	Auto-incremented when the RXXLT Instruction Array Read/Write port is read or written. Rolls over to zero when the last address is read or written.

3.14.4.7 RXXLT Instruction Array Read/Write Port

This register provides read/write access to the instruction array. The instruction array is divided into four groups of 32 entries. Each group is associated with a receive port (0-3) so a nano-program can be loaded for each active port. When this register is read/written, the address provided by the RXXLT Instruction Array Address Port is used to select the array word to be accessed. The RXXLT Instruction Array Address Port is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 128 words x 32 bits

Type Read/Write

Address XXXX 1690

Power On Reset Value x‘0000 0000’

Restrictions None, but the instruction stream of an active nano-program should not be written.

Bit(s)	Name	Description
31-20	Reserved	Reserved.
19-0	Load/Read Instructions	Load/read nano-program instructions.

3.14.4.8 RXXLT Last LCD Index Register

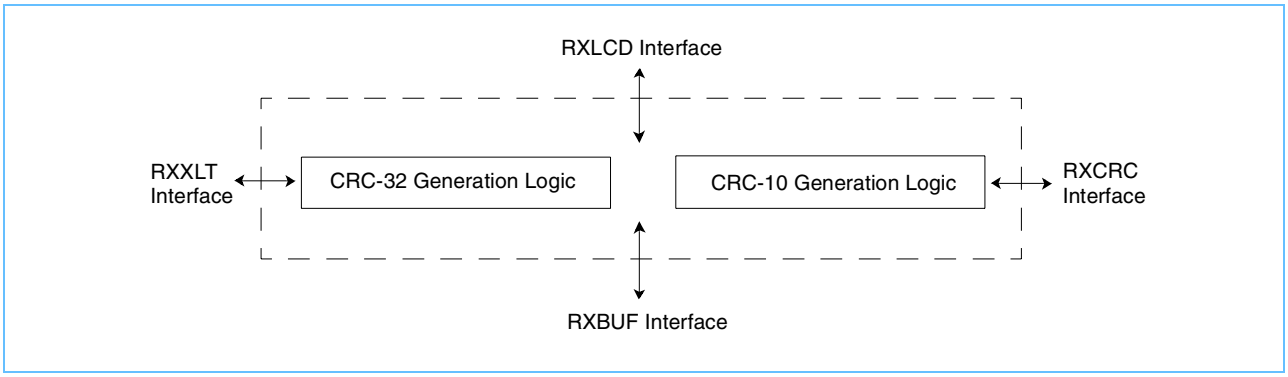
These registers provide the previous LCD index that was used for the corresponding port.

Length	32 bits	
Type	Read/Write	
Address	Port 0	XXXX 16A0
	Port 1	XXXX 16A4
	Port 2	XXXX 16A8
	Port 3	XXXX 16AC
Power On Reset Value		x‘0000 0000’
Restrictions	Can only be written in diagnostic mode.	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Previous LCD Index Used	Index of the LCD that was previously used by RXXLT on the port corresponding to this register.

3.14.5 RXCRC

Figure 26: RXCRC Block Diagram



3.14.5.1 RXCRC Functional Description

RXCRC is the second stage in the cell processing pipeline. It performs the ATM CRC-32 (Ethernet FCS) and ATM CRC-10 functions if necessary. RXCRC gets LCD type, state, and seed information from the LCD cache, and updates the cache on completion. The results are passed to RXAAL upon completion, along with the LCD address.

3.14.5.2 RXCRC Instruction Array Address Port

This register provides the read/write address for accessing the instruction array. When RXCRC Instruction Array Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 16C4

Power On Reset Value x‘0000 0000’

Restrictions Low two bits are always zero.

Bit(s)	Name	Description
31-10	Reserved	Reserved.
9-0	Instruction Array Address	Auto-incremented when the RXCRC Instruction Array Read/Write port is read or written. Rolls over to zero when the last address is read or written.

3.14.5.3 RXCRC Instruction Array Read/Write Port

This register provides read/write access to the instruction array. The instruction array contains a single nano-program. When this register is read/written, the address provided by RXCRC Instruction Array Address Port is used to select the array word to be accessed. The RXCRC Instruction Array Address Port is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 256 words 32 bits

Type Read/Write

Address XXXX 16D0

Power On Reset Value x‘0000 0000’

Restrictions None, but the instruction stream of an active nano-program should not be written.

Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	Load/Read Instructions	Load/read nano-program instructions.

3.14.5.4 RXCRC Processor State Selector

This register allows the user to select which data should be accessed with the RXCRC Processor State Read/Write Port. An encoded selector is provided for accessing internal processor registers and state via reads/writes to the RXCRC Processor State Read/Write Port.

Length 32 bits

Type Read/Write

Address XXXX 16D8

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	State Information Selector	The following are the meanings of the encoded values: 000 Accumulator register 001 Header register 010 Reserved 011 Reserved 100 Reserved 101 Flags 110 Reserved 111 Instruction ptr

3.14.5.5 RXCRC Processor State Read/Write Port

This register provides read/write access to the internal state of the processor. The internal processor state is externalized for debug and testing reasons. See the description of *3.14.5.4: RXCRC Processor State Selector* on page 327 for definitions on the addresses.

Length 32 bits

Type Read/Write

Address XXXX 16DC

Power On Reset Value x‘0000 0000’

Restrictions Processor state can only be set in diagnostic mode.

3.14.5.6 RXCRC Last LCD Index Register

This register provides the previous LCD index that was used.

Length 32 bits

Type Read/Write

Address XXXX 16E0

Power On Reset Value x‘0000 0000’

Restrictions Can only be written in diagnostic mode.

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	LCD Index	Index of the last LCD used by RXCRC.

3.14.5.7 RXCRC Checksum Protocol Registers

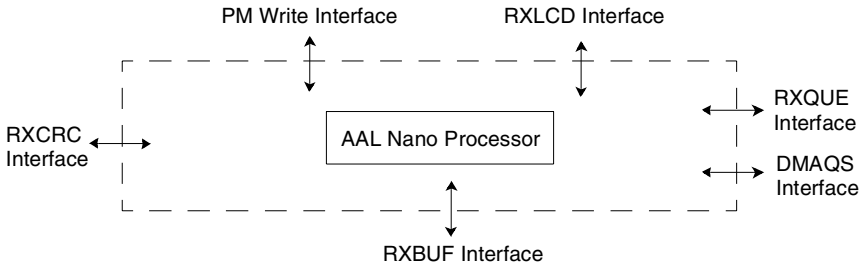
These registers provide additional protocol bytes for which checksum calculations should be enabled. The first register allows up to four protocols to be enabled with headers that are similar to UDP and TCP which use a pseudo-header. The second register allows up to four protocols to be enabled with headers that are similar to ICMP (no pseudo header). IP, UDP, TCP, V4 ICMP, and V6 ICMP are recognized automatically and should not be specified again in these registers.

Each byte specifies a different protocol.

Length	2 x 32 bits	
Type	Read/Write	
Address	Checksum Type: With header	XXXX 16E4
	Checksum Type: With no header	XXXX 16E8
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.14.6 RXAAL

Figure 27: RXAAL Block Diagram



3.14.6.1 RXAAL Functional Description

RXAAL performs the cell and packet reassembly functions. These include the AAL processing and moving cell data and packet headers to Packet Memory.

The nano-program uses state and configuration information from the LCD cache to perform the necessary function for each cell. The nano-processor is capable of executing programs to run the following types of reassembly:

- AAL5
- AAL3/4
- Raw cells
- Non-user data (may be same as raw)
- Packets
- MPEG FIFO Mode

RXAAL also performs the cell/packet post processing step. This includes event generation to RXQUE, cut through processing, scatter processing, and DMA enqueues.

3.14.6.2 RXAAL Instruction Array Address Port

This register provides the read/write address for accessing the instruction array. When the RXAAL Instruction Array Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

Length 32 bits

Type Read/Write

Address XXXX 1704

Power On Reset Value x‘0000 0000’

Restrictions Bits 1-0 are always zero.

Bit(s)	Name	Description
31-11	Reserved	Reserved.
10-0	Instruction Array Address	Auto-incremented when the RXAAL Instruction Array Read/Write port is read or written. Rolls over to zero when the last address is read or written.

3.14.6.3 RXAAL Instruction Array Read/Write Port

This register provides read/write access to the instruction array. The instruction array contains a single nano-program. When this register is read/written, the address provided by the RXAAL Instruction Array Address Port is used to select the array word to be accessed. The RXAAL Instruction Array Address Port is auto-incremented on each read/write. Thus, this port can be read/written multiple times to read/write the entire array.

Length 512 words x 32 bits

Type Read/Write

Address XXXX 1710

Power On Reset Value x‘0000 0000’

Restrictions None, but the instruction stream of an active nano-program should not be written.

Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	Load/Read Instructions	Load/read nano-program instructions.

3.14.6.4 RXAAL Processor State Selector

This register allows the user to select which data should be accessed with the RXAAL Processor State Read/Write Port. An encoded selector is provided for accessing internal processor registers and state via reads/writes to the RXAAL Processor State Read/Write Port.

Length 32 bits

Type Read/Write

Address XXXX 1718

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	State Information Selector	The following are the meanings of the encoded values: 000 Accumulator register 001 Header register 010 Reserved 011 Reserved 100 Reserved 101 Flags 110 Reserved 111 Instruction ptr

3.14.6.5 RXAAL Processor State Read/Write Port

This register provides read/write access to the internal state of the processor. The internal processor state is externalized for debug and testing reasons. See the description of *3.14.5.4: RXCRC Processor State Selector* on page 327 for definitions of the addresses.

Length 32 bits

Type Read/Write

Address XXXX 171C

Power On Reset Value x‘0000 0000’

Restrictions Processor state can only be set in diagnostic mode.

3.14.6.6 RXAAL Last LCD Index Register

This register provides the previous LCD index that was used.

Length 32 bits

Type Read/Write

Address XXXX 1720

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	LCD Index	Last LCD index RXAAL used.

3.14.6.7 RXAAL Transmit Queue Length Compression Configuration

This register allows the user to configure how the transmit queue lengths should be compressed for use in the receive packet header. CSKED provides 12 transmit queue lengths specified in bytes. A 32-bit register (see *3.12.16.7: Bytes Queued Counters* on page 265) is available for the high, medium, and low priority queues for each of the four PHY ports. Using the full counts in the receive packet header generally uses too much room. This register allows the user to configure how this information should be compressed for use in the receive packet header.

Length 32 bits

Type Read/Write

Address XXXX 1730

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)		Description
31-4	Reserved	Reserved.
3-0	Transmit Queue Length Compression Configuration	The following are the options: 0000 Use the full register representation for port zero only (three 32-bit words) 0001 Use the 2-K scaled representation for port zero only (one 32-bit word) 0010 Use the 4-K scaled representation for port zero only (one 32-bit word) 0011 Use the 8-K scaled representation for port zero only (one 32-bit word) 0100 Use the 16-K scaled representation for port zero only (one 32-bit word) 0101 Use the 32-K scaled representation for port zero only (one 32-bit word) 0110 Use the 64-K scaled representation for port zero only (one 32-bit word) 0111 Use the 128-K scaled representation for port zero only (one 32-bit word) 1000 Reserved 1001 Use the 2-K scaled representation for all ports (three 32-bit words) 1010 Use the 4-K scaled representation for all ports (three 32-bit words) 1011 Use the 8-K scaled representation for all ports (three 3- bit words) 1100 Use the 16-K scaled representation for all ports (three 32-bit words) 1101 Use the 32-K scaled representation for all ports (three 32-bit words) 1111 Use the 128-K scaled representation for all ports. (three 32-bit words) For example, using option ‘0001’, a single 32-bit word is used. The most significant byte contains the transmit queue length for the high priority queue for port zero divided by 2 K bytes. If the scaled count overflows (greater than 2K*0xff), a value of x‘ff’ is used. The next byte contains the scaled count for the medium priority queue, and the third byte contains the scaled count for the low priority queue. The least significant byte is not used. Using option ‘1010’ three 32-bit words are used. The first word contains the scaled counts for the high priority queue. The second word contains the scaled counts for the medium priority queue. The third word contains the scaled counts for the low priority queue. Within each word, the first byte contains the scaled count for port zero, and the subsequent bytes are used for the other ports (1, 2, 3). The counts are divided by 4 K in this case.

3.14.6.8 RXAAL Packet Header Configuration

This register allows the user to configure the contents of each optional packet header word, and specify how many optional packet words are used.

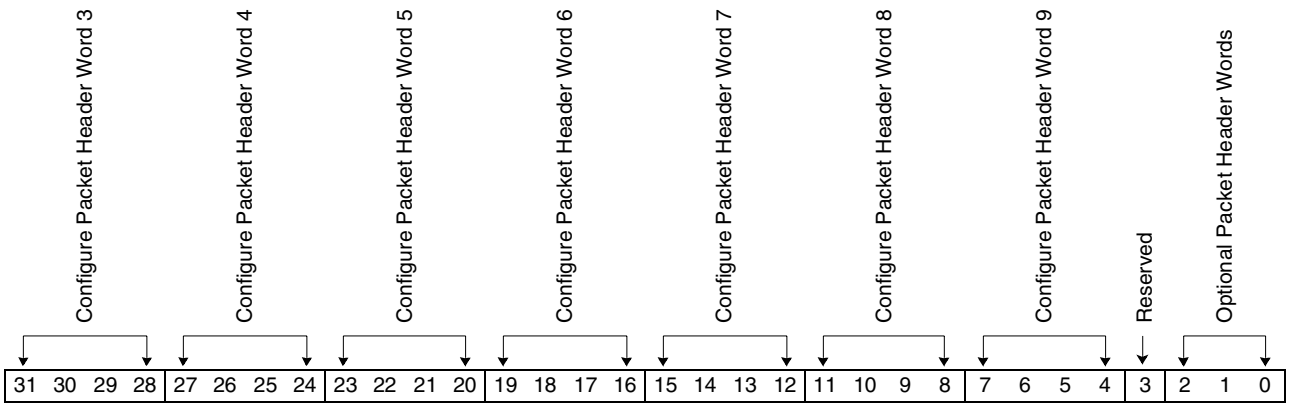
The contents of each optional packet header word are configured in the optional portion of the packet header. There are four possible configurations, and the configuration used is selected with the packHeadSel field in the receive LCD.

The first three words of the packet header are fixed, and up to seven additional words can be configured. The low nibble of this register specifies how many optional packet header words are used, and the remaining nibbles of the register configure each packet header word if used.

Note: The base receive and transmit packet headers must be compatible if internal cell or packet routing is being used. The receive packet header becomes the transmit packet header in this scenario.

User 0 and user 1 values can be used to place non-standard values in the packet header. These values are built by the nano-code, and are then placed in the packet header. In order to use these values, the nano-code must be customized. Do this only under the advisement of IBM technical support.

Length	32 bits	
Type	Read/Write	
Address	Config 0	XXXX 1740
	Config 1	XXXX 1744
	Config 2	XXXX 1748
	Config 3	XXXX 174C
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Reserved	Description
31-28	Configure Packet Header Word 3	Each nibble specifies what should be selected for the corresponding packet header word. The following are the options: 0000 Start Timestamp 0001 End Timestamp 0010 ATM Header 2 0011 Host data 0100 VBA - Virtual buffer address 0101 Transmit queue length word 0 0110 Transmit queue length word 1 0111 Transmit queue length word 2 1000 User 0 1001 User 1 1010 AAL5 trailer, two user bytes and the length 1011 VBA with the number of header bytes in the low 10 bits 1100 Reserved
27-24	Configure Packet Header Word 4	Same definitions as bits 31-28.
23-20	Configure Packet Header Word 5	Same definitions as bits 31-28.
19-16	Configure Packet Header Word 6	Same definitions as bits 31-28.
15-12	Configure Packet Header Word 7	Same definitions as bits 31-28.
11-8	Configure Packet Header Word 8	Same definitions as bits 31-28.
7-4	Configure Packet Header Word 9	Same definitions as bits 31-28.
3	Reserved	Reserved.
2-0	Optional Packet Header Words	Specifies how many optional packet header words to use.

3.14.6.9 RXAAL Error Count Register

This register maintains a count of detected error conditions. For example, CRC errors and other protocol types of errors are counted. This count is useful when the PNR is configured to only surface good packets.

When this counter overflows, a counter overflow event is generated to RXQUE.

Length 32 bits

Type Read/Write

Address XXXX 1734

Power On Reset Value x‘0000 0000’

Restrictions None

3.14.6.10 RXAAL Dropped Count Register

This register maintains a count of packets that are dropped due to a lack of resource. For example, if no POOLS buffer (real or virtual mode) is available, the packet is dropped and this counter is incremented. This count is useful when the PNR is configured to only surface good packets.

When this counter overflows, a counter overflow event is generated to RXQUE.

Length 32 bits

Type Read/Write

Address XXXX 1738

Power On Reset Value x‘0000 0000’

Restrictions None

3.14.6.11 RXAAL Maximum SDU Length Register

This register specifies the maximum SDU size for a packet. This size includes only the protocol data length of the packet. For example, this length would be compared with the AAL5 length field in the AAL5 trailer. When a packet is completely received, this register is used to make sure it does not exceed the MSDU specified.

Length 32 bits

Type Read/Write

Address XXXX 173C

Power On Reset Value x‘0000 FFFF’

Restrictions None

Bit(s)	Name	Description
31-18	Reserved	Reserved.
17-0	Maximum SDU Size	The protocol data length of the packet only.

3.14.6.12 RXAAL OAM LCD Information Register

This register specifies the reassembly information for OAM cells. The format of this register is equivalent to word zero of the receive LCD. The following fields are valid: ppMode, size, storeCrc10, rxqNum, rxPoolId, rxOffset, and cutThruSel. Refer to the format of LCD word zero for Raw receive LCDs in *7.4: Receive LCD Data Structure and Modes* on page 692.

Length	32 bits
Type	Read/Write
Address	XXXX 172C
Power On Reset Value	x‘0000 FFFF’
Restrictions	None

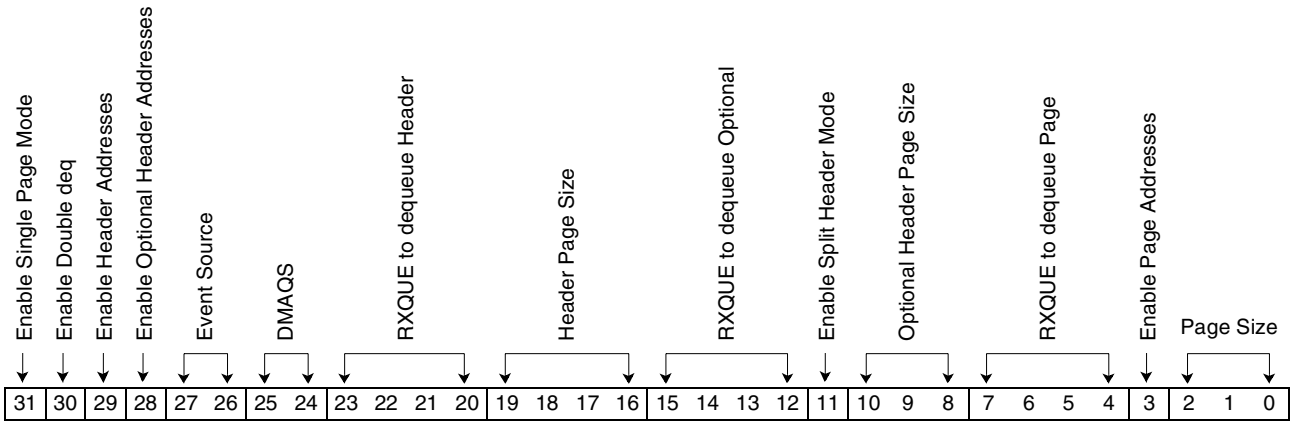
3.14.6.13 RXAAL Scatter/Cut Through Info Registers

These registers specify the scatter/cut through configurations. A configuration is selected in the LCD via the cut through selector field when doing cut through/scatter mode. A configuration consists of three registers. The first two registers, described here, define the four possible configurations for scatter/cut through. The third register, RXAAL - Scatter/Cut Through Flag Registers, is described in section *3.14.6.14: RXAAL Scatter/Cut Through Flag Registers* on page 342.

The first register, one of cti(0-3), is defined as follows:

Scatter/Cut Through Info Register 1

Length	32 bits	
Type	Read/Write	
Address	Config 0	XXXX 1750
	Config 1	XXXX 1754
	Config 2	XXXX 1758
	Config 3	XXXX 175C
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31	Enable Single Page Mode	Enable single page mode. See *Scatter Options* on page 307.
30	Enable Double Dequeue	Enable double dequeue for packet header buffers to get virtual addresses.
29	Enable Header Addresses	Enable header addresses vs. descriptor 1 addresses 0 descriptor
28	Enable Optional Header Addresses	Enable optional header addresses vs. descriptor 1 addresses 0 descriptor
27-26	Event Source	Specify how the event data (if any) is formed. Normally, the DMA descriptor is used for DMA events, but when the entire DMA descriptor is built there is no descriptor address to use. The following sources are possible: 00 Use DMA descriptor address (DMA queue address where built) 01 Use source address 10 Use destination address
25-24	DMAQS	DMAQS DMA queue to enqueue DMA descriptor to.
23-20	RXQUE to Dequeue Header	RXQUE to dequeue header DMA descriptor addresses from.
19-16	Header Page Size	Specify the page size of the buffer that the header is DMAed into. The following encodings are used: 0 128 bytes 1 256 bytes 2 512 bytes 3 1K bytes 4 2K bytes 5 4K bytes 6 8K bytes 7 6K bytes 8 32K bytes 9 64K bytes
15-12	RXQUE to Dequeue Optional Header	RXQUE to dequeue optional header DMA descriptor addresses from.
11	Enable Split Header Mode	Enable Split Header Mode (optional header buffer).

Bit(s)	Name	Description
10-8	Optional Header Page Size	Specifies the page size of the buffer that the header is DMAed into. The following encodings are used: 0 64 bytes 1 128 bytes 2 256 bytes 3 512 bytes 4 1K bytes 5 2K bytes 6 4K bytes 7 8K bytes
7-4	RXQUE to Dequeue Page	RXQUE to dequeue page DMA descriptor addresses from.
3	Enable Page Addresses	Enable page addresses vs. page descriptor. 1 address 0 descriptor
2-0	Page Size	Specifies the page size of the page buffers that the scatter pages are DMAed into. The following encodings are used: 0 512 bytes 1 1K bytes 2 2K bytes 3 4K bytes 4 8K bytes 5 16K bytes 6 32K bytes 7 64K bytes

Scatter/Cut Through Info Register 2

Length 32 bits

Type Read/Write

Address Config 4 XXXX 1770

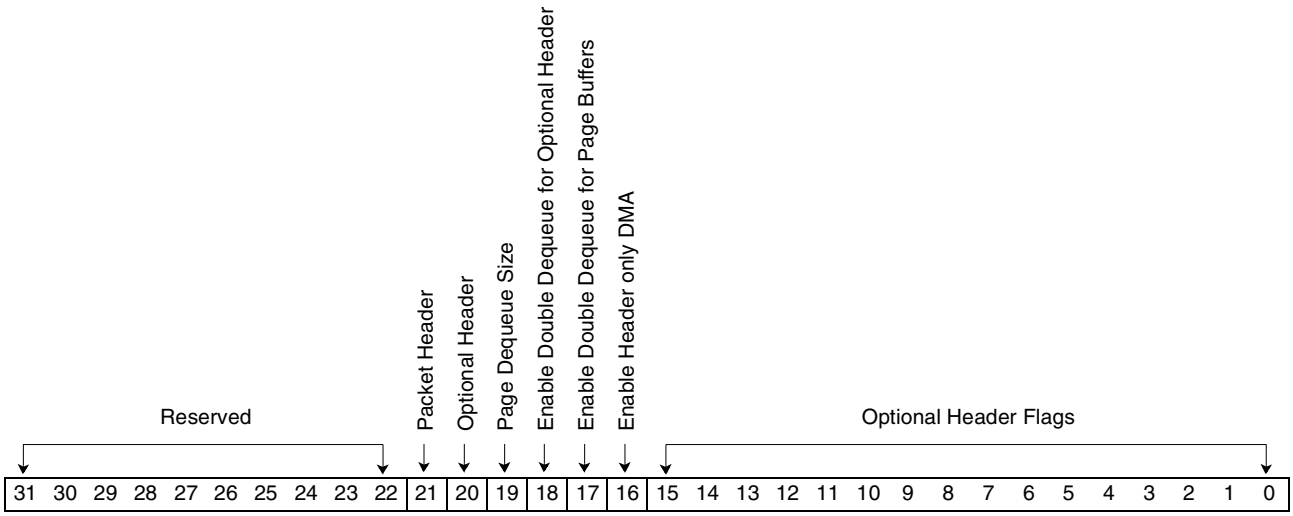
Config 5 XXXX 1774

Config 6 XXXX 1778

Config 7 XXXX 177C

Power On Reset Value x‘0000 0000’

Restrictions None

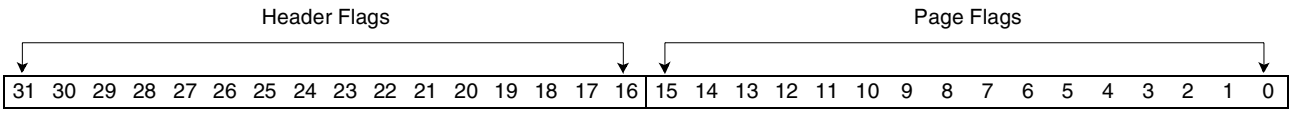


Bit(s)	Name	Description
31-22	Reserved	Reserved.
21	Packet Header	Packet Header dequeue size: 0 32 bit 1 64 bit
20	Optional Header	Optional Header dequeue size: 0 32 bit 1 64 bit
19	Page Dequeue Size	Page dequeue size: 0 32 bit 1 64 bit
18	Enable Double Dequeue for Optional Header	Enable double dequeue for optional header buffers to get virtual addresses.
17	Enable Double Dequeue for Page Buffers	Enable double dequeue for page buffers to get virtual addresses.
16	Enable Header Only DMA	Enable header only DMA. When set, only the header bytes as specified in the LCD or from RXCRC will be DMAed along with the DMA list and packet header.
15-0	Optional Header Flags	Optional Header Flags. These flags are used when DMAing the optional header page.

3.14.6.14 RXAAL Scatter/Cut Through Flag Registers

These registers specify the scatter/cut through flags. A flag register is selected in the LCD via the cut through selector field when doing cut through/scatter mode. The flags are used when building DMA descriptors for scatter pages and the first scatter buffer (packet header, DMA list, etc.).

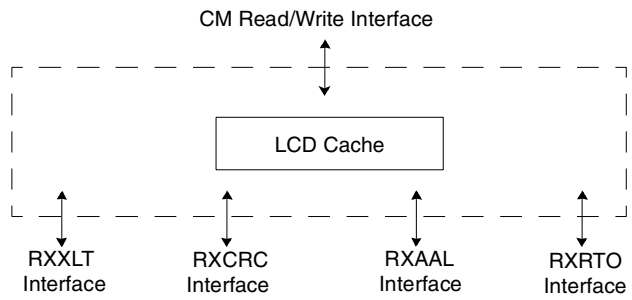
Length	32 bits	
Type	Read/Write	
Address	Config 0	XXXX 1760
	Config 1	XXXX 1764
	Config 2	XXXX 1768
	Config 3	XXXX 176C
Power On Reset Value		x‘0000 0000’
Restrictions	None	



Bit(s)	Name	Description
31-16	Header Flags	These flags are used when DMAing the packet header, DMA list, and header bytes from the packet.
15-0	Page Flags	These flags are used when DMAing a scatter page (other than the header page).

3.14.7 RXLCD

Figure 28: RXLCD Block Diagram



3.14.7.1 RXLCD Functional Description

RXLCD provides an LCD cache for REASM sub-entities. This cache holds the last four receive LCDs. The sub-entities can request to load an LCD, read the LCD words, and update parts of the LCD.

3.14.7.2 RXLCD Cache Data Array Address Port

This register provides the read/write address for accessing the LCD cache data array. When the RXLCD Cache Data Array Read/Write Port is read/written, this register is auto-incremented. When the last address is read/written, the address rolls over to zero.

The cache is organized as sixty-four 32-bit words. Each 16 words comprises an LCD. The first four words and the last word of each LCD do not contain valid data and cannot be written. These locations return zero on reads.

Length 32 bits

Type Read/Write

Address XXXX 1780

Power On Reset Value x‘0000 0000’

Restrictions The low two bits are always zero.

Bit(s)	Name	Description
31-6	Reserved	Reserved.
5-0	LCD Cache Data Array Address	Auto-incremented when the RXLCD Cache Data Array Read/Write Port is read or written. Rolls over to zero when the last address has been read or written.

3.14.7.3 RXLCD Cache Data Array Read/Write Port

This register provides read/write access to the LCD cache data array. When this register is read/written, the address provided by the RXLCD Cache Data Array Address Port is used to select the array word to be accessed. The RXLCD Cache Data Array Address Port is auto-incremented on each read/write so this port can be read/written multiple times to read/write the entire array.

The cache is organized as sixty-four 32-bit words. Each 16 words comprises an LCD. The first four words and the last word of each LCD do not contain valid data and cannot be written. These locations return zero on reads.

Length 64 words x 32 bits

Type Read/Write

Address XXXX 1788

Power On Reset Value x‘0000 0000’

Restrictions Must be in diagnostic mode to read/write the cache.

3.14.7.4 RXLCD Cache Line Info Registers

These registers provide the cache line tags, valid, and dirty bits. There is a register for each of the four cache lines.

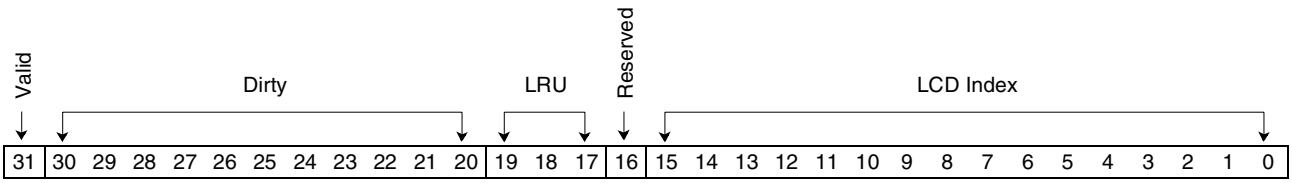
Length 4 x 32 bits

Type Read/Write

Address XXXX 17A0-17AC

Power On Reset Value x‘0000 0000’

Restrictions Must be in diagnostic mode to write these registers.



Bit(s)	Name	Description
31	Valid	This bit indicates if the cache line is valid.
30-20	Dirty	These bits indicate which, if any, sections of the cache line have been modified.
19-17	LRU	These bits are the Least Recently Used (LRU) bits that are used to determine which cache line can be replaced when a new line needs to be loaded.
16	Reserved	Reserved.
15-0	LCD Index	Index of LCD in this cache line.

3.14.7.5 RXLCD Mode Register

This register provides a means to control cache operation.

Length 32 bit

Type Read/Write

Address XXXX 17B8-17BC

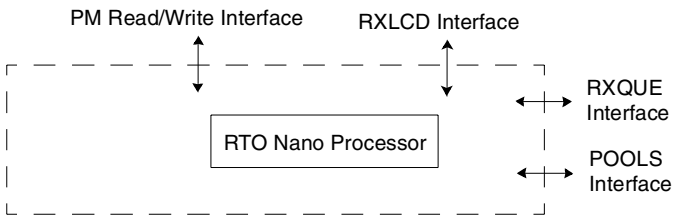
Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-1	Reserved	Reserved.
0	Flush All Entries	When set, all dirty entries are flushed to memory but remain in the cache. This bit will reset when the operation is complete.

3.14.8 RXRTO

Figure 29: RXRTO Block Diagram



3.14.8.1 RXRTO Functional Description

RXRTO performs periodic reassembly timeout processing and LCD update operations.

3.14.8.2 Reassembly Timeout (RTO) Processing

Reassembly timeout processing is generally an AAL5 operation. It is supported for other LCD types as well. It can be enabled on an LCD basis by turning on the RTO enable bit in the LCD. The following registers also need to be properly set up to run RTO processing:

- RXRTO RTO LCD Table Bound Registers
- RXRTO Reassembly Timeout Value Register
- RXRTO Reassembly Timeout Pre-Scaler Register

See the register descriptions for more register details.

The LCD table registers define the LCD table that the RTO process examines. The value register is used as a compare value against a counter that counts based on a pre-scaler. Each time the registers compare, RTO processing is started for a single LCD and the time base is reset. RTO processing checks the RTO test and set bit. If the RTO test and set bit is reset, RTO processing sets it and continues. If the RTO test and set bit is set, then a timeout occurs and the LC is placed in an error state and the current packet is surfaced to the user via an event. Any resource associated with the packet must be recovered by software. For example, if the LCD is setup to use scatter mode, then there may be scatter DMA pages in the DMA list that need to be returned to the proper receive queue. The RTO bit is reset with each inbound cell received. An LCD needs to be touched twice to cause a timeout (once to set it and once to detect that it is already set).

The time base starts running as soon as the RTO processing is complete. Thus, RTO processing is a low priority task.

Shutting Down an LCD

To shut down a receive LCD, the following steps should be followed:

- Clear the entry for this LCD in the LCD table (to stop receiving cells for this LCD).
- Do an LCD update operation that sets the LCD state to down .
- Read the LCD REASM ptr.
- If REASM ptr is non-zero and LCD is set up to do cut through, be sure to free any DMA descriptor that was added with cut through operation.
- If REASM ptr is non-zero and LCD is set up to do scatter, be sure to free any pages in the DMA list.

- If REASM ptr is non-zero, free it to POOLS.

3.14.8.3 RXRTO LCD Update Data Registers

These two registers are used to specify data to write into the receive LCD on the update LC operation. They contain the data used in the LC update operation. For more information on their use, see the *3.14.8.5: RXRTO LCD Update Op Registers* on page 348.

The Update Date Register changes to contain the updated data written to the LC word while the operation is completing.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update 1 register	XXXX 17C0
	Update 2 register	XXXX 17D0
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.14.8.4 RXRTO LCD Update Mask Registers

These two registers are used to specify which data to write into the LCD on the update LC operation. They contain the mask used in the LC update operation. For more information on their use, see the *3.14.8.5: RXRTO LCD Update Op Registers* on page 348.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update 1 register	XXXX 17C4
	Update 2 register	XXXX 17D4
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.14.8.5 RXRTO LCD Update Op Registers

These registers are used to specify the LCD word to update. This operation is used to update a portion of the receive LCD. If this operation is not used, then software or the PNR updates of the LCD may be lost because the receive LCD is cached in the PNR.

This register is written with the address of the LCD word to update. Once this register is written, the update operation starts. All subsequent reads or writes to the data, mask, or update registers are held off until the operation completes. A read-modify-write will occur to update the portion specified by the mask with the masked value in the data register.

Normally this register would not be read. However, if it is read then the low order bit is read as ‘0’ and the next lowest order bit (bit 1) is read as the busy bit. This signifies whether an operation is still going on. If an operation is still going on, then a new write to any of the data, mask, or update operation registers is held off until the original operation is complete.

The second set of LCD update registers is meant for the core to use, but is available for general use.

Length	32 bits	
Type	Read/Write	
Address	Update 1 register	XXXX 17C8
	Update 2 register	XXXX 17D8
Power On Reset Value		x‘0000 0000’
Restrictions	The low order two bits are not writable.	

3.14.8.6 RXRTO RTO LCD Table Bound Registers

These registers are used to specify the lower/upper bounds of the LCD table. The lower bound should be initialized to the LCD index of the first LCD in the LCD table if reassembly timeout processing is to be done. The upper bound should be initialized to the LCD index of the last LC in the LC table if reassembly timeout processing is to be done.

Length	32 bits	
Type	Read/Write	
Address	Lower bound 1 register	XXXX 17E0
	Upper bound 1 register	XXXX 17E4
	Lower bound 2 register	XXXX 17F0
	Upper bound 2 register	XXXX 17F4
Power On Reset Value		x‘0000 0000’
Restrictions	None	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	LCD Table Bounds	If doing reassembly timeout processing, these bits should be set as follows: If setting a lower bound register, set these bits to the LCD index of the first LCD in the LCD table. If setting an upper bound register, set these bits to the LCD index of the last LC in the LC table.

3.14.8.7 RXRTO Reassembly Timeout Value Register

These registers are used to specify the time interval used for reassembly timeout processing. This register is the number of pre-scaler intervals between reassembly processing. The pre-scaler interval is determined by the RXRTO Reassembly Timeout Pre-Scaler Register. A single LC is checked for reassembly timeout during each reassembly processing interval.

When this register is set to ‘0’, reassembly timeout processing is disabled.

For more information on how reassembly timeout conditions are processed see *3.14.8.2: Reassembly Timeout (RTO) Processing* on page 346.

Length	32 bits	
Type	Read/Write	
Address	Timeout 1 register	XXXX 17E8
	Timeout 2 register	XXXX 17F8
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.14.8.8 RXRTO Reassembly Timeout Pre-Scaler Register

This register determines the number of 15 ns intervals between RTO timer ticks. The value in the register plus 1 is the number of 15 ns intervals between RTO timer ticks. Thus, the default value of '0' means that the RTO timer ticks every 15 ns. If a value of nine is placed in this register, the RTO timer ticks every 150 ns (10 * 15 ns).

For more information on how reassembly timeout conditions are processed, see *3.14.8.2: Reassembly Time-out (RTO) Processing* on page 346.

Length	32 bits	
Type	Read/Write	
Address	Prescale 1	XXXX 17EC
	Prescale 2	XXXX 17FC
Power On Reset Value		x'0000 0000'
Restrictions	None	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	RTO Timer Tick Interval	The value in these bits plus 1 is the number of 15 ns intervals between RTO timer ticks.

3.15 Receive Queues (RXQUE)

3.15.1 Functional Description

RXQUE has a single function: to manage the receive queues for software by providing an easy to use primitive interface. When talking about the receive queues, “rxq” refers to a receive queue, “deq” refers to a dequeue operation, and “enq” refers to an enqueue operation.

3.15.2 RXQUE Interface

A group of 16 receive queues is available for software use. The receive queues hold events or user specified data.

Each queue entry (event) is either 32 or 64 bits and contains two fields: event-identifier and event-information. The seven least significant bits in the entry contain the event-identifier field. The most significant bits in the entry comprise the event-information field.

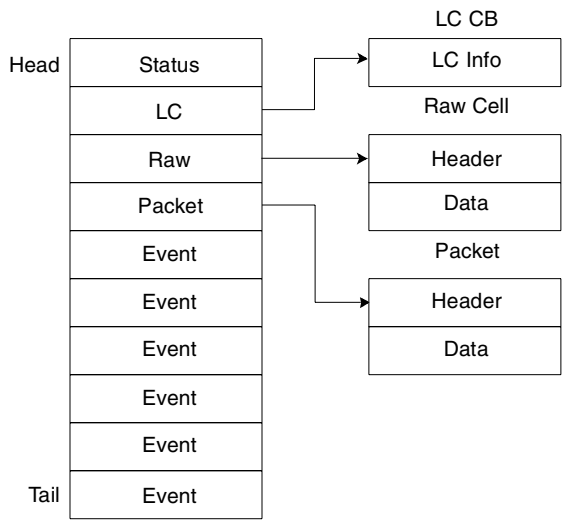
Warning: In order to maintain the atomicity of 64-bit atomic transfers, the user must ensure that 64-bit transfers are bus atomic within the particular bus system in which the PNR is being used.

The receive queues are maintained by RXQUE with the following operations being available to software:

- **dequeue** - Remove the entry at the head of the queue
- **enqueue** - Add an arbitrary entry at the tail of the queue

The following figure shows how events in a receive queue link to other data structures including LC control blocks, packet buffers, and cell buffers.

Figure 30: General Queue, Event, and Data Structure Linkage



3.15.3 RXQUE Events

The event information typically contains a pointer (when low order bits are zeroed) to a packet buffer, a cell buffer, or an LCD. It can also contain a DMA descriptor address or user-specified data. Table 19 lists the different event types. If an event is routed, there will be an “X” in the column corresponding to the queue to which the event is routed. See *3.15.24 RXQUE Event Routing Registers* on page 378 for more information.

Table 19: Event Summary and Routing Information (Page 1 of 3)

Event Number	Description	Event Information	Error	Count	Tx Comp	ABR	POOLS	Note
x’00’=0000000	AAL5 packet event (packet complete)	Packet/LCD						
x’01’=0000001	AAL5 packet header event (packet start)	Packet						
x’02’=0000010	AAL5 packet with bad CRC	Packet/LCD	X					
x’03’=0000011	AAL5 packet with bad length field	Packet/LCD	X					
x’04’=0000100	AAL5 packet that exceeds maximum length in LC	Packet/LCD	X					
x’05’=0000101	AAL5 packet timeout	Packet/LCD	X					
x’06’=0000110	AAL5 packet forward abort	Packet/LCD	X					
x’07’=0000111	AAL5 packet CPI field not equal to zero	Packet/LCD	X					
x’0E’=0001110	AAL5 FIFO packet	Packet						
x’08’=0001000	Cell event (user data)	Packet/LCD						
x’09’=0001001	NUD cell event (non-user data)	Packet/LCD						
x’0A’=0001010	NUD cell with bad CRC-10	Packet/LCD	X					
x’0B’=0001011	Bad cell - bad HEC	Packet	X					
x’0C’=0001100	Bad cell - out of range	Packet	X					
x’0D’=0001101	Bad cell - index equal zero	Packet	X					
x’10’=0010000	AAL0 cell dropped - lack of POOLS buffers	LCD	X					
x’11’=0010001	AAL5 cell dropped - lack of POOLS buffers	LCD	X					
x’12’=0010010	OAM cell dropped - lack of POOLS buffers	LCD	X					
x’18’=0011000	Total user cells receive counter overflow	LCD		X				
x’19’=0011001	Total user cells rx clp=0 counter overflow	LCD		X				
x’1A’=0011010	Total user cells tx counter overflow	LCD		X				
x’1B’=0011011	Total user cells tx clp=0 counter overflow	LCD		X				
x’1C’=0011100	Threshold 1 crossed - down	LCD			X			
x’1D’=0011101	Threshold 1 crossed - up	LCD			X			
x’1E’=0011110	Threshold 1 crossed - down	LCD			X			
x’1F’=0011111	Threshold 2 crossed - up	LCD			X			
x’20’=0100000	Transmit complete	Packet			X			
x’21’=0100001	Transmit complete buffer freed	Packet/LCD			X			
x’22’=0100010	"bad" found in first word of packet	Packet			X			
x’23’=0100011	Connection closed	LCD			X			

1. This event is generated by the RXAAL picoprocessor and is subject to change.

Table 19: Event Summary and Routing Information (Page 2 of 3)

Event Number	Description	Event Information	Error	Count	Tx Comp	ABR	POOLS	Note
x'24'=0100100	Transmit DMA complete	Descriptor						
x'25'=0100101	Receive DMA complete	Descriptor						
x'26'=0100110	Transmit DMA complete with error	Descriptor						
x'27'=0100111	Receive DMA complete with error	Descriptor						
x'28'=0101000	Transmit DMA complete with virtual error	Descriptor						
x'29'=0101001	Zero address in DMA descriptor SRC/DST address	Descriptor						
x'2A'=0101010	Reserved							
x'2C'=0101100	ADTF Event	LCD				X		
x'2D'=0101101	CRM Event	LCD				X		
x'2E'=0101110	CCR=0 Event	LCD				X		
x'2F'=0101111	RM Cell Event	Packet				X		
x'30'=0110000	User event							
x'31'=0110001	User event							
x'32'=0110010	User event							
x'33'=0110011	User event							
x'34'=0110100	User event							
x'35'=0110101	User event							
x'36'=0110110	User event							
x'37'=0110111	User event							
x'38'=0111000	Virtual memory resource event	Packet/LCD	X					
x'39'=0111001	Buffer overflow event	Packet/LCD	X					
x'3A'=0111010	No DMA descriptor for AAL7 packet	Packet/LCD	X					
x'3B'=0111011	DMA canceled for AAL7 packet due to error	Descriptor						
x'3C'=0111100	No scatter pages available and packet complete	Packet/LCD	X					
x'3D'=0111101	Entity counter overflow event	Counter		X				
x'3E'=0111110	POOLS status event	Status					X	
x'3F'=0111111	No descriptor available event	Packet						1
x'40'=1000000	Frame event (good frame)	Packet/LCD						
x'41'=1000001	Frame event (error)	Packet/LCD	X					
x'42'=1000010	Frame event (protocol error)	Packet/LCD	X					
x'43'=1000011	Frame event (reserved)		X					
x'44'=1000100	Frame event (reserved)							
x'45'=1000101	Frame event (reserved)							
x'46'=1000110	Frame event (reserved)							

1. This event is generated by the RXAAL picoprocessor and is subject to change.

Table 19: Event Summary and Routing Information (Page 3 of 3)

Event Number	Description	Event Information	Error	Count	Tx Comp	ABR	POOLS	Note
x'47'=1000111	Frame event (reserved)							
x'50'=1010000	PCORE event							
x'51'=1010001	PCORE event							
x'52'=1010010	PCORE event							
x'53'=1010011	PCORE event							
x'54'=1010100	PCORE event							
x'55'=1010101	PCORE event							
x'56'=1010110	PCORE event							
x'57'=1010111	PCORE event							
x'58'=1011000	REASM counter-overflow event	Counter		X				
x'59'=1011001	SEGBF counter-overflow event	Counter		X				
x'5C'=1011100	System - receive queue event (start of buffer)	Previous lower bound						
x'5D'=1011101	System - receive queue event (end of buffer)	Next lower bound						
x'5E'=1011110	Timestamp event	Timestamp						
x'5F'=1011111	64-bit timestamp event	Timestamp						
x'64'=1100100	Tx DMA complete	Descriptor						
x'65'=1100101	Rx DMA complete	Descriptor						
x'66'=1100110	Tx DMA complete with error	Descriptor						
x'67'=1100111	Rx DMA complete with error	Descriptor						
x'68'=1101000	Tx DMA complete with virtual error	Descriptor						
x'69'=1101001	Zero address in DMA descriptor SRC/DST address	Descriptor						
x'6E'=1101110	No header available event	Packet						1
x'6F'=1101111	No packet header available event	Packet						1

1. This event is generated by the RXAAL picoprocessor and is subject to change.

3.15.3.1 AAL5 Packet Events

For AAL5 packet events, the event specifies the packet buffer address, and the event type field specifies the type of packet event. The following event types are defined:

Event Number	Name	Description
x'00'=0000000	Normal AAL5 Packet Event (Packet Complete)	This event specifies that an AAL5 packet was received and has passed all AAL5 protocol checks (CRC, length). The event information contains a pointer to the packet.
x'0E'=0001110	Normal AAL5 FIFO Packet Event	This event specifies that an AAL5 FIFO packet was received and has passed all AAL5 protocol checks (CRC, length). The event information contains a pointer to the packet.
x'01'=0000001	Normal AAL5 Packet Header Threshold Event (Packet Start)	This event specifies that the AAL5 packet header threshold was exceeded as set in the LCD. The event information contains a pointer to the packet header, and the user can access up to the packet header threshold bytes of data.
x'02'=0000010	AAL5 Packet with Bad CRC was RX on LC	This event specifies that an AAL5 packet was received and the AAL5 CRC is bad. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'03'=0000011	AAL5 Packet with Bad Length Field was RX on LC	This event specifies that an AAL5 packet was received and the AAL5 length field is bad. For example, there is too much data or not enough, but typically the bad CRC is detected first. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'04'=0000100	AAL5 Packet that exceeds Max Len in LC was RX	This event specifies that an AAL5 packet was received but the amount of data has exceeded the maximum length as specified in the LCD or in the MSDU register. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'05'=0000101	AAL5 Packet Timeout on this LC	This event specifies that a reassembly timeout has occurred for an AAL5 packet being reassembled. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'06'=0000110	AAL5 Packet Forward Abort	This event specifies that an AAL5 packet was terminated with a forward abort. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'07'=0000111	AAL5 Packet CPI Field not equal to Zero	This event specifies that a AAL5 packet was received and the AAL5 CPI field was not set to '0' which is an AAL5 protocol violation. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.

3.15.3.2 Cell Events

For AAL0 events, the event specifies a cell buffer address, and the event type field specifies type of AAL0 event. The following event types are defined:

Event Number	Name	Description
x'08'=0001000	AAL0 Cell Event	This event specifies that an AAL0 (non-FIFO mode) cell was received. The event information contains a pointer to the cell.
x'09'=0001001	Non-User Data Cell Event	This event specifies that a non-user data cell was received and the CRC-10 was good if checking was enabled. The event information contains a pointer to the cell.
x'0A'=0001010	Non-User Data Cell with Bad CRC-10 Event	This event specifies that a non-user data cell was received and the CRC-10 was bad. The event information contains either a pointer to the cell if receiving bad frames, or a pointer to the LCD on which this cell was received.
x'0B'=0001011	Cell with Bad HEC Event	This event specifies that a cell was received with a bad HEC. The event information contains a pointer to the cell.
x'0C'=0001100	Cell with VP/VC Out Of Range Event	This event specifies that a cell was received with a VP/VC that was out of range. The event information contains a pointer to the cell.
x'0D'=0001101	Cell with VC Index Equal Zero	This event specifies that a cell was received with a VC index equal zero. The event information contains a pointer to the cell.

3.15.3.3 LC Events

For LC events, the event specifies an LC, and the event type field specifies what happened on the LC. The following event types are defined:

Event Number	Name	Description
x'10'=0010000	AAL0 Cell was Dropped due to Lack of POOLS Buffers	This event specifies that an AAL0 (non-FIFO mode) cell was received, but was discarded because no POOL buffers were available. The event information contains a pointer to the LCD on which this cell was received.
x'11'=0010001	AAL5 Cell was Dropped due to Lack of POOLS Buffers	This event specifies that the first AAL5 cell for a packet was received, but was discarded because no POOL buffers were available. The event information contains a pointer to the LCD on which this cell was received.
x'12'=0010010	Non-user Data Cell was Dropped due to Lack of POOLS Buffers	This event specifies that a non-user data cell was received, but was discarded because no POOL buffers were available. The event information contains a pointer to the LCD on which this cell was received.
x'17'=0010111	Reserved	Reserved.
x'18'=0011000	LC Total User Cells RX Counter Overflow	This event specifies that the TUC RX counter in the LCD has overflowed. The event information contains a pointer to the LCD.
x'19'=0011001	LC Total User Cells CLP=0 RX Counter Overflow	This event specifies that the TUC w/CLP=0 RX counter in the LCD has overflowed. The event information contains a pointer to the LCD.
x'1A'=0011010	LC Total User Cells TX Counter Overflow	This event specifies that the TUC TX counter in the LCD has overflowed. The event information contains a pointer to the LCD.
x'1B'=0011011	LC Total User Cells CLP=0 TX Counter Overflow	This event specifies that the TUC w/CLP=0 TX counter in the LCD has overflowed. The event information contains a pointer to the LCD.
x'58'=1011000	REASM Counter-Overflow Event	This specifies that REASM raised counter-overflow event. The event information specifies which counter overflowed.
x'59'=1011001	SEGBF Counter-Overflow Event	This specifies that SEGBF raised counter-overflow event. The event information specifies which counter overflowed.

3.15.3.4 ABR Events

The following events are used for ABR processing and are routed to the receive queue specified in the ABR event routing register.

Event Number	Name	Description
x'2C'=0101100	ADTF Event	This event specifies that the ADTF timer expired. The event information contains a pointer to the LCD.
x'2D'=0101101	CRM Event	This event specifies that the CRM count has been exceeded. The event information contains a pointer to the LCD.
x'2E'=0101110	CCR = 0 Event	This event specifies that CCR = 0. The event information contains a pointer to the LCD.
x'2F'=0101111	RM Cell Rx-ed	This event specifies that an RM cell was received. The event information contains a pointer to the receive buffer.

3.15.3.5 Miscellaneous Events

Event Number	Name	Description
x'1C'=0011100	Thresh 1 Event - Down	This event specifies that a memory management threshold was crossed downwards. The event information contains the LCD address.
x'1D'=0011101	Thresh 1 Event - Up	This event specifies that a memory management threshold was crossed upwards. The event information contains the LCD address.
x'1E'=0011110	Thresh 2 Event - Down	This event specifies that a memory management threshold was crossed downwards. The event information contains the LCD address.
x'1F'=0011111	Thresh 2 Event - Up	This event specifies that a memory management threshold was crossed upwards. The event information contains the LCD address.
x'20'=0100000	Transmit Complete	This event specifies that a packet/cell was successfully transmitted. The event information contains a pointer to the buffer transmitted.
x'21'=0100001	Transmit Complete Buffer Freed	This event specifies that a packet/cell was successfully transmitted and the buffer was freed back to POOLS. The event information contains a pointer to the buffer transmitted.
x'22'=0100010	Transmit Bad	This event specifies that a packet was to be transmitted, but the buffer was marked as bad, so was canceled. This is caused by getting a page fault when DMAing into the transmit packet buffer. The event information contains a pointer to the bad buffer.
x'23'=0100011	Connection Closed	This event specifies that all packets for the given LCD have been transmitted. The event information contains the LCD address.
x'24'=0100100	TX DMA Complete (into the PNR)	This event specifies that a TX DMA completed successfully. The event information depends on how the DMA was set up. Event-identifier x'64 is an alias.
x'25'=0100101	RX DMA Complete (out of the PNR)	This event specifies that an RX DMA completed successfully. The event information depends on how the DMA was set up. Event-identifier x'65 is an alias.
x'26'=0100110	TX DMA Complete with Error (into the PNR)	This event specifies that a TX DMA had errors. The event information depends on how the DMA was set up. Event-identifier x'66 is an alias.
x'27'=0100111	RX DMA Complete with Error (out of the PNR)	This event specifies that an RX DMA had errors. The event information depends on how the DMA was set up. Event-identifier x'67 is an alias.
x'28'=0101000	TX DMA Complete with Virtual Error	This event specifies that a TX DMA had a virtual error. The remainder of the DMA descriptor was cancelled. The event information contains the DMA descriptor address. Event-identifier x'68 is an alias.
x'29'=0101001	DMA Desc has Zero Address	This event specifies that a DMA descriptor source destination address was zero. The remainder of the DMA descriptor was cancelled. The event information contains the DMA descriptor address. Event-identifier x'69 is an alias.
x'2A'=0101010	Reserved	
x'30'=0110000	User Defined	
x'31'=0110001	User Defined	
x'32'=0110010	User Defined	
x'33'=0110011	User Defined	
x'34'=0110100	User Defined	
x'35'=0110101	User Defined	
x'36'=0110110	User Defined	

Event Number	Name	Description
x'37'=0110111	User Defined	
x'38'=0111000	Virtual Memory Resource Event	This event specifies that an AAL5 cell was received, but could not be written into the buffer because a virtual memory boundary was crossed and a buffer was not available to fill in the next segment. This can also happen if the cell crosses a boundary that would make the buffer larger than the virtual buffer size. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'39'=0111001	Buffer Overflow Event	This event specifies that an AAL5 cell was received, but could not be written into the buffer because it would exceed the real buffer size. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'3A'=0111010	No DMA Desc for AAL7 Packet Event	This event specifies that an AAL7 (AAL5 with cut through) packet was completed, but no DMA descriptors were available to DMA the packet header. The event information contains either a pointer to the packet if receiving bad frames, or a pointer to the LCD on which this packet was received.
x'3B'=0111011	DMA Cancelled for AAL7 Packet Due to Error Event	This event specifies that a DMA descriptor enqueued with a cut-through operation was cancelled because an error condition was detected with the packet (CRC, length). The event information contains the system descriptor address that was cancelled.
x'3C'=0111100	No Pages Available for AAL5 Scatter Packet	This event specifies that an AAL5 packet completed with no errors, but there was a lack of scatter buffers to complete the scatter DMA. The user must interrogate the partial DMA list in the packet header to recover the system pages. Once this is done, the packet should be freed. The user can alternately treat this as a good packet and complete the packet processing by setting up additional DMAs to move the remaining data to system pages. The event information contains the PNR buffer address.
x'3D'=0111101	PNR Counter Overflow Event	This event specifies that a counter overflow event has been raised. The event information specifies which counter overflowed. Multiple counter overflows can be specified with a single event. The following is the definition of the event information: Bit 27 GPDMA Write DMA Byte Count Overflow Bit 26 GPDMA Read DMA Byte Count Overflow Bit 25 RXQUE Timestamp Counter Overflow Bit 24 PCINT Performance Counter 1 Overflow Bit 23 PCINT Performance Counter 2 Overflow
x'3E'=0111110	POOLS Status Event	This event specifies that a POOLS status event has been raised. The event information contains the status. See *3.17 Buffer Pool Management (POOLS)* on page 395 for the definition.
x'5E'=1011110	Timestamp Event	This event specifies that a timestamp event has been placed ahead of next event. The event information contains the timestamp.
x'5F'=1011111	64-bit Timestamp Event	This event specifies that a timestamp event has been placed ahead of next event. The most significant word in the event-information field contains the full 32-bit timestamp.

3.15.3.6 Frame-Based Events

Event Number	Name	Description
x'40'=1000000	Frame Event (good frame)	A valid frame was received from the POS-PHY interface.
x'41'=1000001	Frame Event (error)	Error bit was detected on from the POS-PHY interface.
x'42'=1000010	Frame Event (protocol error)	Unexpected start or end of packet received from the POS-PHY interface.
x'43'=1000011	Reserved	Reserved for future use as event for Frame Dropped - Lack of buffers.
x'44'=1000100	Reserved	Reserved.
x'45'=1000101	Reserved	Reserved.
x'46'=1000110	Reserved	Reserved.
x'47'=1000111	Reserved	Reserved.

3.15.3.7 PCORE Events

Event Number	Name	Description
x'50'=1010000	PCORE Event	Defined by software.
x'51'=1010001	PCORE Event	Defined by software.
x'52'=1010010	PCORE Event	Defined by software.
x'53'=1010011	PCORE Event	Defined by software.
x'54'=1010100	PCORE Event	Defined by software.
x'55'=1010101	PCORE Event	Defined by software.
x'56'=1010110	PCORE Event	Defined by software.
x'57'=1010111	PCORE Event	Defined by software.

3.15.3.8 System-Receive-Queue Events

Event Number	Name	Description
x'5C'=1011100	System-Receive-Queue Start-of-Buffer Event	This event specifies the beginning of a system receive queue buffer, the event information contains the lower bound of the last buffer.
x'5D'=1011101	System-Receive-Queue End-of-Buffer Event	This event specifies the end of a system receive queue buffer, the event information contains the lower bound of the next buffer.

3.15.3.9 RXAAL Picoprocessor Generated Events

Event Number	Name	Description
x'3F'=0111111	No descriptor available event	This event specifies that REASM is doing scatter/cut through and attempted to dequeue a system page address or DMA descriptor address from RXQUE and the Receive Queue was empty. This event is surfaced to the user so the packet can be used and the DMA list recovered.
x'6E'=1101110	No header available event	This event specifies that REASM is doing scatter/cut through and attempted to dequeue the optional header descriptor from RXQUE and the Receive Queue was empty. This event is surfaced to the user so the packet can be used and the DMA list recovered.
x'6F'=1101111	No packet header available event	This event specifies that REASM is doing scatter/cut through and attempted to dequeue a system page address or DMA descriptor address for the packet header from RXQUE and the Receive Queue was empty. This event is surfaced to the user so the packet can be used and the Dma list recovered.

3.15.4 RXQUE Structure

Each queue has a number of registers that define the queue and its behavior:

Lower Bound Pointer to starting address of queue's buffer.

Properties Indicates the queue's size, type, and behavior.

Head Pointer Pointer to head of queue.

Tail Pointer Pointer to the next free entry in queue - points to head if queue is full or empty.

Queue Length Current length of the queue.

Threshold Length threshold used to generate interrupts.

Next Lower Bound Pointer to starting address of a system receive queue's next buffer.

3.15.5 RXQUE Initialization

To set up a receive queue, at least two pieces of information are needed. The first is the receive queue's set of properties, and the second is its base address.

The following restrictions should be taken into account when setting up a queue:

- The properties register must be set up before the lower-bound and next-lower-bound registers can be set up.
- The lower bound and next lower bound must be at least 1 K aligned. The low order 10 bits of these registers are not writable, so the minimum physical size of a receive queue is 1024 bytes (256 32-bit entries). The alignment should correspond to the size specified in the properties register.
- The head and tail pointers are initialized when the lower bound register is written. These registers are only writable for diagnostic purposes.
- The threshold is level sensitive, so as long as the queue length is greater than or equal to the threshold, the appropriate status bit is driven.
- All registers, except the threshold and next-lower-bound registers, can only be written in diagnostic mode and are intended to only be written once when they are set up.

3.15.6 RXQUE Event Routing

Events are routed to a receive queue based on the current event type and mode of the chip. Events fall into these categories:

- Normal Events
- Error Events
- Counter Events
- Transmit Complete Events
- DMA Events (TX/RX)
- ABR Events
- POOLS Status Events

See Table 19: *Event Summary and Routing Information* on page 352 to see how the different events are categorized.

All events other than normal, DMA, and error events are routed using the corresponding RXQUE Event Routing Registers.

Normal events are always routed to the receive queue specified in the receive portion of the LCD.

DMAQS specifies the route for all DMA events.

Error events are routed based on the values of the “receive bad frame mode” bit and the “always route error events” mode bit in RXQUE Control Register. If the “always route error events” bit is on, the error events are always routed to the error queue. Otherwise, if the receive bad frame mode is on, the error events are routed to the receive queue specified in the receive portion of the LCD just like a normal event would be. When receive bad frames is off, the error events are routed to the error queue.

3.15.7 RXQUE Normal Operation

This section describes how to use the receive queues (rxq) and the rxq operations.

The receive queue contains events for the end user to process. These events are obtained by the user by executing the rxq deq operation. The user can be notified of new events by setting up the threshold and interrupt enable registers appropriately. Otherwise, the rxq length register can be polled to check for events.

The deq operation is executed by reading the deq register address for the appropriate rxq. The event at the head of the queue is returned and the event is removed from the queue. Some events have a packet/cell buffer associated with it. This buffer is owned by the user, and it is the user's responsibility to free this buffer.

The following pseudo code illustrates how a receive queue could be processed:

Figure 31: RXQUE Dequeue Event Loop

```
// rxq was polled or int occurred to get here

Event = RXQUE->Deq;                          // read an event from rxq

if (Event neq 0) {                           // need to check for null event
    EventType = Event & 0x7f;                // calc event type
    Event = Event & ~(0x7f);                 // calc lc or buffer ptr

    switch (EventType) {
        case(Event1):
            ProcessSimpleEvent1(Event);
            break;
        case(Event2):
            ProcessSimpleEvent2(Event);
            break;
        .
        .
        .
        case(EventX):
            ProcessSimpleEventX(Event);
            break;
    }
}
```

3.15.8 RXQUE Queue Full Operation

When a receive queue is full (length is equal to maximum length), the appropriate status bit is set. When a queue is full, all subsequent events are flushed until room is available in the receive queue. If a buffer was associated with the event and the RXQUE-Properties-Register bit Disable Auto-Free is not set, the buffer is freed back to POOLS.

When an event is dropped, the event dropped status bit is set and the event data that was dropped can be found in RXQUE Last Event Dropped Register. The RXQUE Last Event Dropped Register will not be changed until the event dropped status bit is cleared.

It is not good to let a receive queue become full.

3.15.9 RXQUE Event Timestamping

When timestamp mode is set in the RXQUE Control Register, events are timestamped. When timestamping is enabled, a timestamp event is placed in the corresponding rxq followed by the actual event. The event information of the timestamp event carries the timestamp. The timestamp is determined from the RXQUE Timestamp Register, RXQUE Timestamp Pre-Scaler Register, and the RXQUE Timestamp Shift Register.

If the corresponding rxq is full, both events are dropped. It is possible to lose only the timestamp event or lose the actual event depending on the length of the queue and the timing of the dequeue operations.

3.15.10 RXQUE System Receive Queues

To set up a system receive queue, set the “Diagnostic-Mode” bit in the RXQUE Control Register. Next, set the system receive queue bit in the RXQUE Properties Register. Load the upper bound and size of event fields, as well. After this, allocate two identical buffers in system memory. Let each buffer be large enough to contain N events (the upper bound field prescribes the value N) and initialize both to all zeros. Write one buffer’s starting address into the RXQUE Lower Bound Register (LOBR), and write the other’s starting address into the RXQUE Next Lower Bound Register (NLBR). Finally, reset the diagnostic mode bit in the RXQUE Control Register. System-receive-queue setup is complete.

The first event enqueued to a system receive queue causes RXQUE to begin filling the buffer which LOBR references. RXQUE fills the buffer’s first entry with a “System-Receive-Queue Start-of-Buffer” event whose information is the value ‘0’. After this, RXQUE fills the buffer’s second entry with the enqueued event and writes the value x‘2’ into the RXQUE Length Register (LENR).

The second event enqueued to the system receive queue causes RXQUE to fill the buffer’s third entry and write the value x‘3’ into LENR.

The third event enqueued to the system receive queue causes RXQUE to fill the buffer’s fourth entry and write the value x‘4’ into LENR.

This continues until LENR contains the value x‘N-1’. At that time, RXQUE fills the buffer’s Nth entry with a System-receive-queue end-of-buffer event whose information is the value in NLBR. After this, RXQUE begins filling the buffer which NLBR references. RXQUE fills its first entry with a “System-Receive-Queue Start-of-Buffer” event whose information is the value in LOBR. After this, RXQUE copies the contents of NLBR into LOBR and writes the value ‘1’ into LENR. Finally, RXQUE writes the value ‘0’ into NLBR. Subsequent events enqueued to the system receive queue fill the buffer which LOBR references. To prevent the system receive queue from becoming full, write a non-zero value into NLBR.

The system receive queue becomes full when the value in LENR becomes x‘N-1’ while NLBR contains the value ‘0’. At that time, RXQUE fills the buffer’s Nth entry with a system-receive-queue end-of-buffer event whose information is the value ‘0’. RXQUE writes the value N into LENR and preserves the contents of LOBR while dropping subsequent enqueued events. To restart the system receive queue from the “full” state, write a non-zero value into NLBR. After restarting, the next event enqueued to the system receive queue causes RXQUE to begin filling the buffer which NLBR references. RXQUE fills the buffer’s first entry with a system-receive-queue start-of-buffer event whose information is the value preserved in LOBR. RXQUE fills the buffer’s second entry with the enqueued event. After this, RXQUE copies the contents of NLBR into LOBR and writes the value x‘2’ into LENR. Finally, RXQUE writes the value ‘0’ into NLBR. Subsequent events enqueued to the system receive queue fill the buffer which LOBR references. To prevent the system receive queue from becoming full, write a non-zero value into NLBR.

The RXQUE Queues’ Status Register bit “Threshold Exceeded” indicates that the value in LENR is greater than or equal to the value in the RXQUE Threshold Register while NLBR contains the value ‘0’. To reset this status bit, write a non-zero value into NLBR.

Events enqueued to a system receive queue may not be dequeued via the RXQUE Dequeue Register. To dequeue from a system receive queue, poll system memory directly. A buffer’s entry is filled if its value is non-zero.

RXQUE synchronizes its internal-register operations with the initiation, rather than completion, of its system-memory operations. Therefore, the state of system memory lags the state of RXQUE.

3.15.11 RXQUE Lower Bound Registers

These registers specify the lower bound of the corresponding receive queue data structure. The head and tail of the receive queue are initialized when this register is written. When the receive queue wraps past the upper bound, it wraps back to the value in the lower bound register, thus implementing the receive queue as a circular buffer.

When this register is written, the corresponding receive queue is essentially reset. This is because the head, tail, and length of the queue are all reset.

The length of the RXQUE Lower Bound Register is 64 bits if all three of the following conditions are met; otherwise, the length is 32 bits.

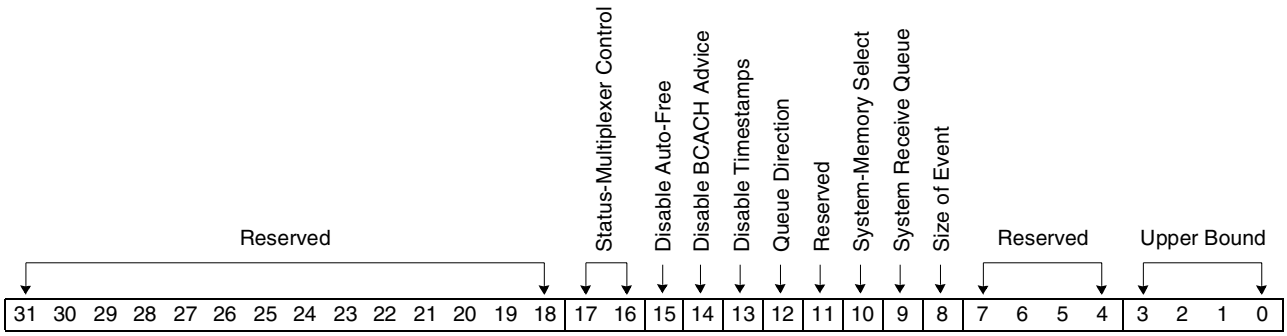
- **System Receive-Queue** in the RXQUE Properties Register is set.
- **System-Memory Select** in the RXQUE Properties Register indicates “PCI Memory.”
- **Enable Master 64-bit Addressing** in the PCINT 64-bit Control Register is set.

Length	32 or 64 bits	
Type	Read/Write	
Address	Queue 0	XXXX 1800
	Queue 1	XXXX 1840
	Queue 2	XXXX 1880
	Queue 3	XXXX 18C0
	Queue 4	XXXX 1900
	Queue 5	XXXX 1940
	Queue 6	XXXX 1980
	Queue 7	XXXX 19C0
	Queue 8	XXXX 1A00
	Queue 9	XXXX 1A40
	Queue 10	XXXX 1A80
	Queue 11	XXXX 1AC0
	Queue 12	XXXX 1B00
	Queue 13	XXXX 1B40
	Queue 14	XXXX 1B80
	Queue 15	XXXX 1BC0
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	During normal operations, these registers are read only. These registers can only be written when the diagnostic bit has been set in the control register. The lower bound registers must be at least 1 K aligned (low order 10 bits not writable). The alignment should also correspond to the size specified in the upper bound register. For example, it should be 4 K aligned if the upper bound specifies 4 K size.	

3.15.12 RXQUE Properties Registers

These registers specify the properties of the corresponding receive queue.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 1808
	Queue 1	XXXX 1848
	Queue 2	XXXX 1888
	Queue 3	XXXX 18C8
	Queue 4	XXXX 1908
	Queue 5	XXXX 1948
	Queue 6	XXXX 1988
	Queue 7	XXXX 19C8
	Queue 8	XXXX 1A08
	Queue 9	XXXX 1A48
	Queue 10	XXXX 1A88
	Queue 11	XXXX 1AC8
	Queue 12	XXXX 1B08
	Queue 13	XXXX 1B48
	Queue 14	XXXX 1B88
	Queue 15	XXXX 1BC8
Power On Reset Value		x‘0001 0001’
Restrictions	Bits 11-0 may only be written when the diagnostic bit has been set in the control register. There are no restrictions for bits 32-12.	



Bit(s)	Name	Description
31-18	Reserved	Reserved.
17-16	Status-Multiplexer control	00 Select “Full/Empty” 01 Select “Threshold Exceeded” (power-on value) 10 Select “Head Valid” 11 Reserved

Bit(s)	Name	Description
15	Disable Auto-Free	Inhibits freeing of packet-buffers when the receive queue is full.
14	Disable BCACH Advice	When set, the BCACH advice is disabled for this queue. This is necessary in order to use a queue as a general purpose container for user data.
13	Disable Timestamps	When set, timestamps are disabled for this queue. This is necessary in order to run cut through modes.
12	Queue Direction	When set, the direction of the queue is assumed to be reversed. This only affects the full condition and the threshold exceeded condition. When this bit is set, the polarity of these status signals changes. Thus, the full condition becomes an empty condition, and the two threshold conditions trigger when the length of the queue is less than the corresponding threshold instead of greater than or equal. This mode is mainly used for queues that relay information from the system to the PNR. Also, event enqueues to a queue that is reversed do not start the event latency timer (since no new event for system has arrived).
11	Reserved	Reserved.
10	System-Memory Select	This is valid only when bit 9 (System Receive Queue) is set. 0 PCI Memory (power-on value) 1 On-Chip Memory
9	System Receive Queue	
8	Size of Event	0 32 bits (power-on value) 1 64 bits
7-4	Reserved	Reserved.
3-0	Upper Bound	This specifies the encoded upper bound of the corresponding receive queue data structure. The actual upper bound is calculated by adding the decoded queue size to the lower bound. When the receive queue wraps past the upper bound, it wraps back to the lower bound register, thus implementing the receive queue as a circular buffer. 0000 Reserved 0001 256 entries (power-on value) 0010 512 entries 0011 1024 entries 0100 2 K entries 0101 4 K entries 0110 8 K entries 0111 16 K entries 1000 32 K entries 1001 64 K entries 101- Reserved 11-- Reserved

3.15.13 RXQUE Head Pointer Registers

These registers point to the head element of the corresponding receive queue. During normal operations, these registers do not need to be read or written, as they are used by the PNR to implement the receive queues. These registers are initialized when the lower bound register for the corresponding receive queue is written.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 1810
	Queue 1	XXXX 1850
	Queue 2	XXXX 1890
	Queue 3	XXXX 18D0
	Queue 4	XXXX 1910
	Queue 5	XXXX 1950
	Queue 6	XXXX 1990
	Queue 7	XXXX 19D0
	Queue 8	XXXX 1A10
	Queue 9	XXXX 1A50
	Queue 10	XXXX 1A90
	Queue 11	XXXX 1AD0
	Queue 12	XXXX 1B10
	Queue 13	XXXX 1B50
	Queue 14	XXXX 1B90
	Queue 15	XXXX 1BD0
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. These registers can only be written when the diagnostic bit has been set in the control register. The head pointer registers are four-byte aligned (low order two bits not writable). Bits 31-19 are calculated internally, and are not writable.	

3.15.14 RXQUE Tail Pointer Registers

These registers point to the next free element of the corresponding receive queue. During normal operations, these registers do not need to be read or written, as they are used by the PNR to implement the receive queues. These registers are initialized when the lower bound register for the corresponding receive queue is written.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 1814
	Queue 1	XXXX 1854
	Queue 2	XXXX 1894
	Queue 3	XXXX 18D4
	Queue 4	XXXX 1914
	Queue 5	XXXX 1954
	Queue 6	XXXX 1994
	Queue 7	XXXX 19D4
	Queue 8	XXXX 1A14
	Queue 9	XXXX 1A54
	Queue 10	XXXX 1A94
	Queue 11	XXXX 1AD4
	Queue 12	XXXX 1B14
	Queue 13	XXXX 1B54
	Queue 14	XXXX 1B94
	Queue 15	XXXX 1BD4
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations, these registers are read only. These registers can only be written when the diagnostic bit has been set in the control register. The tail pointer registers are 4-byte aligned (low order two bits not writable). Bits 31-19 are calculated internally and are not writable.	

3.15.15 RXQUE Length Registers

These registers specify the length (number of valid entries) of the corresponding receive queue. They can be used to query the status of a receive queue.

This register is cleared when the corresponding lower bound is written.

Length	32 bits	
Type	Read Only	
Address	Queue 0	XXXX 1818
	Queue 1	XXXX 1858
	Queue 2	XXXX 1898
	Queue 3	XXXX 18D8
	Queue 4	XXXX 1918
	Queue 5	XXXX 1958
	Queue 6	XXXX 1998
	Queue 7	XXXX 19D8
	Queue 8	XXXX 1A18
	Queue 9	XXXX 1A58
	Queue 10	XXXX 1A98
	Queue 11	XXXX 1AD8
	Queue 12	XXXX 1B18
	Queue 13	XXXX 1B58
	Queue 14	XXXX 1B98
	Queue 15	XXXX 1BD8
Power On Reset Value		x‘0000 0000’
Restrictions	These registers can only be written in diagnostic mode.	

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Queue Length	Specifies the length of the corresponding receive queue.

3.15.16 RXQUE Threshold Registers

These registers specify a queue length threshold at which the corresponding status bit is generated. These registers should be set equal to the number of queue entries that should cause status to be generated. For example, if the value was set to five, then no interrupt would be generated until five or more events were queued on the corresponding receive queue. The threshold is level sensitive, so as long as the length is greater than or equal to the threshold, the corresponding status bit is set. When this register is set to ’0’, no thresholding is done.

When the direction bit is set for a receive queue, the threshold has the opposite polarity. For example, as long as there are more events in the queue than specified in the threshold register, no status would be raised.

Length	32 bits	
Type	Read/Write	
Address	Queue 0	XXXX 181C
	Queue 1	XXXX 185C
	Queue 2	XXXX 189C
	Queue 3	XXXX 18DC
	Queue 4	XXXX 191C
	Queue 5	XXXX 195C
	Queue 6	XXXX 199C
	Queue 7	XXXX 19DC
	Queue 8	XXXX 1A1C
	Queue 9	XXXX 1A5C
	Queue 10	XXXX 1A9C
	Queue 11	XXXX 1ADC
	Queue 12	XXXX 1B1C
	Queue 13	XXXX 1B5C
	Queue 14	XXXX 1B9C
	Queue 15	XXXX 1BDC
Power On Reset Value		x‘0000 0000’
Restrictions	None	

Bit(s)	Name	Description
31-17	Reserved	Reserved.
16-0	Queue Length Threshold	Set equal to the number of queue entries that should cause status to be generated. When set to ‘0’, no thresholding is done.

3.15.17 RXQUE Dequeue Registers

These registers are used to retrieve the event at the head of the corresponding receive queue.

The length of an RXQUE Dequeue Register is 64 bits if Size of Event is set in its corresponding RXQUE Properties Register; otherwise, the length is 32 bits.

Length	32 or 64 bits	
Type	Read Only	
Address	Queue 0	XXXX 1820
	Queue 1	XXXX 1860
	Queue 2	XXXX 18A0
	Queue 3	XXXX 18E0
	Queue 4	XXXX 1920
	Queue 5	XXXX 1960
	Queue 6	XXXX 19A0
	Queue 7	XXXX 19E0
	Queue 8	XXXX 1A20
	Queue 9	XXXX 1A60
	Queue 10	XXXX 1AA0
	Queue 11	XXXX 1AE0
	Queue 12	XXXX 1B20
	Queue 13	XXXX 1B60
	Queue 14	XXXX 1BA0
	Queue 15	XXXX 1BE0
Power On Reset Value		x‘0000 0000’
Restrictions	This is a read only register, and all writes will be ignored. Events are only returned when the diagnostic bit is reset in the control register, otherwise zero will be returned.	

3.15.18 RXQUE Enqueue Registers

These registers are used to enqueue user events at the tail of the corresponding receive queue.

The length of an RXQUE Enqueue Register is 64 bits if Size of Event is set in its corresponding RXQUE Properties Register; otherwise, the length is 32 bits.

Length	32 or 64 bits	
Type	Read/Write	
	Queue 0	XXXX 1828
	Queue 1	XXXX 1868
	Queue 2	XXXX 18A8
	Queue 3	XXXX 18E8
	Queue 4	XXXX 1928
	Queue 5	XXXX 1968
	Queue 6	XXXX 19A8
	Queue 7	XXXX 19E8
	Queue 8	XXXX 1A28
	Queue 9	XXXX 1A68
	Queue 10	XXXX 1AA8
	Queue 11	XXXX 1AE8
	Queue 12	XXXX 1B28
	Queue 13	XXXX 1B68
	Queue 14	XXXX 1BA8
	Queue 15	XXXX 1BE8
Power On Reset Value		x‘0000 0000’
Restrictions	All reads result in zero. RXQUE should be enabled to do this.	

3.15.19 RXQUE Next Lower Bound Registers

These registers specify the next lower bound of the corresponding system receive queue data structure. See *3.15.10 RXQUE System Receive Queues* on page 364 for instruction about managing system receive queues.

The length of the RXQUE Next Lower Bound Register is the same as the length of the RXQUE Lower Bound Register. See *3.15.11 RXQUE Lower Bound Registers* on page 366 for conditions which determine the length.

Length	32 or 64 bits	
Type	Read/Write	
	Queue 0	XXXX 1830
	Queue 1	XXXX 1870
	Queue 2	XXXX 18B0
	Queue 3	XXXX 18F0
	Queue 4	XXXX 1930
	Queue 5	XXXX 1970
	Queue 6	XXXX 19B0
	Queue 7	XXXX 19F0
	Queue 8	XXXX 1A30
	Queue 9	XXXX 1A70
	Queue 10	XXXX 1AB0
	Queue 11	XXXX 1AF0
	Queue 12	XXXX 1B30
	Queue 13	XXXX 1B70
	Queue 14	XXXX 1BB0
	Queue 15	XXXX 1BF0
Power On Reset Value		x‘0000 0000 0000 0000’
Restrictions	None	

3.15.20 RXQUE Last Event Dropped Register

This register contains the last event that was dropped. It holds its value until the event dropped status bit is cleared.

The length of the RXQUE Last Event Dropped Register is 64 bits if Size of Dropped Event is set in the RXQUE Status Register; otherwise, the length is 32 bits.

Length	32 or 64 bits
Type	Read/Write
Address	XXXX 1C10
Power On Reset Value	x‘0000 0000 0000 0000’
Restrictions	None

3.15.21 RXQUE Timestamp Register

This register is used to specify the current timestamp measured using the timestamp pre-scaler ticks. It counts based on the value in the RXQUE Timestamp Pre-Scaler Register. It can be read or written at any time. It is cleared when the pre-scaler register is written.

Length	32 bits
Type	Read/Write
Address	XXXX 1C30
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.15.22 RXQUE Timestamp Pre-Scaler Register

This register is used to specify the time interval of each timestamp timer tick. It determines the number of 15 ns intervals between timestamp timer ticks. The value in the register plus one is the number of 15 ns intervals between timestamp timer ticks. The default value of '0' means that the timestamp timer ticks every 15 ns. If a value of four is placed in this register, the timestamp timer ticks every 75 ns (5 x 15 ns).

Length 32 bits

Type Read/Write

Address XXXX 1C38

Power On Reset Value x'0000 0000'

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Timestamp Pre-Scaler	The value plus one is the number of 15 ns intervals between timestamp timer ticks. The default value of '0' means that the timestamp timer ticks every 15 ns.

3.15.23 RXQUE Timestamp Shift Register

This register determines the number of bits that the timestamps are shifted. For example, if a value of '0' is placed in this register, then the timestamp is not shifted, and the low order seven bits are lost. If a value of '2' is placed in this register, then the timestamps are shifted two places and only the low order five bits of the timestamp are lost. This allows the user to control what portion of the timestamp is lost due to the low order event bits.

Length 32 bits

Type Read/Write

Address XXXX 1C3C

Power On Reset Value x'0000 0002'

Restrictions None

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	Timestamp Shift	Number of bits the timestamps are shifted.

3.15.24 RXQUE Event Routing Registers

These registers contain the receive queue to which different types of events should be routed. See Table 19: *Event Summary and Routing Information* on page 352 for event type mappings.

Length	32 bits	
Type	Read/Write	
Address	Event Tx Complete	XXXX 1C40
	Event Counter Overflow	XXXX 1C44
	Event Error	XXXX 1C48
	Event POOLS Status	XXXX 1C54
	Event ABR	XXXX 1C58
Power On Reset Value		x‘0000 0000’
Restrictions	None	

Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Destination Receive Queue	Receive queue to which the event should be routed.

3.15.25 RXQUE Event Latency Timer Register

This register is used to specify the event latency time interval. It is specified in 15 ns intervals. When a new event is placed on a receive queue, the event latency timer is started (if not already started). When this timer expires, the event latency timer expired status bit is set, and the timer is stopped. The status bit must be reset before the timer is started again. Every time the status register (or prioritized status) is accessed, the timer is stopped. If this register is written while the timer is running, the new value takes effect immediately. If this register is set to ‘0’, the latency timer does not run.

Length	32 bits
Type	Read/Write
Address	XXXX 1C20
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.15.26 RXQUE Queues Status Register

This register indicates the status for all receive queues.

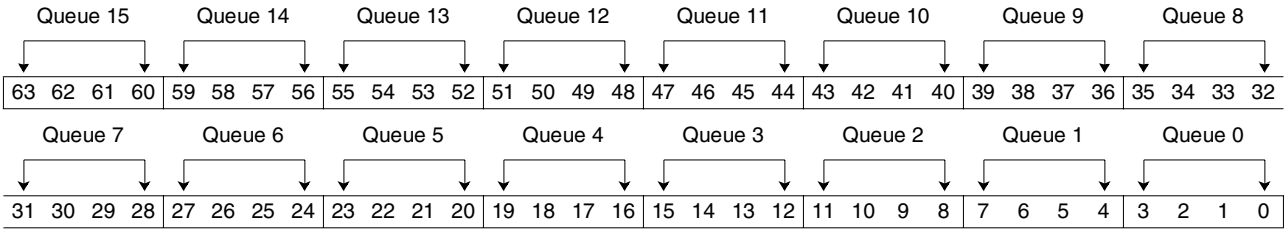
Length 64 bits

Type Read Only

Address XXXX 1D40

Power On Reset Value x‘0000 0000 0000 0000’

Restrictions This is a read only register.



Bit(s)	Name	Description
63-60	Status-nibble for queue 15	For each 4-bit range, bit encoding is as follows: 3 Reserved. 2 Head valid: This is set when the head is valid for the queue. If this bit is set, then a deque operation should complete successfully. 1 Threshold exceeded: This is set when the queue-length register equals or exceeds the value in the queue-threshold register. 0 Queue Full/Empty: This is set when the queue-length register is equal to the queue-maximum-length register. When the direction of the queue is reversed, this bit is set when the queue is empty.
59-56	Status-nibble for queue 14	
55-52	Status-nibble for queue 13	
51-48	Status-nibble for queue 12	
47-44	Status-nibble for queue 11	
43-40	Status-nibble for queue 10	
39-36	Status-nibble for queue 9	
35-32	Status-nibble for queue 8	
31-28	Status-nibble for queue 7	
27-24	Status-nibble for queue 6	
23-20	Status-nibble for queue 5	
19-16	Status-nibble for queue 4	
15-12	Status-nibble for queue 3	
11-8	Status-nibble for queue 2	
7-4	Status-nibble for queue1	
3-0	Status-nibble for queue 0	

3.15.27 RXQUE Interrupt Enable Registers

This register is used to specify which status register bits should be used to generate interrupts. Each mask register is used to drive a different RXQUE status bit in INTST. This makes it possible for different RXQUE status bits to generate interrupts on the PNR's $\overline{\text{MINTA}}$ and $\overline{\text{MINT2}}$ pins. See *RXQUE Status Register* for the bit descriptions.

Length	32 bits	
Type	Clear/Set	
Address	Enable 1	XXXX 1C80 and 1C84
	Enable 2	XXXX 1C88 and 1C8C
Power On Reset Value	Enable 1-2	x'0000 0000'
Restrictions	None	

3.15.28 RXQUE Status Register

This register contains the status bits used to relay RXQUE status information.

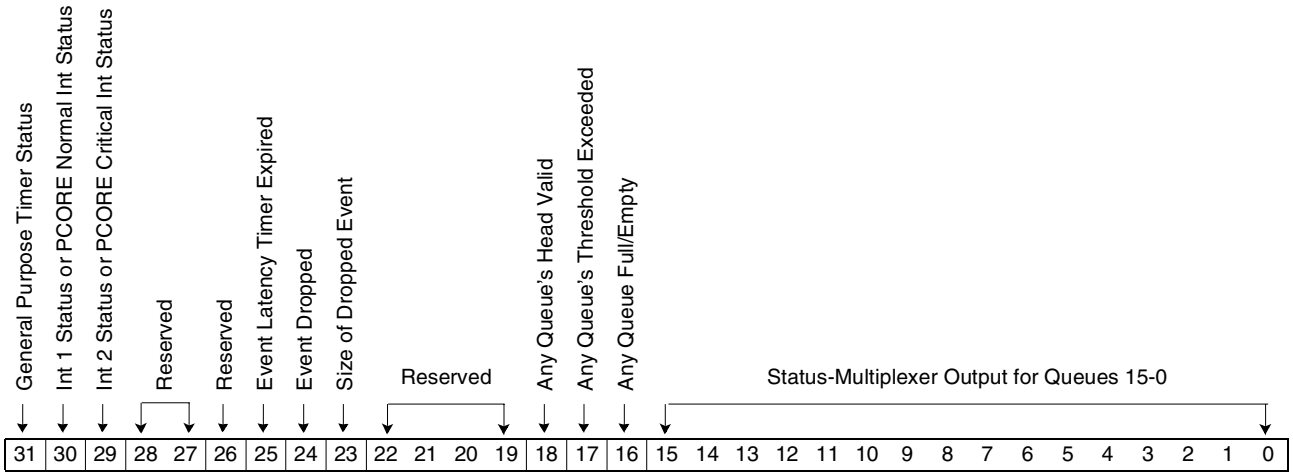
Length 32 bits

Type Clear/Set

Address XXXX 1CA0 and CA4

Power On Reset Value x‘0000 0000’

Restrictions Only bits 26 down to 23 are writable.



Bit(s)	Name	Description
31	General Purpose Timer Status	This is a mirror of the general purpose timer status bit in interrupt status.
30	Int 1 Status or PCORE Normal Int Status	When read from the PCI bus, this bit indicates if there is status other than RXQUE status and general purpose timer status in the interrupt source register using interrupt mask register 1 as a mask. When read from the PCORE polling interface, the mask used is the PCORE normal interrupt register.
29	Int 2 Status or PCORE Critical Int Status	When read from the PCI bus, this bit indicates if there is status other than RXQUE status and general purpose timer status in the interrupt source register using interrupt mask register 2 as a mask. When read from the PCORE polling interface, the mask used is the PCORE critical interrupt register.
28-27	Reserved	Reserved.
26	Sequence-Error in 64-Bit Register-Access	Sequence-Error in 64-Bit Register-Access
25	Event Latency Timer Expired	When this bit is set, the event latency timer has expired. This indicates that new events are waiting to be processed on some queue(s) and the queue has not been processed for a period equal to the latency timer. This bit must be reset to re-enable the event latency timer.
24	Event Dropped	When this bit is set, at least one event has been dropped. RXQUE Last Event Dropped Register contains the event that was dropped.
23	Size of Dropped Event	0 32 bits 1 64 bits This bit does not generate interrupts.

Bit(s)	Name	Description
22-19	Reserved	Reserved.
18	Any Queue's Head Valid	
17	Any Queue's Threshold Exceeded	
16	Any Queue Full/Empty	
15-0	15-0: Status-Multiplexer Output for Queues 15-0	Reports either "Head Valid," "Threshold Exceeded," or "Queue Full/Empty" according to the setting of the Status-Multiplexer-Control field in the RXQUE Properties Register.

3.15.29 RXQUE Enabled Status Registers 1 and 2

These registers return the status register masked with the corresponding Interrupt Enable register. See *3.15.28 RXQUE Status Register* on page 381 for the bitwise descriptions of these registers.

Length 32 bits

Type Read Only

Address Enable Status 1 XXXX 1CB0

Enable Status 2 XXXX 1CB4

Power On Reset Value x'0000 0000'

Restrictions None

3.15.30 RXQUE Control Register

This register is used to set RXQUE modes. It contains the mode bits that specify how RXQUE is to operate.

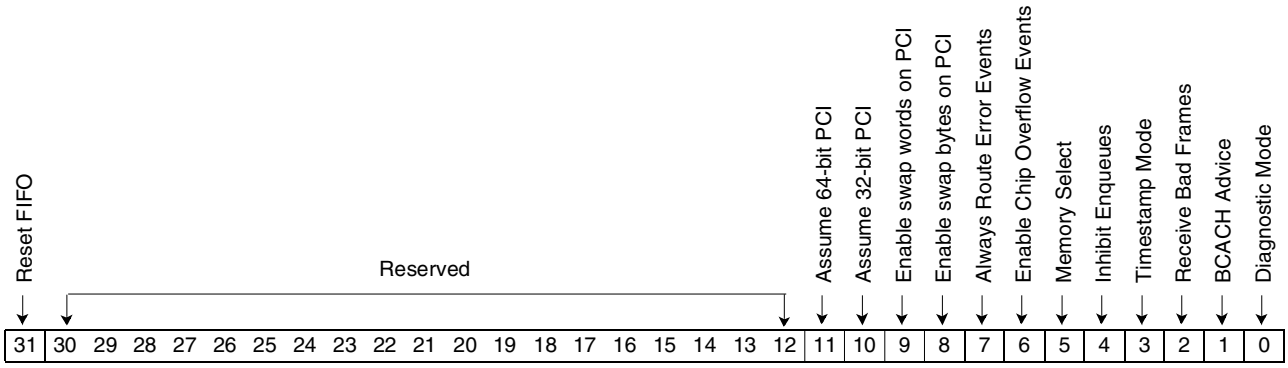
Length 32 bits

Type Clear/Set

Address XXXX 1C00 and C04

Power On Reset Value x'0000 0300'

Restrictions None



Bit(s)	Name	Description
31	Reset FIFO	When this bit is set, the internal FIFO is flushed, and this bit is reset. The result is this bit will always be read as a '0'. This bit can only be set in diagnostic mode.
30-12	Reserved	Reserved.
11	Assume 64-bit PCI	
10	Assume 32-bit PCI	
9	Enable swap words on PCI	This bit is automatically set at power-on.
8	Enable swap bytes on PCI	This bit is automatically set at power-on.
7	Always route error events	When this bit is set, all error events are routed to the error queue even if rx bad frames (bit2) is turned on. When cleared, error events are only routed to the error queue if rx bad frames is turned off. This bit allows the user to keep bad frames in time sequence with good frames or to route them to the error queue. The clear state of this bit is code compatible with previous versions of the processor.
6	Enable chip overflow events	When set, the chip level counter overflow events are surfaced.
5	Memory select	When this bit is set, RXQUE will use Packet Memory instead of Control Memory to store the event queues.
4	Inhibit enqueues	When this bit is set, the enq state machine will not accept any new enq requests. This should be used in extreme cases as it holds off all enqueues indefinitely.
3	Timestamp mode	When this bit is set, timestamp events are inserted before each real event. The timestamps correspond to when the event happened on chip. When this bit is off, timestamps can still be read from the timestamp register. The timestamps corresponds to when the event was dequeued in this scenario.

Bit(s)	Name	Description
2	Receive bad frames	When this bit is set, bad frame events (all error events), will be received in the normal rxq defined in the LCD. All buffers are not freed, and the packet address is raised in the event data. When this bit is reset, bad frame events are routed to the rxq specified by the Error Event Receive Queue Register. All packet based events will carry the LC address in the event data instead of the packet address. All buffers are freed back to POOLS. **Note:** This bit should only be changed sparingly because it changes the way packets are freed and what is surfaced in an event (LCD vs. frame ptr). It should really only be changed when the receive side is inactive.
1	BCACH advice	This bit, when set, allows RXQUE to give BCACH cache fill advice based on events that are dequeued.
0	Diagnostic mode	When this bit is set or when the chip is disabled, the RXQUE entity is in diagnostic mode and primitive execution is disabled.

3.15.31 Debugging Register Access

This section is a very brief documentation of access that has been put in for the internal registers of RXQUE. These addresses need not be written or read during normal operations.

3.15.31.1 RXQUE RXQ State Machine Variable Register

Main state variable for RXQUE processing state machine.

Length 32 bits

Type Read/Write

Address XXXX 1E80

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-0	Receive Queue Machine State	Debug access to the RXQUE state machine.

3.15.31.2 RXQUE RXQ ENQ State Machine Variable Register

Main state variable for RXQUE processing state machine.

Length 32 bits

Type Read/Write

Address XXXX 1E84

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-3	Reserved	Reserved.
2-0	Receive Queue Main Machine State	Debug access to the main RXQUE state machine.

3.15.31.3 RXQUE Enq FIFO Head Ptr Register

This register is used to maintain the enqueue FIFO. Points to the head FIFO entry in the FIFO array. The MSB bit is used to determine if the head is chasing the tail, and is inverted each time the head pointer wraps.

Length 32 bits

Type Read/Write

Address XXXX 1E88

Power On Reset Value x‘0000 0000’

Restrictions Can only be written in diagnostic mode.

Bit(s)	Name	Description
31-5	Reserved	Reserved.
4-0	FIFO Head Pointer	Pointer to the head entry in the FIFO.

3.15.31.4 RXQUE Enq FIFO Tail Ptr Register

This register is used to maintain the enqueue FIFO. Points to the next free FIFO entry in the FIFO array. The MSB bit is used to determine if the head is chasing the tail, and is inverted each time the tail pointer wraps.

Length 32 bits

Type Read/Write

Address XXXX 1E8C

Power On Reset Value x‘0000 0000’

Restrictions Can only be written in diagnostic mode.

Bit(s)	Name	Description
31-5	Reserved	Reserved.
4-0	FIFO Tail Pointer	Pointer to the tail entry in the FIFO.

3.16 Nodal Processor Bus Interface Logic (NPBUS)

This entity controls the signals of the NP Bus. The PHY registers are accessible to the processor via the address space of the PNR. In addition, the operation of the network interface logic is affected by the NPBUS Status Register.

This entity also contains a simple processor that can initialize chip registers at boot time by reading a data stream from EPROM which specifies the address of registers and data values to which the registers are to be initialized. See *3.16.8 EPROM Instructions* on page 394 for a description of the EPROM instructions.

3.16.1 NPBUS Control Register

This register is used to report PHY level hardware errors and interrupts.

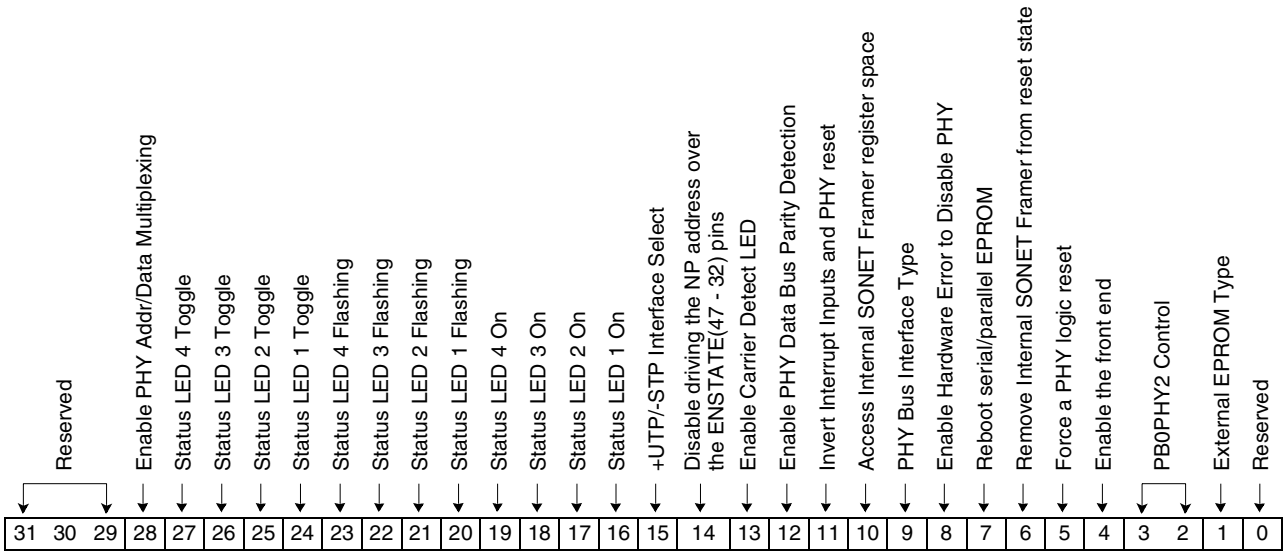
Length 32 bits

Type Clear/Set

Address XXXX 2000 and 2004

Power On Reset Value x'0000 2010'

Restrictions None



Bit(s)	Name	Description
31-29	Reserved	Reserved.
28	Enable PHY Addr/Data multiplexing	This bit set to a '1' will enable the ALE1, ALE2, and ALE3 control lines for PHY and Parallel EPROM accesses so that additional address bytes can be latched for up to 24Meg of addressing. Since there is an access speed penalty for this, the default is a '0' for this function.
27	Status LED 4 Toggle	When this bit is set, the state of bit 19 of this register will be toggled by repeatedly setting bit 19.

Bit(s)	Name	Description
26	Status LED 3 Toggle	When this bit is set, the state of bit 18 of this register will be toggled by repeatedly setting bit 18.
25	Status LED 2 Toggle	When this bit is set, the state of bit 17 of this register will be toggled by repeatedly setting bit 17.
24	Status LED 1 Toggle	When this bit is set, the state of bit 16 of this register will be toggled by repeatedly setting bit 16.
23	Status LED 4 Flashing	When set to a '1', this bit will flash status indicator LED 4. Bit 19 of the register will override this bit.
22	Status LED 3 Flashing	When set to a '1', this bit will flash status indicator LED 3. Bit 18 of the register will override this bit.
21	Status LED 2 Flashing	When set to a '1', this bit will flash status indicator LED 2. Bit 17 of the register will override this bit.
20	Status LED 1 Flashing	When set to a '1', this bit will flash status indicator LED 1. Bit 16 of the register will override this bit.
19	Status LED 4 On	When set to a '1', this bit will turn on status indicator LED 4.
18	Status LED 3 On	When set to a '1', this bit will turn on status indicator LED 3.
17	Status LED 2 On	When set to a '1', this bit will turn on status indicator LED 2.
16	Status LED 1 On	When set to a '1', this bit will turn on status indicator LED 1.
15	+UTP/-STP Interface Select	This bit controls a chip output pin to switch high or low and can be used to select different PHY interfaces, etc. When this bit is off, or a logical '0', the chip output is high, or a logical '1'.
14	Disable driving the NP address over the ENSTATE(47-32) pins	For debug reasons, the driven of the address for EPROM and PHY fetches can be turned off with this bit.
13	Enable Carrier Detect LED	When set to a '1', this bit allow indicator LED 1 to reflect the status of Carrier Detect. This is a chip input.
12	Enable PHY Data Bus Parity Detection	When set to a '1', if a parity error occurs on the PHY Data bus during a PHY register access, bit 1 of the NPBUS Status Register will be set.
11	Enable 16 data bit mode for PHY reg accesses	When this bit is a '1', the upper eight bits of a 16-bit PHY data (bits 15-8) bus will be transferred over 47- 40 bits of the ENSTATE chip I/O bus.
10	Access Internal Framer register space in memory mapped mode	When this bit is a '0', the external PHY register space can be accessed through PHY 1 Registers or PHY 2 Registers. When this bit is set to '1', the internal SONET framer registers can be accessed (see *3.23 Sonet Framer Core (FRAMR Chiplet Address Mapping)* on page 507). The full offset range for this access is x'2100' to x'2FFF'. The SONET Framer register space can also be accessed through the *NPBUS EPROM Address/Command Register* on page 392 and the *NPBUS EPROM Data Register* on page 393.
9	PHY Bus Interface Type	When this bit is '0', PHY access speed is 200 ns (SUNI-like interface). When this bit is '1', access requires an acknowledge input response. This is to support a UTOPIA-like micro-processor interface.
8	Enable Hardware Error to Disable PHY	Allows bit 4 (Master enable) of the INTST Control Register to reset bit 4 of this register (Disables Front End logic). This function assumes that bit 4 of the INTST Control Register has already been enabled and that either a hardware or software event has turned the bit off.
7	Reboot serial/parallel EPROM	This bit will restart the external serial or parallel EPROM initialization code.
6	Remove Internal SONET Framer from reset state	This bit powers up to a zero and keeps the internal SONET Framer in reset mode. Setting this bit to '1' will enable normal operation.
5	Do PHY Reset	Force a PHY logic reset. Before any software reset, turn this bit on and off for the PHY specified amount of time. If the IBM ATM-TC (25 Mbps ENDEC) is used, this bit will power-up to an active reset (since the input to the ENDEC is positive reset). This bit must then be turned off for normal operation.

Bit(s)	Name	Description
4	Enable	Enable the front end. When this bit is '0', no data will be transmitted to or received from the PHYs or the PNR. See bit 8 for more information on control of this bit.
3-2	PB0PHY2 Control	Encoded control for the PB0PHY2 output pin. The enabled of PIBSELO overrides these bits and is controlled by PCINT Cascade Control Register. x'0' Enable PB0PHY2 pin. x'1' Enable PBDATAP pin and its detection of valid parity. x'2' Enable MPMDSEL pin. x'3' Reserved.
1	External EPROM Type	This bit will set at reset time as to what type of EPROM is detected. When set, a serial EPROM has been detected. When set to '0', parallel EPROM is assumed (or none at all). This will also indicate from what type of device a PCI ROM access will retrieve VPD data.
0	Reduce Serial EPROM clock	When set to '1', this bit is used for speeding up sim time for the serial EPROM. It will change the time period for the serial EPROM clock from 10 μs to 85 ns.

3.16.2 NPBUS Status Register

This register is used to report PHY level hardware errors and interrupts.

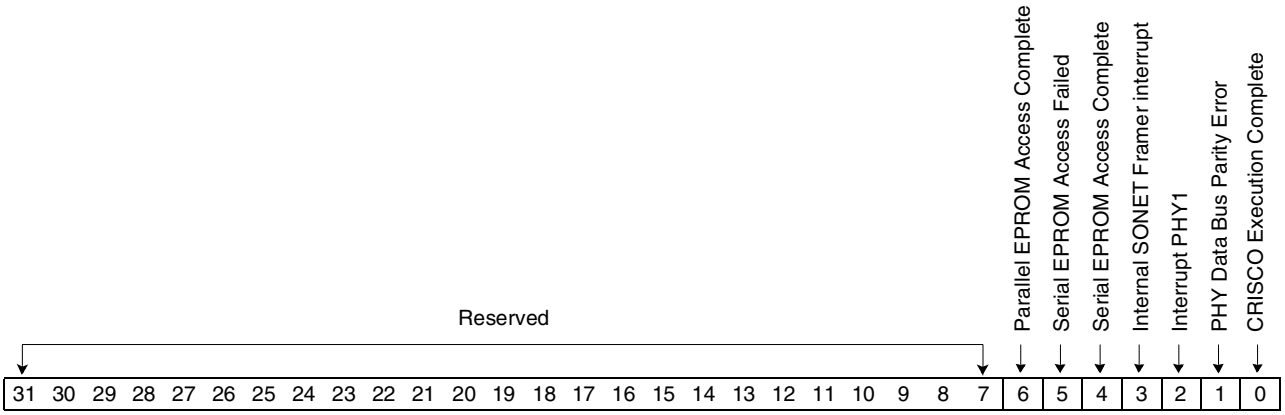
Length 32 bits

Type Clear/Set

Address XXXX 2028 and 202C

Power On Reset Value x‘0000 00X1’, where x is determined by which type of external IPL EPROM is used

Restrictions None



Bit(s)	Name	Description
31-7	Reserved	Reserved.
6	Parallel EPROM Access Complete	The requested action to the parallel EPROM has been completed. See *3.16.4 NPBUS EPROM Address/Command Register* on page 392.
5	Serial EPROM Access Failed	The requested action to the serial EPROM has missed an acknowledge sequence while trying to complete the action. See *3.16.4 NPBUS EPROM Address/Command Register* on page 392.
4	Serial EPROM Access Complete	The requested action to the serial EPROM has been completed. See *3.16.4 NPBUS EPROM Address/Command Register* on page 392.
3	Internal SONET Framer interrupt	The internal Framer has signaled an interrupt.
2	Interrupt PHY1	This bit indicates that an interrupt occurred on PHY 1.
1	PHY Data Bus Parity Error	When set to ‘1’, a data parity was detected over the PHY Data 8-bit bus. Parity checked is odd.
0	CRISCO Execution Complete	External serial/parallel EPROM initialization has run and is completed.

3.16.3 NPBUS Interrupt Enable Register

This register is used to mask bits from the NPBUS Status Register and potentially generate interrupts to the control processor. When both a bit in this register and the corresponding bit in the NPBUS Status Register are set, an interrupt will be generated from NPBUS to INTST. See *3.16.2 NPBUS Status Register* on page 390 for the bit descriptions.

Length	32 bits
Type	Clear/Set
Address	XXXX 2008 and 200C
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.16.4 NPBUS EPROM Address/Command Register

This register is used to access a maximum of 2 K external serial EPROM or 16 M of parallel EPROM or the SONET Framer Core. It is used to access bytes from the external EPROM or the SONET Framer Core.

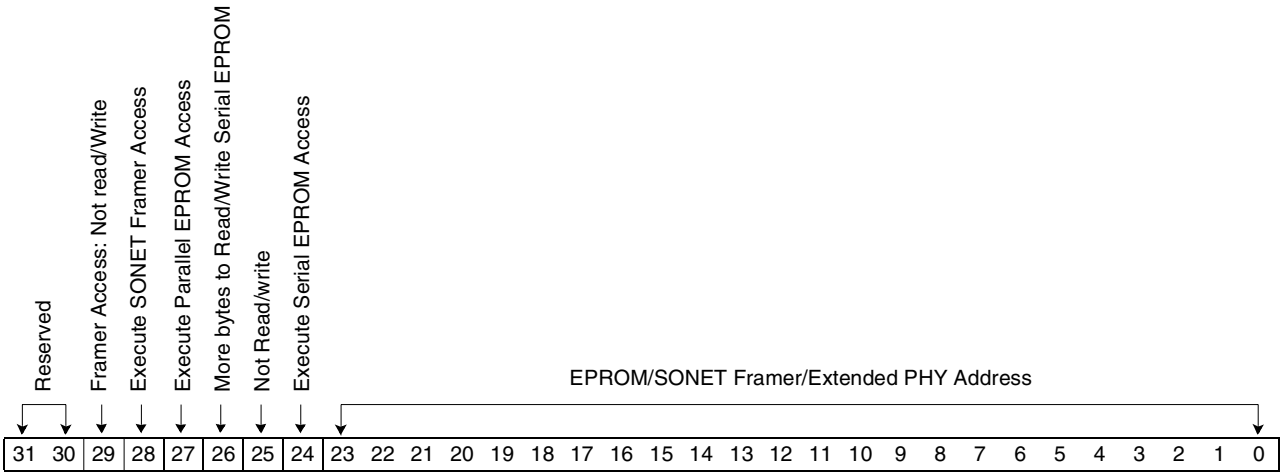
Length 32 bits

Type Read/Write

Address XXXX 2010

Power On Reset Value x‘0000 0100’

Restrictions None



Bit(s)	Name	Description
31-30	Reserved	Reserved.
29	Framer Access: Not read/Write	This bit set to ‘1’ will cause a write function to the SONET Framer Core. This bit set to ‘0’ will cause a read function to the SONET Framer Core.
28	Execute SONET Framer Access	This bit will start a read or write function to the SONET Framer Core. This bit will auto reset after the command is issued.
27	Execute Parallel EPROM Access	This bit will start a read or write function to the parallel EPROM. This bit will auto reset after the command is issued.
26	More bytes to Read/Write Serial EPROM	This bit set to ‘1’ will help speed up sequential accesses to the serial EPROM. If writing, there is a limit as to how many bytes can be written before the serial EPROM write buffer is full. Typical range is from two to eight bytes, depending on the device.
25	Not Read/Write	This bit set to ‘1’ will cause a write function to the serial/parallel EPROM. This bit set to ‘0’ will cause a read function to the serial/parallel EPROM.
24	Execute Serial EPROM Access	This bit will start a read or write function to the serial EPROM. This bit will auto reset after the command is issued.
23-0	EPROM/SONET Framer/ Extended PHY Address	This holds the address field that will be used to address the serial/parallel EPROM or the internal SONET Framer. If accessing the interal SONET Framer, the addresses listed in *Sonet Framer Core (FRAMR Chiplet Address Mapping)* on page 507 should be used. It is where the 15-8 address bits will be held if addressing a PHY with more addressability than eight bits.

3.16.5 NPBUS EPROM Data Register

This register is used to access a maximum of 2 K external serial EPROM or 16 M of parallel EPROM. It can also be used to access the registers of the internal SONET Framer.

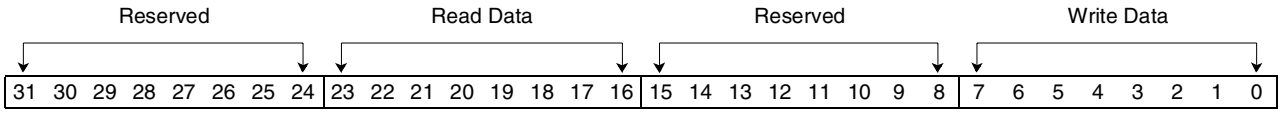
Length 32 bits

Type Read/Write

Address XXXX 2018

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-16	Read Data	Holds the data that was read back from the serial/parallel EPROM or the internal SONET Framer.
15-8	Reserved	Reserved.
7-0	Write Data	Holds the data that is destined to be written to the serial/parallel EPROM or the internal SONET Framer.

3.16.6 PHY 1 Registers

This address range provides access to the PHY 1 hardware. The details of the registers can be found in the specific publication for the PHY hardware.

Length 256 Doublewords (only lowest eight bits valid)

Type Read/Write

Address XXXX 2400 - 27FF

Power On Reset Value Reference the PHY-specific publication.

Restrictions Reference the PHY-specific publication.

3.16.7 PHY 2 Registers

This address range provides access to the PHY 2 hardware. It should be noted that not all applications of the PNR will use this access port. The details of the registers can be found in the specific publication for the PHY hardware.

Length 256 Doublewords (only lowest eight bits valid)

Type Read/Write

Address XXXX 2800 - 2BFF

Power On Reset Value Reference the PHY-specific publication.

Restrictions Reference the PHY-specific publication.

3.16.8 EPROM Instructions

When using an external EPROM connected to the PNR, registers can be initialized using instructions stored in the EPROM. The instructions need to begin at offset x‘0100’ in the EPROM and the last instruction must be a Stop instruction. The instruction formats are as follows:

EPROM Instruction	Format
Single Register Write	x‘17 AAAA DDDD DDDD’ where: x‘AAAA’ = the offset of the register into the address space of the PNR and x‘DDDD DDDD’ = the 32-bit value that is to be stored in the register. For example, to write x‘1234 5678’ to the Comet Control Register’s set address (x‘0904’), the instruction would be x‘17 0904 1234 5678’.
Looping Register Write	x‘27 AAAA DDDD DDDD IIII IINN NNNN’ where: x‘AAAA = the offset of the register into the address space of the PNR, x‘DDDD DDDD’ = the 32 bit value to be stored in the register, x‘II IIII’ = the amount to increment the address in each iteration, and x‘NN NNNN’ = the number of iterations to perform. For example, to initialize the CSKED Time Wheel Array which is x‘8000’ entries long and is accessed by the CSKED Time Wheel Array Data register (at offset x‘12CC’), the code would first need to set the CSKED Time Wheel Array Pointer Register (at offset x‘12C8’) to 0 via a single register write command and then initialize the array with a looping command. The two commands would then be x‘17 12C8 0000 0000’ and x‘27 12CC 0000 0000 0000 0000 8000’.
Stop Instruction	x‘FF’ is the stop instruction. It should be placed immediately after all other instructions.

3.17 Buffer Pool Management (POOLS)

POOLS acts as a memory manager for the PNR. Memory buffers are checked out and checked in via two operations (primitives) supported by POOLS: the get pointer primitive and the free pointer primitive. These primitives can be performed explicitly from software by accessing specified addresses within the POOLS entity, and they may also be done by other PNR entities. For example, CSKED can free a buffer upon transmission if specified by the corresponding packet header (see *Packet Header* on page 673), and REASM gets buffers to store received data. POOLS also contains mechanisms to control resource utilization and supports a Real Memory Mode and a Virtual Memory Mode.

3.17.1 Basic Operation in Real Memory Mode

If memory is viewed as a series of buffers, POOLS maintains a circular list of available buffers. There are pointers (the head and tail) to the start and the end of the list. When a get pointer primitive is executed, the buffer at the head of the list is checked out, the head pointer is advanced and the correct resource group(s) is debited. When a free pointer primitive is executed, the freed buffer is checked in at the end of the list, the tail pointer is advanced, and the correct resource group is credited.

3.17.2 Basic Operation in Virtual Memory Mode

With the addition of Virtual Memory, POOLS must maintain five sets of head and tail pointers, thresholds, and common counts: one for the virtual buffers themselves and the rest for the four regions of real buffers that constitute the virtual buffers. In this case, the buffer's virtual address is the item returned from a get pointer operation and passed as a parameter to a free pointer operation. When the get buffer primitive is executed, POOLS creates an active buffer map (page table) for the virtual address. As the virtual address is used and buffer (page) boundaries are crossed, VIMEM will request buffers from POOLS when a buffer (page) fault occurs. VIMEM then places the buffer index in the buffer map. When the virtual buffer is no longer needed and a free pointer primitive is issued with the buffer's starting virtual address, POOLS takes the contents of the buffer map and frees the resources that were assigned to the buffer map.

3.17.3 Resource Controls

POOLS adds another layer of service by creating "pools" of buffers (currently a maximum of 16 pools). For each pool, a maximum number of allowable buffers can be specified. The intent is to make it possible for several applications to use the PNR at once without one or more applications starving the remaining applications for memory buffers. Particular pools buffers are divided into "guaranteed" and "common" buffers. All the guaranteed buffers are considered to be dedicated to their respective pool and are therefore not available for general use. The common buffers are all the memory buffers remaining after the guaranteed buffers are subtracted from the total buffers. To maintain the buffer limits on each pool, every pool has a guaranteed threshold, total threshold, and an active count. When a request is made for a buffer from a particular pool, the guaranteed threshold is first checked. If the active count of the pool is less than the guaranteed threshold, the buffer is provided. If the guaranteed threshold has been reached, then the total threshold is checked. If the active count is equal to the total threshold, no buffer is provided. If the active count is less than the total threshold, and a common buffer is available, a buffer is provided. If there are no common buffers available, a buffer cannot be provided and a null index is returned. To determine if a common buffer is available, a count is maintained for each size of buffer.

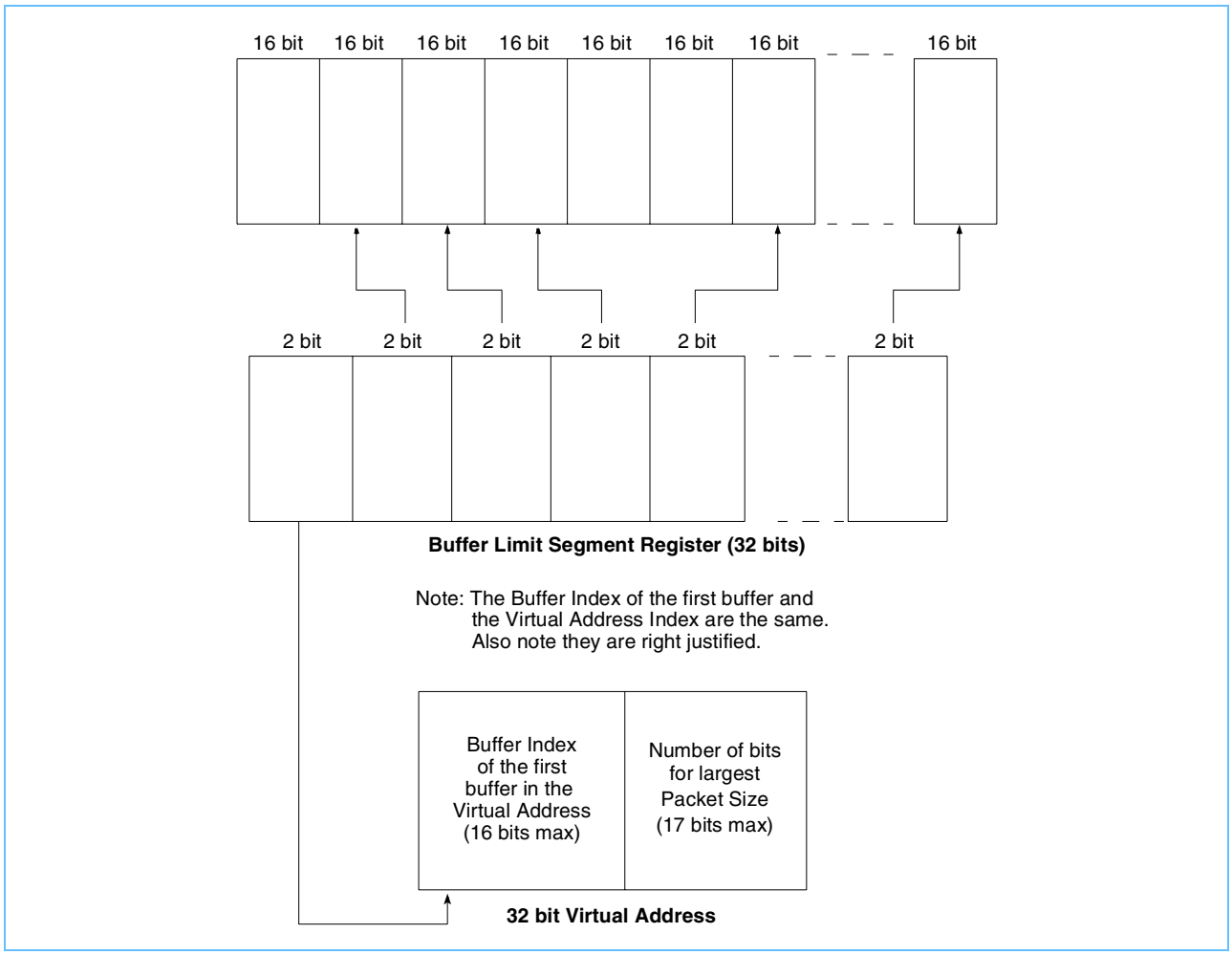
3.17.4 Virtual Memory Overview

Each virtual buffer consists of a number of real buffers. For each virtual buffer there is a buffer map that defines the size and number of real buffers that may be allocated to the virtual buffer. Each map is built from a common template (the VIMEM Virtual Buffer Segment Size Register) that associates 1 to n buffer indexes in the map to a real buffer in one of the four real buffer regions defined in VIMEM. In VIMEM, the VIMEM Buffer Map Base Address Register defines the size of the map and therefore also the number of buffer indexes in the virtual buffer map. Each 8-byte entry of the map contains the pool ID of the pool to which the buffer is allocated plus space for three real buffer segment indexes. This implies the smallest map yields a virtual buffer of one to four real buffer segments (three real buffer segments plus the implicit real buffer that all virtual buffers are allocated). The biggest map defines a virtual buffer of 1-16 real buffer segments (15 plus the implicit one).

The intention of this structure is to allow the user to customize the value in the VIMEM Virtual Buffer Segment Size Register to utilize memory in an efficient manner relative to network data traffic. For example, if network traffic contained 50% packets of < 512 bytes, 35% packets of < 1 K bytes, and the rest was < 5 K bytes, the user could set up Virtual Memory to use three real segments of 512 bytes, 512 bytes, and 4 K bytes, respectively. The incoming data would neatly fit into the segments and minimize wasted memory.

POOLS and VIMEM maintain the maps for the virtual buffers. On a write that crosses a real buffer boundary into an as-yet unresolved region of a virtual buffer, a page fault occurs. When a page fault occurs, POOLS determines whether a real buffer can be assigned. If it can be assigned, the index of the real buffer relative to the base address of the particular buffer size is placed by VIMEM into the buffer map. The first buffer is implicitly associated with the Virtual Memory address for a particular virtual buffer and enough real memory must be available to support the first real buffer of each virtual buffer at initialization time. There is not necessarily enough real storage for all the possible real buffers associated with a virtual buffer.

Figure 32: Virtual Address Buffer Map



All real buffers of a particular size are stored in a contiguous region of memory. The buffer index, in conjunction with the base address for this real buffer size, points to a particular real buffer. The implicit buffers are also stored in a data structure of this type.

Figure 33: Buffer/Virtual Memory Allocation Structure in Memory

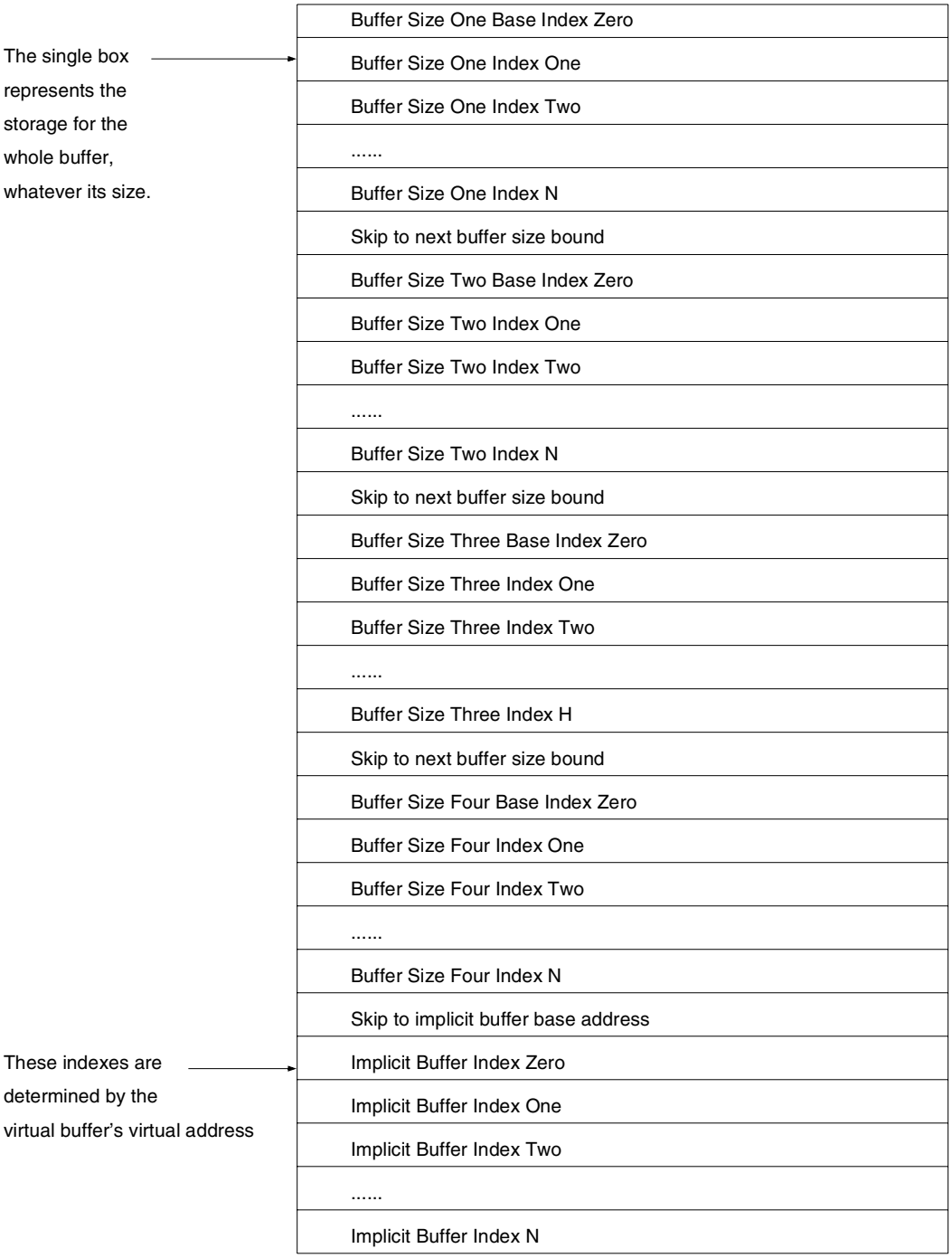
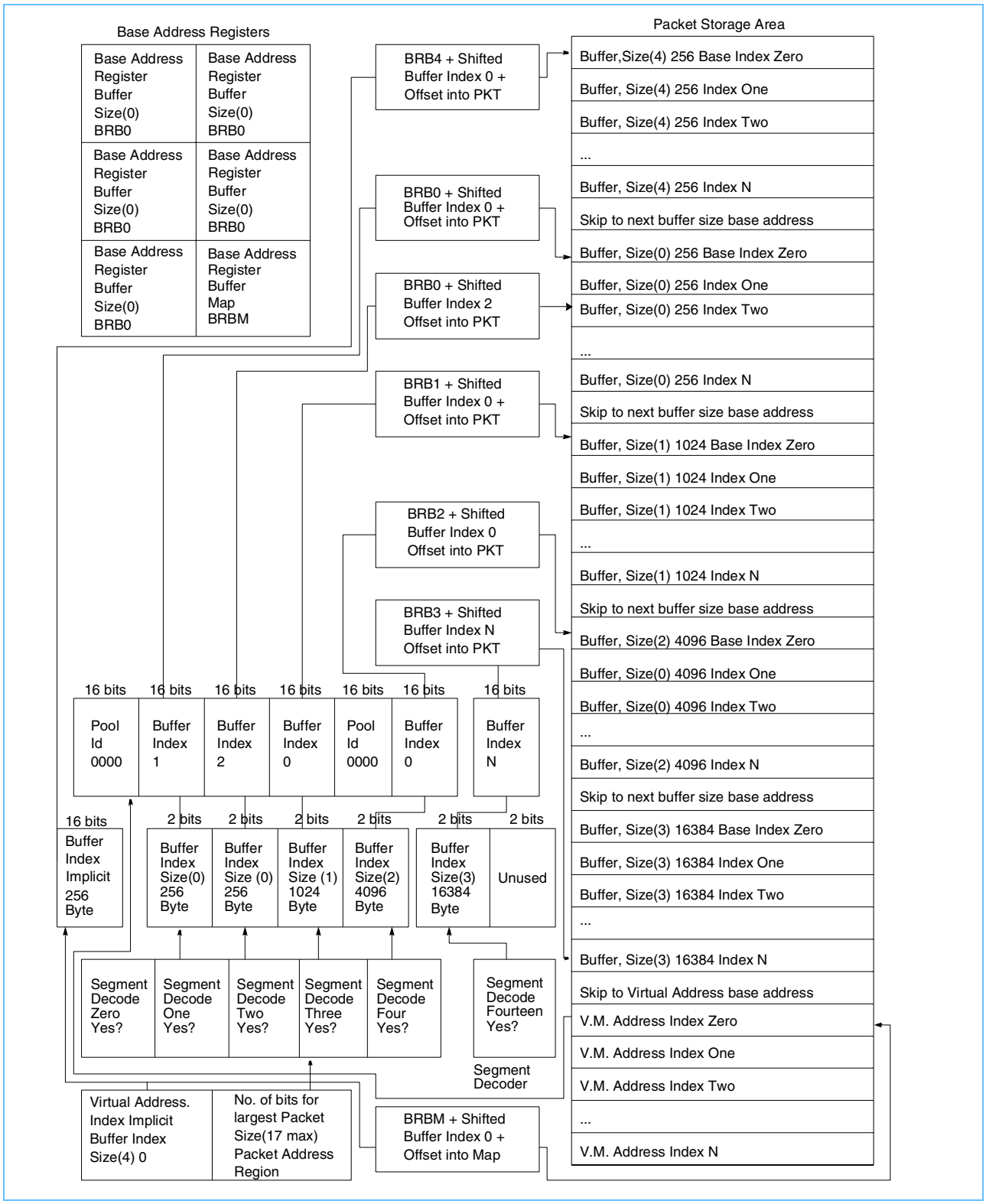


Figure 34: Virtual Address Buffer Map



The lower 17 bits of the virtual address are used in conjunction with the segment template in the VIMEM Virtual Buffer Segment Size Register to determine from which portion of the buffer map the buffer index is retrieved. Once the buffer index is retrieved, it is combined with the appropriate base address for that particular buffer size. The offset into the buffer is then added to get the real 32-bit address that is used in physical memory.

POOLS uses the data structures above to manage Packet Memory resources. Each LCD is associated with a particular POOL and multiple different LCDs may be associated with that same POOL. Within a POOL, there are five different resource categories and two variables to go with each resource.

Resource Type, Pool 0000	Guaranteed Number	Total Number
Virtual Memory Addresses	100	150
Buffer Type One	200	300
Buffer Type Two	50	100
Buffer Type Three	10	5
Buffer Type Four	0	10

3.17.5 POOLS Get Pointer Primitive

The POOLS Get Pointer Primitive returns a buffer pointer to the requester. The request to the virtual packet/ buffer size 4 address will always return a memory address. If in virtual mode, the address will be virtual. Requests made for buffer sizes 0-3 will not return an address but rather a buffer index in bits 15-0. The real address associated with this index can be generated by shifting the index by the buffer size (for example, six bit positions for a 64-byte buffer) and adding the result to the base address for this size buffer. Access to buffer sizes 0-3 is not permitted in operational mode.

The address of the primitive also selects the pool ID. The pool ID is contained in address bits 5-2, and it selects which pool will be charged for the pointer. The buffer size is selected with address bits 8-6.

If there are no more buffers available in the specified pool, a null pointer is returned. The active pointer count for that pool is incremented if a non-null pointer is returned. If the guaranteed threshold has been exceeded and a buffer from the common pool is returned, the common pools count for that size is decremented by 1.

Length	32 bits	
Type	Read Only	
Address	Buffer Size 0	XXXX 3200
	Buffer Size 1	XXXX 3240
	Buffer Size 2	XXXX 3280
	Buffer Size 3	XXXX 32C0
	Virtual Packets/ Buffer Size 4	XXXX 3300
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations this register is to be used as a read only register. Writes to this address will be ignored.	

3.17.6 POOLS Free Pointer Primitive

The POOLS Free Pointer Primitive returns the buffer to the proper free list. If it is a Virtual Memory address, the Virtual Memory Buffer Map is traversed to free the indexes associated with the Virtual Memory address. In the case where it is a real memory buffer, the single index is freed.

This primitive uses address mapping to select the size of the object to be freed. The size is contained in address bits 4-2. During normal operation, only frees to buffer size four are relevant. During initialization mode, buffer sizes 0 to 3 can be used to load indexes. The indexes are loaded into bits 31-16.

In normal operations, it is not necessary to read this register.

Length	32 bits	
Type	Write Only	
Address	Buffer Size 0	XXXX 3350
	Buffer Size 1	XXXX 3354
	Buffer Size 2	XXXX 3358
	Buffer Size 3	XXXX 335C
	Virtual Packets/ Buffer Size 4	XXXX 3360
Power On Reset Value		x‘0000 0000’
Restrictions	During normal operations this register is to be used as a write only register. Reads from this address will return ‘0’.	

3.17.7 POOLS Common Pools Count Registers

The POOLS Common Pools Count Registers indicate the number of buffers for their respective buffer sizes that are available for use by any of the 16 pools. If the value of the register is non-zero, any pool that gets a buffer beyond its guaranteed number will decrement the register's value by one. If the value of the register is zero, any attempt to get a buffer will fail. If a pool frees a buffer it has gotten from the common supply, this register will increment by one. Software should initialize these registers to the number of common buffers of each size that it requires.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3000
	Buffer Size 1	XXXX 3004
	Buffer Size 2	XXXX 3008
	Buffer Size 3	XXXX 300C
	Virtual Packets / Buffer Size 4	XXXX 3010
Power On Reset Value		x'0000 0000'
Restrictions	During normal operations, these registers should be only be read. Writing to these registers during normal operation could create a data loss situation. These registers should be set up by software at initialization time.	

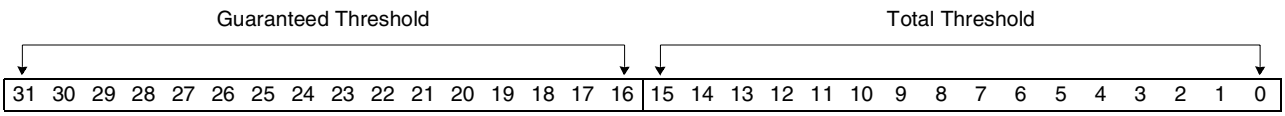
Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Common Count	Number of free buffers in the common pool for the respective buffer size.

3.17.8 POOLS Client Thresholds Array

The POOLS Client Thresholds Array holds the guaranteed and total threshold values for the 16 pools and the four (five) pointer sizes. To access the thresholds for a respective pool and buffer size, take the base address of x'3400' and replace bits 5-2 with the pool ID and bits 8-6 with the buffer size. For example, to access the pool 6 thresholds for buffer size 3, replace bits 5-2 with binary '0110' and bits 8-6 with binary '011'. The result is address x'34D8'.

When a Get Pointer primitive is processed, the values in this array are used to determine if a primitive can return a pointer to a buffer. The active count from the Active Packet Count Array is used with these registers to determine if a threshold has been exceeded. If the guaranteed threshold has been exceeded and the total has not been exceeded and there is a common buffer available, then the common count will be incremented. If there are no common buffers available or the request will cause the total threshold to be exceeded, the request will be rejected. During a Free Pointer primitive processing, the buffer is returned to the free list and these thresholds are used to determine if a common count should be credited.

Length	32 bits x 16 Words	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3400
	Buffer Size 1	XXXX 3440
	Buffer Size 2	XXXX 3480
	Buffer Size 3	XXXX 34C0
	Virtual Packets/ Buffer Size 4	XXXX 3500
Power On Reset Value		x'0000 0000'
Restrictions	None	



Bit(s)	Name	Description
31-16	Guaranteed Threshold	The number of buffers of the respective size that the selected pool is guaranteed to have available.
15-0	Total Threshold	The total number of buffers of the respective size that the selected pool is allowed to have.

3.17.9 POOLS User Threshold and Client Active Packet Count Array

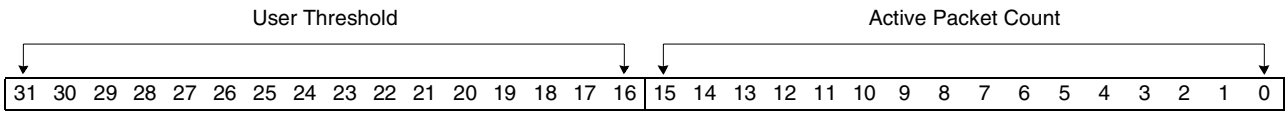
The POOLS User Threshold and Client Active Packet Count Array holds the user thresholds and active pointer counts for each of the 16 managed pools and four (five) pointer sizes. To access the user threshold and active packet count for a respective pool and buffer size, take the base address of x'3600' and replace bits 5-2 with the pool ID and bits 8-6 with the buffer size. For example, to access the pool 6 user threshold and active packet count for buffer size 3, replace bits 5-2 with binary '0110' and bits 8-6 with binary '011'. The result is address x'36D8'.

When a Get Pointer primitive is processed, the active count is retrieved and compared with the threshold counts. If it falls within bounds and a buffer is available, the active count will be incremented by one reflecting the additional buffer charged to that queue.

When a Free Pointer primitive is processed, the active count is retrieved, and, when the buffer is returned to the free list, the active buffer count is decremented by one.

The user threshold may be used to check on resource utilization as opposed to resource allocation. The Guaranteed and Total Thresholds are used when allocating resources to make decisions. The User Threshold is not used to govern resource allocation directly. One use for the User Threshold is for high water mark indication. When a Free Pointer primitive is processed or a Get Pointer is processed, the active packet count is compared to the user threshold. If the event interface is enabled and a boundary condition is crossed, an event is issued to the event interface.

Length	32 bits x 16 Words	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3600
	Buffer Size 1	XXXX 3640
	Buffer Size 2	XXXX 3680
	Buffer Size 3	XXXX 36C0
	Virtual Packets/ Buffer Size 4	XXXX 3700
Power On Reset Value		x'0000 0000'
Restrictions	None	



Bit(s)	Name	Description
31-16	User Threshold	The number of buffers of the respective size that the selected pool is guaranteed to have available
15-0	Active Packet Count	The current number of buffers charged to the selected pool.

3.17.10 POOLS Pointer Queues DRAM Head Pointer Offset Address Register

The POOLS Pointer Queues DRAM Head Pointer Offset Address Register indicates the address in DRAM where the head of the queue starts. This address, however, is only relative to the DRAM portion of the queue. Unless the head of the queue portion of the cache is locked out and needs two frames, the actual head of the queue is in the cache.

These 19 bits on write represent the offset to the address in DRAM of the head of the queue relative to the DRAM base address. On a read, the address in DRAM of the pointer is returned. This pointer is adjusted every time a cache frame boundary is crossed and a cache update cycle is completed to write through the additional queue elements. Because each memory reference contains four indices, this allows for a possible 128 K index location in the queue.

Length	32 bits Read/19 bits Write	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3014
	Buffer Size 1	XXXX 3018
	Buffer Size 2	XXXX 301C
	Buffer Size 3	XXXX 3020
	Virtual Packets/ Buffer Size 4	XXXX 3024
Power On Reset Value	Buffer Size 0	x‘0001 C000’
	Buffer Size 1	x‘0002 0000’
	Buffer Size 2	x‘0002 4000’
	Buffer Size 3	x‘0002 6000’
	Virtual Packets/ Buffer Size 4	x‘0002 7000’
Restrictions	During normal operations this register is to be used as a read only register. This register defaults to zero at initialization. It is assumed that the queues start on a maximum size queue boundary. These registers should be set up at initialization time. This register is cleared when the POOLS Pointer Queues DRAM Lower Bound Address Register is written to.	

3.17.11 POOLS Pointer Queues DRAM Tail Pointer Offset Address Register

The POOLS Pointer Queues DRAM Tail Pointer Offset Address Register indicates the offset address in DRAM where the tail of the queue starts. This address, however, is only relative to the DRAM portion of the queue. Unless a 'no cache frames to be written through' state is in effect, the actual tail of the queue is in the cache.

These 19 bits on write represent the offset to the address in DRAM of the tail of the queue relative to the DRAM base address. On a read, the address in DRAM of the pointer is returned. This pointer is adjusted every time a cache frame boundary is crossed and a cache update cycle is completed to write through the additional queue elements. Because each memory reference contains four indices, this allows for a possible 128 K index location in the queue.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3028
	Buffer Size 1	XXXX 302C
	Buffer Size 2	XXXX 3030
	Buffer Size 3	XXXX 3034
	Virtual Packets/ Buffer Size 4	XXXX 3038
Power On Reset Value	Buffer Size 0	x'0001 C000'
	Buffer Size 1	x'0002 0000'
	Buffer Size 2	x'0002 4000'
	Buffer Size 3	x'0002 6000'
	Virtual Packets/ Buffer Size 4	x'0002 7000'
Restrictions	During normal operations this register is to be used as a read only register. This register defaults to zero at initialization. It is assumed that the queues start on the maximum size queue boundary. This register should be set up at initialization time. This register is cleared when the POOLS Pointer Queues DRAM Lower Bound Address Register is written to.	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Tail Pointer	Pointer to the tail of the queue for the respective buffer size.

3.17.12 POOLS Pointer Queues DRAM Lower Bound Address Register

The POOLS Pointer Queues DRAM Lower Bound Address Register indicates the address in DRAM where the queue data structure is initially started. When the queue reaches the maximum address allowed for in the upper bound register, it wraps back around to the address specified in this register. This implements the queue in a circular buffer.

These 32 bits represent the address in DRAM where the queue begins and eventually wraps to. At initialization, this register and the POOLS Pointer Queues DRAM Tail Pointer Offset Address Register and the POOLS Pointer Queues DRAM Head Pointer Offset Address Register must be equal.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 303C
	Buffer Size 1	XXXX 3040
	Buffer Size 2	XXXX 3044
	Buffer Size 3	XXXX 3048
	Virtual Packets/ Buffer Size 4	XXXX 304C
Power On Reset Value	Buffer Size 0	x‘0001 C000’
	Buffer Size 1	x‘0002 0000’
	Buffer Size 2	x‘0002 4000’
	Buffer Size 3	x‘0002 6000’
	Virtual Packets/ Buffer Size 4	x‘0002 7000’

Restrictions During normal operations, this register is to be used as a read only register. This register should be set up at initialization time. The size of the DRAM queue storage formed with the lower and upper bounds is constrained in its size. It can be written when the diagnostic mode bit is set, otherwise the write is ignored. Note that if the maximum queue length exceeds the space available in the circular buffer, data corruption will occur when the actual queue length exceeds the maximum queue space available.

3.17.13 POOLS Pointer Queues DRAM Upper Bound Register

The POOLS Pointer Queues DRAM Upper Bound Register indicates the max queue length in DRAM of the queue data structure. When the queue reaches this address, it wraps back to the address specified by the lower bound register. This implements the queue in a circular buffer. This upper bound is to be provided as an encoded field. The encoded field represents the number of 8-byte addresses that can be contained by the queue.

The four non-reserved bits represent the encoded maximum queue length in DRAM which, when matched, trigger the queue to wrap back to the address contained in the DRAM Lower Bound Address Register.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3050
	Buffer Size 1	XXXX 3054
	Buffer Size 2	XXXX 3058
	Buffer Size 3	XXXX 305C
	Virtual Packets/ Buffer Size 4	XXXX 3060
Power On Reset Value	Buffer Size 0	x‘0000 000B’
	Buffer Size 1	x‘0000 000A’
	Buffer Size 2	x‘0000 0009’
	Buffer Size 3	x‘0000 0009’
	Virtual Packets/ Buffer Size 4	x‘0000 000B’

Restrictions During normal operations, this register is to be used as a read only register. This register should be set up at initialization time. The size of the DRAM queue storage which is formed with the lower and upper bounds is constrained in its size. It can be written when the diagnostic mode bit is set, otherwise the write is ignored. Note that if the maximum queue length exceeds the space available in the circular buffer, data corruption will occur when the actual queue length exceeds the maximum queue space available.

Bit(s)	Name	Description		
31-4	Reserved	Reserved.		
3-0	Max Queue Length	Encoded Value	Number of 32 Bit Words	Number of Indexes
		X‘0’	8	16
		X‘1’	16	32
		X‘2’	32	64
		X‘3’	64	128
		X‘4’	128	256
		X‘5’	256	512
		X‘6’	512	1024
		X‘7’	1024	2048
		X‘8’	2048	4096
		X‘9’	4096	8192
		X‘A’	8192	16384
		X‘B’	16384	32768
		X‘C’	32768	65536
		X‘D’	65536	131072
		X‘E’	65536	131072
		X‘F’	65536	131072

3.17.14 POOLS Pointer Queues Length Registers

The POOLS Pointer Queues Length Registers indicate the length of the queue. The bits are a 16-bit count. A primitive that adds to the queue increments this counter. Primitives that remove items from the queue decrement this counter.

Length 32 bits

Type Read/Write

Address

Buffer Size 0	XXXX 3064
Buffer Size 1	XXXX 3068
Buffer Size 2	XXXX 306C
Buffer Size 3	XXXX 3070
Virtual Packets / Buffer Size 4	XXXX 3074

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, this register is to be used as a read only register. It can be written when the diagnostic mode bit is set, otherwise the write is ignored. This register is cleared when the POOLS Pointer Queues DRAM Lower Bound Address Register is written to.

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Queue Length	Length of the queue for the respective size buffer.

3.17.15 POOLS Interrupt Enable Register

This register is used to enable bits from the POOLS Status Register to generate interrupts to INTST. When both a bit in this register and the corresponding bit in the POOLS Status Register are set, the POOLS interrupt to INTST will be enabled.

See *3.17.19 POOLS Status Register* on page 414 for the bit descriptions.

Length 32 bits

Type Clear/Set

Address XXXX 3078 and 307C

Power On Reset Value x‘0003 F800’

Restrictions None

3.17.16 POOLS Event Enables Register

This register is used to enable an event based on bits from the corresponding primitive transaction. If the bits are set in the enable and a transaction occurs that matches the event, an event will be sent to the RXQUE.

Length 32 bits

Type Clear/Set

Address

Guaranteed Event Enables	XXXX 3A00 and 3A04
Total Event Enables	XXXX 3A08 and 3A0C
User Event Enables	XXXX 3A10 and 3A14

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Event Enables	The bit numbers of the bits in this register correspond to pool IDs (bit 15 corresponds to pool 15, etc.). If a bit in this register is on, and the corresponding pool has reached the threshold type this register supports (Guaranteed, Total User), an event is generated to RXQUE.

3.17.17 POOLS Event Hysteresis Register

The POOLS Event Hysteresis Register provides the capability for hysteresis on threshold checking.

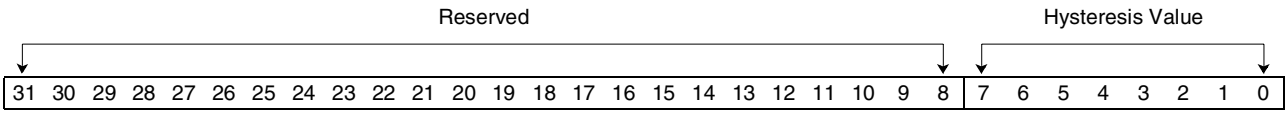
Length 32 bits

Type Read/Write

Address XXXX 3A18

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7-0	Hysteresis Value	When a free occurs, the value in this register is added to the next Active Packet Count. This value will be then tested against the threshold value. If it is equal to the threshold, an event will be issued if events are enabled and the event associated with this transaction is enabled.

3.17.18 POOLS Event Data Register

The POOLS Event Data Register provides the data sent on the last event.

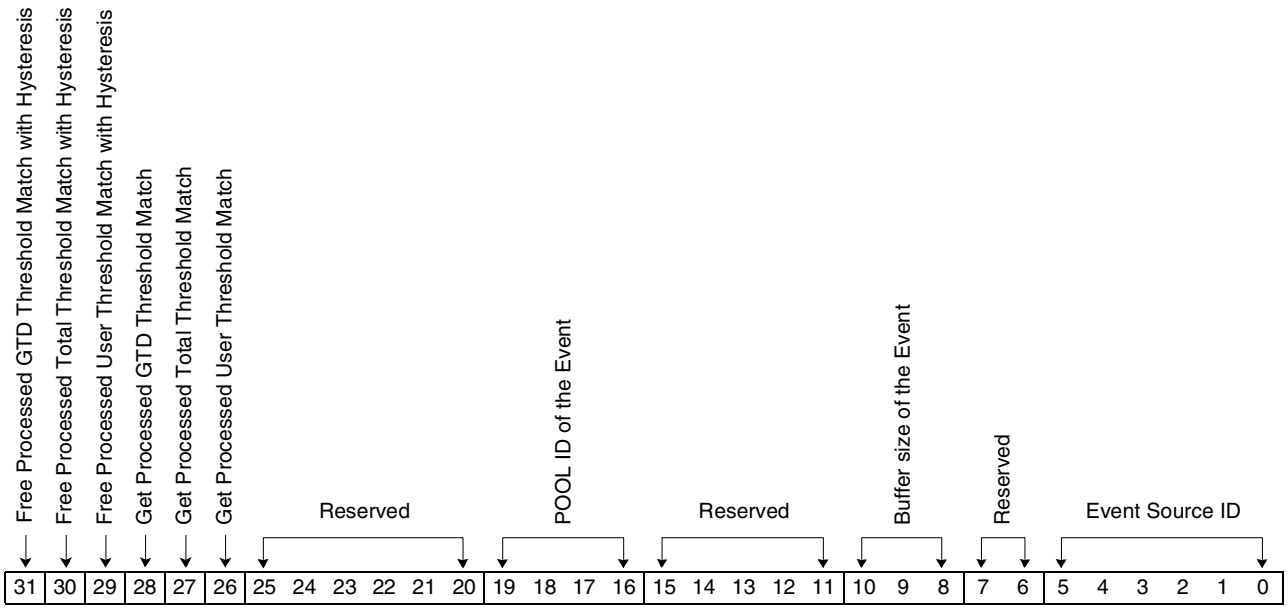
Length 32 bits

Type Read Only

Address XXXX 3A1C

Power On Reset Value x‘0000 003E’

Restrictions None



Bit(s)	Name	Description
31	Free Processed GTD Threshold Match with Hysteresis	This event occurs when a free is processed and the threshold is matched. The threshold is modified by the value in the hysteresis register. The event is issued when the actual value of the Active Packet count plus the hysteresis equals the threshold.
30	Free Processed Total Threshold Match with Hysteresis	This event occurs when a free is processed and the threshold is matched. The threshold is modified by the value in the hysteresis register. The event is issued when the actual value of the Active Packet count plus the hysteresis equals the threshold.
29	Free Processed User Threshold Match with Hysteresis	This event occurs when a free is processed and the threshold is matched. The threshold is modified by the value in the hysteresis register. The event is issued when the actual value of the Active Packet count plus the hysteresis equals the threshold.
28	Get Processed GTD Threshold Match	This event occurs when a get is processed and the threshold is matched. The event is issued when the new Active Packet count equals the threshold.
27	Get Processed Total Threshold Match	This event occurs when a get is processed and the threshold is matched. The event is issued when the new Active Packet count equals the threshold.
26	Get Processed User Threshold Match	This event occurs when a get is processed and the threshold is matched. The event is issued when the new Active Packet count equals the threshold.
25-20	Reserved	Reserved.

Bit(s)	Name	Description
19-16	POOL ID of the Event	This indicates which POOL is associated with this event.
15-11	Reserved	Reserved.
10-8	Buffer size of the Event	This indicates which size is associated with this event.
7-6	Reserved	Reserved.
5-0	Event Source ID	This indicates that POOLS is associated with this event.

3.17.19 POOLS Status Register

The POOLS Status Register provides status information about POOLS operations.

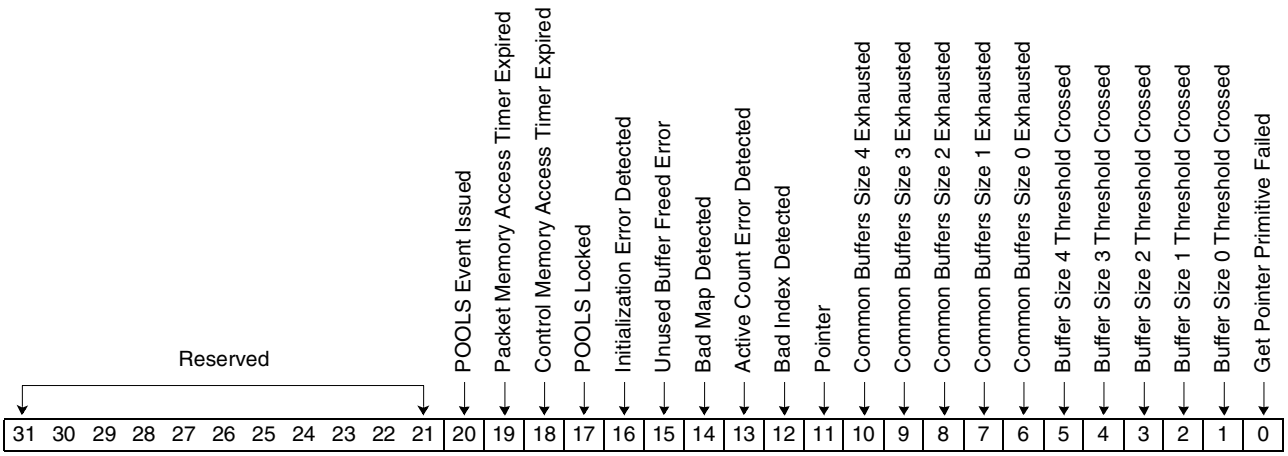
Length 32 bits

Type Clear/Set

Address XXXX 3080 and 3084

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31-21	Reserved	Reserved.
20	POOLS Event Issued	This bit is set when a POOLS event is issued.
19	Packet Memory Access Timer Expired	This bit is set when the Packet Memory access timer hits the Packet Memory access threshold and the control bit in the control register is set to enable this function.
18	Control Memory Access Timer Expired	This bit is set when the Control Memory access timer hits the Control Memory access threshold and the control bit in the control register is set to enable this function.
17	POOLS Locked	This bit is set when a lock enable bit is set and the corresponding status bit is set. This causes all state machines to be held in idle once this bit is set. It is the functional equivalent to POOLS Control Register bit 0.
16	Initialization Error Detected	This bit is set when too many indexes are freed to a queue.

Bit(s)	Name	Description
15	Unused Buffer Freed Error	This bit is set when a previously freed buffer is detected during a free operation. This typically would occur when the buffer was freed two or more times.
14	Bad Map Detected	This bit is set when a bad map is detected during a free operation.
13	Active Count Error Detected	This bit is set when an active packet count is decremented from '0' to x'FFFF'. This is most likely the result of a subtle map corruption where a POOL ID has been changed.
12	Bad Index Detected	This bit is set when an Index Threshold is crossed.
11	Free Pointer Primitive Null Detected/Max Pointer Queue Length Exceeded.	This bit is set as a result of one of two detectable errors: Null index detected within free address. Total allowed storage for a particular queue has been exceeded.
10	Common Buffers Size 4 Exhausted	Common buffer count for size 4 is zero.
9	Common Buffers Size 3 Exhausted	Common buffer count for size 3 is zero.
8	Common Buffers Size 2 Exhausted	Common buffer count for size 2 is zero.
7	Common Buffers Size 1 Exhausted	Common buffer count for size 1 is zero.
6	Common Buffers Size 0 Exhausted	Common buffer count for size 0 is zero.
5	Buffer Size 4 Threshold Crossed	The number of size 4 buffers is equal to or less than the threshold that was set for size 4 buffers.
4	Buffer Size 3 Threshold Crossed	The number of size 3 buffers is equal to or less than the threshold that was set for size 3 buffers.
3	Buffer Size 2 Threshold Crossed	The number of size 2 buffers is equal to or less than the threshold that was set for size 2 buffers.
2	Buffer Size 1 Threshold Crossed	The number of size 1 buffers is equal to or less than the threshold that was set for size 1 buffers.
1	Buffer Size 0 Threshold Crossed	The number of size 0 buffers is equal to or less than the threshold that was set for size 0 buffers.
0	Get Pointer Primitive Failed	This bit is set when a null address is returned on a get.

3.17.20 POOLS Control Register

The POOLS Control Register provide status information about POOLS operations.

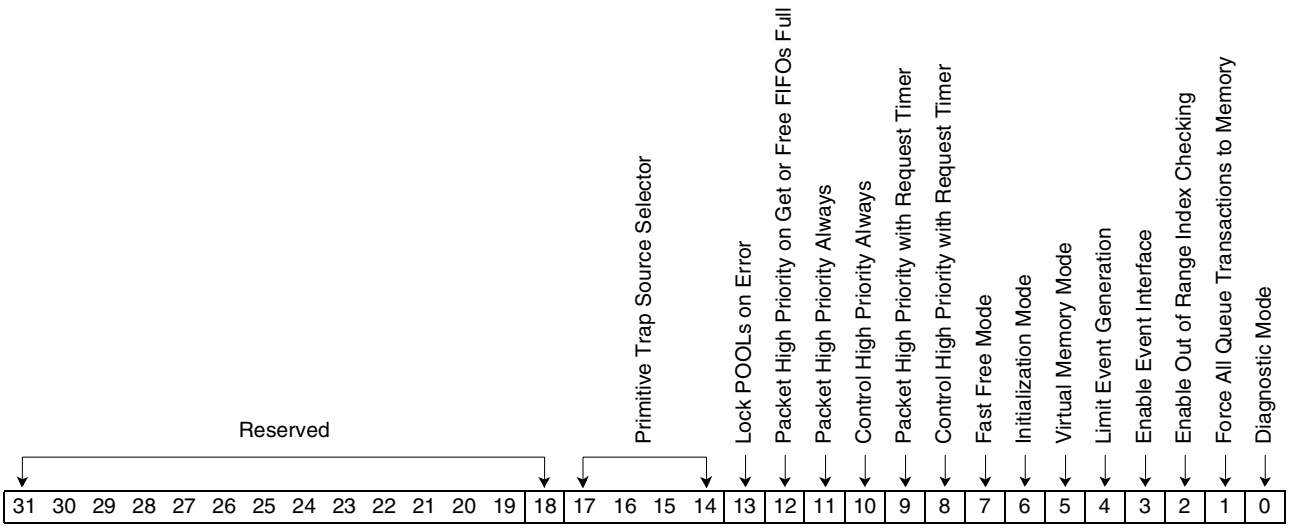
Length 32 bits

Type Clear/Set

Address XXXX 30C8 and 30CC

Power On Reset Value x‘0000 2001’

Restrictions Caution must be used when asserting some of the bits during operation.



Bit(s)	Function	Description
31-19	Reserved	Reserved.
18	Use Compressed Virtual Maps	This bit selects compressed virtual maps when set.
17-14	Primitive Trap Source Selector	These bits will select the source of the last primitive trapped register. 0000 Free from the PCI bus 0001 Free from REASM 0010 Free from RXQUE 0011 Free from CSKED 0100 Free from SEGBF 0101 Free from DMAQS 0110 Get from PCI Bus 0111 Get from REASM 1(RA) 1000 Get from DMAQS 1001 Get from VIMEM (POOL ID (4 bits)), size (2 bits), blank (10 bits), index (16 bits)) 1010 Get from REASM 0(RC) 1011 Free from PCORE DCR 1100 Get from PCORE DCR
13	Lock POOLS on Error	When set, this bit in conjunction with the lock mask will hold POOLS state machines in an idle state until cleared.

Bit(s)	Function	Description
12	Packet High Priority on Get or Free FIFOs Full	When set, this bit causes POOLS to turn on its high priority request to Packet Memory when either the free or get FIFO is full.
11	Packet High Priority Always	When set, this bit causes POOLS to always use its high priority request to Packet Memory.
10	Control High Priority Always	When set, this bit causes POOLS to always use its high priority request to Control Memory.
9	Packet High Priority with Request Timer	When set, this bit causes POOLS to time the wait for Packet Memory service and when the timer expires move to high priority.
8	Control High Priority with Request Timer	When set, this bit causes POOLS to time the wait for Control Memory service and when the timer expires move to high priority.
7	Fast Free Mode	When this bit is set, Fast Free Mode is enabled. When POOLS is in Fast Free Mode, it does not write out the buffer map with the modified control information that indicates that the map is unused. When in this mode unused buffer-free error checking is disabled.
6	Initialization Mode	When the value of the bit is ‘0’, initialization mode is set. When the value is ‘1’, operational mode is set. During initialization mode indexes are in the upper 16 bits of the data word. It is assumed that when initialization mode is on other normal operations are not active such as transmit or receive. During operational mode packet addresses assumed to be on the data bus.
5	Virtual Memory Mode	When set to ‘0’, Virtual Memory mode is enabled. When set to ‘1’, real memory mode is enabled.
4	Limit Event Generation	When set, this bit causes POOLS to limit the issuance of events to RXQUE when a GTD threshold, Total Threshold or POOL Threshold is reached. It will issue the first event and disable the related event enable bit. Software must then reset the bit if it wishes to see another such event. However, it is possible that events may be lost when this bit is set on.
3	Enable Event Interface	When set, this bit causes POOLS to issue resource events to RXQUE when a GTD threshold, Total Threshold or POOL Threshold is reached.
2	Enable Out of Range Index Checking	When set, this bit causes POOLS to check the indexes that are streaming by to be checked against a maximum value for that size index. If the normal initialization sequence is used, these maximum values will auto set.
1	Force All Queue Transactions to Memory	When set, this bit disables the internal tail to head transfer path within the queue. All indexes will proceed into memory before being brought to the head of the queue. This effectively preserves the operational history in memory. However, some caution is warranted since four full entries are required for a write to memory. This could cause indexes to get “stuck” at the back of the queue. When this residue occurs, a zero pointer is returned even though the operation might have otherwise returned a valid pointer.
0	Diagnostic Mode	When set, POOLS is in diagnostic mode. When cleared, POOLS is in normal mode. When in diagnostic mode, state machines are idle. If they are already active, once they go idle they will hold there.

3.17.21 POOLS Buffer Threshold Registers 0-4

The POOLS Buffer Threshold Registers 0-4 is the threshold set by the software to set the threshold crossed bit in the POOLS Status Register. This register is used to compare with the queue length register.

This register consists of a 16-bit count match. The threshold count is compared to the queue length count. If the queue length is less than the value in this register, the appropriate bit is set in the status register respective to this queue.

Length	32 bits	
Type	Read/Write	
Address	Buffer Size 0	XXXX 3088
	Buffer Size 1	XXXX 308C
	Buffer Size 2	XXXX 3090
	Buffer Size 3	XXXX 3094
	Virtual Packets/ Buffer Size 4	XXXX 3098
Power On Reset Value		x‘0000 0000’
Restrictions	None	

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Buffer Threshold	User defined value to compare with the queue length register for the respective queue size.

3.17.22 POOLS Index Threshold Registers 0-4

The POOLS Index Threshold Registers 0-4 provide error checking. These are the thresholds set by the software or hardware to set the index threshold crossed bit in the POOLS Status Register. This register is used to check indexes during free operations to look for an out of bounds index.

Each register consists of a 16-bit compare value. The threshold count is compared to the index while being processed. If an index is greater than the value in this register, the appropriate bit is set in the status register.

Length 32 bits

Type Read/Write

Address

Buffer Size 0	XXXX 30F0
Buffer Size 1	XXXX 30F4
Buffer Size 2	XXXX 30F8
Buffer Size 3	XXXX 30FC
Virtual Packets/ Buffer Size 4	XXXX 3100

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Index Threshold	Value used to compare indexes during free operations.

3.17.23 POOLS Last Primitive Trap Register

The POOLS Last Primitive Trap Register provide debug assistance. It contains the 32-bit last primitive address, and it is the last primitive address to POOLS, as selected in the POOLS Control Register, while in operational mode.

Length 32 bits

Type Read Only

Address XXXX 30E8

Power On Reset Value x‘0000 0000’

Restrictions None

3.17.24 POOLS Last Buffer Map Read on Free Register

The POOLS Last Buffer Map Read on Free Register provides debug assistance. It contains the 32-bit address of the buffer map used in the last free operation, and it is the address of the last buffer map read on a free.

Length 32 bits

Type Read Only

Address XXXX 30EC

Power On Reset Value x‘0000 0000’

Restrictions None

3.17.25 POOLS Error Lock Enable Register

The POOLS Error Lock Enable Register provides the ability to halt POOLS when the corresponding status bit in the status register is set.

When a bit in this register corresponds to a bit set in the status register, the state machines in POOLS will be held in idle state until the lock is disabled.

Length 32 bits

Type Clear/Set

Address XXXX 30D8 and 30DC

Power On Reset Value x‘0000 F800’

Restrictions None

Bit(s)	Name	Description
31-22	Reserved	Reserved.
21-0	Lock Enables	When one of these bits is on and the corresponding bit in the *POOLS Status Register* is on, the memory subsytem will halt.

3.17.26 POOLS Packet and Control Memory Access Threshold

The POOLS Packet and Control Memory Access Threshold timers are used to help limit the amount of time that POOLS can be held off from its respective memory.

The bits are a 12-bit count. When the proper bit in the POOLS Control Register is set and a request is made to the requisite memory, a counter is loaded with this value. The counter will then count down to zero in 15 ns ticks. When it hits zero, it forces the request to high priority.

Length	32 bits	
Type	Read/Write	
Address	Packet Memory Timer Threshold	XXXX 30E4
	Control Memory Timer Threshold	XXXX 30E0
Power On Reset Value		x‘0000 0080’
Restrictions	None	

Bit(s)	Name	Description
31-12	Reserved	Reserved.
11-0	Access Holdoff Time	Value to load into access timers. When a timer is loaded with this value, it will count down until either memory is accessed or it hits 0. If it hits 0, POOLS will change its memory request from low to high priority.

3.17.27 POOLS Buffer Map Group

The POOLS Buffer Map Group holds the buffer map of the packet that is in the process of being freed. From this map, the POOL ID and the indexes used are returned to their correct queue.

This register consists of a 16-bit flag field and 16-bit indexes.

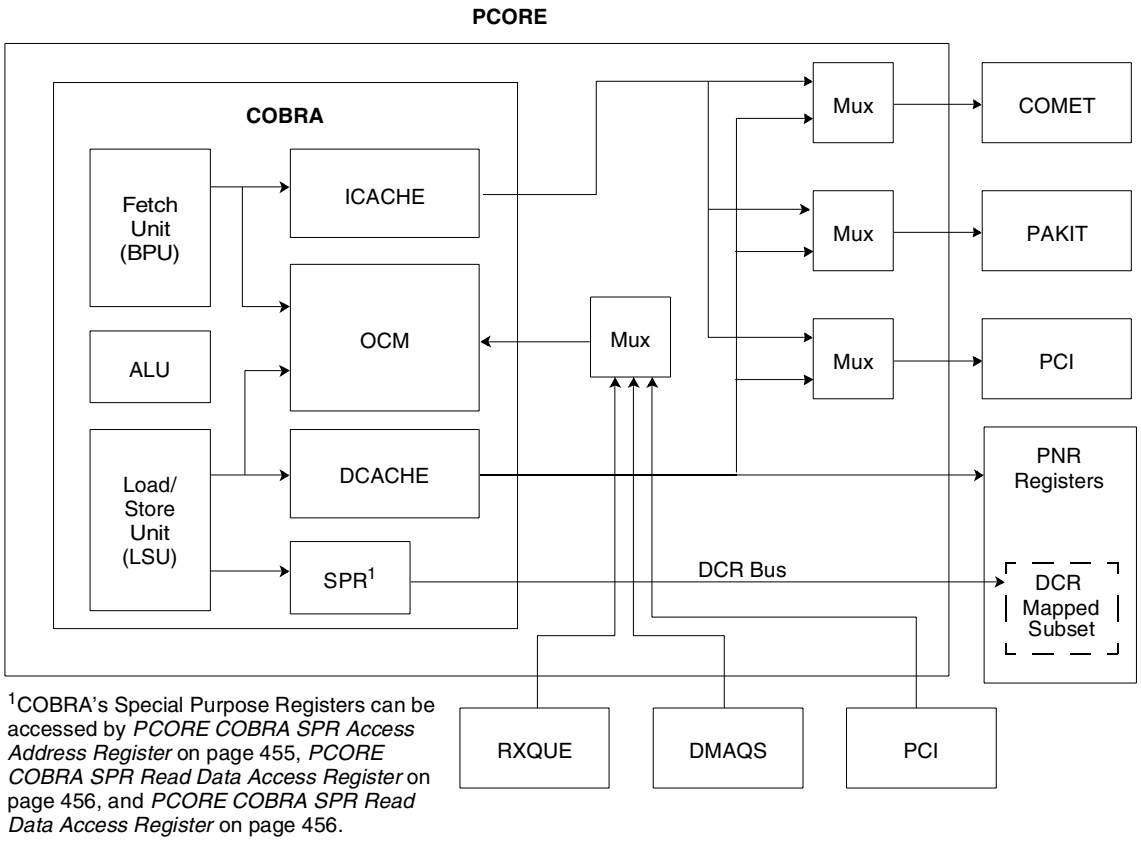
The flag field contains the POOL ID and the valid bit. When a packet is freed, the valid bit is set to '0'. When a get operation occurs, the valid bit is then set. This helps to find address duplicates and other address related problems that software can generate.

Length	32 bits		
Type	Read/Write		
Address	**Upper 16 Bits:**	**Lower 16 Bits:**	
	Flag Field 0	Index 0	XXXX 309C
	Index 1	Index2	XXXX 30A0
	Flag Field 1	Index 3	XXXX 30A4
	Index 4	Index 5	XXXX 30A8
	Flag Field 2	Index 6	XXXX 30AC
	Index 7	Index 8	XXXX 30B0
	Flag Field 3	Index 9	XXXX 30B4
	Index 10	Index 11	XXXX 30B8
	Flag Field 4	Index 12	XXXX 30BC
	Index 13	Index 14	XXXX 30C0
Power On Reset Value			x'FFFF FFFF'
Restrictions	None		

3.18 Processor Core (PCORE)

PCORE contains the on-board processor and its local subsystems. The primary intent is to run Available Bit Rate (ABR) control software and user application code such as protocol termination/assist code. PCORE contains all of the arbitration logic used to give COBRA (the Chip OnBoard Risc Architecture entity) access to the chip facilities, and for the other chip facilities to access OCM.

Figure 35: PCORE Structure



3.18.1 PCORE Entity Overview

3.18.1.1 DCR Interface

The Device Control Register (DCR) interface is a special processor bus to access local registers. These include serial port registers and various other registers.

3.18.1.2 Interrupt Controller

This logic manages the interrupts that are passed to the COBRA Core. There are two levels of interrupt for the core: Critical Interrupts and Normal Interrupts. Interrupts can be taken from both on chip and off chip sources. PCORE has a variety of interrupt source and enable registers.

3.18.1.3 Bridge-Address Translation

The COBRA Core can access a variety of memory subsystems. Facilities are provided that allow multiple subsystem accesses. Processor address space is translated into target memory system addresses. For the most part, this allows the processor to be unaware of target memory address space considerations while running mainline code.

3.18.1.4 OCM SRAM

OCM is provided for the use of the processor. Typical access time to the OCM is a single cycle, the same as for cache. Address translation facilities have been added to make more efficient use of this memory via additional and extended BAT registers.

3.18.1.5 Control Memory

Control Memory can be accessed by the processor. This memory may be mapped into the processor space in a number of different ways.

3.18.1.6 Packet Memory

Packet memory can be accessed by the processor. This memory may be mapped into the processor space in a number of different ways. Packet memory space also includes the virtual memory space of the PNR.

3.18.1.7 PCI Master Interface-External

The processor can access the PCI bus through this interface. Parts of PCI space are mapped into processor space. There are a number of different ways this can be mapped into processor space.

3.18.1.8 PNR Register Space

This access mode of the PCI master interface allows access to the internal PNR registers. This access is handled internally and does not affect the external PCI bus.

3.18.2 PCORE Control Register

The PCORE Control Register provides control information about PCORE operations.

Length 32 bits

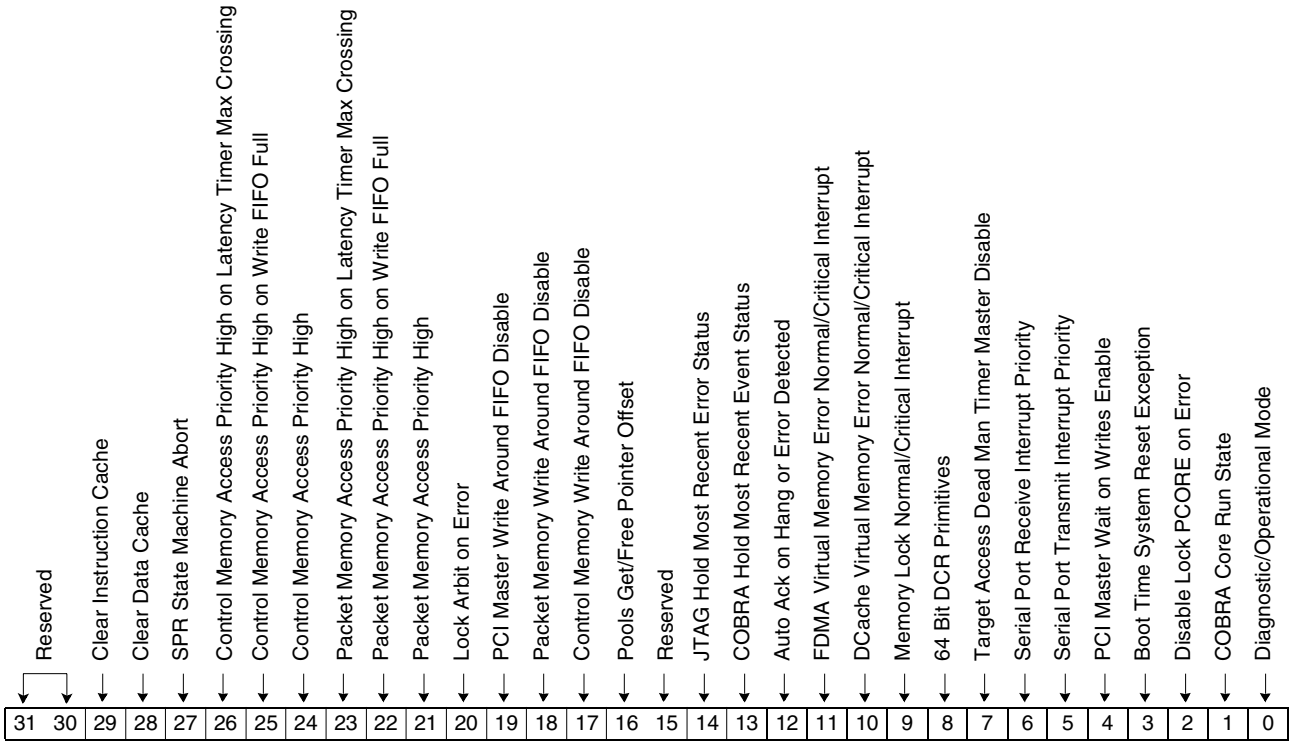
Type Clear/Set

Address XXXX 4000 and 4004

DCR Address x‘262’ and x‘263’

Power On Reset Value x‘000E 4009’

Restrictions Caution must be used when asserting some of the bits during operation.



Bit(s)	Name	Description
31-30	Reserved	Reserved.
29	Clear Instruction Cache	This bit will cause the instruction cache to clear itself to a known state. It will also cause the processor to be in stop state when this happens. It will be cleared when the cache has finished.
28	Clear Data Cache	This bit will cause the data cache to clear itself to a known state. It will also cause the processor to be in stop state when this happens. It will be cleared when the cache has finished.
27	SPR State Machine Abort	This bit will put the SPR Access Machine into a reset state, so it should be used by setting and then clearing.
26	Reserved	Reserved.

Bit(s)	Name	Description
25	Control Memory Access Priority High on Write FIFO Full	When set, Control Memory accesses will switch to high priority when the Control Memory write around FIFO is full.
24	Control Memory Access Priority High	When set, Control Memory accesses will be at high priority always.
23	Reserved	Reserved.
22	Packet Memory Access Priority High on Write FIFO Full	When set, Packet Memory accesses will switch to high priority when the Packet Memory write around FIFO is full.
21	Packet Memory Access Priority High	When set, Packet Memory accesses will be at high priority always.
20	Lock Arbit on Error	When set to '1', this will cause a lock command to be issued to ARBIT to halt the memory subsystem.
19	PCI Master Write Around FIFO Disable	Disables the write around buffer for PCI Master. When enabled, write data from either the ICACH or DCACH is buffer through this FIFO on writes.
18	Packet Memory Write Around FIFO Disable	Disables the write around buffer for Packet Memory. When enabled, write data from either the ICACH or DCACH is buffer through this FIFO on writes.
17	Control Memory Write Around FIFO Disable	Enables the write around buffer for Control Memory. When enabled write data from either the ICACH or DCACH is buffer through this FIFO on writes.
16	Pools Get/Free Pointer Offset	When this bit is written to '1', the addition of an offset to the get pointer primitive and the subtraction of an offset from the free pointer primitive are enabled.
15	Reserved	Reserved.
15	Disable Xfer Abort on Pseudo Core Reset	When this bit is written to '1', transfer aborts on Pseudo resets are disabled; when '0', the core master state machines will be put into idle.
14	JTAG Hold Most Recent Error Status	When this bit is written to '0', the JTAG error status register will free run. When set to '1' it will hold the most recent error status.
13	COBRA Hold Most Recent Event Status	When this bit is written to '1', COBRA Core hold its most recent internal event status. When set to '0' it will free run.
12	Auto Ack on Hang or Error Detected	When this bit is written to '0', PCORE will not auto ack on hang or error. This may leave the processor in a totally stuck state. However corrupted information may be stopped from entering the processor. When set to '1' and hang or error conditions manifest reads may return garbage and write data may be lost BUT the processor should not be stopped cold.
11	FDMA Virtual Memory Error Normal/Critical Interrupt	When this bit is written to '0', PCORE will treat an PNR virtual memory write error as a critical interrupt. When it is '1', this condition will be treated as a normal interrupt.
10	DCache Virtual Memory Error Normal/Critical Interrupt	When this bit is written to '0', PCORE will treat an PNR virtual memory write error as a critical interrupt. When it is '1', this condition will be treated as a normal interrupt.
9	Memory Lock Normal/Critical Interrupt	When this bit is written to '0', PCORE will treat memory locked as a critical interrupt. When it is '1', this condition will be treated as a normal interrupt.
8	64 Bit DCR Primitives	When set, the three DCR primitives work in 64-bit mode. In this mode, the first access to the primitive register is to the upper 32 bits. The second reference is to the lower 32 bits. The second access triggers the completion of the operation at the destination.
7	Target Access Dead Man Timer Master Disable	When set, this will disable all of the Target Access Dead Man Timers: PCI Master, Control Memory, Packet Memory, PNR Registers, and DCR.
6	Serial Port Receive Interrupt Priority	When set, this will cause the receive interrupt to be a Critical Interrupt. When not set, it is a regular interrupt.
5	Serial Port Transmit Interrupt Priority	When set, this will cause the transmit interrupt to be a Critical Interrupt. When not set, it is a regular interrupt.
4	PCI Master Wait on Writes Enable	When set, this will cause the PCI access machine to wait until the data is actually confirmed written to the device. Normally, this bit is set to off since it decreases performance when enabled.

Bit(s)	Name	Description
3	Boot Time System Reset Exception	When set, this bit will issue a system boot reset exception to the COBRA Core Processor. It is reset by the COBRA Core Processor after it has received the system reset exception.
2	Disable Lock PCORE on Error	When this bit is set and an error occurs and the corresponding lock enable bit is set, PCORE will lock. This state is equivalent to being in diagnostic mode.
1	COBRA Core Run State	When set, this will place the COBRA Core into run state. When not set, the processor will return to idle state.
0	Diagnostic/Operational Mode	When set, PCORE is in diagnostic mode. When cleared, PCORE is in operational mode. When in diagnostic mode, state machines are held in idle. If they are already active, when they go to idle they will hold there.

3.18.3 PCORE Reset Control Register

The PCORE Reset Control Register provides control information about PCORE reset operations.

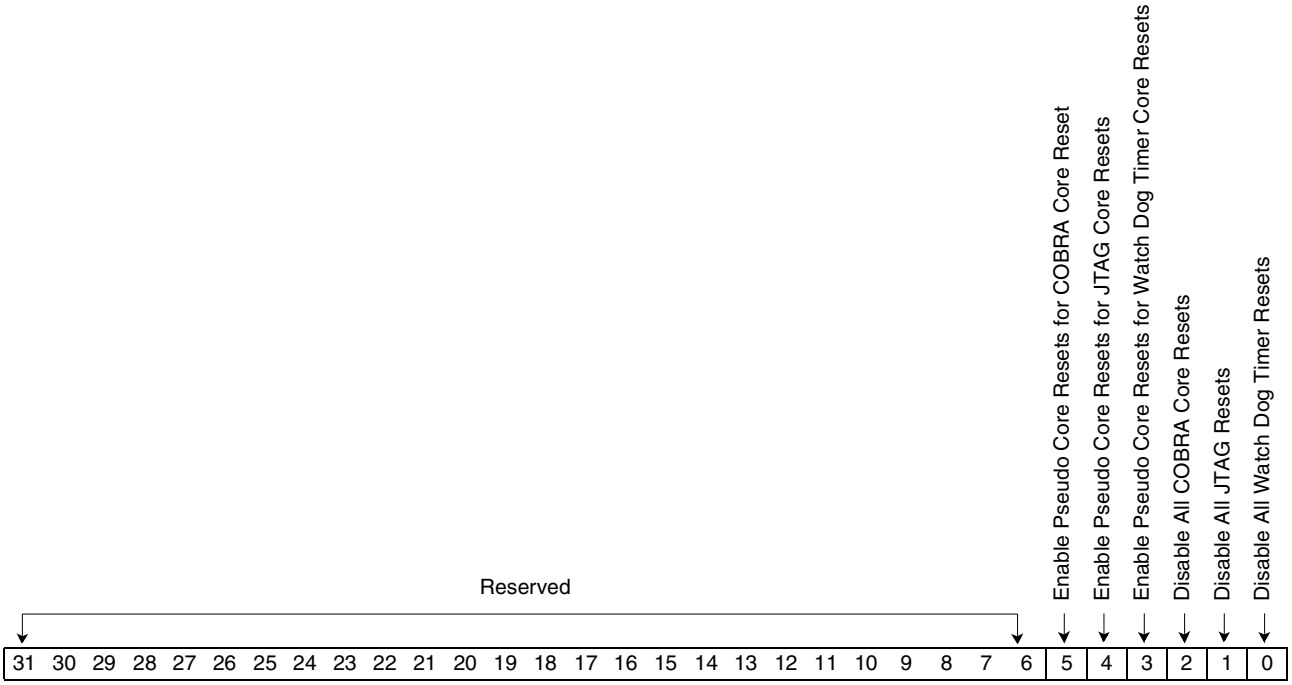
Length 32 bits

Type Clear/Set

Address XXXX 4238 and 423C

Power On Reset Value x‘000E 0009’

Restrictions Caution must be used when asserting some of the bits during operation.



Bit(s)	Name	Description
31-6	Reserved	Reserved.
5	Enable Pseudo Core Resets for COBRA Core Reset	When this bit is written to ‘0’, COBRA Core resets are converted to chip resets. When this bit is written to ‘1’, a pseudo core reset is issued instead.
4	Enable Pseudo Core Resets for JTAG Core Resets	When this bit is written to ‘0’, COBRA Core resets are converted to chip resets. When this bit is written to ‘1’, a pseudo core reset is issued instead.
3	Enable Pseudo Core Resets for Watch Dog Timer Core Resets	When this bit is written to ‘0’, COBRA Core Watch Dog Timer core resets are converted to chip resets. When this bit is written to ‘1’, a pseudo core reset is issued instead.
2	Disable All COBRA Core Resets	When this bit is written to ‘1’, all COBRA Core resets are disabled.
1	Disable All JTAG Resets	When this bit is written to ‘1’, JTAG resets are disabled.
0	Disable All Watch Dog Timer Resets	When this bit is written to ‘1’, Watch Dog Timer resets are disabled.

3.18.4 PCORE Status Register

The PCORE Status Register provides status information about PCORE operations.

Length 32 bits

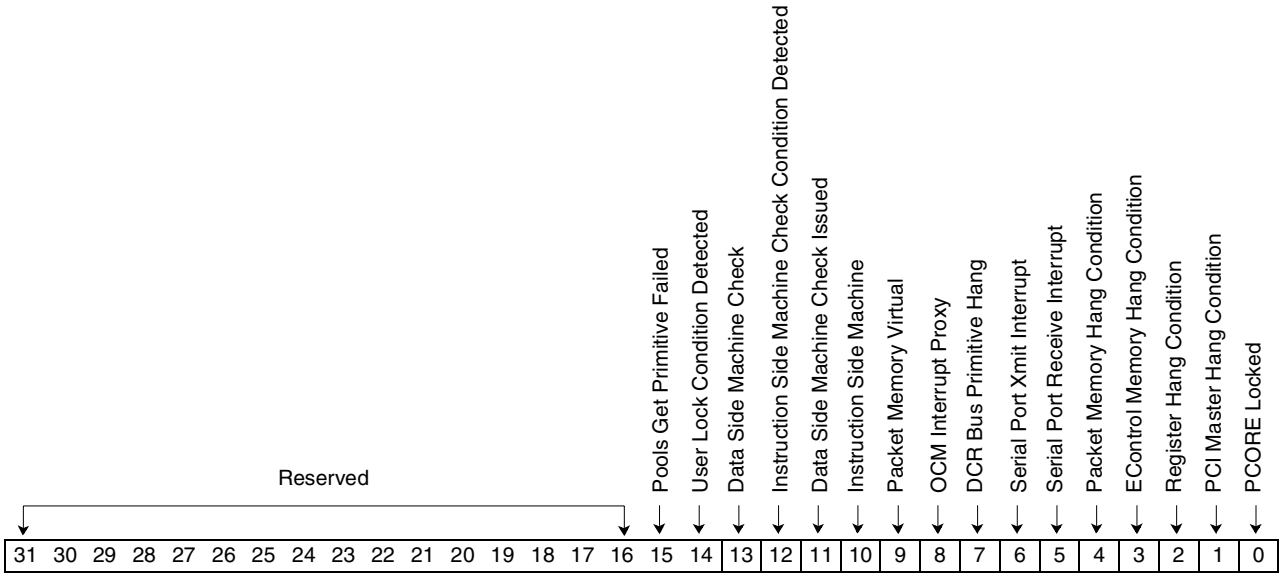
Type Clear/Set

Address XXXX 4008 and 400C

DCR Address x‘264’ and x‘265’

Power On Reset Value x‘0000 8000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15	Pools Get Primitive Failed	When a get is attempted from POOLS and the request is rejected, this bit will be set.
14	User Lock Condition Detected	When a bit in the PCORE User Status Register and the corresponding bit in the PCORE User Error Lock Enable Register are both set, this bit will be set.
13	Data Side Machine Check Condition Detected	A Data Side Machine Check Condition was detected but not necessarily sent to the COBRA Core.
12	Instruction Side Machine Check Condition Detected	An Instruction Side Machine Check Condition was detected but not necessarily sent to the COBRA Core.
11	Data Side Machine Check Issued	A machine check has been issued to the COBRA Core due to a Data Side PCORE error.
10	Instruction Side Machine Check Issued	A machine check has been issued to the COBRA Core due to an Instruction Side PCORE error.
9	Packet Memory Virtual Write Failure	When this is set, a virtual write has failed to virtual memory. Either a NAK was returned during the write or while holding for error checking after the write. In either case, it indicates the required storage to complete the operation was not available.

Bit(s)	Name	Description
8	OCM Interrupt Proxy	When set, OCM is indicating an interrupt condition.
7	DCR Bus Primitive Hang Condition	One of the DCR primitive accesses has timed out.
6	Serial Port Xmit Interrupt	When the serial port surfaces a Xmit Interrupt, it will be reflected here.
5	Serial Port Receive Interrupt	When the serial port surfaces a Receive Interrupt, it will be reflected here.
4	Packet Memory Hang Condition	Packet memory interface Dead Man Timer has expired.
3	Control Memory Hang Condition	Control Memory interface Dead Man Timer has expired.
2	Register Hang Condition	Register interface Dead Man Timer has expired.
1	PCI Master Hang Condition	PCI Master interface Dead Man Timer has expired.
0	PCORE Locked	This bit is set when locking is enabled; an error has occurred and the lock mask bit is set that matches the error.

3.18.5 PCORE User Status Register

The PCORE User Status Register provides user-defined status information about PCORE software operations.

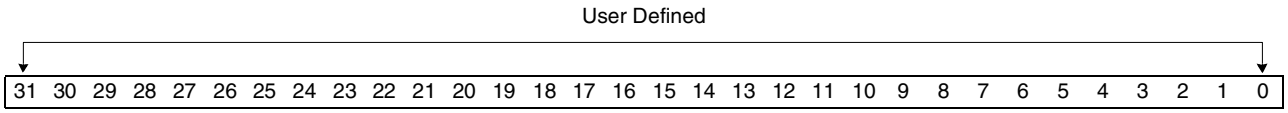
Length 32 bits

Type Clear/Set

DCR Address x‘200’ and x‘201’

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31-0	User defined	Reserved.

3.18.6 PCORE COBRA Core External Status Register

The PCORE COBRA Core External Status Register provides COBRA Core-defined status information about PCORE.

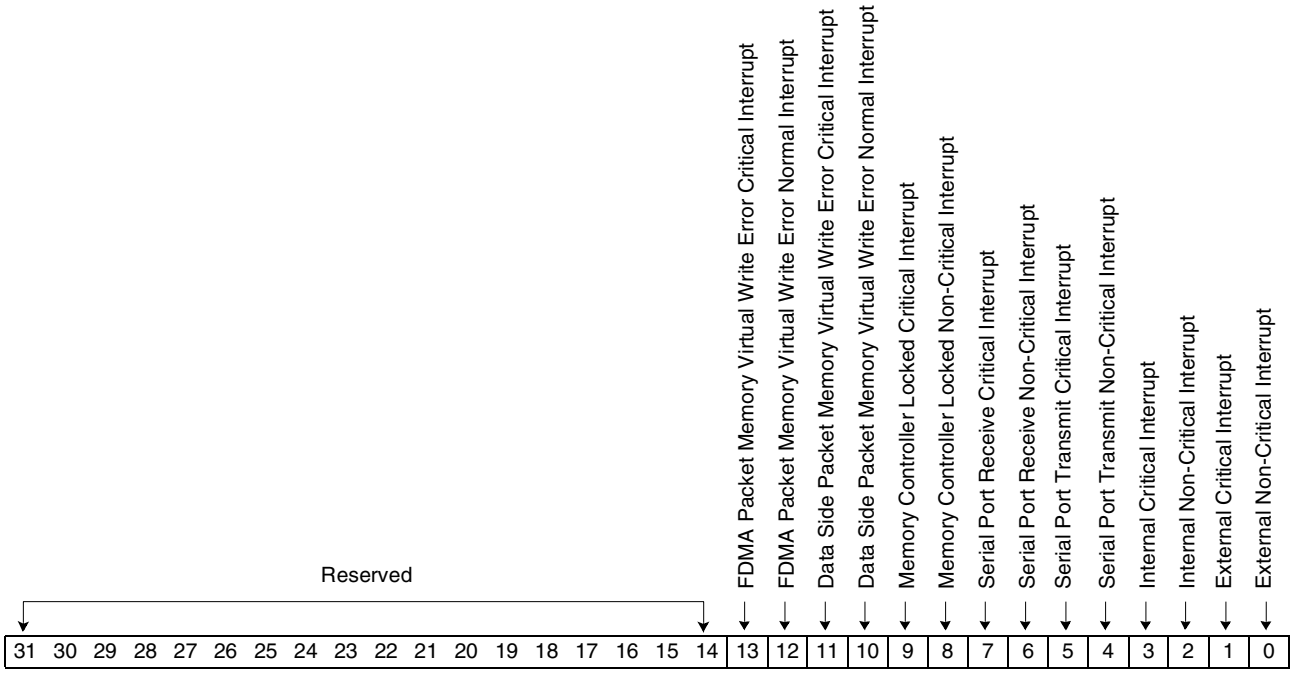
Length 32 bits

Type Clear/Set

DCR Address x‘202’ and x‘203’

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31-14	Reserved	Reserved.
13	FDMA Packet Memory Virtual Write Error Critical Interrupt	This occurs when the Packet Memory controller returns an error on a packet virtual memory write and the FDMA-side is accessing and this condition is set as critical.
12	FDMA Packet Memory Virtual Write Error Normal Interrupt	This occurs when the Packet Memory controller returns an error on a packet virtual memory write and the FDMA-side is accessing this condition is set as normal.
11	Data Side Packet Memory Virtual Write Error Critical Interrupt	This occurs when the Packet Memory controller returns an error on a packet virtual memory write and the D-side is accessing and this condition is set as critical.
10	Data Side Packet Memory Virtual Write Error Normal Interrupt	This occurs when the Packet Memory controller returns an error on a packet virtual memory write and the D-side is accessing this condition is set as normal.
9	Memory Controller Locked Critical Interrupt	This occurs when the memory controller is locked and this condition is set as critical.

Bit(s)	Name	Description
8	Memory Controller Locked Non-Critical Interrupt	This occurs when the memory controller is locked and this condition is set as non-critical.
7	Serial Port Receive Critical Interrupt	This occurs when the serial controller has a transmit interrupt and the corresponding critical interrupt enable is on in the control register.
6	Serial Port Receive Non-Critical Interrupt	This occurs when the serial controller has a transmit interrupt and the corresponding critical interrupt enable is on in the control register.
5	Serial Port Transmit Critical Interrupt	This occurs when the serial controller has a transmit interrupt and the corresponding critical interrupt enable is on in the control register.
4	Serial Port Transmit Non-Critical Interrupt	This occurs when the serial controller has a transmit interrupt and the corresponding critical interrupt enable is on in the control register.
3	Internal Critical Interrupt	This occurs when a bit in the PNR primary status register is set and the corresponding critical interrupt enable is on.
2	Internal Non-Critical Interrupt	This occurs when a bit in the PNR primary status register is set and the corresponding non-critical interrupt enable is on.
1	External Critical Interrupt	This occurs when an off chip interrupt is received and the non-critical enable for off chip interrupts is set.
0	External Non-Critical Interrupt	This occurs when an off chip interrupt is received and the non-critical enable for off chip interrupts is set.

3.18.7 PCORE COBRA Core External Machine Check Status Register

The PCORE COBRA Core External Machine Check Status Register provides COBRA Core machine check status information about PCORE.

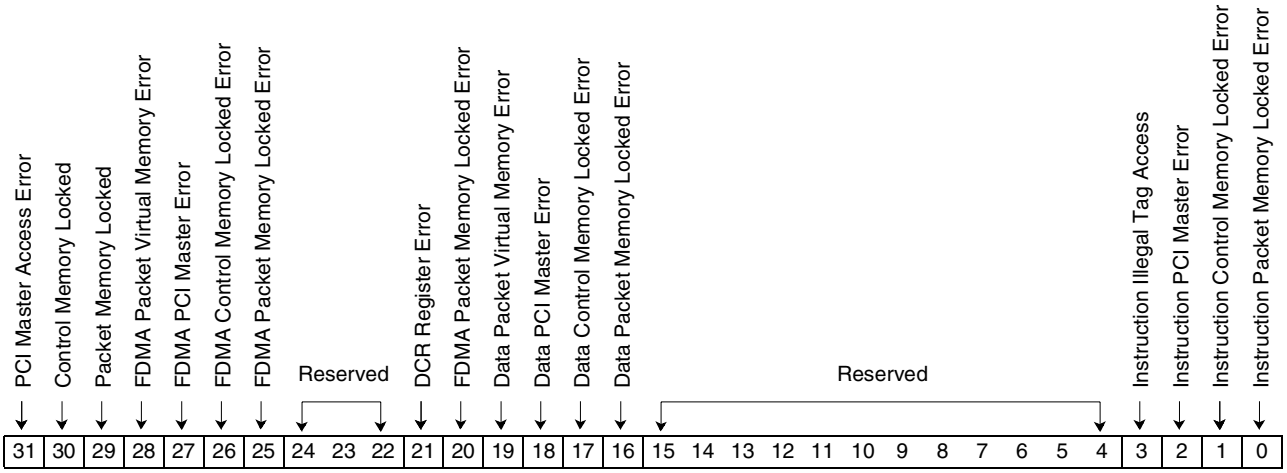
Length 32 bits

Type Clear/Set

DCR Address x‘25C’ and x‘25D’

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31	PCI Master Access Error	This occurs when the PCI Master Machine returns an error and no requestor currently owns the machine.
30	Control Memory Locked	This occurs when Packet Memory is in a locked state.
29	Packet Memory Locked	This occurs when Packet Memory is in a locked state.
28	FDMA Packet Virtual Memory Error	This occurs when Packet Memory indicates a write error during access of a virtual buffer.
27	FDMA PCI Master Error	This occurs when a PCI master access has an error returned while the data path is accessing it.
26	FDMA Control Memory Locked Error	This occurs when Control Memory locks while the data path is actively accessing it.
25	FDMA Packet Memory Locked Error	This occurs when Packet Memory locks while the data path is actively accessing it.
24-22	Reserved	Reserved.
21	DCR Register Error	This occurs when a fatal error, typically a hang, occurs on a DCR register timeout.
20	FDMA Packet Memory Locked Error	This occurs when Packet Memory locks while the data path is actively accessing it.
20	Data Register Error	This occurs when a fatal error, typically a hang, occurs on an PNR register timeout.

Bit(s)	Name	Description
19	Data Packet Virtual Memory Error	This occurs when Packet Memory indicates a write error during access of a virtual buffer.
18	Data PCI Master Error	This occurs when a PCI master access has an error returned while the data path is accessing it.
17	Data Control Memory Locked Error	This occurs when Control Memory locks while the data path is actively accessing it.
16	Data Packet Memory Locked Error	This occurs when Packet Memory locks while the data path is actively accessing it.
15-4	Reserved	Reserved.
3	Instruction Illegal Tag Access	This occurs when the Instruction side specifies the register space or OCM for the instruction source via the cache. Since there are no physical connections, these accesses can not occur.
2	Instruction PCI Master Error	This occurs when PCI master access has an error returned while the instruction path is accessing it.
1	Instruction Control Memory Locked Error	This occurs when Control memory locks while the instruction path is actively accessing it.
0	Instruction Packet Memory Locked Error	This occurs when Packet Memory locks while the instruction path is actively accessing it.

3.18.8 PCORE JTAG Debug Control Register

The PCORE JTAG Debug Control Register enables the JTAG port or a PCI interface processor debugger to control the processor core.

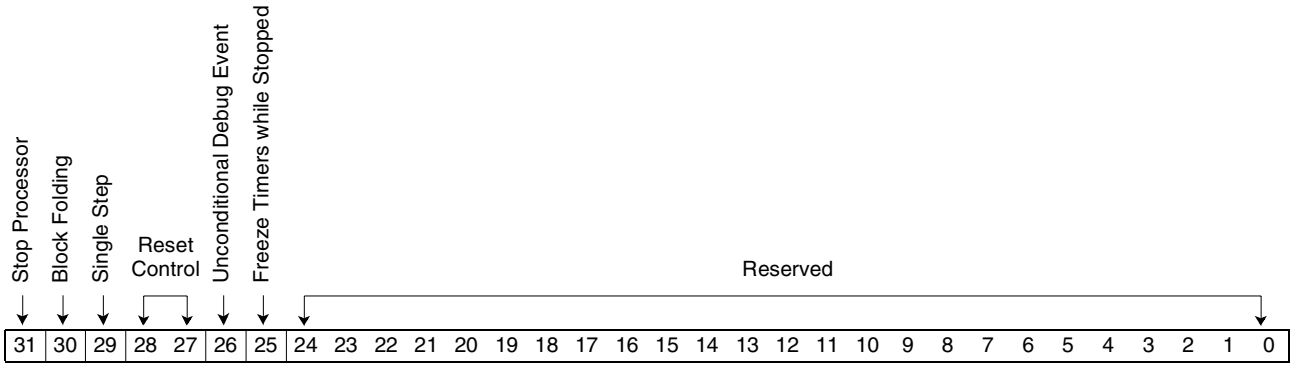
Length 32 bits

Type Read/Write

Address XXXX 4200

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31	Stop Processor	This bit forces the processor to halt execution.
30	Block Folding	The processor normally dispatches two instructions at a time. Setting this bit forces instruction dispatches to be serialized.
29	Single Step	Setting this bit when the processor is stopped causes the processor to execute one or two instructions depending on the value of bit 30. This bit clears itself after one cycle automatically.
28-27	Reset Control	These bits potentially generate one of three resets depending on their value. They reset to ‘00’ after one cycle automatically. The bits decode as follows: 00 No reset 01 Core reset 10 Chip reset 11 System reset
26	Unconditional Debug Event	This bit generates an interrupt to the processor. It resets to ‘0’ after one cycle automatically.
25	Freeze Timers while Stopped	This bit freezes the state of all timers in the core if the processor is stopped.
24-0	Reserved	Reserved.

3.18.9 PCORE JTAG Debug Status Register

The PCORE JTAG Debug Status Register returns core status.

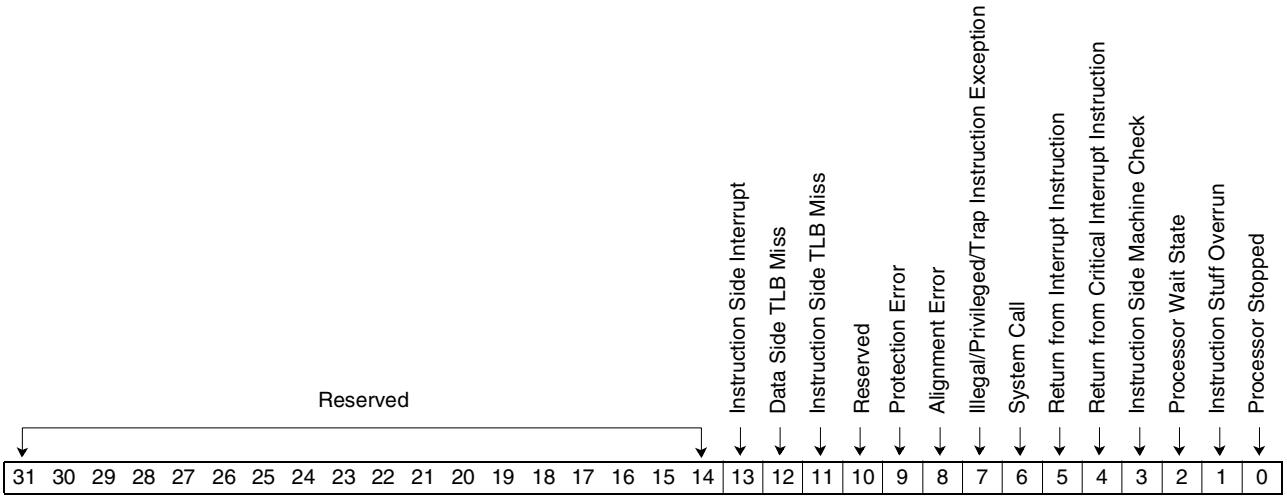
Length 32 bits

Type Read Only

Address XXXX 4204

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-14	Reserved	Reserved.
13	Instruction Side Interrupt	An exception has occurred in the instruction processing portion of the core.
12	Data Side TLB Miss	A miss has occurred in the data side Translation Look-aside Buffer.
11	Instruction Side TLB Miss	A miss has occurred in the instruction side Translation Look-aside Buffer.
10	Reserved	Reserved.
9	Protection Error	A protection error occurred.
8	Alignment Error	An alignment error occurred.
7	Illegal/Privileged/Trap Instruction Exception	An instruction was encountered that caused an exception because it was illegal, generated a privilege violation, or was a trap instruction.
6	System Call	A system call exception occurred.
5	Return from Interrupt Instruction	An RFI instruction was executed.
4	Return from Critical Interrupt Instruction	An RFCI instruction was executed.
3	Instruction Side Machine Check	A machine check condition has occurred in the instruction processing portion of the core.
2	Processor Wait State	The processor is in a wait state.

Bit(s)	Name	Description
1	Instruction Stuff Overrun	The debug port has attempted to insert an instruction into the processor via the JTAG Instruction Stuff Buffer (JISB) and it was not accepted by the processor. The instruction must be reloaded into the JISB.
0	Processor Stopped	The processor is currently in a stopped state.

3.18.10 PCORE JTAG Instruction Stuff Buffer

The PCORE JTAG Instruction Stuff Buffer is used to insert an instruction into the processor for execution.

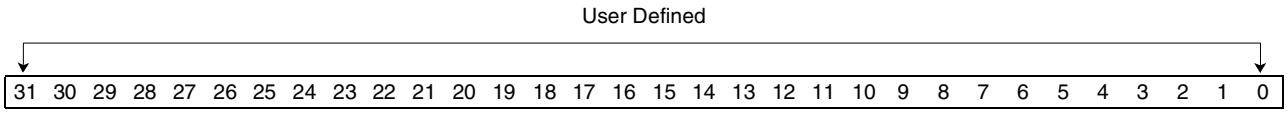
Length 32 bits

Type Read/Write

Address XXXX 4208

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Instruction	Instruction to be passed from the JTAG/PCI debug interface to the core GPRs.

3.18.11 PCORE JTAG Debug Data Register

The PCORE JTAG Debug Data Register enables passing data between the JTAG/PCI debug port and the general purpose registers of the processor core.

Length 32 bits

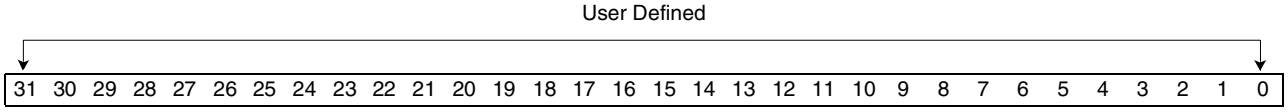
Type Read/Write

Address XXXX 420C

SPR Address x‘3F3’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Data	Data to be passed to/from the JTAG/PCI debug interface to the core GPRs.

3.18.12 PCORE COBRA Core Boot Address

The PCORE COBRA Core Boot Address provides COBRA Core its boot time address.

Length 32 bits

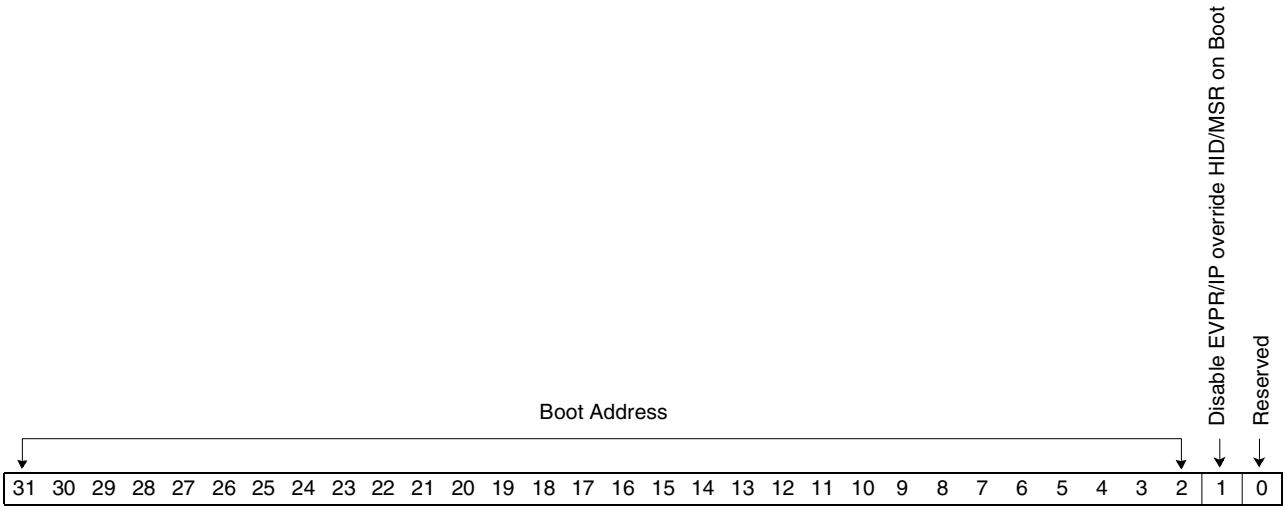
Type Read/Write

Address XXXX 4018

Power On Reset Value x‘FFF0 0100’

Restrictions None

This is the PCORE register. It is used to provide the address used to fetch the first instruction.



Bit(s)	Name	Description
31-2	Boot Address	This is the address the processor will use at boot time.
1	Disable EVPR/IP override HID/ MSR on Boot	Override MSR settings on System Reset Exception to use all of the PCORE COBRA Core Boot Address.
0	Reserved	Reserved.

3.18.13 PCORE COBRA Core Access Priority Control Register

The PCORE COBRA Core Access Priority Control Register provides COBRA Core defined status information about PCORE. It is used to control the order and priority of access to the various memory subsystems that the COBRA Core has access to. It is to be set up at initialization time and not dynamically changed.

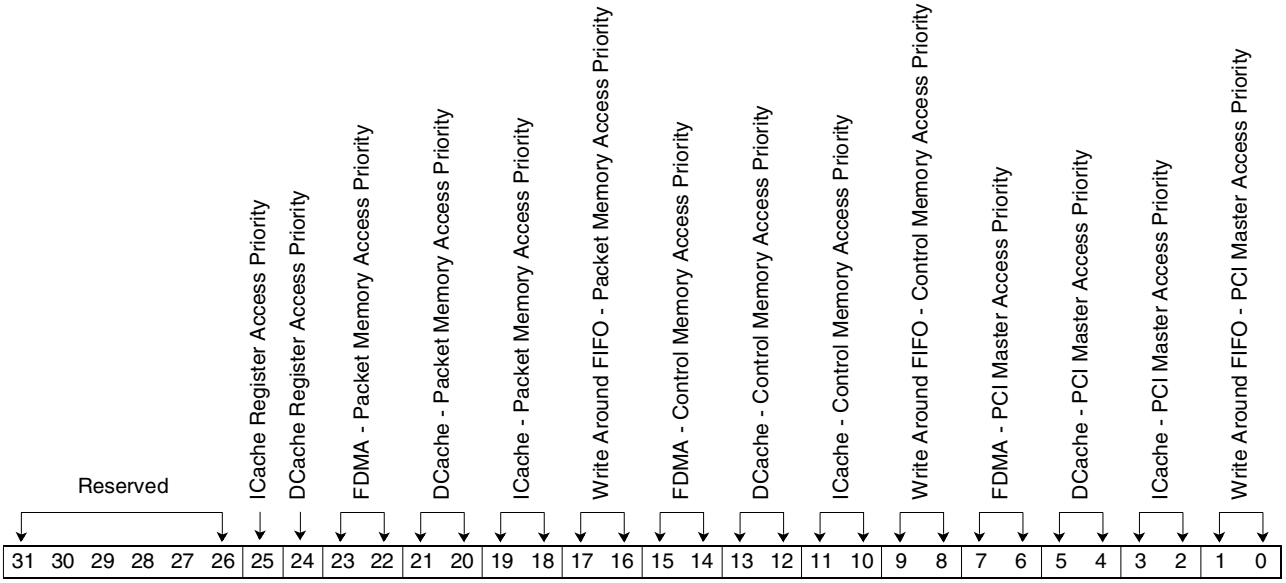
Length 32 bits

Type Read/Write

Address XXXX 401C

Power On Reset Value x‘01E4 E4E4’

Restrictions For each controller accessed, the values cannot be duplicated. That is, all the priorities to a given target subsystem must be unique.



Bit(s)	Name	Description
31-26	Reserved	Reserved.
25	ICache Register Access Priority	This sets the priority into the PNR register port. Zero is low priority; one is high priority.
24	DCache Register Access Priority	This sets the priority into the PNR register port. Zero is low priority; one is high priority.
23-22	FDMA - Packet Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
21-20	DCache - Packet Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
19-18	ICache - Packet Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
17-16	Write Around FIFO - Packet Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
15-14	FDMA - Control Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.

Bit(s)	Name	Description
13-12	DCache - Control Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
11-10	ICache - Control Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
9-8	Write Around FIFO - Control Memory Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
7-6	FDMA - PCI Master Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
5-4	DCache - PCI Master Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
3-2	ICache - PCI Master Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority.
1-0	Write Around FIFO - PCI Master Access Priority	This sets the priority of access to Packet Memory. Zero is the lowest priority; three is the highest priority

3.18.14 PCORE Transaction Dead Man Timer Value Registers

These registers are used to load timers that count to zero from the value loaded in this register. The maximum wait for an I/O transaction is about 2 ms when this register is set to x‘0000 FFFF’. The value of this register is written into the corresponding timer after the transaction is initiated with the target. It continues to count down until the target responds or zero is reached in the timer. When the timer reaches zero, a status bit is set and action can be taken.

Length 32 bits

Type Read/Write

Address

PCI Master Dead Man Timer Value	XXXX 4020
PNR Register Dead Man Timer Value	XXXX 4024
Control Memory Dead Man Timer Value	XXXX 4028
Packet Memory Dead Man Timer Value	XXXX 402C
DCR Primitive Access Dead Man Timer Value	XXXX 40F8

Power On Reset Value x‘0000 FFFF’

Restrictions None

Bit(s)	Name	Description
31-0	Reserved	Reserved
15-0	Dead Man Timer Load Value	Value to load into the related dead man timer at the start of a transaction. This value is the limit on the time the transaction is allowed to take before completion.

3.18.15 PCORE Transaction Dead Man Timer Register

These timers are used to time transactions that are valid but the target does not respond right away. The timer counts on a 7.5 ns time base. The maximum wait for an I/O transaction is about 2 ms when the timer counts down from x‘0000 FFFF’. This timer counts down to zero from the values set in the value register. When zero is reached, the transaction is considered broken and the request will be acknowledged back to the requestor.

Length 32 bits

Type Read Only

Address

PCI Master Dead Man Timer	XXXX 40E0
PNR Register Dead Man Timer	XXXX 40E4
Control Memory Dead Man Timer	XXXX 40E8
Packet Memory Dead Man Timer	XXXX 40EC
DCR Primitive Access Dead Man Timer Value	XXXX 40F0

Power On Reset Value x‘0000 FFFF’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Transaction Dead Man Timer	Timer that loads with the corresponding Dead Man Timer Value Register when the respective transaction type is initiated. If the transaction does not complete before the timer reaches 0, a status bit is set in the *PCORE Status Register*.

3.18.16 PCORE PNR Shadow Status Register

This register is used to shadow the INTST Interrupt Source. The purpose of this register is to allow polling for PNR interrupts without using the PCI bus. See *INTST Interrupt Source Register* on page 89 for detailed bit descriptions.

Length	32 bits
Type	Read Only
DCR Address	x‘208’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.17 PCORE PNR Packet Last Write with Error Address

This register holds the address that has been sent from the Data Cache to Pcore when a virtual memory error in Charm has occured as a result of this address being used to access Packet Memory. Note that this address and the one sent to Packet memory may be different due to the address translation offset facilities.

Length	32 bits
Type	Read Only
DCR Address	x‘260’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.18 PCORE PNR RXQUE Status Register

This register is used to shadow the RXQUE Status Register. The purpose of this register is to allow fast access to RXQUE’s Status Register without having to use the regular register interface. See *RXQUE Status Register* on page 381 for detailed bit descriptions.

Length	32 bits
Type	Read Only
DCR Address	x‘20F’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.19 PCORE PNR RXQUE Enabled Status Register 1

This register is used to shadow the RXQUE Enabled Status Register 1. The purpose of this register is to allow fast read access of the RXQUE Enabled Status Register 1 without having to use the normal PNR register interface. See *RXQUE Enabled Status Registers 1 and 2* on page 382 for detailed bit descriptions.

Length 32 bits

Type Read Only

DCR Address x‘250’

Power On Reset Value x‘0000 0000’

Restrictions None

3.18.20 PCORE PNR RXQUE Enabled Status Register 2

This register is used to shadow the RXQUE Enabled Status Register 1. The purpose of this register is to allow fast read access of the RXQUE Enabled Status Register 2 without having to use the normal PNR register interface. See *RXQUE Enabled Status Registers 1 and 2* on page 382 for detailed bit descriptions.

Length 32 bits

Type Read Only

DCR Address x‘251’

Power On Reset Value x‘0000 0000’

Restrictions None

3.18.21 PCORE PNR RXQUE Upper Queues Status Register

This register is used to shadow the RXQUE Upper Queues Status Register. The purpose of this register is to allow fast read access of the RXQUE Upper Queues Status Register without having to use the normal PNR register interface. See *RXQUE Queues Status Register* on page 379 for detailed bit descriptions.

Length 32 bits

Type Read Only

DCR Address x‘252’

Power On Reset Value x‘0000 0000’

Restrictions None

3.18.22 PCORE PNR RXQUE Lower Queues Status Register

This register is used to shadow the RXQUE Lower Queues Status Register. The purpose of this register is to allow fast read access of the RXQUE Lower Queues Status Register without having to use the normal PNR register interface. See *RXQUE Queues Status Register* on page 379 for detailed bit descriptions.

Length	32 bits
Type	Read Only
DCR Address	x‘253’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.23 PCORE DMAQS Status Register

This register is used to shadow the DMAQS Status Register. The purpose of this register is to allow fast read access of the DMAQS Status Register without having to use the normal PNR register interface. See *DMAQS Status Register* on page 123 for detailed bit descriptions.

Length	32 bits
Type	Read Only
DCR Address	x‘257’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.24 PCORE DMAQS Interrupt Enable Register

This register is used to shadow the DMAQS Interrupt Enable Register. The purpose of this register is to allow fast read access of the DMAQS Interrupt Enable Register without having to use the normal PNR register interface. See *DMAQS Interrupt Enable Register* on page 125 for detailed bit descriptions.

Length	32 bits
Type	Read Only
DCR Address	x‘25B’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.25 PCORE DMAQS Head and Tail Pointer Shadow Registers

This register is used to shadow the DMAQS Head and Tail Pointer Registers. It allows fast read access of the DMAQS Head and Tail Pointer Registers without having to use the normal PNR register interface. See *DMAQS Head Pointer Registers* on page 121 and *DMAQS Tail Pointer Registers* on page 121 for detailed bit descriptions.

Length	32 Bits	
Type	Read Only	
DCR Address	Head 0	x‘268’
	Head 1	x‘269’
	Head 2	x‘26A’
	Tail 0	x‘26B’
	Tail 1	x‘26C’
	Tail 2	x‘26D’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.26 PCORE POOLS Get Pointer Primitive

This register is used to issue POOLS Get Primitive requests. It allows fast pools get primitives without having to use the normal PNR register interface. The lower 4 bits of the address are used to determine the pool that the transaction will be charged against.

Length	32 Bits	
Type	Read Only	
DCR Address	Pool 0	x‘270’
	Pool 1	x‘271’
	Pool 2	x‘272’
	Pool 3	x‘273’
	Pool 4	x‘274’
	Pool 5	x‘275’
	Pool 6	x‘276’
	Pool 7	x‘277’
	Pool 8	x‘278’
	Pool 9	x‘279’
	Pool 10	x‘27A’
	Pool 11	x‘27B’
	Pool 12	x‘27C’
	Pool 13	x‘27D’
	Pool 14	x‘27E’
	Pool 15	x‘27F’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.27 PCORE POOLS Free Pointer Primitive

This register is used to issue POOLS Free Primitive Requests to POOLS. It allows fast pools free primitives without having to use the normal PNR register interface.

Length	32 Bits
Type	Write Only
DCR Address	x‘26E’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.28 PCORE POOLS Pointer Primitive Offset Register

When enabled, this register’s contents are added to any returned get pointer primitive and subtracted from any free pointer primitive.

Length	32 Bits
Type	Read/Write
DCR Address	x‘26F’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.29 PCORE RXQUE Queue Length Registers

The PCORE RXQUE Queue Length Registers provide event queue lengths to the COBRA Core. Reads from this address will return event queue lengths from RXQUE.

Length	32 bits	
Type	Read/Write	
DCR Address	Queue 0	x‘220’
	Queue 1	x‘221’
	Queue 2	x‘222’
	Queue 3	x‘223’
	Queue 4	x‘224’
	Queue 5	x‘225’
	Queue 6	x‘226’
	Queue7	x‘227’
	Queue 8	x‘228’
	Queue 9	x‘229’
	Queue 10	x‘22A’
	Queue 11	z‘22B’
	Queue 12	x‘22C’
	Queue 13	x‘22D’
	Queue 14	x‘22E’
	Queue 15	x‘22F’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.30 PCORE DMAQS Queue Length Registers

The PCORE DMAQS Queue Length Registers provide DMAQS queue lengths to the COBRA Core. Reads from this address will return descriptor queue lengths from DMAQS.

Length	32 bits	
Type	Read/Write	
DCR Address	Queue 0	x ‘254’
	Queue 1	x ‘255’
	Queue 2	x ‘256’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.31 PCORE Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *PCORE Status Register*. When both a bit in this register and the corresponding bit(s) in the PCORE Status Register are set, the PCORE interrupt to INTST will be enabled. See *3.18.4 PCORE Status Register* on page 429 for the bit descriptions.

Length	32 bits
Type	Clear/Set
Address	XXXX 4010 and 4014
Power On Reset Value	x‘0000 8000’
Restrictions	None

3.18.32 PCORE User Interrupt Enable

This register is used to enable an interrupt based on bits from the corresponding PCORE User Status Register and potentially generate interrupts to the control processor. When both a bit in this register and the corresponding bit in the PCORE User Status register are set, an interrupt is generated to the INTST entity. See *3.18.5 PCORE User Status Register* on page 430 for the bit descriptions.

Length	32 bits
Type	Clear/Set
DCR Address	x‘204’ and x‘205’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.33 PCORE COBRA Core Interrupt Enable Register

This register is used to enable bits from the PCORE COBRA Core External Status Register and generate interrupts to the COBRA Core processor. When both a bit in this register and the corresponding bit(s) in the PCORE COBRA Core External Status Register are set, the COBRA Core interrupt to the COBRA Core will be enabled. See *3.18.4 PCORE Status Register* on page 429 for the bit descriptions.

Length	32 bits
Type	Clear/Set
DCR Address	x‘206’ and x‘207’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.34 PCORE COBRA Core External Machine Check Enable Register

This register is used to enable bits from the PCORE COBRA Core External Machine Check Status Register and generate machine checks to the COBRA Core processor. When both a bit in this register and the corresponding bit(s) in the PCORE COBRA Core External Machine Check Status Register are set, the requisite COBRA Core Machine Check to the COBRA Core will be enabled. See *3.18.4 PCORE Status Register* on page 429 for the bit descriptions.

Length	32 bits
Type	Clear/Set
DCR Address	x‘25E’ and x‘25F’
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.35 PCORE Error Lock Enable Register

The PCORE Error Lock Enable Register provides the ability to halt PCORE when the corresponding status bit in the status register is set and locking is enabled. When a bit in this register corresponds to a bit set in the status register, the state machines in PCORE will be held in idle state until the lock is disabled.

Length	32 bits
Type	Clear/Set
Address	XXXX 4030 and 4034
DCR Address	x‘266’ and x‘267’
Power On Reset Value	x‘0000 FE9F’
Restrictions	None

3.18.36 PCORE User Error Lock Enable Register

The PCORE User Error Lock Enable Register provides the ability to halt PCORE when the corresponding status bit in the User Status Register is set and locking is enabled. When a bit in this register corresponds to a bit set in the Status Register, the state machines in PCORE will be held in idle state until the lock is disabled.

Length	32 bits
Type	Clear/Set
Address	XXXX 4038 and 403C
Power On Reset Value	x‘FFFF FFFF’
Restrictions	None

3.18.37 PCORE RXQUE Event Interface Enqueue Register

The PCORE RXQUE Event Interface Enqueue Register provides an event enqueue interface for the COBRA Core. Writes to this address will enqueue an event to an RXQUE queue.

Length	32 bits	
Type	Read/Write	
DCR Address	Queue 0	x‘230’
	Queue 1	x‘231’
	Queue 2	x‘232’
	Queue 3	x‘233’
	Queue 4	x‘234’
	Queue 5	x‘235’
	Queue 6	x‘236’
	Queue 7	x‘237’
	Queue 8	x‘238’
	Queue 9	x‘239’
	Queue 10	x‘23A’
	Queue 11	x‘23B’
	Queue 12	x‘23C’
	Queue 13	x‘23D’
	Queue 14	x‘23E’
	Queue 15	x‘23F’
Power On Reset Value		x’0000 0000’
Restrictions	None	

3.18.38 PCORE DMAQS DMA Enqueue Register

The PCORE DMAQS DMA Enqueue Register provides a DMAQS interface for the COBRA Core. Writes to this address will enqueue a descriptor to a DMAQS queue.

Length	32 bits	
Type	Read/Write	
DCR Address	Queue 0	x‘258’
	Queue 1	x‘259’
	Queue 2	x‘25A’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.39 PCORE RXQUE Event Interface Deque Register

The PCORE RXQUE Event Interface Dequeue Register provides an event deque interface for the COBRA Core. Reads from this address return an event.

Length	32 bits	
Type	Read Only	
DCR Address	Queue 0	x‘240’
	Queue 1	x‘241’
	Queue 2	x‘242’
	Queue 3	x‘243’
	Queue 4	x‘244’
	Queue 5	x‘245’
	Queue 6	x‘246’
	Queue 7	x‘247’
	Queue 8	x‘248’
	Queue 9	x‘249’
	Queue 10	x‘24A’
	Queue 11	x‘24B’
	Queue 12	x‘24C’
	Queue 13	x‘24D’
	Queue 14	x‘24E’
	Queue 15	x‘24F’
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.40 PCORE COBRA SPR Access Address Register

The PCORE SPR Access Address Register is used in combination with the next two registers to access the internal facilities in COBRA. This includes SPRs, DCRs, and Debug facilities. The address and type of the internal COBRA facility are written to this register. The contents of the facility can then be read or written through the *PCORE COBRA SPR Read Data Access Register* or *PCORE COBRA SPR Write Data Access Register*, respectively. The address represents a 4-byte access. This facility should not be used while COBRA is running, if the Exception Vector Override facilities are active.

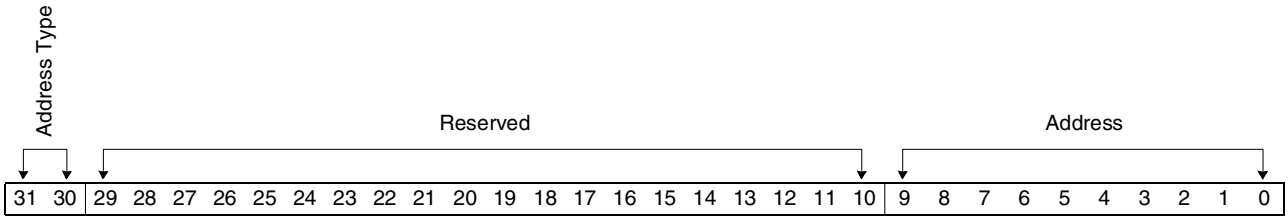
Length 32 bits

Type Read/Write

Address XXXX 4044

Power On Reset Value x‘8000 0000’

Restrictions None



Bit(s)	Name	Description
31-30	Address Type	These bits describe the address type. 00 Reserved 01 SPR Access 10 DCR Access 11 Register/Debug Access
29-10	Reserved	Reserved.
9-0	Address	Address of Target Register.

3.18.41 PCORE COBRA SPR Read Data Access Register

The PCORE COBRA SPR Read Data Access Register causes a read of the COBRA facility specified by the *PCORE COBRA SPR Access Address Register*, and returns the data to the requester. This can be used for initializing the COBRA processor and its facilities, or as a message passing facility used for inter-device communication.

These facilities, with their control register bits, allow for either interrupt or polling-based message passing from the COBRA Core to a PCI bus device.This facility should not be used while COBRA is running if the Exception Vector Override facilities are active.

Length	32 bits
Type	Read Only
Address	XXXX 4040
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.42 PCORE COBRA SPR Write Data Access Register

The PCORE COBRA SPR Write Data Access Register causes a write of the COBRA facility specified by the *PCORE COBRA SPR Access Address Register*, storing the given data. This can be used for initializing the COBRA processor and its facilities, or as a message passing facility used for inter-device communication.

These facilities, with their control register bits, allow for either interrupt or polling-based message passing from the COBRA Core to a PCI bus device.This facility should not be used while COBRA is running if the Exception Vector Override facilities are active.

Length	32 bits
Type	Write Only
Address	XXXX 40F4
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.43 PCORE Address Translation Offset Address Facilities

The PCORE Address Translation Offset Address Facilities provides the offset that is added to the COBRA Real Address to create the target subsystem address.

When an address is issued from the COBRA Core, it is accompanied by four target translation bits. The translation bits indicate which translation facility is to be used to translate the processor “real” physical address into a target system actual address. This grouping provides for the offset addresses for each target memory system. The offset is added to the COBRA Real Address to create the target system address. Table 20: *PCORE Address Translation Target Bit Encoding* on page 458 is a list of targets, each with its own translation facilities.

Length	32 bits	
Type	Read/Write	
Address	Packet Memory Offset View 0	XXXX 4048
	Packet Memory Offset View 1	XXXX 404C
	Packet Memory Offset View 2	XXXX 4050
	PNR Registers Offset View 0	XXXX 4054
	Control Memory Offset View 0	XXXX 4058
	Control Memory Offset View 1	XXXX 405C
	Control Memory Offset View 2	XXXX 4060
	PCI Master Offset View 0	XXXX 4064
	PCI Master Offset View 1	XXXX 4068
	PCI Master Offset View 2	XXXX 406C
	PCI Master Offset View 3	XXXX 4070
	Control/Packet Memory Offset View 0	XXXX 4074
	Control/Packet Memory Offset View 1	XXXX 4078
	Control/Packet Memory Offset View 2	XXXX 407C
	Control/Packet Memory Offset View 3	XXXX 4080
Power On Reset Value		x‘0000 0000’
Restrictions	None	

Table 20: PCORE Address Translation Target Bit Encoding

Target Bit Encoding	Translation Facility
0000	OCM (Translation provided for in the MMUs)
0001	Packet Memory View 0
0010	Packet Memory View 1
0011	Packet Memory View 2
0100	PNR Registers
0101	Control Memory View 0
0110	Control Memory View 1
0111	Control Memory View 2
1000	PCI Master Access (Non PNR) View 0
1001	PCI Master Access (Non PNR) View 1
1010	PCI Master Access (Non PNR) View 2
1011	PCI Master Access (Non PNR) View 3
1100	Control/Packet View 0
1101	Control/Packet View 1
1110	Control/Packet View 2
1111	Control/Packet View 3

3.18.44 PCORE PCI 64 Bit Address Translation Facilities

The PCORE PCI 64 Bit Address Translation Facilities provide the upper 32 bits of address in 64-bit addressing mode. When an access is issued to the PCI Master Interface in 64-bit addressing mode, these registers are used to create the upper 32 bits of the 64-bit address.

Length	32 bits	
Type	Read/Write	
Address	Upper 32 Address Bits PCI Master View 0	XXXX 4084
	Upper 32 Address Bits PCI Master View 1	XXXX 4088
	Upper 32 Address Bits PCI Master View 2	XXXX 408C
	Upper 32 Address Bits PCI Master View 3	XXXX 4090
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.45 PCORE PCI Master Target Tag Controls

The PCORE PCI Master Target Tag Controls contains the control for each PCI Tag/View. This register contains bits for each of the four PCI Master Views.

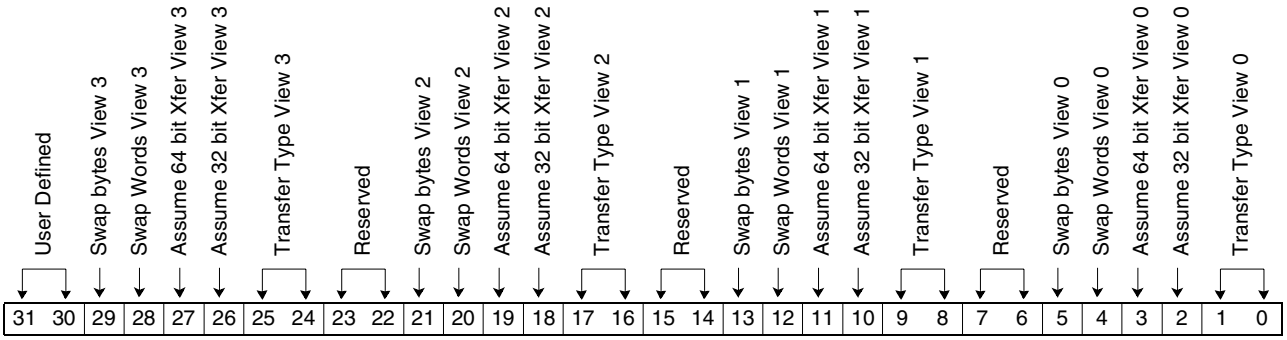
Length 32 bits

Type Read/Write

Address XXXX 40FC

Power On Reset Value x‘0606 0606’

Restrictions None



Bit(s)	Name	Description
31-30	Reserved	Reserved.
29	Swap bytes View 3	When set, this bit tells the PCI Master Logic to do byte swapping.
28	Swap Words View 3	When set, this bit tells the PCI Master to do word swapping.
27	Assume 64 bit Xfer View 3	When set, this bit tells the PCI Master Logic to assume a 64-bit data access.
26	Assume 32 bit Xfer View 3	When set, this bit tells the PCI Master Logic to assume a 32-bit data access.
25-24	Transfer Type View 3	These bits indicate the transaction type. 00 Config Cycle 01 I/O Cycle 1- Memory Cycle
23-22	Reserved	Reserved.
21	Swap bytes View 2	When set, this bit tells the PCI Master Logic to do byte swapping.
20	Swap Words View 2	When set, this bit tells the PCI Master to do word swapping.
19	Assume 64 bit Xfer View 2	When set, this bit tells the PCI Master Logic to assume a 64-bit data access.
18	Assume 32 bit Xfer View 2	When set, this bit tells the PCI Master Logic to assume a 32-bit data access.
17-16	Transfer Type View 2	These bits indicate the transaction type. 00 Config Cycle 01 I/O Cycle 1- Memory Cycle
15-14	Reserved	Reserved.
13	Swap bytes View 1	When set, this bit tells the PCI Master Logic to do byte swapping.

Bit(s)	Name	Description
12	Swap Words View 1	When set, this bit tells the PCI Master to do word swapping.
11	Assume 64 bit Xfer View 1	When set, this bit tells the PCI Master Logic to assume a 64 bit data access.
10	Assume 32 bit Xfer View 1	When set, this bit tells the PCI Master Logic to assume a 32 bit data access
9-8	Transfer Type View 1	These bits indicate the transaction type. 00 Config Cycle 01 I/O Cycle 1- Memory Cycle
7-6	Reserved	Reserved.
5	Swap bytes View 0	When set, this bit tells the PCI Master Logic to do byte swapping.
4	Swap Words View 0	When set, this bit tells the PCI Master to do word swapping.
3	Assume 64 bit Xfer View 0	When set, this bit tells the PCI Master Logic to assume a 64 bit data access.
2	Assume 32 bit Xfer View 0	When set, this bit tells the PCI Master Logic to assume a 32 bit data access.
1-0	Transfer Type View 0	These bits indicate the transaction type 00 Config Cycle 01 I/O Cycle 1- Memory Cycle

3.18.46 PCORE Last Packet Address Register

The PCORE Last Packet Address Register is the last address to the Packet Memory bus at the time of the hang condition. When the system locks up, this register holds the last Packet Memory address that was or is currently being presented to the Packet Memory subsystem.

Length	32 bits
Type	Read Only
Address	XXXX 4094
Power On Reset Value	x‘FFFF FFFC’
Restrictions	None

3.18.47 PCORE Last Control Address Register

The PCORE Last Control Address Register is the last address to the Control Memory bus at the time of the hang condition. When the system locks up, this register holds the last Control Memory address that was or is currently being presented to the Control Memory subsystem.

Length	32 bits
Type	Read Only
Address	XXXX 4098
Power On Reset Value	x‘FFFF FFFC’
Restrictions	None

3.18.48 PCORE Last PCI Lower Address Register

The PCORE Last PCI Lower Address Register is the last address to the PCI bus at the time of the hang condition. When the system locks up, this register holds the last PCI bus address that was or is currently being presented to the Control Memory subsystem.

Length	32 bits
Type	Read Only
Address	XXXX 409C
Power On Reset Value	x‘FFFF FFFC’
Restrictions	None

3.18.49 PCORE Last Register Address Register

The PCORE Last Register Address Register is the last address to the PCI bus at the time of the Hang Condition. When the system locks up, this register holds the last PCI bus address that was or is currently being presented to the Control Memory subsystem.

Length	32 bits
Type	Read Only
Address	XXXX 40A0
Power On Reset Value	x‘FFFF FFFC’
Restrictions	None

3.18.50 PCORE OCM Window Address Register

The OCM Window Address register is used to select which 4-KB portion of OCM is accessible through PNR address range x‘5000 - 5FFF’.

Length	32 bits (17:12) Active
Type	Read/Write
Address	XXXX 40A4
Power On Reset Value	x‘0000 0000’
Restrictions	None

3.18.51 PCORE Read Data Transfer Buffers

The PCORE Read Data Transfer Buffers hold the read data that is being transferred from one of the target subsystems and the COBRA Core. Eight bytes are buffered on the interfaces except for the PNR register interface which buffers four bytes.

Length	32 bits	
Type	Read Only	
Address	PCI Upper Read Data Transfer Buffer	XXXX 40A8
	PCI Lower Read Data Transfer Buffer	XXXX 40AC
	Packet Upper Read Data Transfer Buffer	XXXX 40B0
	Packet Lower Read Data Transfer Buffer	XXXX 40B4
	Control Upper Read Data Transfer Buffer	XXXX 40B8
	Control Lower Read Data Transfer Buffer	XXXX 40BC
	PNR Register Space Read Data Transfer Buffer	XXXX 40C0
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.52 PCORE Write Data Transfer Buffers

The PCORE Write Data Transfer Buffers hold the data that is being transferred between the COBRA Core and one of the target subsystems. Eight bytes can be stored for each target subsystem, with the exception of the PNR Register Target which holds just four bytes.

Length	32 bits	
Type	Read Only	
Address	PCI Upper Write Data Transfer Buffer	XXXX 40C4
	PCI Lower Write Data Transfer Buffer	XXXX 40C8
	Packet Upper Write Data Transfer Buffer	XXXX 40CC
	Packet Lower Write Data Transfer Buffer	XXXX 40D0
	Control Upper Write Data Transfer Buffer	XXXX 40D4
	Control Lower Write Data Transfer Buffer	XXXX 40D8
	PNR Register Space Write Data Transfer Buffer	XXXX 40DC
Power On Reset Value		x‘0000 0000’
Restrictions	None	

3.18.53 PCORE Polling Register

The PCORE Polling Register provides status information to PCORE about PNR operations. It allows PCORE to poll specific PNR status without using PCI bus bandwidth.

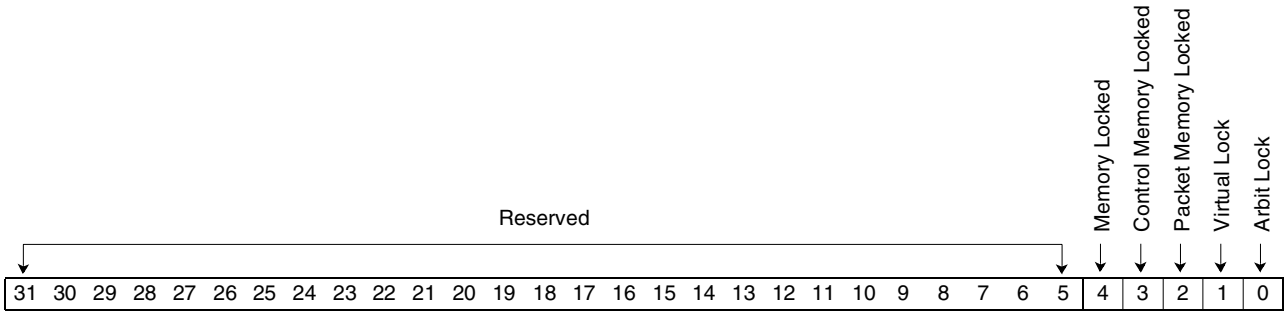
Length 32 bits

Type Read Only

DCR Address x‘20E’

Power On Reset Value x‘0000 0000’

Restrictions During normal operations, if a status bit is cleared, it will be reset if the condition that is causing it is still present.



Bit(s)	Name	Description
31-5	Reserved	Reserved.
4	Memory Locked	Memory is locked.
3	Control Memory Locked	Control Memory is locked.
2	Packet Memory Locked	Packet Memory is locked.
1	Virtual Lock	VIMEM is the locker of memory.
0	ARBIT Lock	ARBIT is the locker of memory.

3.18.54 PCORE Integer Input Rate Conversion Register

This register is the integer input port for the rate conversion logic. An integer rate is placed in this register. The on-board logic converts it to an ABR rate format.

Length 32 bits

Type Read/Write

DCR Address x‘20B’

Power On Reset Value x‘0000 0000’

Restrictions None

3.18.55 PCORE ABR Output Rate Register

This register is the output port of the rate conversion logic. An integer rate was placed in the *PCORE Integer Input Rate Conversion Register*. The logic converts it to an ABR rate and places the result in this register.

Length 32 bits

Type Read Only

DCR Address x‘20C’

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	ABR Rate	The value written into the *PCORE Integer Input Rate Conversion Register* converted to ABR format.

3.18.56 PCORE Debug States Control

This register serves as the PCORE control for external debug states. The INTST Debug states control for the address range desired must be set to select these PCORE state bits. If that is done, this register acts to select the four ranges. See bit descriptions below.

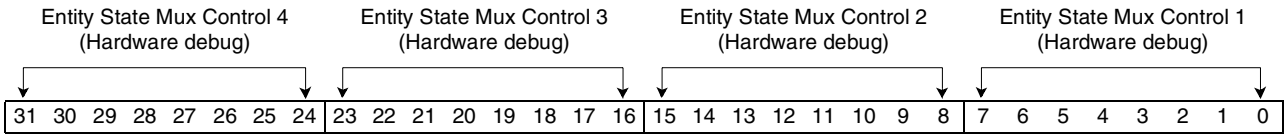
Length 32 bits

Type Read/Write

Address XXXX 431C

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-24	Entity State Mux Control 4 (Hardware debug)	Select of these bits allows internal state machines, counters, etc., to show up on chip outputs ENSTATE(63:48). Selection encoding is the same as mux 1 control.
23-16	Entity State Mux Control 3 (Hardware debug)	Select of these bits allow internal state machines, counters, etc., to show up on chip outputs ENSTATE(47:32). Selection encoding is the same as mux 1 control.
15-8	Entity State Mux Control 2 (Hardware debug)	Select of these bits allow internal state machines, counters, etc., to show up on chip outputs ENSTATE(31:16). Selection encoding is the same as mux 1 control.
7-0	Entity State Mux Control 1 (Hardware debug)	Select of these bits allow internal state machines, counters, etc., to show up on chip outputs ENSTATE(15:0). x‘00’ Disabled (no transition on outputs) x‘01’ Select 15-0 states x‘40’-x‘FF’ Reserved

3.18.57 PCORE Debug States Config

This register selects the sources of debug information from PCORE. The INTST debug states control register needs to select PCORE as a source of debug state information in order for this information to be visible external to the PNR.

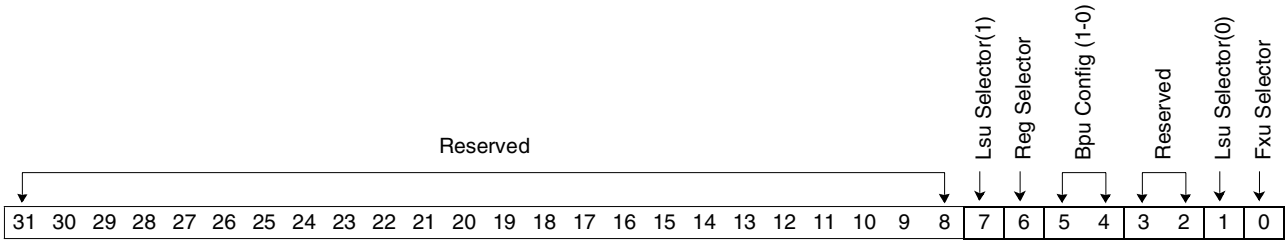
Length 32 bits

Type Read/Write

Address XXXX 4320

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-8	Reserved	Reserved.
7	LSU selector(1)	Used to configure debug information from source 1 in the load store unit.
6	Reg selector	Used to configure debug information from the register unit.
5-4	Bpu Config (1-0)	Used to configure debug information from the branch processing unit.
3-2	Reserved	Reserved
1	LSU selector(0)	Used to configure debug information from source 0 in the load/store unit.
0	FXU selector	Used to configure debug information from the fixed point unit.

3.19 Embedded PowerPC Processor (COBRA)

The COBRA Core is a 32-bit PowerPC RISC embedded controller. It is fully compatible with the PowerPC User Instruction Set Architecture. Details about the exact instruction set are given below. The COBRA Core has a PowerPC instruction execution complex, separate 32-KB instruction and data caches, and 401-style interrupts, timers and debug facilities. The COBRA Core has a direct connection to 96 KB of on-chip memory (OCM), as well as interfaces to the PNR's PCI and register buses and both of the PNR's memory controllers. The COBRA Core can execute instructions stored in OCM, remote PCI devices, or in either of the PNR's memory controllers. The DCR bus provides fast and private access to specific PNR performance-sensitive registers.

3.19.1 Features

Instruction Execution

- Compatible with PowerPC User Instruction Set Architecture (UISA).
- Separate Branch, Condition Register, Integer, and Load/Store units for super-scalar execution.
- Supports limited out-of-order execution.
- Dispatches up to two and executes up to four instructions per clock cycle.
- Four-stage pipeline allows single cycle execution for most instructions.
- 32 x 32-bit general purpose registers (GPRs).
- Two cycle loads and stores.
- Byte, halfword, word, and string accesses to any byte alignment supported in hardware.
- Hardware multiply up to ten cycles.
- Hardware divide up to 32 cycles.
- No FPU hardware. FPU instructions result in interrupts.

Timers

- 32-bit decrementer
- 64-bit time base
- Programmable and fixed interval timers
- Watchdog timer

COBRA Core Exceptions

- Two priority levels
  - Normal - uses SRR0/1 (603)
  - Critical - uses SRR2/3 (401 extension)
- Exception Types
  - System Reset (boot vector)
  - Machine Check
  - Data Storage Interrupt
  - Instruction Storage Interrupt
  - External
  - Alignment
  - Trap
  - Invalid Opcode
  - Privilege Violation
  - Floating Point Unavailable
  - Decrementer
  - System Call
  - Trace
  - System Management (603)
  - Programmable Interval Timer (401)
  - Fixed Interval Timer (401)
  - Watch Dog Timer (401)
  - Critical Interrupt (401)
  - Debug Interrupt (401)

Optional Architecture Extensions

- Programmable boot address (system interrupt vector)
- Interrupt enhancements
  - Individually re-locatable interrupts
  - Individually programmable interrupt level - normal and critical

Caches

- 32-byte cache lines (eight words per line)
- Four-way set associative write back 32-KB instruction and data caches

Memory Management

- Real Flat Address Mode supported

Interrupt Controller

- Two interrupt levels external to COBRA - normal and critical
- Three-way interrupts
  - From PNR to COBRA
  - From COBRA to PCI
  - From PCI to COBRA

Debug Support

- PowerPC JTAG debugger support (401 RISCWatch)
- 401 debug facilities
- Serial Port Debugger support
- PCI Debug access to JTAG debug facilities

3.19.2 Interfaces

On-Chip Memory

- 96 KB of on-chip memory
- Can be used simultaneously by instruction and data accesses

PNR Registers

- Read/Write access to the PNR register bus
- Some PNR registers are also mapped to COBRA Core DCR register space for faster access

PCI Bus

- Read/Write master access to PCI Bus
- Currently no actual streaming/bursting supported
- Pseudo bursting supported (multiple back to back single transfers)
- Interrupt sink
- No arbitration supported (not a complete bridge)

Comet/Pakit Memory

- Able to use both memory controllers for both instruction and data accesses

3.19.3 Performance

- 133 MHz operating frequency
- Performance estimates unavailable

3.19.4 Instruction Set

Instruction Set with 401 as a Base

Supports all 401 instructions with the following exceptions:

- Added from 603
  - mfsr, mfsrin, mtsr, mtsrin, tlbie, tlbld, tlbli, tlbsync
    Note: virtual memory not supported
  - mftb (for 603 style time base support)
- Removed from 401
  - dcread, icread (replaced with SPR access to the caches)
- Changed mfspr and mtspr to accommodate new SPRs

Instruction Set with 603 as a Base

Supports all 603 instructions with the following exceptions:

- Added from 401
  - dccci, icbt, iccci, mfdcr, mtdcr, rfci, wrtee, wrteei
- Removed from 603
  - fXXXXX, lfXXX, stfXXX, mffXXX (floating point instructions)
  - eciwx, ecowx (PowerPC I/O addressing not supported - only memory space addressing)
- Changed mfspr and mtspr to accommodate new SPRs

3.19.5 COBRA Instruction Overview

The PNR COBRA Core supports all of the instructions in either the PowerPC 603 User's Manual (MPR603UMU-01, MPC603UM/AD) or the Power PC 401 Core User's Manual (v0.07 1/28/98) with the following changes. If an instruction does not exist in both user's manuals, it is described below.

Instruction(s)	Source	Description
dccci, icbt, iccci	401	Added for cache management.
mfdcr, mtdcr	401	Added for DCR bus support.
rfci, wrtee, wrteei	401	Added for 40x interrupt support.
mfsr, mfsrin, mtsr, mtsrin	603	Added for 60x MMU support. Not supported.
mftb	603	Added for 60x style time base support.
tlbie	603	Added for 60x MMU support. Not supported.
tlbsync	603	Added for 60x compatibility. Acts as a no-op.
mfbus, mtbus	COBRA Core	Added. See *3.19.6 COBRA Unique Instructions* on page 473.
dcread, icread	401	Removed. Cache layout is different.
dcba	405	405 only instruction. Not supported.
tlbre, tlbsx(.), tlbwe	405	Removed. 40x style MMU not supported.
eciwx, ecowx	603	Removed. Only memory space addressing supported.
fxxxxx	603	Removed floating point support.
lfd, lfdu, lfdux, lfdx, lfs, lfsu, lfsux, lfsx	603	Removed floating point support.
mffs, mffsb0, mffsb1, mffsf, mffsfi	603	Removed floating point support.
stfd, stfdu, stfdux, stfdx, stfiwx, stfs, stfsu, stfsux, stfsx	603	Removed floating point support.
tlbld, tlbli	603	Removed - 603 style MMU support.

3.19.6 COBRA Unique Instructions

COBRA adds two instructions not found in the standard PowerPC instruction set: Move from Internal Bus (mfbus) and Move to Internal Bus (mtbus). These instructions are useful for indirect addressing access to SPRs/DCRs. These instructions replace the use of branch table based SPR/DCR lookups.

3.19.6.1 Move from Internal Bus (mfbus)

The mfbus instruction is a supervisor-level instruction that loads data from an SPR, DCR, or DEBUG register into a selected processor general purpose register. The opcode for the instruction is as follows:

Bit(s)	Description
0-5	Major Opcode = '01 1111'.
6-10	Destination general purpose register. This is the only register affected by this instruction.
11-15	If bits 11-15 are '00000', bits 0-7 of the general purpose register selected by bits 16-20 of this instruction select the target bus from which to read. If bits 11-15 are non-zero, bits 11-15 are prepended with zero and are then used to select the target bus from which to read. The bits used to select the target bus are decoded as follows x'01' SPR bus x'02' DCR bus x'03' DEBUG bus All other values are undefined, and will result in the destination register being loaded with an undefined value.
16-20	Specifies a general purpose register that provides the address of the source register on the target bus, and, depending of the value of bits 11-15 of this instruction, may also select the target bus. Bits 22-31 of the register are used as the address of the source register. If bits 11-15 of this instruction are zero, bits 0-7 of the register will also indicate the target bus.
21-30	Minor Opcode = '01 0110 0011'.
31	Reserved.

3.19.6.2 Move to Internal Bus (mtbus)

The mtbus instruction is a supervisor-level instruction that stores data to an SPR, DCR, or DEBUG register from a selected processor general purpose register. The op code for the instruction is as follows:

Bit(s)	Description
0-5	Major Opcode = ‘01 1111’.
6-10	Source general purpose register.
11-15	If bits 11-15 are ‘00000’, bits 0-7 of the general purpose register selected by bits 16-20 of this instruction select the bus to which to target the write. If bits 11-15 are non-zero, bits 11-15 are prepended with zero and used to select the target bus to which to write. The bits used to select the target bus are decoded as follows: x‘01’ SPR bus x‘02’ DCR bus x‘03’ DEBUG bus All other values are undefined, and no write will occur.
16-20	Specifies a general purpose register that provides the address of the destination register on the target bus, and, depending of the value of bits 11-15 of this instruction, may also select the target bus. Bits 22-31 of the register are used as the address of the destination register. If bits 11-15 of this instruction are zero, bits 0-7 of the register will also indicate the target bus.
21-30	Minor Opcode = ‘01 1110 0011’.
31	Reserved.

3.19.7 COBRA Facilities Overview

The following registers are patterned after the registers in either the PowerPC 603 User's Manual (MPR603UMU-01,MPC603UM/AD) or the Power PC 401 Core User's Manual (v0.07 1/28/98). Every register in a 603 or 401 is included below. Differences between the two implementations and the COBRA Core implementation are explained.

The registers are split into eight functional groupings: Machine Control/Status Registers, Branch Control Registers, Debug Control Registers, Special Purpose Facilities, Interrupt and Exception Registers, Timer Registers, Cache Control Registers, Translation Control Registers. The register groups are summarized in Tables 21 through 28.

Source Key

BOTH	same bit definitions as 603 and 401
401	same bit definitions as 401
603	same bit definitions as 603
PPC	same bit definitions as general Power PC architecture
COBRA	COBRA Configuration. See *3.19.8 COBRA Specific Register Definitions* on page 482 for bit descriptions

Table 21: Machine Control/Status Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
cr	NA	NA	BOTH	x'0000 0000'	
hid0	1023	x'3FF'	COBRA	x'0000 00FC'	This has a different SPR Number than the 603 and 401.
ear	282	x'11A'	603		Not supported. Writes ignored. Reads as zeros (603 I/O addressing support).
msr	NA	NA	COBRA	x'0000 0040'	Contains a combination of bits from 401 and 603.
xer	1	x'1'	BOTH	x'0000 0000'	
mchk	688/689	x'2B0'/ x'2B1'	COBRA	x'0000 0000'	Machine Check Enable - set bits off/ set bits on.
pvr	287	x'11F'	COBRA	x'1010 0000'	COBRA specific PVR.

Table 22: Branch Control Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
ctr	9	x'9'	BOTH	x'0000 0000'	
lr	8	x'8'	BOTH	x'0000 0000'	

Table 23: Debug Control Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
dabr	1013	x‘3F5’	PPC		Not implemented. Use DAC1.
dac1	1014	x‘3F6’	401	x‘0000 0000’	Data Address Compare.
dbcr	1010	x‘3F2’	401	x‘0000 0000’	Debug Control register.
dbdr	1011	x‘3F3’	401	x‘0000 0000’	Debug Data register.
dbsr	1008	x‘3F0’	401	x‘0000 0000’	Debug Status register.
iabr	1010	x‘3F2’	603		Not implemented. Use IAC1.
iac1	1012	x‘3F4’	401	x‘0000 0000’	Instruction Address Compare 1 register.
iac2	1013	x‘3F5’	401	x‘0000 0000’	Instruction Address Compare 2 register.

Table 24: Special Purpose Facilities

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
sprg0	272	x‘110’	BOTH	x‘0000 0000’	
sprg1	273	x‘111’	BOTH	x‘0000 0000’	
sprg2	274	x‘112’	BOTH	x‘0000 0000’	
sprg3	275	x‘113’	BOTH	x‘0000 0000’	
sprg4-7	276-279	x‘114’ - x‘117’	COBRA	x‘0000 0000’	Read/Write addresses (privileged SPRs).
sprg4-7	68-71	x‘44’ - x‘47’	COBRA	x‘0000 0000’	Read Only addresses (non-privileged SPRs).

Table 25: Interrupt and Exception Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
dar	19	x‘13’	603		Same facility as dear with different address.
dear	981	x‘3D5’	401	x‘0000 0000’	Data Error Address register.
dsisr	18	x‘12’	603	x‘0000 0000’	Status on Data exceptions.
esr	980	x‘3D4’	401	x‘0000 0000’	Only MCI, PIL, PPR, PTR, DST, and PFEU bits implemented.
evpr	982	x‘3D6’	401	x‘0000 0000’	Exception Vector Prefix register.
srr0	26	x‘1A’	BOTH	x‘0000 0000’	Address of exception for normal interrupts.

Table 25: Interrupt and Exception Registers (Continued)

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
srr1	27	x‘1B’	BOTH	x‘0000 0000’	Status of exception / previous MSR contents for normal interrupts. HID0(27) = 0 (603 mode) the upper 16 bits act as status; the lower 16 bits are set from the MSR. HID0(27) = 1 (401 mode) - all bits are set from the MSR (the ESR is used for status).
srr2	990	x‘3DE’	401	x‘0000 0000’	Behaves like srr0. Used for critical level interrupts.
srr3	991	x‘3DF’	401	x‘0000 0000’	Behaves like srr1. Used for critical level interrupts.

Table 26: Timer Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
dec	22	x‘16’	603	x‘FFFF FFFF’	Decrementer.
pit	987	x‘3DB’	401	x‘0000 0000’	Programmable Interval Timer.
tbhi	988	x‘3DC’	401	x‘0000 0000’	Upper half of 64-bit time base register. Read/Write. Privileged spr.
tblo	989	x‘3DD’	401	x‘0000 0000’	Lower half of 64-bit time base register. Read/Write. Privileged spr.
tbhu	972	x‘3CC’	401	x‘0000 0000’	Upper half of 64-bit time base register. Read Only. Non-privileged spr.
tblu	973	x‘3CD’	401	x‘0000 0000’	Lower half of 64-bit time base register. Read Only. Non-privileged spr.
tbl	284	x‘11C’	603	x‘0000 0000’	Same as tblo, but Write Only.
tbu	285	x‘11D’	603	x‘0000 0000’	Same as tbhi, but Write Only.
tbl	268	x‘10C’	603	x‘0000 0000’	tbr (not spr) same as tblu.
tbu	269	x‘10D’	603	x‘0000 0000’	tbr (not spr) same as tbhu.
tcr	986	x‘3DA’	401	x‘0000 0000’	Timer Control register.
tsr	984	x‘3D8’	401	x‘0000 0000’	Timer Status register.

Table 27: Cache Control Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
dccr	1018	x‘3FA’	401	x‘0000 0000’	Data Cacheability Control register.
dlcr	917	x‘395’	COBRA	x‘0000 0000’	Data Cache Locking Control register. Bits 0-15 correspond to target tags 0-15, enabling auto data cache line locking.
dtwf	919	x‘397’	COBRA	x‘0000 0000’	Data Cache Target Word First Fills Control register. Bits 0-15 correspond to target tags 0-15, enabling target word first data cache fills.
iccr	1019	x‘3FB’	401	x‘0000 0000’	Instruction Cacheability Control register.
ilcr	916	x‘394’	COBRA	x‘0000 0000’	Instruction Cache Locking Control register. Bits 0-15 correspond to target tags 0-15, enabling auto instruction cache line locking.
itwf	918	x‘396’	COBRA	x‘0000 0000’	Instruction Cache Target Word First Fills Control register. Bits 0-15 correspond to target tags 0-15, enabling target word first instruction cache fills.
cdcbr	983	x‘3D7’	401		Not implemented.
dcwr	954	x‘3BA’	401		Not implemented.
icdbdr	979	x‘3D3’	401		Not implemented.

Table 28: Translation Control Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
sdr1	25	x‘19’	603	x‘0000 0000’	Not supported. Translation not supported.
sgr	953	x‘3B9’	401	x‘0000 0000’	Has no affect. All storage is non-guarded.
sler	955	x‘3BB’	401		Not supported. Writes ignored, reads as ‘0’.
stt0	912	x‘390’	COBRA	x‘0000 0000’	These registers are used to assign target tags to instruction or data memory accesses. The mapping is stt0(0:3) = x‘0000 0000’:x‘07FF FFFF’ through stt3(28:31) = x‘F800 0000’ :x‘FFFF FFFF’.
stt1	913	x‘391’	COBRA	x‘0000 0000’	
stt2	914	x‘392’	COBRA	x‘0000 0000’	
stt3	915	x‘393’	COBRA	x‘0000 0000’	
sr0-15	NA	NA	603	x‘0000 0000’	Not supported. Translation not supported.
dbat0u	536	x‘218’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat0l	537	x‘219’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat1u	538	x‘21A’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat1l	539	x‘21B’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat2u	540	x‘21C’	603	x‘0000 0000’	Not supported. Translation not supported.

Table 28: Translation Control Registers (Continued)

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
dbat2l	541	x‘21D’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat3u	542	x‘21E’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat3l	543	x‘21F’	603	x‘0000 0000’	Not supported. Translation not supported.
dbat4u	568	x‘238’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat4l	569	x‘239’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat5u	570	x‘23A’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat5l	571	x‘23B’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat6u	572	x‘23C’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat6l	573	x‘23D’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat7u	574	x‘23E’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
dbat7l	575	x‘23F’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat0u	528	x‘210’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat0l	529	x‘211’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat1u	530	x‘212’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat1l	531	x‘213’	603	x‘0000 0000’	Not supported. Translation not supported
ibat2u	532	x‘214’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat2l	533	x‘215’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat3u	534	x‘216’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat3l	535	x‘217’	603	x‘0000 0000’	Not supported. Translation not supported.
ibat4u	560	x‘230’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat4l	561	x‘231’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat5u	562	x‘232’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat5l	563	x‘233’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat6u	564	x‘234’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat6l	565	x‘235’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat7u	566	x‘236’	COBRA	x‘0000 0000’	Not supported. Translation not supported.
ibat7l	567	x‘237’	COBRA	x‘0000 0000’	Not supported. Translation not supported.

Table 29: Exception Vector Override Registers

Register Name	SPR Number		Source	POR Value	Notes
	Decimal	Hex			
evc-off	700	x‘2BC’	COBRA	x‘0000 0000’	See *COBRA Core Exceptions* on page 470.
evc-on	701	x‘2BD’	COBRA	x‘0000 0000’	See *COBRA Core Exceptions* on page 470.
evov-off	702	x‘2BE’	COBRA	x‘0000 0000’	See *COBRA Core Exceptions* on page 470.
evov-on	703	x‘2BF’	COBRA	x‘0000 0000’	See *COBRA Core Exceptions* on page 470.
evr-mc	720	x‘2D0’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-dsi	721	x‘2D1’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-isi	722	x‘2D2’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-ex1	723	x‘2D3’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-aln	724	x‘2D4’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-inv	725	x‘2D5’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-prv	726	x‘2D6’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-trp	727	x‘2D7’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-fpu	728	x‘2D8’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-dec	729	x‘2D9’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-sc	730	x‘2DA’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-trc	731	x‘2DB’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-smi	732	x‘2DC’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-pit	733	x‘2DD’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-fit	734	x‘2DE’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-wdt	735	x‘2DF’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-ex2	752	x‘2F0’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.
evr-dbg	753	x‘2F1’	COBRA	x‘FFFF FFFE’	See *COBRA Core Exceptions* on page 470.

Table 30: Internal Debug Access Address Map

Unit	Debug Bus Address Range
Bpu Internals	x‘000’ - x‘07F’ (for development use only).
Reg Internals	x‘080’ - x‘0FF’ (for development use only).
Lsu Internals	x‘100’ - x‘17F’ (for development use only).
Fxu Internals	x‘180’ - x‘1BF’ (for development use only).
ICache Internals	x‘1C0’ - x‘1FF’ (for development use only).
Immu Internals	x‘200’ - x‘2BF’ (for development use only).
DCache Internals	x‘2C0’ - x‘2FF’ (for development use only).
Dmmu Internals	x‘300’- x‘3BF’ (for development use only).
Reserved	x‘3C0’ - x‘3FF’ (for development use only).

3.19.8 COBRA Specific Register Definitions

For most of the registers named above, either a 40x or 60x spec will give the bit definition. A few registers are different and are described in detail below.

3.19.8.1 Hardware Implementation Detail 0 Register (HID0)

Enables caches and controls architecture specific functionality. This register controls whether COBRA Core acts as a 40x or 60x series processor and allows the different features of each architecture to be individually selected.

Length 32 bits

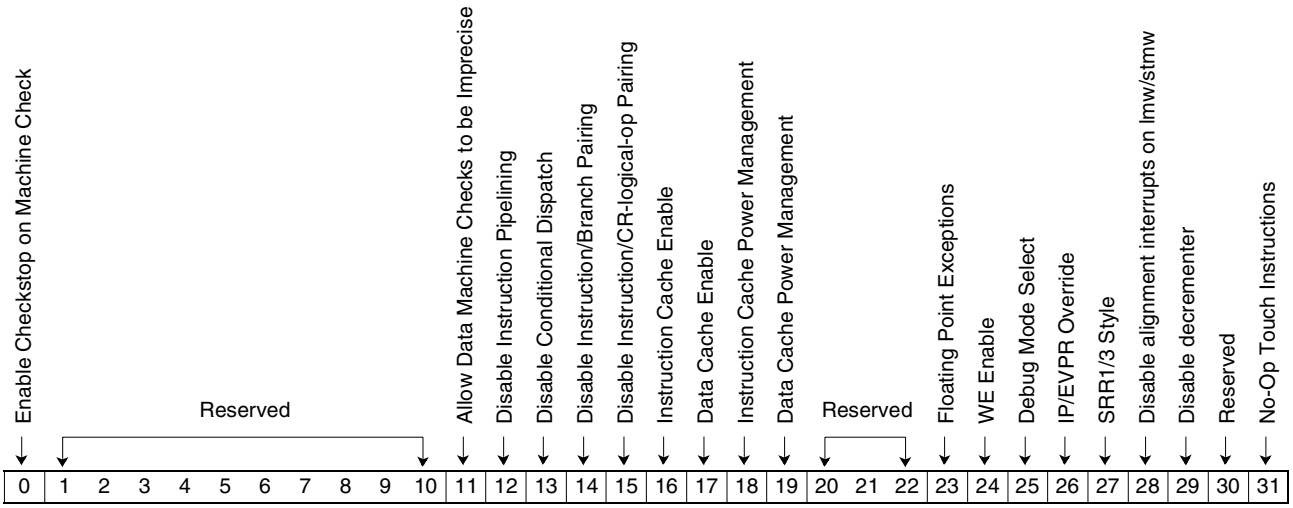
Type Read/Write

SPR Address 1023 (Decimal)
x‘3FF’ (Hex)

Address

Power On Reset Value x‘0000 00FC’ (40x mode)
x‘8000 0000’ - Alternative value (60x mode suggested value)

Restrictions None



Bit(s)	Name	Description
0	Enable Checkstop on Machine Check	1 A machine check that occurs when MSR(ME)=0 will cause the hardware to freeze, maintaining much of the state of the machine. 0 The processor will attempt to continue execution when a machine check occurs when MSR(ME)=0. **Note:** When MSR(ME)=1 and a machine check occurs, a machine check exception is taken regardless of the setting of this bit.
1-10	Reserved	Reserved.

Bit(s)	Name	Description
11	Allow Data Machine Checks to be Imprecise	Setting this to '1' will result in a very small performance gain, at the expense of accuracy in the SRR0/2 of a machine check.
12	Disable Instruction Pipelining	1 Disable 0 Enable
13	Disable Conditional Dispatch	1 Disable 0 Enable
14	Disable Instruction/Branch Pairing	1 Disable 0 Enable
15	Disable Instruction/CR-logical-op Pairing	1 Disable 0 Enable
16	Instruction Cache Enable	0 Disable 1 Enable
17	Data Cache Enable	0 Disable 1 Enable
18	Instruction Cache Power Management	0 Power management active 1 Power management inactive
19	Data Cache Power Management	0 Power management active 1 Power management inactive
20-22	Reserved	Reserved.
23	Floating Point Exceptions	0 Treat floating point instructions as illegal instructions. 1 Allow floating point instructions to cause floating point unavailable exceptions, if enabled by MSR. Otherwise, cause illegal instruction exception.
24	WE Enable	Enables the MSR(WE) bit to cause a 40x style WE. 0 Disabled 1 Enabled
25	Debug Mode Select	0 Enables the BE and SE bits of the MSR to function as a 60x. 1 Enables the MSR(DE) bit as a 40x. **Note:** All 40x debug facilities (IAC, DAC, etc.) are disabled when in 60x mode.
26	IP/EVPR Override	0 EVPR contents are used as the upper 16 bits of the exception vector, regardless of the value of MSR(IP). 1 MSR(IP) determines the upper 16 bits of the exception vector. HID0(IPO=26) MSR(IP=25) Exception Vector 0 0 0000vvvv 0 1 FFF0vvvv 1 - eeeevvvv **Note:** eeee = EVPR register contents, vvvv = exception vector offset (for example, 0700).
27	SRR1/3 Style	0 Interrupts cause srr1/3 to receive interrupt codes in bits 0:15, and MSR contents in bits 16:31. Likewise, rfi/rfci restore bits 16:31 of srr1/3 to the MSR (60x mode). 1 Interrupts cause srr1/3 to receive MSR contents in bits 0:31. Likewise, rfi/rfci restore bits 0:31 of srr1/3 to the MSR (40x mode). **Note:** Status is stored in ESR register regardless.
28	Disable alignment interrupts on lmw/stmw	0 lmw/stmw instructions to non-word aligned addresses cause alignment interrupts (60x mode). 1 lmw/stmw instructions never cause alignment interrupts (40x mode).

Bit(s)	Name	Description
29	Disable decrementer	0 The decrementer register is a free running countdown register which causes a decrementer interrupt when it decrements through '0'. 1 The decrementer register does not decrement.
30	Reserved	Reserved.
31	No-Op Touch Instructions	0 Touch instructions work 1 Touch instructions disabled

3.19.8.2 Machine State Register (MSR)

Controls the run time state of the COBRA Core.

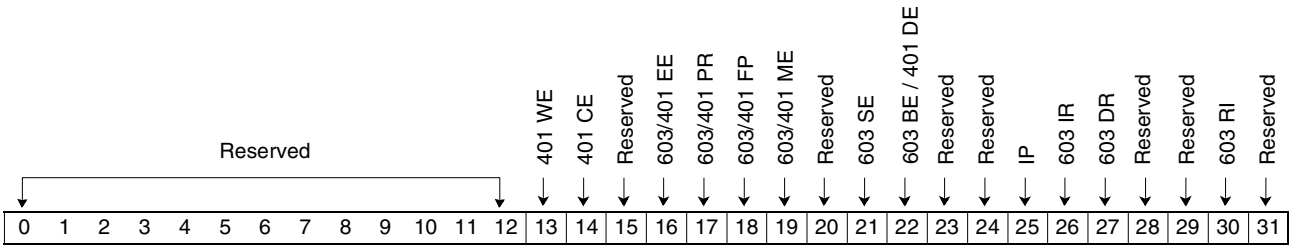
Length 32 bits

Type Read/Write

Address Accessible via the mtmsr/mfmsr instructions

Power On Reset Value x'0000 0040'

Restrictions None



Bit(s)	Name	Description
0-12	Reserved	Reserved.
13	401 WE	If HID0(24) = 0, this is a read/write bit with no effect (603 POW). Otherwise it is the (401 WE) bit. When this bit is set, the processor halts operation until this bit is cleared (automatically by any interrupt).
14	401 CE	Enables critical level exceptions. Critical level exceptions are higher priority than normal exceptions. Any exception can be assigned critical level in COBRA Core. This bit can only mask off exceptions programmed to be critical level through other COBRA Core facilities. By default, no exception is critical level. **Note:** The 60x does not have the concept of critical level exceptions. The 40x has both critical level exceptions and a critical interrupt. The critical interrupt is just a second external interrupt. In the 40x, specific exceptions were hard wired to be critical level, and the rest were hard wired to be normal level.
15	Reserved	Unimplemented (603 ILE). COBRA Core does not support Little Endian execution.
16	603/401 EE	External Interrupt Enable. Used to mask off non-critical level exceptions.
17	603/401 PR	Privilege Instruction Restricted. If this bit is '1', attempting to execute a privileged (supervisor) instruction will result in a privilege violation exception. If this bit is '0', all instructions may be executed normally.

Bit(s)	Name	Description
18	603/401 FP	If HID0(23) = 1: If FP=0, all floating point instructions cause a floating point disabled interrupts. If FP=1, all floating point instructions cause illegal instruction interrupts. If HID0(23) = 0: this is a read/write bit with no effect.
19	603/401 ME	Enables Machine Check Exceptions. If this bit is '1', a machine check will cause a machine check exception to occur. If this bit is '0', a machine check will cause COBRA Core to halt execution (if HID0(0) = 1), or the machine check will be ignored (if HID0(0) = 0).
20	Reserved	Unimplemented (603 FE0). COBRA Core does not support floating point.
21	603 SE	If HID0(25) = 0 this is 603 SE. Otherwise, it is a read/write bit with no effect.
22	603 BE / 401 DE	If HID0(25) = 0 this is 603 BE. Otherwise, it is 401 DE.
23	Reserved	Unimplemented (603 FE1). COBRA Core doesn't support floating point.
24	Reserved	Reserved.
25	IP	In combination with HID0(IPO = 26), this bit determines the upper 16 bits of an exception vector. See *3.19.8.1 Hardware Implementation Detail 0 Register (HID0)* on page 482 for full details.
26	603 IR	Translation is not supported. Do not set this bit.
27	603 DR	Translation is not supported. Do not set this bit.
28	Reserved	Reserved.
29	Reserved	Reserved.
30	603 RI	Recoverable Interrupt. This bit is cleared when an exception is taken.
31	Reserved	Unimplemented (603/401 LE). COBRA Core does not support Little Endian execution.

3.19.8.3 Exception Status Register (ESR)

When an exception occurs, this register is updated to indicate which condition caused the exception. If an exception vector can only be reached by one exception, this register is cleared.

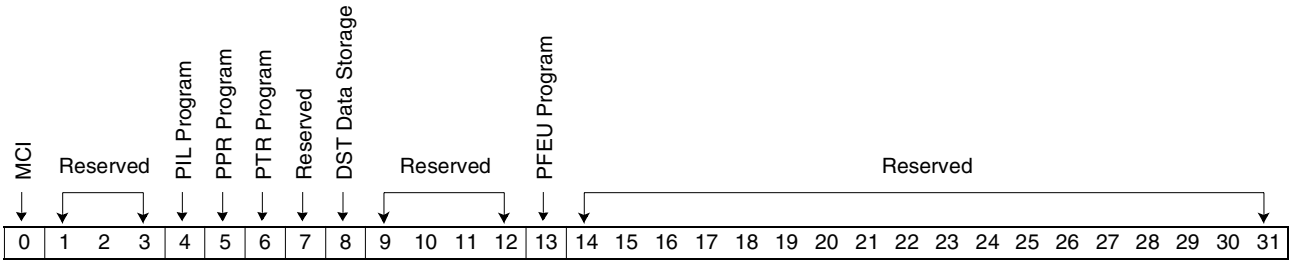
Length 32 bits

Type Read/Write

SPR Address 980 (Decimal)
x‘3D4’ (Hex)

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
0	MCI	Machine Check - Instruction.
1-3	Reserved	Reserved.
4	PIL Program	Program - Illegal Instruction Exception.
5	PPR Program	Program - Privileged Instruction Exception.
6	PTR Program	Program - Trap Instruction Exception.
7	Reserved	Reserved.
8	DST Data Storage	A store instruction or (dcbz/dcbi) caused the data exception.
9-12	Reserved	Reserved.
13	PFEU Program	Floating point enabled, but instruction unimplemented exception.
14-31	Reserved	Reserved.

3.19.8.4 Machine Check Enable Register (MCHK)

When an exception occurs, this register is updated to indicate which condition caused the exception. If an exception vector can only be reached by one exception, this register is cleared.

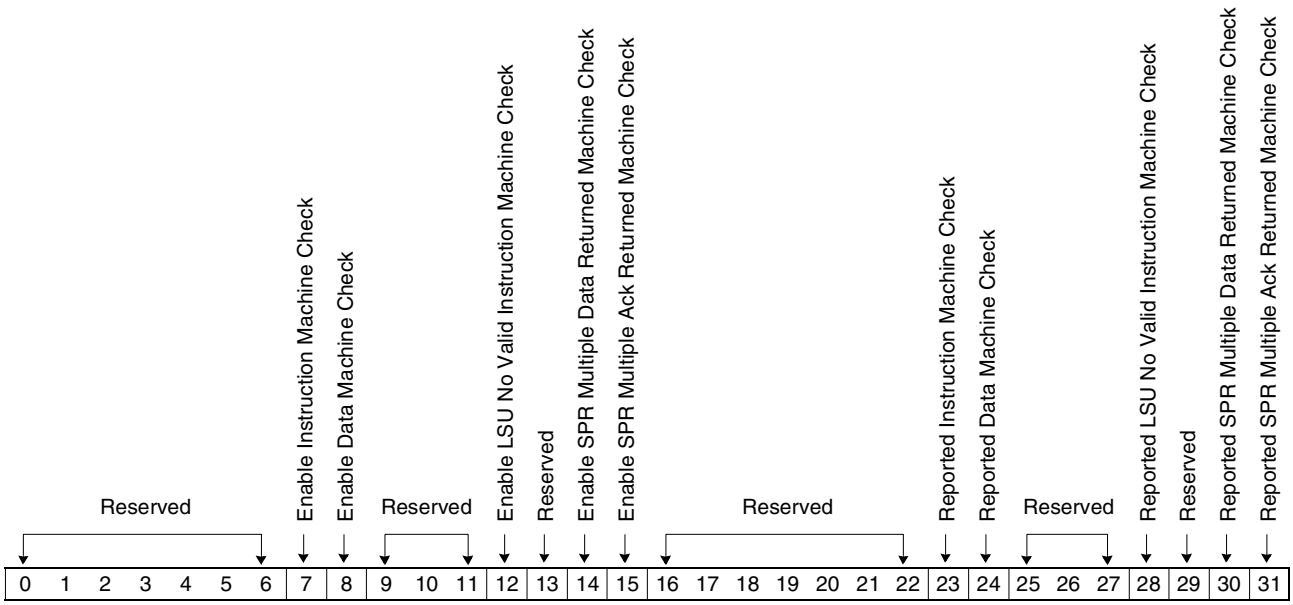
Length 32 bits

Type Clear/Set

SPR Address 688 and 689 (Decimal)
x‘2B0’ and x‘2B1’ (Hex)

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
0-6	Reserved	Reserved.
7	Enable Instruction Machine Check	This bit set to a ‘1’ allows bit 23 of this register to cause a machine check in COBRA.
8	Enable Data Machine Check	This bit set to a ‘1’ allows bit 24 of this register to cause a machine check in COBRA.
9-11	Reserved	Reserved.
12	Enable LSU No Valid Instruction Machine Check	This bit set to a ‘1’ allows bit 28 of this register to cause a machine check in COBRA.
13	Reserved	Reserved.
14	Enable SPR Multiple Data Returned Machine Check	This bit set to a ‘1’ allows bit 30 of this register to cause a machine check in COBRA.
15	Enable SPR Multiple Ack Returned Machine Check	This bit set to a ‘1’ allows bit 31 of this register to cause a machine check in COBRA.
16-22	Reserved	Reserved.

Bit(s)	Name	Description
23	Reported Instruction Machine Check	This bit is set when any of bits 3-0 of the *PCORE COBRA Core External Machine Check Status Register* on page 433 are set.
24	Reported Data Machine Check	This bit is set when any of bits 19-16 of the *PCORE COBRA Core External Machine Check Status Register* on page 433 are set.
25-27	Reserved	Reserved.
28	Reported LSU No Valid Instruction Machine Check.	This bit, when set, is indicative of a hardware failure.
29	Reserved	Reserved.
30	Reported SPR Multiple Data Returned Machine Check	This bit, when set, is indicative of a hardware failure.
31	Reported SPR Multiple Ack Returned Machine Check	This bit, when set, is indicative of a hardware failure.

3.20 RS-232 Interface Logic (RS-232)

The RS-232 entity provides a means by which an external debugger and the processor core can communicate. The RS-232 operates on a one- or four-byte wide basis.

3.20.1 RS-232 Control Register

This register controls the operation of the RS-232 logic.

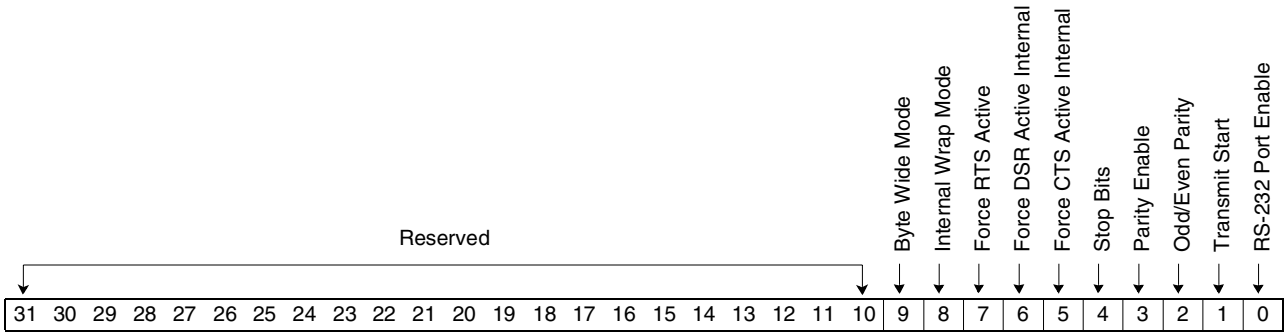
Length 32 bits

Type Clear/Set

DCR Address x‘210’ and x‘211’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-10	Reserved	Reserved.
9	Byte Wide Mode	This bit set to ‘1’ makes the port operate in byte-wide mode. When a transmit is started, only bits 7-0 of the transmit buffer are sent. A receive interrupt is generated whenever a byte is received.
8	Internal Wrap Mode	This bit set to ‘1’ connects the transmit data stream to the receive data stream.
7	Force RTS Active	This bit set to ‘1’ forces RTS to be driven active, regardless of what the transmit state machine is doing.
6	Force DSR Active Internal	This bit set to ‘1’ forces DSR internal to RS-232 to appear active, regardless of the DSR input’s state.
5	Force CTS Active Internal	This bit set to ‘1’ forces CTS internal to RS-232 to appear active, regardless of the CTS input’s state.
4	Stop Bits	This bit set to ‘1’ indicates the port should use two stop bits. This bit set to ‘0’ indicates the port should use one stop bit.
3	Parity Enable	This bit set to ‘1’ enables parity.
2	Odd/Even Parity	If parity is enabled, this bit, set to ‘1’, sets the parity type to odd. This bit set to ‘0’ sets the parity type to even.
1	Transmit Start	This bit set to ‘1’ initiates the transmission of what is in the transmit buffer. This bit is cleared by hardware when the transmission is complete.
0	RS-232 Port Enable	This bit set to ‘1’ enables the RS-232 port.

3.20.2 RS-232 Status Register

This register controls the operation of the RS-232 logic.

Length 32 bits

Type Clear/Set

DCR Address x‘212’ and x‘213’

Power On Reset Value x‘0000 0000’

Restrictions None

Bit(s)	Name	Description
31-7	Reserved	Reserved.
6	DSR Inactive	This bit set to ‘1’ indicates DSR has gone inactive.
5	CTS Inactive	This bit set to ‘1’ indicates CTS has gone inactive.
4	Transmit Complete	This bit set to ‘1’ indicates the current transmission has completed.
3	Framing Error	This bit set to ‘1’ indicates a framing error has been detected.
2	Overrun Error	This bit set to ‘0’ indicates four bytes were received before the previous (1-byte mode) or four bytes (4-byte mode) had been read from the receive buffer.
1	Parity Error	This bit set to ‘1’ indicates a parity error has been detected.
0	Receive Complete	This bit set to ‘1’ indicates data from a clean reception is in the receive buffer.

3.20.3 RS-232 Interrupt Enable Register

This register contains bits corresponding to the bits in the *RS-232 Status Register*. If a bit in this register is set and the corresponding bit is set in the RS-232 status register, an interrupt is generated. Bits 6-4 generate a transmit interrupt and bits 3-0 generate a receive interrupt.

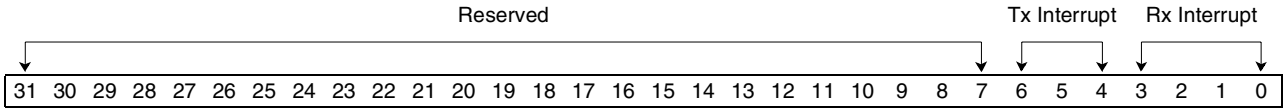
Length 32 bits

Type Clear/Set

DCR Address x‘214’ and x‘215’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-7	Reserved	Reserved.
6-4	Tx Interrupt	Generates a transmit interrupt.
3-0	Rx Interrupt	Generates a receive interrupt.

3.20.4 RS-232 Transmit Buffer

This register contains the data to be sent over the RS-232 connection.

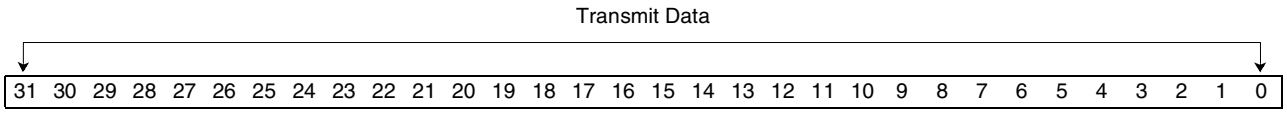
Length 32 bits

Type Read/Write

DCR Address x‘216’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Transmit Data	Data to be sent over link. Only bits 7-0 are sent in byte mode. The other bits are shifted, so the user can write all four bytes at once and just set the transmit bit four times.

3.20.5 RS-232 Receive Buffer

This register contains the data received over the RS-232 connection. Once this buffer is full, software has four byte receive times minimum to read it before an overrun condition can occur.

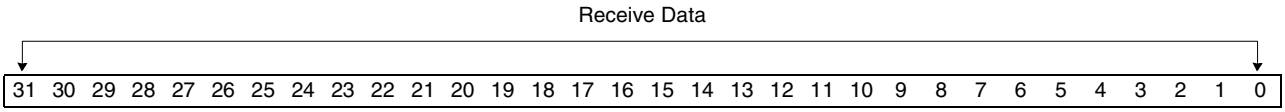
Length 32 bits

Type Read/Write

DCR Address x‘217’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-0	Receive Data	Data received over the link. Only bits 7-0 are valid in byte mode.

3.20.6 RS-232 Baud Rate Register

This register contains the value used to determine the baud rate. The value to place in this register can be determined by this formula: Baud Rate = 133 MHz/(8*(Baud Rate Register + 1)).

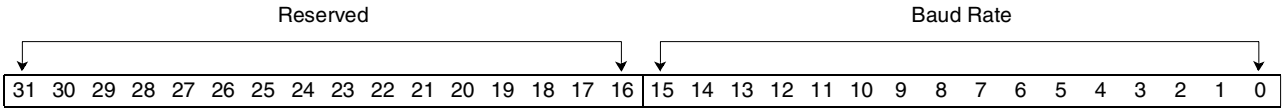
Length 32 bits

Type Read/Write

DCR Address x‘218’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Baud Rate	Suggested values: x‘120’ - 56600 x‘1B0’ - 38400 x‘240’ - 28800 x‘360’ - 19200

3.20.7 RS-232 CTS/DSR Glitch Timer Rate

This register contains the number of (baud rate/8) clocks CTS/DSR must be active/inactive before the state of CTS/DSR is considered valid. Transitions of shorter duration are assumed to be glitches.

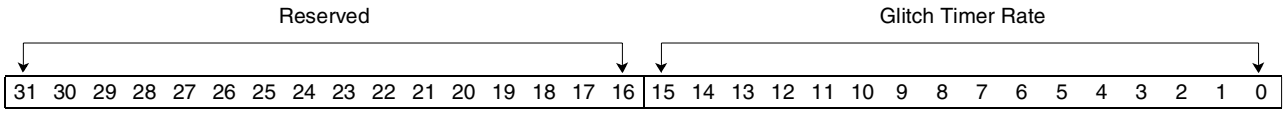
Length 32 bits

Type Read/Write

DCR Address x‘219’

Power On Reset Value x‘0000 0020’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
15-0	Glitch Timer Rate	Number of (baud rate/8) clocks CTS or DSR must be active before they are considered valid.

3.20.8 RS-232 Reset Register

This register resets the port.

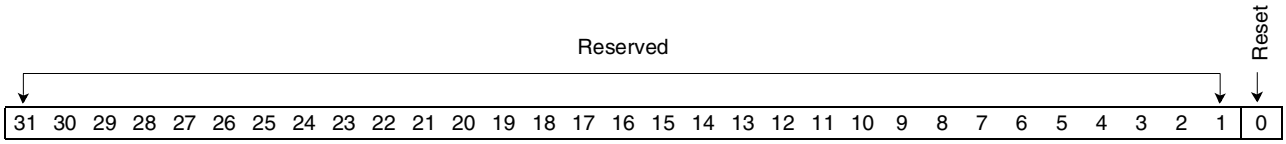
Length 32 bits

Type Clear/Set

DCR Address x‘21A’ and x‘21B’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-1	Reserved	Reserved.
0	Reset	This bit set to ‘1’ resets the port. The port will remain reset until this bit is cleared.

3.20.9 RS-232 Error Forcing Register

This register can be used by diagnostics in a wrap environment (external or internal) to force frame and parity errors. Overrun errors can be generated by sending four bytes, not reading the receive buffer, and sending four more bytes.

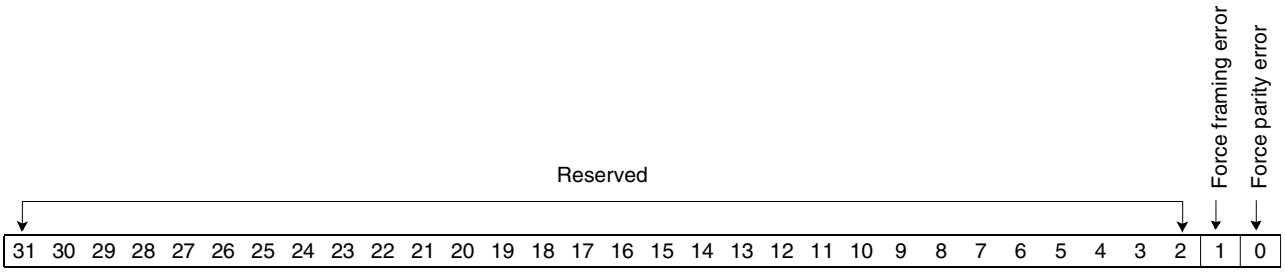
Length 32 bits

Type Read/Write

DCR Address x‘21C’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-2	Reserved	Reserved.
1	Force framing error	Setting this bit to a ‘1’ forces the first frame bit to a ‘0’ on all transmits.
0	Force parity error	Setting this bit to a ‘0’ forces the receive logic to check for the opposite parity the transmit logic is using.

3.21 PowerPC On-Chip Memory (PPOCM) Entity

The PPOCM entity is comprised of several SRAM arrays that provide a 96-KB memory that may be used by the internal processor or the PNR. Also included in PPOCM is a DMA controller that the processor may use to do bulk data moves between the SRAM arrays and Control Memory, Packet Memory, or memory on an external PCI device. The PPOCM arrays are referred to as on-chip memory and the three external memories (Control, Packet, PCI) are referred to collectively as off-chip memory.

3.21.1 DMA Controller

The DMA controller moves data in 8-byte aligned, 8-byte portions. In real addressing mode, up to 64 KB can be transferred at once. In virtual addressing mode, there are more restrictions. The DMA must remain within the virtual 4-KB page for both the PPOCM array address and the off-chip memory address.

3.21.2 PPOCM Control Register

This register contains information which controls the functions of the entity.

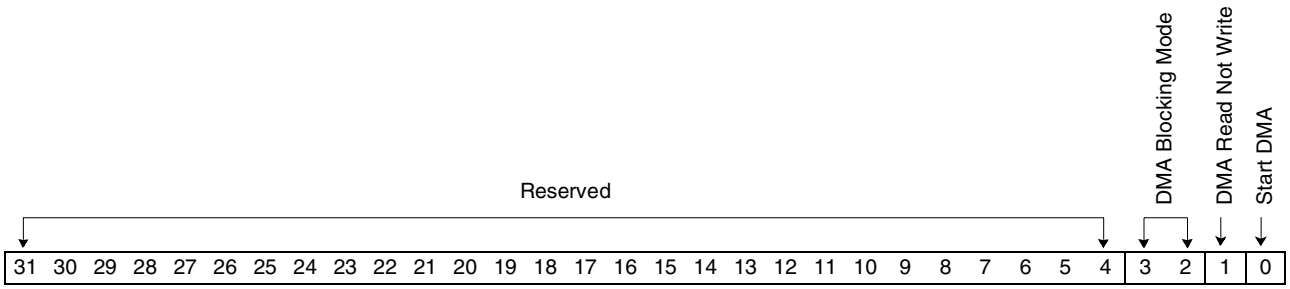
Length 32 bits

Type Clear/Set

DCR Address x‘100’ and x‘101’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-4	Reserved	Reserved.
3-2	DMA Blocking Mode	These bits control how non-DMA accesses to PPOCM are handled while a DMA is in progress. They are encoded as follows: 00 Non-DMA PPOCM accesses are held off until the DMA is complete. 01 Non-DMA PPOCM accesses are held off only if the requester is attempting to use an array that will be involved in the DMA. 10 Reserved. 11 Reserved.
1	DMA Read Not Write	Setting this bit will indicate the DMA being set up is to transfer data from off-chip memory into PPOCM. Clearing this bit indicates the DMA should transfer data from PPOCM to off-chip memory.
0	Start DMA	Setting this bit initiates the DMA operation. This bit will clear automatically when the DMA is completed.

3.21.3 PPOCM Status Register

This register contains status information that can be used to generate interrupts.

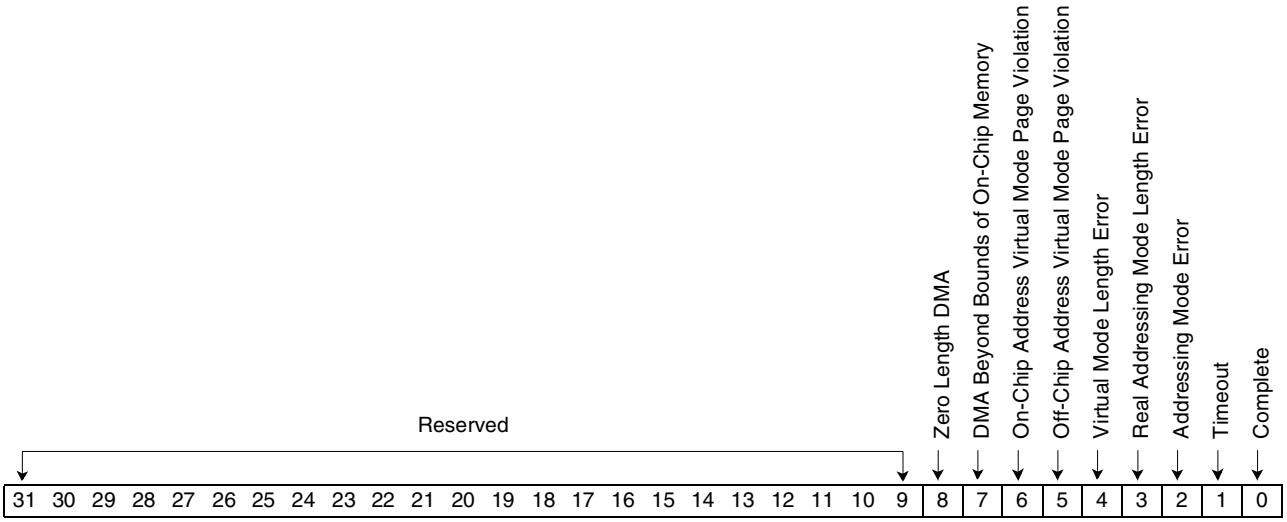
Length 32 bits

Type Clear/Set

DCR Address x‘102’ and x‘103’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-9	Reserved	Reserved.
8	Zero Length DMA	This bit, set to a ‘1’, indicates a DMA with a length of zero was attempted.
7	DMA Beyond Bounds of On-Chip Memory	This bit, set to a ‘1’, indicates the on-chip address plus the DMA length yields a value that exceeds the address pace of the on-chip memory.
6	On-Chip Address Virtual Mode Page Violation	This bit, set to a ‘1’, indicates the on-chip virtual address provided to PPOCM in combination with the DMA length results in a virtual page cross.
5	Off-Chip Address Virtual Mode Page Violation	This bit, set to a ‘1’, indicates the off-chip virtual address provided to PPOCM in combination with the DMA length results in a virtual page cross.
4	Virtual Mode Length Error	This bit, set to a ‘1’, indicates a virtual address mode DMA was started and the value in the DMA length register is greater than 4 KB.
3	Real Addressing Mode Length Error	This bit, set to a ‘1’, indicates a real address mode DMA was started and the value in the DMA length register is greater than 64 KB.
2	Addressing Mode Error	This bit, set to a ‘1’, indicates the off-chip memory and on-chip address written to the DMA address registers must be either both real or both virtual.
1	Timeout	This bit, set to a ‘1’, indicates the DMA timer expired.
0	Complete	This bit, set to a ‘1’, indicates the DMA completed. The other bits in this register being a ‘0’ will indicate a good completion.

3.21.4 PPOCM Interrupt Enable Register

This register allows the user to enable interrupts for each of the conditions reported in the *PPOCM Status Register*. Each bit corresponds to the same bit in the status register and when set to '1' generates an interrupt to the processor if the condition is detected.

Length 32 bits

Type Clear/Set

DCR Address x'104' and x'105'

Power On Reset Value x'0000 0000'

Restrictions None

3.21.5 PPOCM DMA Off-Chip Effective Address Register

This register provides the DMA controller the effective address of the off-chip portion of the DMA.

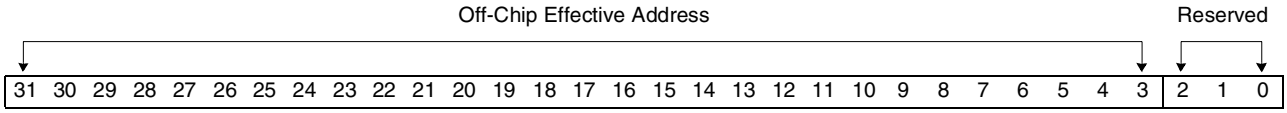
Length 32 bits

Type Read/Write

DCR Address x'106'

Power On Reset Value x'0000 0000'

Restrictions None



Bit(s)	Name	Description
31-3	Off-Chip Effective Address	Off-Chip address involved in DMA transfer.
2-0	Reserved	Reserved.

3.21.6 PPOCM DMA On-Chip Effective Address Register

This register provides the DMA controller the effective address of the on-chip portion of the DMA.

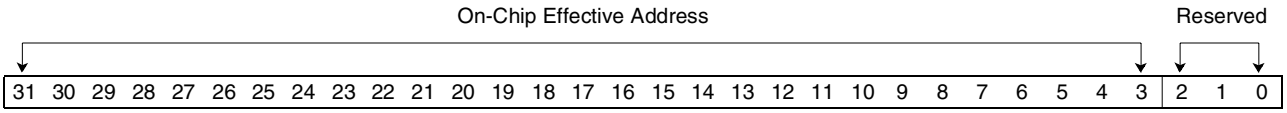
Length 32 bits

Type Read/Write

DCR Address x‘107’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-3	On-Chip Effective Address	On-Chip address involved in DMA transfer.
2-0	Reserved	Reserved.

3.21.7 PPOCM DMA Length Register

This register provides the DMA controller the length of the DMA. The maximum DMA length in real addressing mode is x‘0001 0000’ (64 KB). The maximum DMA length in virtual addressing mode is x‘0000 1000’ (4 KB).

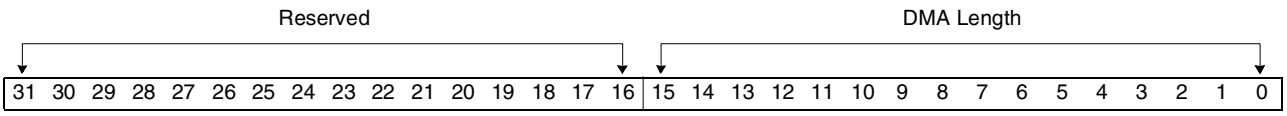
Length 32 bits

Type Read/Write

DCR Address x‘108’

Power On Reset Value x‘0000 0000’

Restrictions None



Bit(s)	Name	Description
31-16	Reserved	Reserved.
16-0	DMA Length	Only bits 16-3 are writable as DMAs are done only in 8-byte segments.

3.21.8 PPOCM DMA Timeout Timer Register

This register is compared to a timer that begins running when bit 0 of the control register is set to ‘1’. When the timer reaches the value in this register, the DMA is terminated and a status bit is set. The default value of x‘FF FFFF’ results in a timeout value of 125 ms.

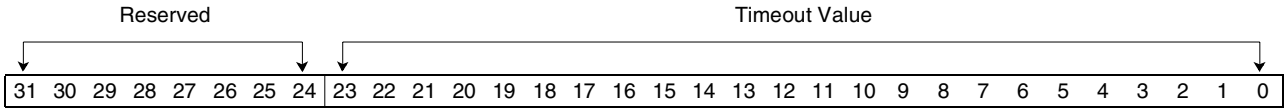
Length 32 bits

Type Read/Write

DCR Address x‘109’

Power On Reset Value x‘00FF FFFF’

Restrictions None



Bit(s)	Name	Description
31-24	Reserved	Reserved.
23-0	Timeout Value	Timeout value.

3.22 JTAG Interface Logic (CJTAG)

The CJTAG entity contains logic to support a test access port (TAP) controller compliant with the IEEE 1149.1-1993 standard. The TAP controller is accessed via the following five pins:

TCK Test Clock. All activity of the JTAG interface is clocked via TCK. Events occur on the rising or falling edge of TCK. TCK should have a maximum frequency of 20 MHz.

TMS Test Mode Select. Test Mode Select is used to control state transitions in the TAP controller. These transitions occur on the rising edge of TCK.

TDI Test Data In. Serial data input to the JTAG logic.

TDO Test Data Out. Serial data output to the JTAG logic.

TRST Test Reset. Asynchronous, minus active reset to the TAP controller. Assertion of this input causes the TAP controller to reset and the JTAG instruction register to load the IDCODE instruction. It is preferable to have TRST be independent of any chip reset. With an independent reset, the JTAG logic can be reset, allowing the chip's state to be examined without having to reset the core logic.

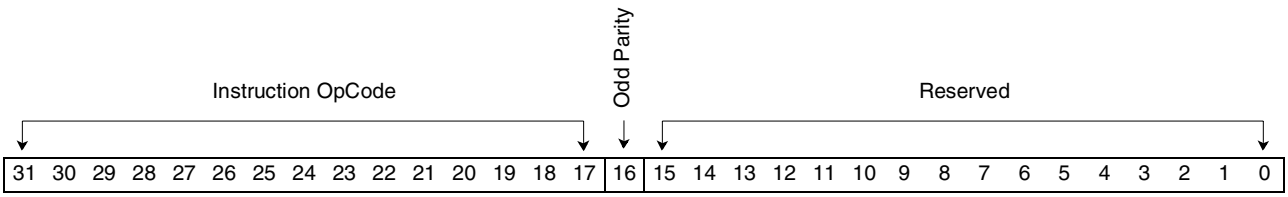
The proper operation of these signals and the TAP controller is defined in the IEEE 1149.1-1993 standard.

3.22.1 Scanning

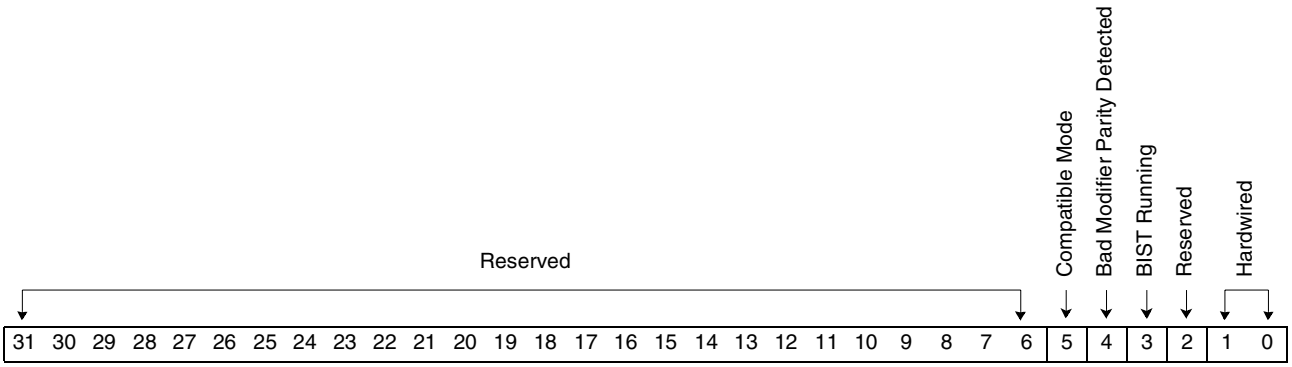
The TAP controller supports two types of scans: instruction scans and data scans. Instruction scans control the type of operation and select which, if any, scan chains are involved in the operation. Data scans generally clock the data on TDI into the selected scan chain.

3.22.2 Instruction Format

The processor's JTAG logic supports 32-bit instructions in one of two formats: the first format uses opcodes comply with the IEEE standard; the other supports opcodes that are compatible but not compliant with the IEEE standard. As an instruction is scanned in, status for the previous instruction is presented on TDO.



Bit(s)	Name	Description
31-17	Instruction OpCode	Instruction OpCode.
16	Odd Parity	In compatible mode, this is odd parity over bits 15-0.
15-0	Reserved	Reserved.



Bit(s)	Name	Description
31-6	Reserved	Reserved.
5	Compatible Mode	Compatible Mode.
4	Bad Modifier Parity Detected	Bad Modifier Parity Detected.
3	BIST Running	BIST Running.
2	Reserved	Reserved.
1-0	Hardwired	Hardwired to '01' as required by IEEE specification.

3.22.3 Instructions

3.22.3.1 IDCODE

Returns a 32-bit identification code when a data scan is performed. The IDCODE has the following structure:

Opcode x‘0300 XXXX’

Bit(s)	Name	Description
31-28	Version Number	This is set to x‘1’ for 2.61.
27-12	Part Number	This is set to x‘4700’ for IBM32NPCXX1EPABBE66.
11-0	Manufacturer	This is set to x‘049’ for IBM.

3.22.3.2 SAMPLE/PRELOAD

Captures the state of the boundary scan I/O. As the values captured are scanned out, new values can be loaded into the boundary scan latches. This operation will not affect functional operation.

Opcode x‘0402 XXXX’

3.22.3.3 EXTEST

Drives the values in the boundary scan latches onto their respective I/O. This function can be used in conjunction with SAMPLE/PRELOAD to perform card wire tests.

Opcode (Compliant) x‘0000 0000’

Opcode (Compatible) x‘0600 XXXX’

3.22.3.4 BYPASS

Selects the single bit bypass register for data scans.

Opcode (Compliant) x‘FFFF FFFF’

Opcode (Compatible) x‘FFFF XXXX’ or x‘0000 XXXX’

3.22.3.5 RUNBIST

Causes built in self test (BIST) to execute.

Opcode x‘0770 XXXX’

3.22.3.6 BIST_RESULTS

Returns a 64-bit value when a data scan is performed. Bits 63-32 are the PRPG and bits 31-0 are the MISR from the BIST logic.

Opcode x‘1F02 XXXX’

3.22.3.7 COMPATIBLE_MODE

This command enables JTAG compatible but not compliant mode.

Opcode x‘3000’

3.22.3.8 COMPLIANT_MODE

This command enables JTAG compliant mode.

Opcode ‘3301 0000’

3.22.3.9 STOP

This command halts the functional clocks of the PNR in anticipation of a scan. After the STOP command is scanned in, a data scan that takes the TAP controller through the Capture-DR, Exit1-DR, and Update-DR states should be performed. This will capture the state of the I/O so that they can be held in a known state if a scan command is issued.

Opcode x‘2002’

3.22.3.10 SCAN

This command causes TDI to be clocked into the scan chain during a subsequent data scan. The scan out of the scan chain is placed on TDO. This command will not work unless a STOP command is sent down immediately before the SCAN command is issued.

Opcode x‘0802’

3.22.3.11 SCAN_IN

This command causes TDI to be clocked into the scan chain during a subsequent data scan. TDO is forced to ‘0’. This command will not work unless a STOP command is sent down immediately before the SCAN_IN command is issued.

Opcode x‘0900’

3.22.3.12 SCAN_OUT

This command causes the scan out of the scan chain to be placed on TDO. Data is recirculated through the scan chains. TDI is ignored. This command will not work unless a Stop command is sent down immediately before the SCAN_OUT command is issued.

Opcode x‘0A00’

3.22.3.13 Private_RW1

This command is used by RISCWATCH.

Opcode x‘0500’

3.22.3.14 Private_RW2

This command is used by RISCWATCH.

Opcode x‘0582’

3.22.3.15 Private_RW3

This command is used by RISCWATCH.

Opcode x‘05C0’

3.23 Sonet Framer Core (FRAMR Chiplet Address Mapping)

Table 31: FRAMR Chiplet Address Mapping

Chiplet Name	Short Name	Chiplet Base Address	Chiplet Address Range	Number of Bytes
Reserved		x‘000’	x‘000 - 0FF’	256
ACH_Tx	HT	x‘100’	x‘100 - 1FF’	256
ACH_Rx	HR	x‘200’	x‘200 - 2FF’	256
Reserved		x‘300’	x‘300 - 3FF’	256
OFP_Tx	OT	x‘400’	x‘400 - 7FF’	1024
OFP_Rx	OR	x‘800’	x‘800 - BFF’	1024
GPPINT	GP	x‘C00’	x‘C00 - CFF’	256
Reserved		x‘D00’	x‘D00 - FFF’	768

3.23.1 Description of GPPINT

3.23.1.1 Overview

The General Purpose Processor INTerface (GPPINT) provides direct access to registers located in the GPPINT module; it provides delayed access to registers and counters located in the GppHandler modules of the various chiplets of the SONET core. GPPINT controls the handshaking with the external microprocessor as well as the handshaking with the GppHandlers at the asynchronous chiplet interfaces. Address decoding is done to the chiplet level in GPPINT. In addition, addresses are decoded to the register level for the local GPPINT registers.

3.23.1.2 Reset Register

Each chiplet is controlled by one reset bit. At power-on, all reset bits are active and the chiplets are disabled. They can be released by the General Purpose Processor (GPP) only after all global configuration parameters have been set and the clocks to the chiplets have been established. In addition, there are reset bits for the chiplets that do not have their own GppHandler.

3.23.1.3 Interrupt Registers

The interrupt register is used as a pointer to the chiplet interrupt registers with pending requests: the clock status error register, and the handshaking error register. An active bit of the interrupt register is reset by removing the cause for the request in the corresponding chiplet or by masking the active IRQ bit(s) in the chiplet; therefore, the interrupt registers (including the pointer) are read only. All interrupt and pointer registers have a corresponding MASK register (R/W). Every unmasked, active interrupt bit causes an active pointer bit. Every unmasked, active pointer bit causes activation of the interrupt signal to the microprocessor.

3.23.1.4 Handshaking Error Registers

Each bit of the handshaking error registers indicates a locked interface to one of the chiplet GppHandlers. Two additional bits indicate various timeout events. To reset an individual bit of the handshaking error register, the cause for the request must be removed and a ‘1’ must be written into the bit location of the register (R/W). Reading the register will reset the whole (8-bit) register if the corresponding “clear-register” option is set

in the configuration register. The handshaking error indication register has a corresponding MASK register (R/W). Every unmasked, active handshaking error bit causes activation of the pointer bit in the GPPINT interrupt register.

3.23.1.5 Clock Monitor Status Registers

The clock monitor status register bits indicate the loss of a specific chiplet's clock. They are set whenever a difference between the clock test signal and the individual chiplet clock acknowledge signal occurs after one clock monitor test period. To reset an individual bit of the clock monitor status registers, the clock of the corresponding chiplet must be restored and a '1' must be written into the bit location of the register (R/W). Reading one of the registers will reset the whole (8-bit) register if the corresponding "clear-register" option is set in the configuration register. The clock monitor status register has a corresponding MASK register (R/W). Every unmasked, active clock monitor status bit causes activation of the pointer bit in the GPPINT register.

3.23.1.6 Local GPPINT Configuration Registers

There are registers (R/W) for the Clock Monitor Test Period, the Watchdog Timer Period and the "clear-register" option. A read-only register provides the Vital Product Data (VPD).

3.23.1.7 Global Static Configuration Registers

These are configuration parameters that are shared by many chiplets or are needed by chiplets that have no GppHandler. The initial values can be modified by the microprocessor after power-on, but should not be changed later on. All global static configuration registers are R/W.

3.23.1.8 Status Registers

These registers provide status information from chiplets that have no GppHandler and are read only. Presently, there is only one status register for the SIM chiplet (PLL lock status).

3.23.2 Description of GPPHandler

3.23.2.1 Overview

All GPP handlers for the various chiplets have the following general register structure.

Table 32: GPPHandler Architecture

Address Range	Register Function
x‘0’ - x‘1’	Read-on-the-fly registers
x‘2’ - x‘3’	Counter enable registers
x‘4’ - x‘2F’	Counters and counter threshold registers
x‘30’	Reset register
x‘31’ - x‘32’	Command registers
x‘33’ - x‘37’	Event latch registers (was called status)
x‘38’ - x‘47’	Interrupt registers (addr=int reg, addr-1=int mask reg)
x‘48’ - x‘57’	Configuration registers

3.23.2.2 Counter Registers

Every counter has an enable bit in the counter enable register (addr 2 or 3), and optionally up to two programmable thresholds. Each counter has an interrupt bit for overflow and up to two interrupt bits for threshold crossing in the counter interrupt registers. For all counters in one handler there is one common ‘read-on-the-fly register’ that is used to store the higher order bytes to obtain a correct readback value for counters larger than eight bits. Counters are read-only registers; the count enable registers are read/write.

Note: COUNTER reading is independent of the counter length, given that a counter has address n as base, reading address n or address n-1 both yield the least significant byte of the counter. Reading address n has no influence on the counter, but reading address n-1 will reset the counter after the read. Reading address n or n-1 will always latch the higher order bytes into the read-on-the-fly register (before the optional automatic reset). Counters can only be read and not written to. For a 16-bit counter, the most significant byte should be read from ROFmid (address 0). For a 24-bit counter, the most significant byte is read from ROFhi (address 1), the next byte from ROFmid (address 0). To completely read a 24-bit counter: first read least significant byte from counter address n or n-1, then read ROFmid and ROFhi (address 0; address 1).

3.23.2.3 Reset Registers

Each handler has a two-bit reset register. Bit 0 is the chiplet reset control. This bit is active high after power on reset, causing the chiplet to be disabled. Bit 1 is the chiplet halt signal, which for selected chiplets freezes the state machines for diagnostic purposes. This is a read/write register.

3.23.2.4 Command Registers

The optional command register(s) will generate events to the chiplet. When a bit is written high by the microprocessor, it will remain high for one chiplet clock cycle. Therefore, reading back a command register will always read back zeroes. This is a read/write register.

3.23.2.5 Event Latch Registers

The optional event latch register(s) remember one ore more occurrences of events that happen in a chiplet. This may be considered as a one-bit saturating counter. Each bit in the register corresponds to an event in the chiplet. Such bits remain high after the event happened until the microprocessor implicitly or explicitly resets the bit. This is configurable: implicit reset is done by writing a high value to the bit that is to be reset. Explicit will reset all bits of one register when the register is read. This is a read/write register.

3.23.2.6 Interrupt Registers

When there are counters, user interrupts, or fatal bits in a chiplet, a MAIN INTERRUPT register will be present. Bit 0 always is the fatal interrupt bit, which is set as soon as any of the fatal interrupt events occur. The other bits refer to counters or user interrupt registers to allow easy determination of the interrupt cause. Each Interrupt register has an interrupt MASK register to enable or disable interrupt. After PowerOn Reset, interrupts are disabled. The interrupt registers are the same as the event latch registers, with the addition that when an interrupt register bit is set, and the corresponding mask register bit is set, the interrupt signal to the GPPINT chiplet is activated. The same mechanism to reset the interrupt register bits is used as for the event latch registers. The interrupt MASK registers are only changed by the microprocessor. The interrupt and interrupt mask registers are read/write.

3.23.2.7 Configuration Registers

These registers are programmed by the microprocessor with setup information, and are read/write. The first configuration register reserves bits 1 and 7 to configure explicit or implicit reset of the event latch registers and interrupt registers, respectively (when such registers are present).

3.23.2.8 Register Types

F Read-on-the-fly register (auto-generated)

N Counter register

R Reset register

I Interrupt register (auto-generated)

C Configuration register

X Control or mask register (auto-generated)

S Status (event latch) register

O Command register

3.23.3 GPPINT Registers

Table 33: GPPINT Chiplet Address Mapping Overview: Base Address = x‘C00’

Register Name	Description[1]	Address Offset	Type	Initial Value
RESGP1	Reset register	x‘00’	R/W	‘11111111’
RESGP2	Reset register	x‘01’	R/W	‘11111111’
...	Reserved	x‘02 - 0F’		
IRQGP1	Chiplet interrupt request register #1	x‘10’	R	‘00000000’
...	Reserved	x‘11 - 17’		
IRMGP1	Chiplet interrupt mask register #1	x‘18’	R/W	‘00000000’
...	Reserved	x‘19 - 1F’		
HShake1	Handshaking error register #1	x‘20’	R/W	‘00000000’
...	Reserved	x‘21 - 27’		
HSMask1	Handshaking error mask register #1	x‘28’	R/W	‘00000000’
...	Reserved	x‘29 - 2F’		
ClkStat1	Clock status register #1	x‘30’	R/W	‘00000000’
...	Reserved	x‘31 - 37’		
ClkMask1	Clock status mask register #1	x‘38’	R/W	‘00000000’
...	Reserved	x‘39 - 47’		
CMonGP1	Clock monitor test period	x‘48’	R/W	‘00000000’
WDTGP1	Watchdog Timer Period	x‘49’	R/W	‘11111111’
ConfGP1	“Clear-register” option register	x‘4A’	R/W	‘11111111’
...	Reserved	x‘4B - 4F’		
VMD	Vital Macro Data register	x‘50’	R	‘10000001’
...	Reserved	x‘51 - 57’		
GATMCS	Common ATM/CS static configuration register	x‘58’	R/W	‘00000000’
GCasc	Common Cascading static configuration register	x‘59’	R/W	‘10101010’
GLoopTx	Transmit Loopback static configuration register	x‘5A’	R/W	‘00000000’
GLoopRx	Receive Loopback static configuration register	x‘5B’	R/W	‘00000000’
GExtRes	External clock recovery circuit reset register	x‘5C’	R/W	‘00000000’
...	Reserved	x‘5D - 67’		
OFPTXGP	OFP_Tx static configuration register	x‘68’	R/W	‘00000000’
OFPRXGP1	OFP_Rx static configuration register #1	x‘69’	R/W	‘00000000’
OFPRXGP2	OFP_Rx static configuration register #2	x‘6A’	R/W	‘00000000’
...	Reserved	x‘6B - 71’		
PIMRConf2	PIM_Rx static configuration register #2	x‘73’	R/W	‘00000000’
...	Reserved	x‘74 - 7E’		
SIMStat	SIM status register	x‘7F’	R	N.A.
...	Reserved	x‘80 - FF’		

1. All registers are of 32-bit width.

3.23.3.1 Chiplet Reset Register 1 (RESGP1)

The bits of the chiplet reset register control the resetting (enabling/disabling) of complete chiplets.

For each bit position:

0 = Reset inactive for this chiplet.

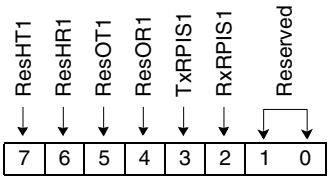
1 = Reset active (chiplet is disabled; DEFAULT).

Length 8 bits

Type Read/Write

Framer Address C00

Power On Reset Value x‘FF’



Bit(s)	Name	Description
7	ResHT1	Reset to chiplet ACH_Tx 1.
6	ResHR1	Reset to chiplet ACH_Rx 1.
5	ResOT1	Reset to chiplet OFP_Tx 1.
4	ResOR1	Reset to chiplet OFP_Rx 1.
3	TxRPIS1	Reset to chiplet PIS_Tx 1.
2	RxRPIS1	Reset to chiplet PIS_Rx 1.
1-0	Reserved	Reserved.

3.23.3.2 Chiplet Reset Register 2 (RESGP2)

The bits of the chiplet reset register control the resetting (enabling/disabling) of complete chiplets.

For each bit position:

0 = Reset inactive for this chiplet

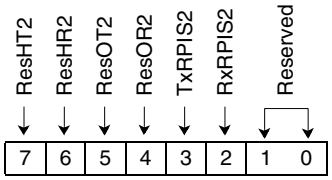
1 = Reset active (chiplet is disabled; DEFAULT).

Length 8 bits

Type Read/Write

Framer Address C01

Power On Reset Value x‘FF’



Bit(s)	Name	Description
7	ResHT2	Reset to chiplet ACH_Tx 2.
6	ResHR2	Reset to chiplet ACH_Rx 2.
5	ResOT2	Reset to chiplet OFP_Tx 2.
4	ResOR2	Reset to chiplet OFP_Rx 2.
3	TxRPIS2	Reset to chiplet PIS_Tx 2.
2	RxRPIS2	Reset to chiplet PIS_Rx 2.
1-0	Reserved	Reserved.

3.23.3.3 Chiplet Interrupt and Mask Registers (IRQGP1 (IRMGP1))

The chiplet interrupt request register indicates pending interrupt requests from individual chiplets. An active bit of this register is reset by removing the cause for the request in the corresponding chiplet or by masking the active IRQ bit(s) in the chiplet; therefore, this register is read only.

For each bit position:

0 = No chiplet interrupt request pending.

1 = Chiplet has pending interrupt request(s). The chiplet interrupt request mask register bits control the propagation of a chiplet interrupt request to the SONET Macro Interrupt output pin. The mask registers allow read and write access.

For each bit position:

0 = The corresponding interrupt request bit is masked (DEFAULT).

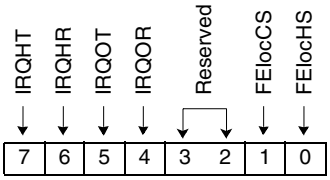
1 = The corresponding interrupt request bit is active (for IRMGP1, the corresponding interrupt request bit activates the SONET Macro Interrupt).

Length 8 bits

Type Read Only

Framer Address C10

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	IRQHT	IRQ from ACH_Tx.
6	IRQHR	IRQ from ACH_Rx.
5	IRQOT	IRQ from OFP_Tx.
4	IRQOR	IRQ from OFP_Rx.
3-2	Reserved	Reserved.
1	FElocCS	Pending clock status error active.
0	FElocHS	Pending handshaking error active.

3.23.3.4 Handshaking Error Indication and Mask Registers (HShake1)

The local handshaking error indication register indicates pending handshaking error requests from the GPPINT chiplets.

For each bit position:

0 = Normal operation of the corresponding chiplet.

1 = The corresponding chiplet did not deassert its DTACK signal.

Exception: The signals TOError and IntError (HShake2(1-0)) have the following meaning: Normal operation GPP deasserts Strobes without waiting for DTACK assertion Watchdog Timeout in REST state Watchdog Timeout in REQ state. An active bit of the handshaking error indication register is reset by removing the cause for the malfunctioning of the chiplet and by writing a '1' into the corresponding bit position. Reading one register will reset all bits of this register if the "clear-register" option is set in ConfGP1(2). The handshaking error indication mask register bits control the propagation of the GPPINT handshaking error request of the register HShake1. HSMask1 controls propagation to the signal FElocHS (bit 0 of IRQGP1 register). The mask registers allow read and write access.

For each bit position:

0 = The corresponding handshaking error indication bit is masked (DEFAULT).

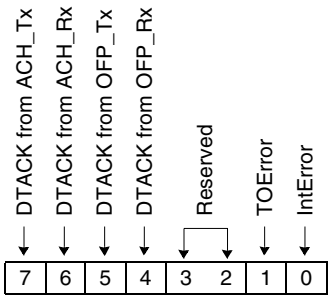
1 = The corresponding request bit is active (for HSMask1, the corresponding request bit activates signal FElocHS (bit 0 of IRQGP1 register). "Clear-register" option set in ConfGP1(2).

Length 8 bits

Type Read/Write

Framer Address C20

Power On Reset Value x'00'



Bit(s)	Name	Description
7	DTACK from ACH_Tx	DTACK from ACH_Tx stuck at ONE.
6	DTACK from ACH_Rx	DTACK from ACH_Rx stuck at ONE.
5	DTACK from OFP_Tx	DTACK from OFP_Tx stuck at ONE.
4	DTACK from OFP_Rx	DTACK from OFP_Rx stuck at ONE.
3-2	Reserved	Reserved.
1	TOError	Time Out Error of the GPP interface (see above).
0	IntError	GPP interface error (see above).

3.23.3.5 Clock Monitor Status and Mask Registers (ClkStat1 (ClkMask1))

The clock monitor status register bits indicate the loss of a specific island's clock. They are set whenever a difference between the clock test signal and the individual island's clock acknowledge signal occurs after the clock monitor test period.

For each bit position:

0 = Normal operation of the corresponding clock island

1 = The corresponding island clock is lost. An active bit of this register is reset by restoring the clock of the corresponding clock island and by writing a one into the corresponding bit position. Reading one register will reset all bits of this register if the "clear-register" option is set in bit ConfGP1(3). The clock monitor mask register ClkMask1 controls the propagation of active clock monitor status signals. ClkMask1 controls propagation to the signal FElocCS (bit 1 of IRQGP1 register). The mask registers allow read and write access.

For each bit position:

0 = The corresponding clock status bit is masked (DEFAULT).

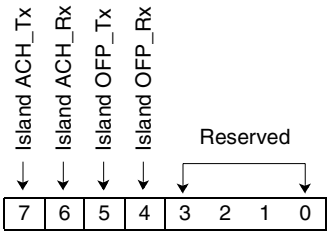
1 = The corresponding clock status bit is active (for ClkMask1, the corresponding bit activates the signal FElocCS (bit 1 of IRQGP1 register).

Length 8 bits

Type Read/Write

Framer Address C30

Power On Reset Value x'00'



Bit(s)	Name	Description
7	Island ACH_Tx	Island ACH_Tx lost clock.
6	Island ACH_Rx	Island ACH_Rx lost clock.
5	Island OFP_Tx	Island OFP_Tx lost clock.
4	Island OFP_Rx	Island OFP_Rx lost clock.
3-0	Reserved	Reserved.

3.23.3.6 Clock Monitor Test Period Register (CMonGP1)

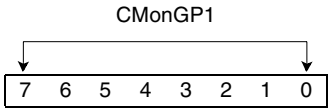
Divider ratio to derive the clock monitor test period from the GPPCLK clock. Clock monitoring is disabled if equal x‘0000 0000’ (DEFAULT).

Length 8 bits

Type Read/Write

Framer Address C48

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	CMonGP1(7-0)	Number of GPPCLK cycles/test period.

3.23.3.7 Watchdog Timer Period Register (WDTGP1)

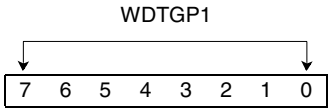
Divider ratio to derive the interface timeout period from the GPPCLK clock. This register is reset to x‘0000 00FF’ whenever a timeout occurs; it has to be reconfigured by a GPP write access.

Length 8 bits

Type Read/Write

Framer Address C49

Power On Reset Value x‘FF’



Bit(s)	Name	Description
7-0	WDTGP1(7-0)	Number of GPPCLK clock cycles per timeout period.

3.23.3.8 GPPINT Local Configuration Registers (ConfGP1)

The bits of this local configuration register control the resetting of complete registers upon read access (“clear register” option).

For each bit position:

0 = No action upon read access.

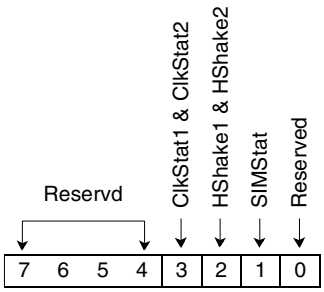
1 = The corresponding register is reset upon read access (DEFAULT).

Length 8 bits

Type Read/Write

Framer Address C4A

Power On Reset Value x‘FF’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	ClkStat1 & ClkStat2	Clear-bit for registers ClkStat1 & ClkStat2.
2	HShake1 & HShake2	Clear-bit for registers HShake1 & HShake2.
1	SIMStat	Clear-bit for register SIMStat.
0	Reserved	Reserved.

3.23.3.9 Vital Macro Data Register (VPD)

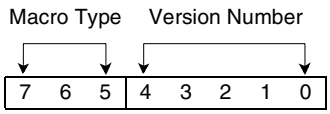
This read-only register displays the macro identification.

Length 8 bits

Type Read Only

Framer Address C50

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-5	Macro type	Macro type (000).
4-0	Version number	Version number.

3.23.3.10 Static Configuration Register (GATMCS)

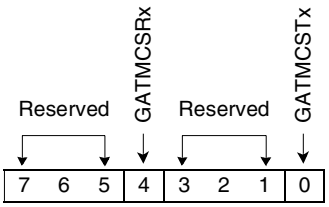
This register shows common static configuration data, providing control signals that are distributed to multiple chiplets. It is set once by the GPP before the individual chiplets get enabled and does not change during normal operation.

Length 8 bits

Type Read/Write

Framer Address C58

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	GATMCSRx	ATM cell or CS mode for SDH macro in receive direction: 0 SDH macro in ATM mode 1 SDH macro in CS mode
3-1	Reserved	Reserved.
0	GATMCSTx	ATM cell or CS mode for SDH macro in transmit direction: 0 SDH macro in ATM mode 1 SDH macro in CS mode

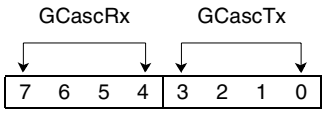
3.23.3.11 GCasc

Length 8 bits

Type Read/Write

Framer Address C59

Power On Reset Value x‘88’



Bit(s)	Name	Description
7-4	GCascRx(7-4)	Defines SDH macros in receive direction: 0001 STS3c 1000 STM1 others Reserved
3-0	GCascTx(7-4)	Defines SDH macros in transmit direction: 0001 STS3c 1000 STM1 others Reserved

3.23.3.12 GLoopTx

Transmit loopback control.

For each bit position:

0 = ACH Loopback disabled (DEFAULT).

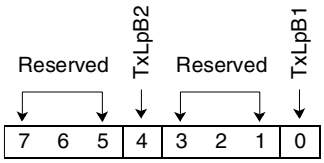
1 = ACH Loopback enabled.

Length 8 bits

Type Read/Write

Framer Address C5A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	TxLpB2	Loopback #2 control, Tx macro.
3-1	Reserved	Reserved.
0	TxLpB1	Loopback #1 control, Tx macro.

3.23.3.13 GLoopRx

Receive loopback control.

For each bit position:

0 = ACH Loopback disabled (DEFAULT).

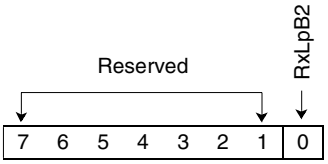
1 = ACH Loopback enabled.

Length 8 bits

Type Read/Write

Framer Address C5B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-1	Reserved	Reserved.
0	RxLpB2	Loopback #2 control, Rx macro.

3.23.3.14 GExtRes

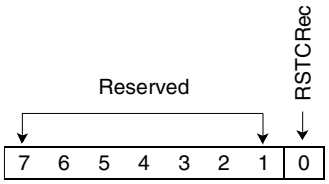
External clock recovery circuit reset signal. Delivered to external circuit (deserializer) via device pins. The active level depends on the external circuit used. Default value at power-on-reset is LOW.

Length 8 bits

Type Read/Write

Framer Address C5C

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-1	Reserved	Reserved.
0	RSTCRec	External recovery reset.

3.23.3.15 OFPTXGP

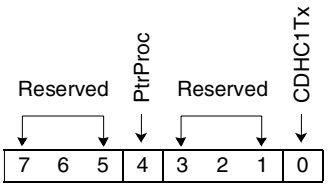
This register shows static configuration data, providing control signals for chiplet OFP_Tx. It is set once by the GPP before the individual chiplets are enabled and does not change during normal operation.

Length 8 bits

Type Read/Write

Framer Address C68

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	PtrProc	0 = AU pointer processing disabled in ATM mode. 1 = AU pointer processing enabled in ATM mode.
3-1	Reserved	Reserved.
0	SDHC1Tx	0 = C1 byte replaced by section trace J1 byte (ITU-T standard) 1 = Old numbering scheme is used. OFPRXGP1 & 2: Static configuration data, providing control signals for chiplets OFP_Rx. Set once by the GPP before the individual chiplets are enabled and not changing during normal operation.

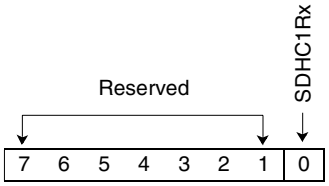
3.23.3.16 OFPRXGP1

Length 8 bits

Type Read/Write

Framer Address C69

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-1	Reserved	Reserved.
0	SDHC1Rx	0 = The new (ITU-T standard) numbering scheme is used. 1 = Old numbering scheme is used.

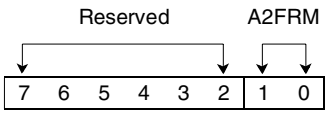
3.23.3.17 OFPRXGP2

Length 8 bits

Type Read/Write

Framer Address C6A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1-0	A2Frm	OFP_Rx RxSoFrm assertion controls: 00 RxSoFrm asserted during 3rd A2 byte 01 RxSoFrm asserted during 1st A2 byte 10 RxSoFrm asserted during 2nd A2 byte 11 RxSoFrm asserted during 3rd A2 byte

3.23.3.18 PIMRConf2

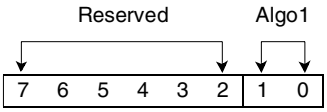
This register shows static configuration data, providing control signals for chiplets PIM_Tx/PIM_Rx. It is set once by the GPP before the individual chiplets are enabled and does not change during normal operation.

Length 8 bits

Type Read/Write

Framer Address C73

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1-0	Algo1(7-6)	Selects frame pattern recognition algorithm: 00 All bits checked; maximum four bad frames 01 12 bits checked; only maximum four bad frames 10 All bits checked; maximum five bad frames 11 12 bits checked only; maximum five bad frames

3.23.3.19 SIMStat

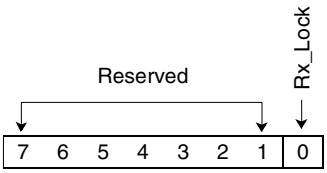
Status register, providing the GPP with information from the SIM chiplet via PIM. Either SIM-internal or external PLL lock status. “Clear-register” option set in ConfGP1(1).

Length 8 bits

Type Read Only

Framer Address C7F

Power On Reset Value N/A



Bit(s)	Name	Description
7-1	Reserved	Reserved.
0	Rx_Lock	0 Rx PLL is still in phase acquisition process 1 Rx PLL is enabled and has locked to the incoming data stream incoming data stream

3.23.4 ATM Cell Handler Registers: Transmit Direction

Table 34: ACH_Tx GPP Handler Address Mapping Base Address = x‘100’

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Counter	ROFmid	Read-on-the-fly register	x‘0’	F 8	‘00000000’
	ROFhi	Read-on-the-fly register (MSByte)	x‘1’	F 8	‘00000000’
	CntEn1	COUNT ENABLE register	x‘2’	X 3	‘000’
	ACBC	Cell counter (read from external FIFO), no threshold[2]	x‘4/5’[2]	N 24	x‘000000’
	IUC	Idle/unassigned cell counter, no threshold[2]	x‘6/7’[2]	N 24	x‘000000’
	ACBE	Corrupted cell error counter[2]	x‘8/9’[2]	N 8	‘00000000’
	ACBETh11	Threshold register for counter ACBE	x‘A’	X 8	‘10000000’
Reset	RESET	Default RESET register	x‘30’	R 2	‘01’
Status	STAT1	Status register #1	x‘33’	S 8	
	IUCSTAT1	Status register #2	x‘34’	S 2	
Interrupt Request and Mask	MainIRQ	MAIN INTerrupt register	x‘38’	I 2	
	M_MainIRQ	INT MASK register (for MainIRQ)	x‘39’	X 2	‘00’
	CntrIRQ1	COUNTER INTerrupt register	x‘3A’	I 4	
	M_CntrIRQ1	INT MASK register (for CntrIRQ1)	x‘3B’	X 4	‘0000’
Configuration	CELLTENABLE	Chiplet configuration register	x‘48’	C 6	‘001111’
	ACBTXTHRPAE	Programmable almost empty threshold	x‘49’	C 7	‘0001110’
	HEADERBYTE1	IU-cell header byte 1[1]	x‘4A’	C 8	‘00000000’
	HEADERBYTE2	IU-cell header byte 2[1]	x‘4B’	C 8	‘00000000’
	HEADERBYTE3	IU-cell header byte 3[1]	x‘4C’	C 8	‘00000000’
	HEADERBYTE4	IU-cell header byte 4[1]	x‘4D’	C 8	‘00000001’
	HEADERBYTE5	IU-cell header byte 5[1]	x‘4E’	C 8	‘01010010’
	PAYLOADBYTE	IU-cell payload byte	x‘4F’	C 8	‘01101010’
	HECENCTRL	HEC processing control	x‘50’	C 7	‘0001100’
	HECOFFSET	HEC offset pattern register	x‘51’	C 8	‘01010101’
	HECMASKAND	HEC error corruption mask (AND)	x‘52’	C 8	‘11111111’
	HECMASKOR	HEC error corruption mask (OR)	x‘53’	C 8	‘00000000’
	SDBTXTHRPAF	Programmable almost full threshold	x‘54’	C 6	‘110000’

1. Defaults according ITU I.432
2. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.

3.23.4.1 ROFmid

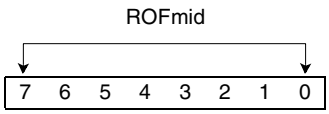
Read-on-the-fly register, middle significant byte.

Length 8 bits

Type Read Only

Framer Address 100

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ROFmid(7-0)	Read-on-the-fly register, middle significant byte.

3.23.4.2 ROFhi

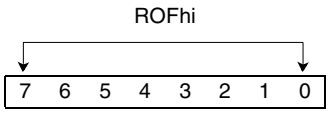
Read-on-the-fly register, most significant byte.

Length 8 bits

Type Read Only

Framer Address 101

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ROFhi(7-0)	Read-on-the-fly register, most significant byte.

3.23.4.3 ACBC

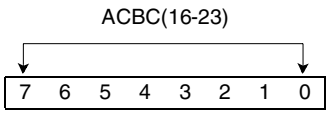
Number of cells read from external FIFO (24-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 104/105

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ACBC(16-23)	External FIFO cell counter, least significant byte.

3.23.4.4 IUC

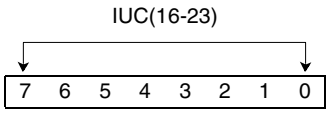
Number of transmitted idle and unassigned cells (24-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 106/107

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	IUC(16-23)	Idle/unassigned cell counter, least significant byte.

3.23.4.5 ACBE

Number of errors (corrupted cell read from external FIFO). Eight-bit counter overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 108/109

Power On Reset Value x‘00’

Bit(s)	Name	Description
7-0	ACBE(7-0)	External FIFO error counter.

3.23.4.6 ACBETh11

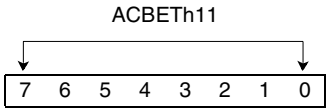
Threshold for number of errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 10A

Power On Reset Value x‘80’



Bit(s)	Name	Description
7-0	ACBETh11(7-0)	Threshold for error counter.

3.23.4.7 CntEn1

Counter On/Off control register for ACH_Tx.

For each bit position:

0 = Counter is disabled.

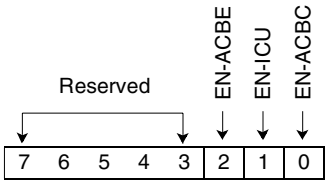
1 = Counter is enabled.

Length 8 bits

Type Read/Write

Framer Address 102

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	EN-ACBE	Error counter enable.
1	EN-IUC	Idle/unassigned cell counter enable.
0	EN-ACBC	Cell counter enable.

3.23.4.8 Reset Register (RESET)

Reset/Halt chiplet control register. This register is automatically preset to the default value by the reset signal ResHT from the GPPINT.

For each bit position:

0 = Reset/Halt not active.

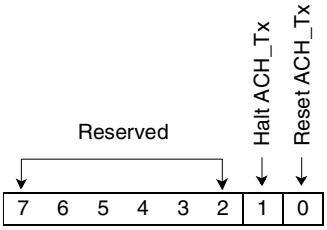
1 = Reset/Halt active.

Length 8 bits

Type Read/Write

Framer Address 130

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	Halt ACH_Tx	Halt (freeze) ACH_Tx chiplet.
0	Reset ACH_Tx	Reset (disable) ACH_Tx chiplet.

3.23.4.9 STAT1

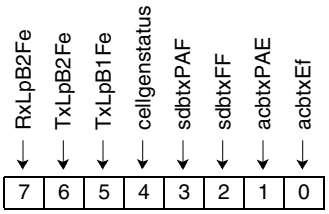
Status register 1 of this chiplet. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 133

Power On Reset Value



Bit(s)	Name	Description
7	RxLpB2Fe	Rx Loopback #2 configuration mismatch.
6	TxLpB2Fe	Tx Loopback #2 configuration mismatch.
5	TxLpB1Fe	Tx Loopback #1 configuration mismatch.
4	cellgenstatus	0 Idle/unassigned cell is transmitted. 1 Cell from external FIFO is transmitted.
3	sdbtxPAF	Programmable almost full flag from SDB_Tx.
2	sdbtxFF	FIFO full flag from SDB_Tx.
1	acbtxPAE	Programmable almost empty flag from External Transmit FIFO.
0	acbtxEf	FIFO empty flag from external Transmit FIFO.

3.23.4.10 IUCSTAT1

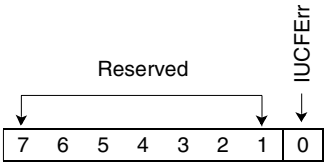
Status register 2 of this chiplet. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 134

Power On Reset Value



Bit(s)	Name	Description
7-1	Reserved	Reserved.
0	IUCFErr	Unexpected state transition in FSM.

3.23.4.11 MainIRQ

This register is used to indicate fatal interrupt events and point to user IRQ registers with active requests.

For each bit position;

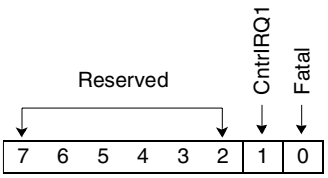
0 = No interrupt request pending.
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 138

Power On Reset Value



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.4.12 M_MainIRQ

This register is used to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

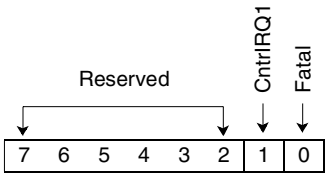
1 = The corresponding pending request bit activates signal IRQHT1 to GPPINT.

Length 8 bits

Type Read/Write

Framer Address 139

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.4.13 CntrIRQ1

This register is used to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

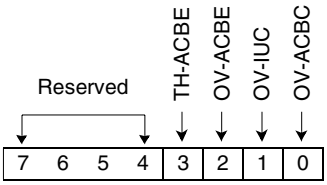
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 13A

Power On Reset Value



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	TH-ACBE	Threshold overstep error counter.
2	OV-ACBE	Overflow error counter.
1	OV-IUC	Overflow idle/unassigned cell counter.
0	OV-ACBC	Overflow cell counter.

3.23.4.14 M_CntrIRQ1

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

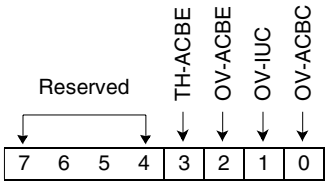
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 13B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	TH-ACBE	Threshold overstep error counter.
2	OV-ACBE	Overflow error counter.
1	OV-IUC	Overflow idle/unassigned cell counter.
0	OV-ACBC	Overflow cell counter.

3.23.4.15 CELLTENABLE

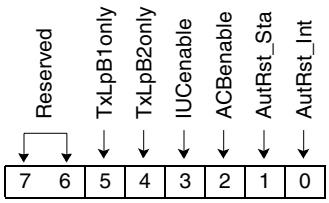
This register is used to control various modes of operation of this chiplet.

Length 8 bits

Type Read/Write

Framer Address 148

Power On Reset Value x‘0F’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	TxLpB1only	0 On-the-fly monitoring (LpB #1) 1 Loopback #1 only
4	TxLpB2only	0 On-the-fly monitoring (LpB #2) 1 Loopback #2 only
3	IUCenable	0 Generation of IUC disabled 1 Generation of IUC enabled
2	ACBenable	0 External FIFO read disabled 1 External FIFO read enabled
1	AutRst_Sta	0 No action on read access 1 Auto-reset status registers upon read access
0	AutRst_Int	0 No action on read access 1 Auto-reset interrupt request registers upon read access

3.23.4.16 ACBTXTHRPAE

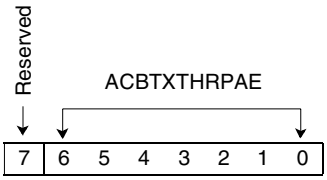
Threshold for Programmable Almost Empty flag of external FIFO in transmit direction.

Length 8 bits

Type Read/Write

Framer Address 149

Power On Reset Value x‘0E’



Bit(s)	Name	Description
7	Reserved	Reserved.
6-0	ACBTXTHRPAE(7-1)	Threshold for PAE flag.

3.23.4.17 SDBTXTHRPAF

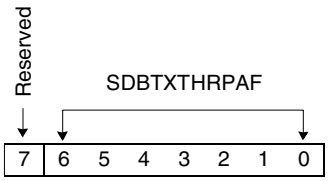
Threshold for Programmable Almost Full flag (SDB_Tx).

Length 8 bits

Type Read/Write

Framer Address 154

Power On Reset Value x‘30’



Bit(s)	Name	Description
7	Reserved	Reserved.
5-0	SDBTXTHRPAF(7-2)	Threshold for PAF flag.

3.23.4.18 HEADERBYTE1

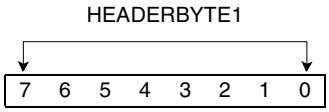
Idle/Unassigned cell header byte 1. Default pattern according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 14A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	HEADERBYTE1(7-0)	IU-cell header byte #1.

3.23.4.19 HEADERBYTE2

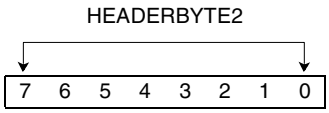
Idle/Unassigned cell header byte 2. Default pattern according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 14B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	HEADERBYTE2(7-0)	IU-cell header byte #2.

3.23.4.20 HEADERBYTE3

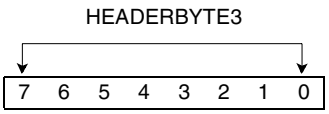
Idle/Unassigned cell header byte 3. Default pattern according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 14C

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	HEADERBYTE3(7-0)	IU-cell header byte #3.

3.23.4.21 HEADERBYTE4

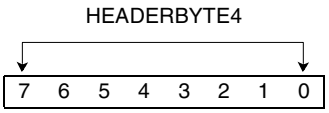
Idle/Unassigned cell header byte 4. Default pattern according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 14D

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-0	HEADERBYTE4(7-0)	IU-cell header byte #4.

3.23.4.22 HEADERBYTE5

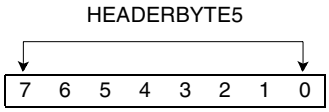
Idle/Unassigned cell header byte 5. Default pattern according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 14E

Power On Reset Value x‘52’



Bit(s)	Name	Description
7-0	HEADERBYTE5(7-0)	IU-cell header byte #5.

3.23.4.23 PAYLOADBYTE

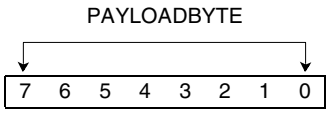
Idle/Unassigned cell payload byte.

Length 8 bits

Type Read/Write

Framer Address 14F

Power On Reset Value x‘6A’



Bit(s)	Name	Description
7-0	PAYLOADBYTE(7-0)	IU-cell payload byte.

3.23.4.24 HECENCTRL

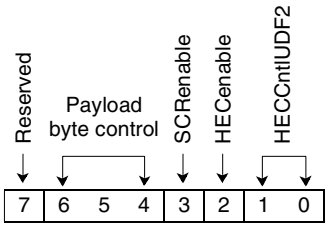
HEC processing control configuration register.

Length 8 bits

Type Read/Write

Framer Address 150

Power On Reset Value x‘0C’



Bit(s)	Name	Description
7	Reserved	Reserved.
6-4	Payload byte control	000 Each payload byte is the same (default) 001 Increment payload byte for each ATM cell, start with default after reset 010 Increment each payload byte of a cell; start each cell with default byte 011 Increment each PL byte of a cell; cross cell boundaries; start first cell after reset with default byte 1xx Each payload byte is the same
3	SCRenable	0 ATM cell payload scrambling disabled 1 ATM cell payload scrambling enabled
2	HECenable	0 HEC calculation/manipulation disabled 1 HEC calculation/manipulation enabled
1-0	HECCntlUDF2	Mode of final HEC manipulation by UDF1 byte after HECOffset, HECMaskAND, HEC-MaskOR operations: 00 No manipulation 01 HEC XOR UDF1 10 HEC AND UDF1 11 HEC OR UDF1

3.23.4.25 HECOFFSET

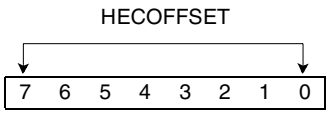
HEC offset pattern register for the byte pattern used in the ATM cell header HEC calculation as base offset according to ITU I.432.

Length 8 bits

Type Read/Write

Framer Address 151

Power On Reset Value x‘55’



Bit(s)	Name	Description
7-0	HECOFFSET(7-0)	HEC offset pattern.

3.23.4.26 HECMASKAND

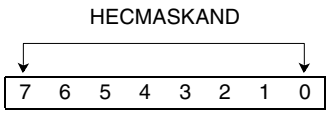
HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ANDing) HEC error corruption mask.

Length 8 bits

Type Read/Write

Framer Address 152

Power On Reset Value x‘FF’



Bit(s)	Name	Description
7-0	HECMASKAND(7-0)	HEC error corruption mask (AND).

3.23.4.27 HECMASKOR

HEC mask pattern register for the byte pattern used in the ATM cell header HEC calculation as dedicated (ORing) HEC error corruption mask.

Length 8 bits

Type Read/Write

Framer Address 153

Power On Reset Value x‘00’

Bit(s)	Name	Description
7-0	HECMASKOR(7-0)	HEC error corruption mask (OR).

3.23.5 ATM Cell Handler Registers: Receive Direction

Table 35: ACH_Rx GPP Handler Address Mapping Base Address = x‘200’

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Counter	ROFmid	Read-on-the-fly register	x‘0’	F 8	‘00000000’
	ROFhi	Read-on-the-fly register (MSByte)	x‘1’	F 8	‘00000000’
	CntEn1	COUNT ENABLE register	x‘2’	X 4	‘0000’
	FHR	Counter, ATM cells written into external FIFO, no threshold	x‘4/5’[1]	N 24	x‘000000’
	IHR	Counter, received Idle cells from OFP, no threshold	x‘6/7’[1]	N 24	x‘000000’
	EHR1	Counter, detected HEC errors with threshold	x‘8/9’[1]	N 16	x‘0000’
	EHR1Th12	Threshold reg Byte2 (LSByte) for counter EHR1	x‘A’	X 8	‘00000001’
	EHR1Th11	Threshold reg Byte1 for counter EHR1	x‘B’	X 8	‘10000000’
	BHR	Counter, FIFO full discarded cells: (DiscPAF1=1) AND (TxLpB11=0) with threshold.[1]	x‘C/D’[1]	N 16	x‘0000’
	BHRTh12	Threshold reg Byte2 (LSByte) for counter BHR	x‘E’	X 8	‘00000001’
	BHRTh11	Threshold register Byte1 for counter BHR	x‘F’	X 8	‘10000000’
Reset	RESET	Default RESET register	x‘30’	R 2	‘01’
Command	CMD1	Command register (FIFO reset)	x‘31’	O 2	‘00’
Status	STAT2	Status register	x‘34’	S 6	
Interrupt	MainIRQ	MAIN INTerrupt register	x‘38’	I 2	
	M_MainIRQ	INTerrupt MASK register (for MainIRQ)	x‘39’	X 2	‘00’
	CntrIRQ1	COUNTER INTerrupt register	x‘3A’	I 6	
	M_CntrIRQ1	INTerrupt MASK register (for CntrIRQ1)	x‘3B’	X 6	‘000000’
Configuration	CONF5	Chiplet configuration register	x‘48’	C 8	‘00000011’
	CONF6	Chiplet configuration register (Alpha/Delta)	x‘49’	C 8	‘01100101’
	H1CONF	Confirmation bytes to identify idle or unassigned cells.	x‘4B’	C 8	‘00000000’
	H2CONF	Confirmation bytes to identify idle or unassigned cells.	x‘4C’	C 8	‘00000000’
	H3CONF	Confirmation bytes to identify idle or unassigned cells.	x‘4D’	C 8	x‘0000 0000’
	H4CONF	Confirmation bytes to identify idle or unassigned cells.	x‘4E’	C 8	‘00000001’
	H5CONF	Dummy byte to align Payload in external FIFO	x‘50’	C 8	‘11010000’
	CONFC	External FIFO buffer Almost Full threshold	x‘51’	C 7	‘1100000’

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.

3.23.5.1 ROFmid

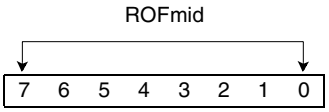
Read-on-the-fly registers, middle significant byte.

Length 8 bits

Type Read Only

Framer Address 200

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ROFmid(7-0)	Read-on-the-fly register, middle significant byte.

3.23.5.2 ROFhi

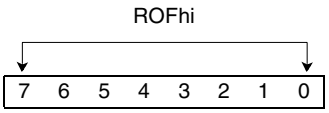
Read-on-the-fly registers, most significant byte.

Length 8 bits

Type Read Only

Framer Address 201

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ROFhi(7-0)	Read-on-the-fly register, most significant byte.

3.23.5.3 FHR

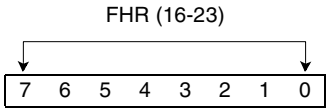
Number of ATM cells written into external FIFO (24-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 204/205

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	FHR(16-23)	ATM cell counter, least significant byte.

3.23.5.4 IHR

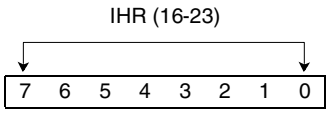
Number of idle cells received from OFP_Rx (24-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 206/207

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	IHR(16-23)	Idle/unassigned cell counter, least significant byte.

3.23.5.5 EHR1

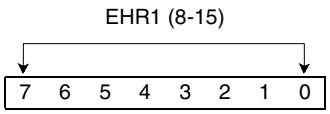
Number of detected HEC errors (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 208/209

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	EHR1(8-15)	HEC error counter, least significant byte.

3.23.5.6 EHR1Th11

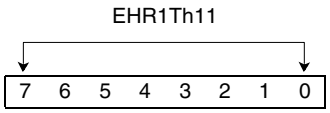
Threshold for number of HEC cells, most significant byte.

Length 8 bits

Type Read/Write

Framer Address 20B

Power On Reset Value x‘80’



Bit(s)	Name	Description
7-0	EHR1Th11(7-0)	Threshold for HEC error counter, most significant byte.

3.23.5.7 EHT1Th12

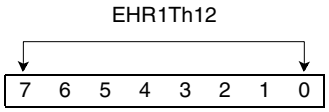
Threshold for number of HEC errors (least significant byte). Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 207

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-0	EHR1Th12(7-0)	Threshold for HEC error counter, least significant byte.

3.23.5.8 BHR

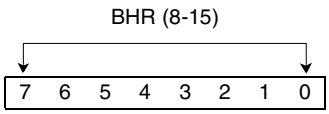
Number of discarded cells because of FIFO full condition (16 bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 20C/20D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	BHR(8-15)	Discarded cell counter, least significant byte.

3.23.5.9 BHRTh11

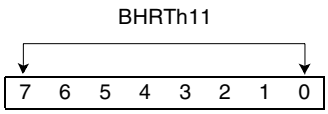
Threshold for number of discarded cells, most significant byte.

Length 8 bits

Type Read/Write

Framer Address 20F

Power On Reset Value x‘80’



Bit(s)	Name	Description
7-0	BHRTh11(7-0)	Threshold for discarded cell counter, most significant byte.

3.23.5.10 BHRTh12

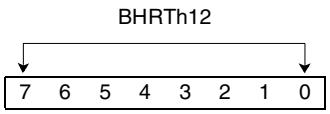
Threshold for number of discarded cells (least significant byte). Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 20E

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-0	BHRTh12(7-0)	Threshold for discarded cell counter, least significant byte.

3.23.5.11 CntEn1

Counter On/Off control register for ACH_Rx.

For each bit position:

0 = Counter is disabled.

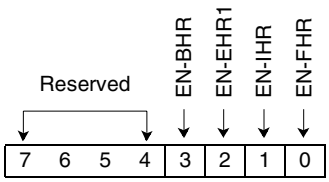
1 = Counter is enabled.

Length 8 bits

Type Read/Write

Framer Address 202

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	EN-BHR	Discarded cell counter enable.
2	EN-EHR1	HEC error counter enable.
1	EN-IHR	Idle cell counter enable.
0	EN-FHR	ATM cell counter enable.

3.23.5.12 Reset Register (RESET)

Reset/Halt chiplet control register. This register is preset automatically to the default value by the reset signal ResHR from the GPPINT.

For each bit position:

0 = Reset/Halt not active.

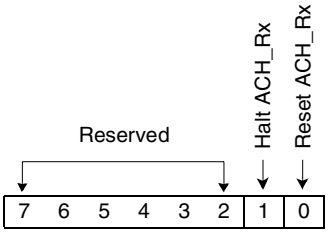
1 = Reset/Halt active.

Length 8 bits

Type Read/Write

Framer Address 230

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	Halt ACH_Rx	Halt (freeze) ACH_Rx chiplet.
0	Reset ACH_Rx	Reset (disable) ACH_Rx chiplet.

3.23.5.13 Command Register (CMD1)

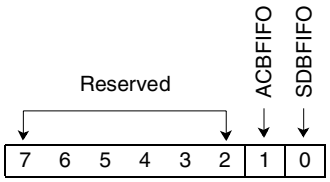
Command register for this chiplet. Single-cycle active if '1' is written into bit position.

Length 8 bits

Type Read/Write

Framer Address 231

Power On Reset Value x'00'



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	ACBFIFO	Reset External FIFO.
0	SDBFIFO	Reset SDB_Rx FIFO.

3.23.5.14 Status Register (STAT2)

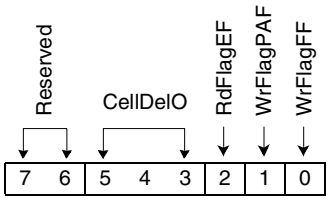
Status register of this chiplet. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 234

Power On Reset Value -



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5-3	CellDelO	State of the cell delineation process: 000 Reset state 001 Hunt state 010 Presync state 100 Sync state

Bit(s)	Name	Description
2	RdFlagEF	SDB FIFO: Read FIFO Empty Flag.
1	WrFlagPAF	External FIFO: Write FIFO programmable almost full flag.
0	WrFlagFF	External FIFO: Write FIFO Full flag.

3.23.5.15 MainIRQ

This register is used to indicate fatal interrupt events and point to user IRQ registers with active requests.

For each bit position:

0 = No interrupt request pending.

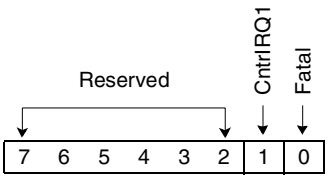
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 238

Power On Reset Value



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.5.16 M_MainIRQ

This register is used to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

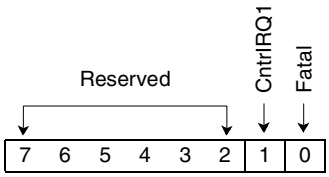
1 = The corresponding pending request bit activates signal IRQHR1 to GPPINT.

Length 8 bits

Type Read/Write

Framer Address 239

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.5.17 CntrIRQ1

This register is used to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

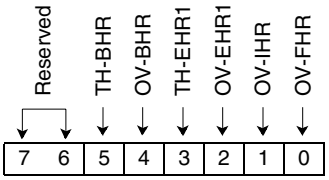
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 240

Power On Reset Value



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	TH-BHR	Threshold overstep discarded cell counter.
4	OV-BHR	Overflow discarded cell counter.
3	TH-EHR1	Threshold overstep HEC error counter.
2	OV-EHR1	Overflow HEC error counter.
1	OV-IHR	Overflow idle cell counter.
0	OV-FHR	Overflow ATM cell counter.

3.23.5.18 M_CntrIRQ1

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

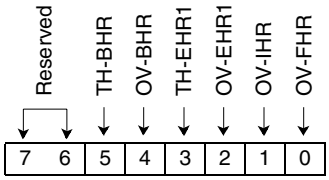
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 241

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	TH-BHR	Threshold overstep discarded cell counter.
4	OV-BHR	Overflow discarded cell counter.
3	TH-EHR1	Threshold overstep HEC error counter.
2	OV-EHR1	Overflow HEC error counter.
1	OV-IHR	Overflow idle cell counter.
0	OV-FHR	Overflow ATM cell counter.

3.23.5.19 CONF5

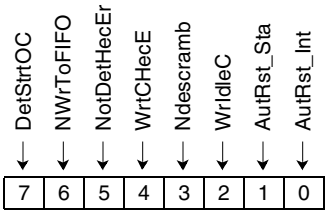
This register is used to control various modes of operation of this chiplet.

Length 8 bits

Type Read/Write

Framer Address 248

Power On Reset Value x‘03’



Bit(s)	Name	Description
7	DetStrtOC	0 Do not detect start of cell. 1 Detect start of cell.
6	NWrToFIFO	0 Write into ACB FIFO. 1 Do not write into ACB FIFO; all received cells are discarded.
5	NotDetHecEr	0 Detect ATM cell with HEC errors. 1 Do not detect ATM cell with HEC errors.
4	WrtCHecE	0 Do not write ATM cell with HEC errors. 1 Write ATM cell with HEC errors.
3	Ndescramb	0 Descramble ATM cell payload. 1 Do not descramble ATM cell payload.
2	WrIdleC	0 Do not write Idle cell into external FIFO. 1 Write Idle cell into ACB FIFO.
1	AutRst_Sta	0 No action on read access. 1 Auto-reset status register upon read access.
0	AutRst_Int	0 No action on read access. 1 Auto-reset interrupt request registers upon read access.

3.23.5.20 CONF6

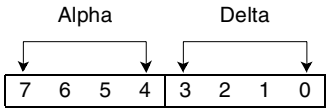
This register is used to control ATM cell synchronization in this chiplet.

Length 8 bits

Type Read/Write

Framer Address 249

Power On Reset Value x‘65’



Bit(s)	Name	Description
7-4	Alpha(7-4)	Required number of consecutive false HEC detected to return from SYNC to HUNT state.
3-0	Delta(7-4)	Required number of consecutive good HEC detected to jump from PRESYNC to SYNC state.

3.23.5.21 CONFC

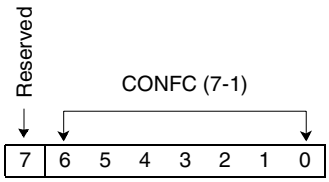
Threshold for Programmable Almost Full flag of the external FIFO.

Length 8 bits

Type Read/Write

Framer Address 251

Power On Reset Value x‘60’



Bit(s)	Name	Description
7	Reserved	Reserved.
6-0	CONFC(7-1)	Threshold for PAF flag HEADERBYTE1/2/3/4/5: Idle/Unassigned cell header bytes, default pattern according to ITU I.432.

3.23.5.22 H1CONF

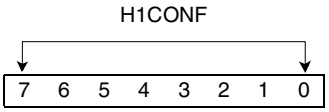
Header pattern #1 to identify idle/unassigned cells.

Length 8 bits

Type Read/Write

Framer Address 24B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	H1CONF(7-0)	Header byte #1.

3.23.5.23 H2CONF

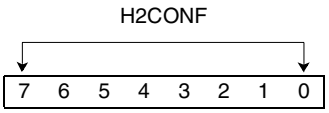
Header pattern #2 to identify idle/unassigned cells.

Length 8 bits

Type Read/Write

Framer Address 24C

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	H2CONF(7-0)	Header byte #2.

3.23.5.24 H3CONF

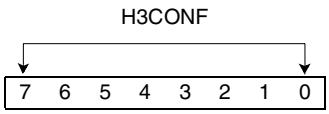
Header pattern #3 to identify idle/unassigned cells.

Length 8 bits

Type Read/Write

Framer Address 24D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	H3CONF(7-0)	Header byte #3.

3.23.5.25 H4CONF

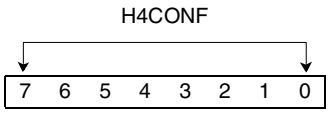
Header pattern #4 to identify idle/unassigned cells.

Length 8 bits

Type Read/Write

Framer Address 24E

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-0	H4CONF(7-0)	Header byte #4.

3.23.5.26 H5CONF

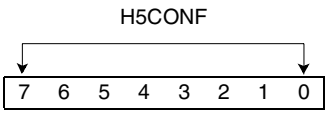
Dummy byte to align the Payload in the ACB_Rx buffer.

Length 8 bits

Type Read/Write

Framer Address 250

Power On Reset Value x‘D0’



Bit(s)	Name	Description
7-0	H5CONF(7-0)	Payload alignment byte.

3.23.6 Overhead Frame Processor Architecture: Transmit Direction

Table 36: OFP_Tx GPP Handler Address Mapping Base Address = x‘400’ (Page 1 of 3)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Counter	CntEn1	COUNT ENABLE register	x‘2’	X 4	‘0000’
	PTRINC	Pointer increment event counter, no threshold[1]	x‘4/5’[1]	N 8	‘00000000’
	PTRDEC	Pointer decrement event counter, no threshold[1]	x‘6/7’[1]	N 8	‘00000000f’
	ND_EVCNT	New data event counter, no threshold[1]	x‘8/9’[1]	N 8	‘00000000’
	JUSCNT	Justification error counter with no threshold[1]	x‘A/B’[1]	N 8	‘00000000’
	JUSCNTTh11	Threshold register for counter JUSCNT	x‘C’	X 8	‘10000000’
Reset	RESET	Default RESET register	x‘30’	R 2	‘01’
Command	CMD1	Njus, Pjus, NDF	x‘31’	O 3	‘000’
Status	STAT1	Init, hug, mode(7-5)	x‘33’	S 6	
	STAT2	Njus, Pjus, NDF	x‘34’	S 3	
Interrupt and Mask	MainIRQ	MAIN INTerrupt register	x‘38’	I 3	
	M_MainIRQ	INTerrupt MASK register (for MainIRQ)	x‘39’	X 3	‘000’
	CntrIRQ1	COUNTER INTerrupt register	x‘3A’	I 5	
	M_CntrIRQ1	INTerrupt MASK register (for CntrIRQ1)	x‘3B’	X 5	‘00000’
	IRQ3	USER INTerrupt register	x‘3C’	I 6	
	M_IRQ3	INTerrupt MASK register (for IRQ3)	x‘3D’	X 6	‘000000’
Configuration	CONF1	Configuration register #1 (general A)	x‘48’	C 8	‘00000011’
	CONF2	Configuration register #2 (general B)	x‘49’	C 3	’000’
	CONF3	Configuration register #3 (fscr reload pattern)	x‘4A’	C 8	’11111110’
	CONF4	Configuration register #4 (errmask)	x‘4B’	C 8	’00000000’
	CONF5	Configuration register #5 (erraddress)	x‘4C’	C 8	’00000000’
	CONF6	Configuration register #6 (fscr control)	x‘4D’	C 8	’00000001’
	CONF7	Configuration register #7 (DCC control)	x‘4E’	C 4	’0000’
	CONF8	Configuration register #8 (ThrLoW)	x‘4F’	C 6	’000011’
	CONF9	Configuration register #9 (ThrNoW)	x‘50’	C 6	’010001’
	CONF10	Configuration register #10 (ThrHiW)	x‘51’	C 6	’100000’
Debug	SOH-A11	First A1	x‘100’	8	
	SOH-A12	Second1 A1	x‘101’	8	
	SOH-A13	Third A1	x‘102’	8	
	SOH-A21	First A2	x‘103’	8	
	SOH-A22	Second A2	x‘104’	8	
	SOH-A23	Third A2	x‘105’	8	
	SOH-J0	J0	x‘106’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8 GRA. Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16-byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 36: OFP_Tx GPP Handler Address Mapping Base Address = x‘400’ (Page 2 of 3)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Debug		Reserved for national use and not included in frame scrambling	x‘107-8’	8	
	SOH-B1	B1	x‘109’	8	
		Media dependant bytes	x‘10A-B’	8	
	SOH-E1	E1	x‘10C’	8	
		Media dependant byte	x‘10D’	8	
		Reserved for future standardization	x‘10E’	8	
	SOH-F1	F1	x‘10F’	8	
		Reserved for national use	x‘110-11’	8	
	SOH-D1	D1	x‘112’	8	
		Media dependant bytes	x‘113-14’	8	
	SOH-D2	D2	x‘115’	8	
		Media dependant byte	x‘116’	8	
		Reserved for future standardization	x‘117’	8	
	SOH-D3	D3	x‘118’	8	
		Reserved for future standardization	x‘119-1A’	8	
	SOH-H1	H1	x‘11B’	8	
	SOH-J0		x‘11C-1D’	8	‘1001SS11’ with S unspecified
	SOH-H2	H2	x‘11E’	8	
	SOH-1s	x‘FF’	x‘11F-20’	8	
	SOH-H31	First H3	x‘121’	8	
	SOH-H32	Second H3	x‘122’	8	
	SOH-H23	Third H3	x‘123’	8	
	SOH-B21	First B2	x‘124’	8	
	SOH-B22	Second B2	x‘125’	8	
	SOH-B23	Third B2	x‘126’	8	
	SOH-K1	K1	x‘127’	8	
		Reserved for future standardization	x‘128-29’	8	
	SOH-K2	K2	x‘12A ’	8	
		Reserved for future standardization	x‘12B-2C’	8	
	SOH-D4	D4	x‘12D’	8	
		Reserved for future standardization	x‘12E-2F’	8	
	SOH-D5	D5	x‘130’	8	
		Reserved for future standardization	x‘131-32’	8	
	SOH-D6	D6	x‘133’	8	
		Reserved for future standardization	x‘134-35’	8	
	SOH-D7	D7	x‘136’	8	
		Reserved for future standardization	x‘137-38’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8 GRA. Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16-byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 36: OFP_Tx GPP Handler Address Mapping Base Address = x‘400’ (Page 3 of 3)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Debug	SOH-D8	D8	x‘139’	8	
		Reserved for future standardization	x‘13A-3B’	8	
	SOH-D9	D9	x‘13C’	8	
		Reserved for future standardization	x‘13D-3E’	8	
	SOH-D10	D10	x‘13F’	8	
		Reserved for future standardization	x‘140-41’	8	
	SOH-D11	D11	x‘142’	8	
		Reserved for future standardization	x‘143-44’	8	
	SOH-D12	D12	x‘145’	8	
		Reserved for future standardization	x‘146-47’	8	
	SOH-S1	S1	x‘148’	8	
	SOH-Z11	Reserved for future standardization	x‘149-4C’	8	
	SOH-M1	M1	x‘14D’	8	
	SOH-M1	E2	x‘14E’	8	
		Reserved for future standardization	x‘14F-50’	8	
		Justification stuff bytes	x‘151-53’	8	
	POH-J1	J1	x‘154’	8	
	POH-B3	B3	x‘155’	8	
	POH-C2	C2	x‘156’	8	
	POH-G1	G1	x‘157’	8	
	POH-F2	F2	x‘158’	8	
	POH-H4	H4	x‘159’	8	
	POH-F3	F3	x‘15A’	8	
	POH-K3	K3	x‘15B’	8	
	x‘POH-N1’	N1	15C	8	
		Reserved	x‘15D-5F’	8	
	POH-J0-16	16 byte J0 section trace	x‘160-6F’	8	
		Reserved	x‘170-7F’	8	
	POH-J1-16	16-byte J1 path trace[3]	x‘180-8F’	8	
	POH-J1-64	64-byte J1 path trace[3]	x‘190-BF’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8 GRA. Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16-byte addresses of 16 byte J1 path trace to map a full 64 byte space.

3.23.6.1 PTRINC

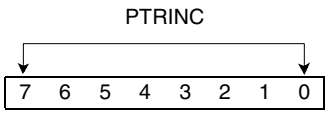
Number of pointer increment events (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 404/405

Power On Reset Value x'00'



Bit(s)	Name	Description
7-0	PTRINC(7-0)	Pointer increment counter.

3.23.6.2 PTRDEC

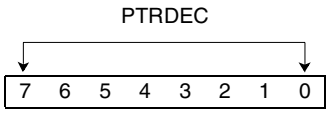
Number of pointer decrement events (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 406/407

Power On Reset Value x'00'



Bit(s)	Name	Description
7-0	PTRDEC(7-0)	Pointer decrement counter.

3.23.6.3 ND_EVCNT

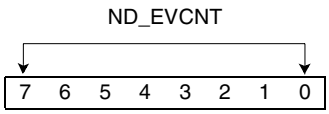
Number of new data events (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 408/409

Power On Reset Value x'00'



Bit(s)	Name	Description
7-0	ND_EVCNT(7-0)	New data event counter.

3.23.6.4 JUSCNT

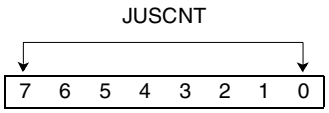
Number of justification errors detected (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 40A/40B

Power On Reset Value x'00'



Bit(s)	Name	Description
7-0	JUSCNT(7-0)	Justification error counter.

3.23.6.5 JUSCNTTh11

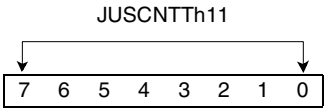
Threshold for number of justification errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 40C

Power On Reset Value x'80'



Bit(s)	Name	Description
7-0	JUSCNTTh11(7-0)	Threshold for justification error counter.

3.23.6.6 CntEn1

Counter On/Off control register for OFP_Tx.

For each bit position:

0 = Counter is disabled.

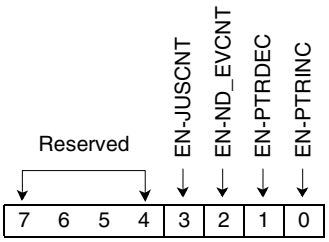
1 = Counter is enabled.

Length 8 bits

Type Read/Write

Framer Address 402

Power On Reset Value x'00'



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	EN-JUSCNT	Justification error counter enable.
2	EN-ND_EVCNT	New data event counter enable.
1	EN-PTRDEC	Pointer decrement counter enable.
0	EN-PTRINC	Pointer increment counter enable.

3.23.6.7 Reset Register (RESET)

Reset/Halt chiplet control register. This register is preset automatically to the default value by the reset signal ResOT coming from GPPINT chiplet.

For each bit position:

0 = Reset/Halt not active.

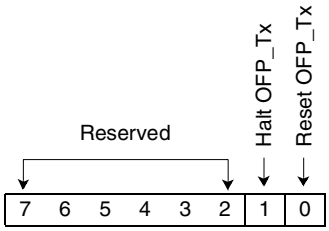
1 = Reset/Halt active.

Length 8 bits

Type Read/Write

Framer Address 430

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	Halt OFP_Tx	Halt (freeze) OFP_Tx chiplet.
0	Reset OFP_Tx	Reset (disable) OFP_Tx chiplet.

3.23.6.8 Command Register (CMD1)

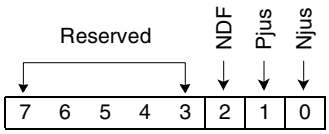
Command register for the chiplet. Single-cycle active if ‘1’ is written into bit position.

Length 8 bits

Type Read/Write

Framer Address 431

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	NDF	Force a start-of-new-VC-4 event.

Bit(s)	Name	Description
1	Pjus	Perform a positive frequency justification.
0	Njus	Perform a negative frequency justification.

3.23.6.9 STAT1

Status register #1 of the chiplet. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 433

Power On Reset Value x‘00’

Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	HUG	0 Higher order unequipped generator inactive. 1 Higher order unequipped generator active.
0	Init	0 Default GRA initialization not completed. 1 Default GRA initialization completed.

3.23.6.10 STAT2

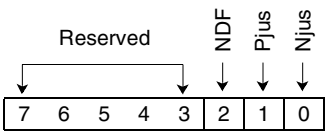
Status register #2 of the chiplet. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 434

Power On Reset Value -



Bit(s)	Name	Description
7-3	Reserved	Reserved.

Bit(s)	Name	Description
2	NDF	0 No NDF transmitted. 1 NDF transmitted.
1	Pjus	0 No positive frequency justification transmitted. 1 Positive frequency justification transmitted.
0	Njus	0 No negative frequency justification transmitted. 1 Negative frequency justification transmitted.

3.23.6.11 MainIRQ

This register is used to indicate fatal interrupt events and to point to user IRQ registers with active requests.

For each bit position:

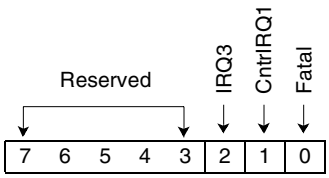
0 = No interrupt request pending.
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 438

Power On Reset Value



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	IRQ3	Active request in IRQ3 register.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.6.12 M_MainIRQ

This register is used to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

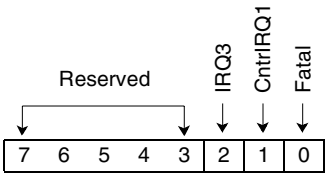
1 = The corresponding pending request bit activates signal IRQOT to GPPINT.

Length 8 bits

Type Read/Write

Framer Address 439

Power On Reset Value x'00'



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	IRQ3	Active request in IRQ3 register.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.6.13 CntrIRQ1

This register is used to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

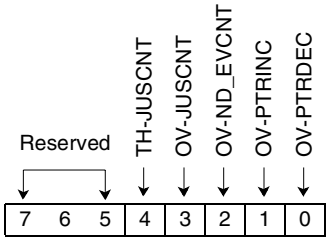
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 43A

Power On Reset Value



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	TH-JUSCNT	Threshold overstep justification error counter.
3	OV-JUSCNT	Overflow justification error counter.
2	OV-ND_EVCNT	Overflow new data event counter.
0	OV-PTRINC	Overflow pointer increment counter.
1	OV-PTRDEC	Overflow pointer decrement counter.

3.23.6.14 M_CntrIRQ1

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

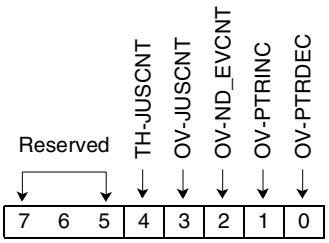
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 43B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	TH-JUSCNT	Threshold overstep justification error counter.
3	OV-JUSCNT	Overflow justification error counter.
2	OV-ND_EVCNT	Overflow new data event counter.
0	OV-PTRINC	Overflow pointer increment counter.
1	OV-PTRDEC	Overflow pointer decrement counter.

3.23.6.15 IRQ3

This register is used to indicate active user interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

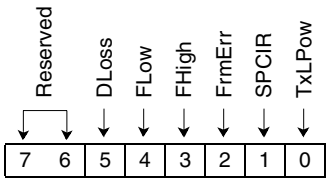
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 43C

Power On Reset Value



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	DLoss	Data loss = Data FIFO empty.
4	FLow	FIFO low threshold overflow.
3	FHigh	FIFO high threshold overflow.
2	FrmErr	Framing error detected.
1	SPCIR	SPC FSM interrupt request.
0	TxLPow	Low Power indication from Optical/Electrical module.

3.23.6.16 M_IRQ3

This register is used to mask pending user interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

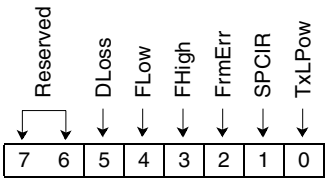
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 43D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	DLoss	Data loss = Data FIFO empty.
4	FLow	FIFO low threshold overflow.
3	FHigh	FIFO high threshold overflow.
2	FrmErr	Framing error detected.
1	SPCIR	SPC FSM interrupt request.
0	TxLPow	Low Power indication from Optical/Electrical module.

3.23.6.17 CONF1

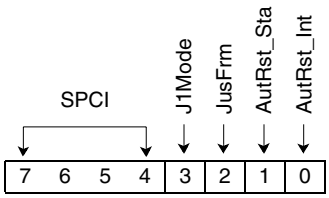
Configuration register #1. General OFP_Tx configuration signals A.

Length 8 bits

Type Read/Write

Framer Address 448

Power On Reset Value x‘03’



Bit(s)	Name	Description
7-4	SPCI(7-4)	Specifies STM-N row number in which an interrupt request will be issued.
3	J1Mode	0 Transmit 16-byte J1 path trace. 1 Transmit 64-byte J1 path trace.
2	JusFrm	0 Allow pointer modification to be performed on frame-to-frame basis. 1 Enforces three frames being interleaved between two pointer modification operations.
1	AutRst_Sta	0 No action on read access. 1 Auto-reset status register upon read access.
0	AutRst_Int	0 No action on read access. 1 Auto-reset interrupt request registers upon read access.

3.23.6.18 CONF2

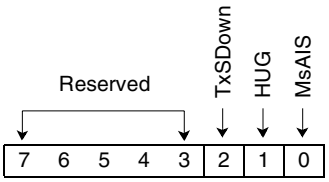
Configuration register #2. General OFP_Tx configuration signals B.

Length 8 bits

Type Read/Write

Framer Address 449

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	TxSDown	Directly connected to output pin: 0 Optical/Electrical normal operation 1 Transmit shutdown for Optical/Electrical module
1	HUG	0 No unequipped STM-N signal 1 Enforce unequipped STM-N signal
0	MsAIS	0 No multiplex section AIS 1 Enforce multiplex section AIS

3.23.6.19 CONF3

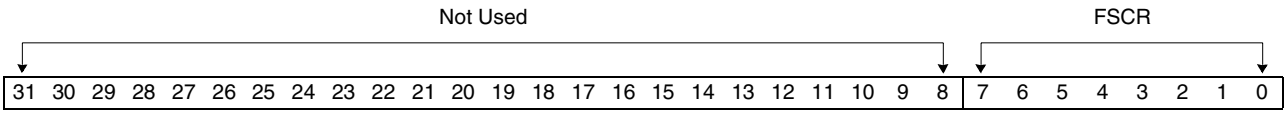
Configuration register #3.

Length 32 bits

Type Read/Write

Framer Address 44A

Power On Reset Value x‘FE’



Bit(s)	Name	Description
31-0	Not used	Not used.
7-0	FSCR(7-0)	Reload pattern for frame scrambler.

3.23.6.20 CONF4

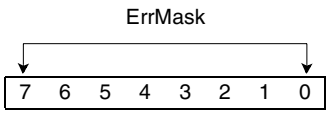
Configuration register #4.

Length 8 bits

Type Read/Write

Framer Address 44B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ErrMask(7-0)	Mask register forcing bit error insertion. XORed with retrieved SOH/POH.

3.23.6.21 CONF5

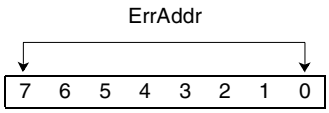
Configuration register #5.

Length 8 bits

Type Read/Write

Framer Address 44C

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ErrAddr(7-0)	Error mask address register. Indicates address of SOH/POH byte to be corrupted.

3.23.6.22 CONF6

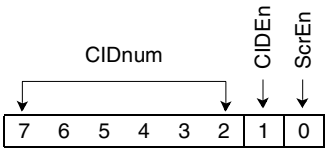
Configuration register #6. Frame scrambling control register.

Length 8 bits

Type Read/Write

Framer Address 44D

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-2	CIDnum(7-2)	Number of all - ‘1’/‘0’ bytes
1	CIDEn	CID Insertion Enable: 0 No CID insertion 1 Perform CID insertion
0	ScrEn	Scramble Enable: 0 No scrambling 1 Perform scrambling

3.23.6.23 CONF7

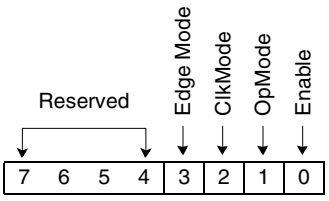
Configuration register #7. DCC control register.

Length 8 bits

Type Read/Write

Framer Address 44E

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	EdgeMode	0 Active falling edge. 1 Actlve rising edge.

Bit(s)	Name	Description
2	ClkMode	0 Continuous clock. 1 Strobed clock.
1	OpMode	0 DCC1 channel (D1 - D3). 1 CC2 channel (D4 - D12).
0	Enable	0 Disable DCC1 processing. 1 Enable DCC1 processing.

3.23.6.24 CONF8

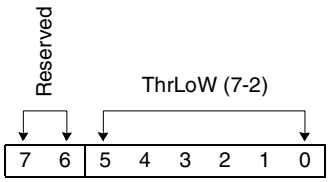
Configuration register #8. Low water FIFO threshold register.

Length 8 bits

Type Read/Write

Framer Address 44F

Power On Reset Value x‘03’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5-0	ThrLoW(7-2)	Low Water FIFO threshold; default value is three.

3.23.6.25 CONF9

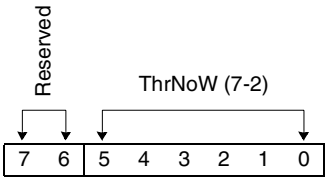
Configuration registers #9. Normal water FIFO threshold register.

Length 8 bits

Type Read/Write

Framer Address 450

Power On Reset Value x‘11’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5-0	ThrNoW(7-2)	Normal Water FIFO threshold; default value is 17.

3.23.6.26 CONF10

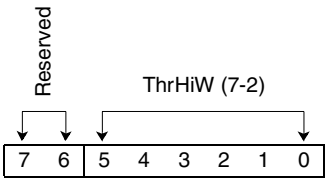
Configuration registers #10. High water FIFO threshold register.

Length 8 bits

Type Read/Write

Framer Address 451

Power On Reset Value x‘20’



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5-0	ThrHiW(7-2)	High Water FIFO threshold; default value is 32.

3.23.7 Overhead Frame Processor Architecture: Receive Direction

Table 37: OFP_Rx GPP Handler Address Mapping Base Address = x‘800’ (Page 1 of 5)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Counter	ROFmid	Read-on-the-fly register	x‘0’	F 8	‘00000000’
	CntEn1	COUNT ENABLE register #1	x‘2’	X 8	‘00000000’
	CntEn2	COUNT ENABLE register #2	x‘3’	X 3	‘000’
	B1BITCNT	BIP-8 B1 bit error counter	x‘4/5’[1]	N 16	x‘0000’
	B1BITCNTTh12	Threshold register Byte2 (least significant byte) for B1BITCNT	x‘6’	X 8	‘00000000’
	B1BITCNTTh11	Threshold register Byte1 for counter B1BITCNT	x‘7’	X 8	‘01111101’
	B1BLKCNT	BIP-8 B1 block error counter[1])	x‘8/9’[1]	N 16	x‘0000’
	B1BLKCNTTh12	Threshold register Byte2 (least significant byte) for B1BLKCNT	x‘A’	X 8	‘00000000’
	B1BLKCNTTh11	Threshold register Byte1 for counter B1BLKCNT	x‘B’	X 8	‘01111101’
	B2BITCNT	BIP-24 B2 bit error counter, 2 thresholds[1]	x‘C/D’[1]	N 16	x‘0000’
	B2BITCNTTh12	Degradation threshold Byte2 (least significant byte) for B2BITCNT	x‘E’	X 8	‘00100000’
	B2BITCNTTh11	Degradation threshold Byte1 for B2BITCNT	x‘F’	X 8	‘01001110’
	B2BITCNTTh22	Failure threshold Byte2 (least significant byte) for B2BITCNT	x‘10’	X 8	‘00000000’
	B2BITCNTTh21	Failure threshold Byte1 for B2BITCNT	x‘11’	X 8	‘01111101’
	B2BLKCNT	BIP-24 B2 block error counter, 2 thresholds[1]	x‘12/13’[1]	N 16	x‘0000’
	B2BLKCNTTh12	Degradation threshold Byte2 (least significant byte) for B2BLKCNT	x‘14’	X 8	‘00100000’
	B2BLKCNTTh11	Degradation threshold Byte1 forB2BLKCNT	x‘15’	X 8	‘01001110’
	B2BLKCNTTh22	Failure threshold Byte2 (least significant byte) for B2BLKCNT	x‘16’	X 8	‘00000000’
	B2BLKCNTTh21	Failure threshold Byte1 for B2BLKCNT	x‘17’	X 8	‘01111101’
	B3BITCNT	BIP-8 B3 bit error counter[1]	x‘18/19’[1]	N 16	x‘0000’
	B3BITCNTTh12	Threshold register Byte2 (least significant byte) for B3BITCNT	x‘1A’	X 8	‘00000000’
	B3BITCNTTh11	Threshold register Byte1 for counter B3BITCNT	x‘1B’	X 8	‘01111101’
	B3BLKCNT	BIP-8 B3 block error counter[1]	x‘1C/1D’[1]	N 16	x‘0000’
	B3BLKCNTTh12	Threshold register Byte2 (least significant byte) for B3BLKCNT	x‘1E’	X 8	‘00000000’
	B3BLKCNTTh11	Threshold register Byte1 for counter B3BLKCNT	x‘1F’	X 8	‘01111101’

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8. GRA Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16 byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 37: OFP_Rx GPP Handler Address Mapping Base Address = x‘800’ (Page 2 of 5)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Counter	MSREICNT	Multiplex section remote error indication counter[1]	x‘20/21’[1]	N 16	x‘0000’
	MSREICNTTh12	Threshold register Byte2 (least significant byte) for MSREICNT	x‘22’	X 8	‘00000000’
	MSREICNTTh11	Threshold register Byte1 for counter MSREICNT	x‘23’	X 8	‘01111101’
	HPREICNT	Higher-order path remote error indication counter [1]	x‘24/25’[1]	N 16	x‘0000’
	HPREICNTTh12	Threshold register Byte2 (least significant byte) for HPREICNT	x‘26’	X 8	‘00000000’
	HPREICNTTh11	Threshold register Byte1 for counter HPREICNT	x‘27’	X 8	‘01111101’
	PJ_EVCNT	Positive justification counter, no threshold[1]	x‘28/29’[1]	N 8	‘00000000’
	NJ_EVCNT	Negative justification counter, no threshold[1]	x‘2A/2B’[1]	N 8	‘00000000’
	ND_EVCNT	New data event counter, no threshold[1]	x‘2C/2D’[1]	N 8	‘00000000’
Reset	RESET	Default RESET register	x‘30’	R 2	‘01’
Status	STAT1	Status register #1 (Mode)	x‘33’	S 3	
	STAT2	Status register #2 (AU pointer)	x‘34’	S 6	
	STAT3	Status register #3 (SOH)	x‘35’	S 6	
	STAT4	Status register #4 (POH)	x‘36’	S 4	
Interrupt and Mask	MainIRQ	MAIN INTerrupt register	x‘38’	I 7	
	M_MainIRQ	INTerrupt MASK register for MainIRQ	x‘39’	X 7	‘0000000’
	CntrIRQ1	COUNTER INTerrupt register	x‘3A’	I 8	
	M_CntrIRQ1	INTerrupt MASK register for CntrIRQ1	x‘3B’	X 8	‘00000000’
	CntrIRQ2	COUNTER INTerrupt register	x‘3C’	I 8	
	M_CntrIRQ2	INTerrupt MASK register for CntrIRQ2	x‘3D’	X 8	‘00000000’
	CntrIRQ3	COUNTER INTerrupt register	x‘3E’	I 5	
	M_CntrIRQ3	INTerrupt MASK register for CntrIRQ3	x‘3F’	X 5	‘00000’
	IRQ6	USER INTerrupt register	x‘40’	I 4	
	M_IRQ6	INTerrupt MASK register for IRQ6	x‘41’	X 4	‘0000’
	IRQ7	USER INTerrupt register	x‘42’	I 8	
	M_IRQ7	INTerrupt MASK register for IRQ7	x‘43’	X 8	‘00000000’
	IRQ8	USER INTerrupt register	x‘44’	I 8	
	M_IRQ8	INTerrupt MASK register for IRQ8	x‘45’	X 8	‘00000000’
Configuration	CONF1	Configuration register #1 (general)	x‘48’	C 8	‘00111111’
	CONF2	Configuration register #2 (SOH processing)	x‘49’	C 6	‘0000’

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8. GRA Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16 byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 37: OFP_Rx GPP Handler Address Mapping Base Address = x‘800’ (Page 3 of 5)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Configuration	CONF3	Configuration register #3 (POH processing)	x‘4A’	C 4	‘0000’
	CONF4	Configuration register #4 (APS processing)	x‘4B’	C 8	‘00000000’
	CONF7	Configuration register #7 (miscellaneous)	x‘4E’	C 8	‘00100000’
	CONF8	Configuration register #8 (FSCR)	x‘4F’	C 8	‘11111110’
	CONF9	Configuration register #9 (SL)	x‘50’	C 8	‘00010011’
Debug	SOH-A11	First A1	x‘100’	8	
	SOH-A12	Second1 A1	x‘101’	8	
	SOH-A13	Third A1	x‘102’	8	
	SOH-A21	First A2	x‘103’	8	
	SOH-A22	Second A2	x‘104’	8	
	SOH-A23	Third A2	x‘105’	8	
	SOH-J0	J0	x‘106’	8	
		Reserved for national use and not included in frame scrambling (C1)	x‘107-8’	8	
	SOH-B1	B1	x‘109’	8	
		Media dependant bytes	x‘10A-0B’	8	
	SOH-E1	E1	xx‘10C’	8	
		Media dependant byte	x‘10D’	8	
		Reserved for future standardization	x‘10E’	8	
	SOH-F1	F1	x‘10F’	8	
		Reserved for national use	x‘110-11’	8	
	SOH-D1	D1	x‘112’	8	
		Media dependant bytes	x‘113-14’	8	
	SOH-D2	D2	x‘115’	8	
		Media dependant byte	x‘116’	8	
		Reserved for future standardization	x‘117’	8	
	SOH-D3	D3	x‘118’	8	
		Reserved for future standardization	x‘119-1A’	8	
	SOH-H1	H1	x‘11B’	8	
	SOH-J0	’1001SS11’ with S unspecified	x‘11C-1D’	8	
	SOH-H2	H2	x‘11E’	8	
	SOH-1s	x‘FF’	x‘11F-20’	8	
	SOH-H31	First H3	x‘121’	8	
	SOH-H32	Second H3	x‘122’	8	
	SOH-H23	Third H3	x‘123’	8	
	SOH-B21	First B2	x‘124’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8. GRA Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16 byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 37: OFP_Rx GPP Handler Address Mapping Base Address = x‘800’ (Page 4 of 5)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Debug	SOH-B22	Second B2	x‘125’	8	
	SOH-B23	Third B2	x‘126’	8	
	SOH-K1	K1	x‘x‘127’	8	
		Reserved for future standardization	x‘128-29’	8	
	SOH-K2	K2	x‘12A’	8	
		Reserved for future standardization	x‘12B-2C’	8	
	SOH-D4	D4	x‘12D’	8	
		Reserved for future standardization	x‘12E-2F’	8	
	SOH-D5	D5	x‘130’	8	
		Reserved for future standardization	x‘131-32’	8	
	SOH-D6	D6	x‘133’	8	
		Reserved for future standardization	x‘134-35’	8	
	SOH-D7	D7	x‘136’	8	
		Reserved for future standardization	x‘137-38’	8	
	SOH-D8	D8	x‘139’	8	
		Reserved for future standardization	x‘13A-3B’	8	
	SOH-D9	D9	x‘13C’	8	
		Reserved for future standardization	x‘13D-3E’	8	
	SOH-D10	D10	x‘13F’	8	
		Reserved for future standardization	x‘140-41’	8	
	SOH-D11	D11	x‘142’	8	
		Reserved for future standardization	x‘143-44’	8	
	SOH-D12	D12	x‘145’	8	
		Reserved for future standardization	x‘146-47’	8	
	SOH-S1	S1	x‘148’	8	
		Reserved for future standardization	x‘149-9C’	8	
	SOH-M1	M1	x‘14D’	8	
	SOH-M1	E2	x‘14E’	8	
		Reserved for future standardization	x‘14F-50’	8	
		Reserved	x‘151-53’	8	
	POH-J1	J1	x‘154’	8	
	POH-B3	B3	x‘155’	8	
	POH-C2	C2	x‘156’	8	
	POH-G1	G1	x‘157’	8	
	POH-F2	F2	x‘158’	8	
	POH-H4	H4	x‘159’	8	
	POH-F3	F3	x‘15A’	8	
	POH-K3	K3	x‘15B’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8. GRA Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16 byte addresses of 16 byte J1 path trace to map a full 64 byte space.

Table 37: OFP_Rx GPP Handler Address Mapping Base Address = x‘800’ (Page 5 of 5)

Register Group	Register Name	Description	Address Offset	Type Width	Initial Value
Debug	POH-N1	N1	x‘15C’	8	
		Reserved	x‘15D-5F’	8	
	POH-J0-16-E	Expected 16-byte J0 section trace	x‘160-6F’	8	
	POH-J0-16-R	Received 16-byte J0 section trace	x‘170-7F’	8	
	POH-J1-16	Expected 16-byte J1 path trace[3]	x‘180-8F’	8	
	POH-J1-64	64-byte J1 path trace[3]	x‘190-BF’	8	

1. Independent of the counter width, given that a counter has chiplet address N as a base. Reading address N or address N-1 both yield the least significant byte of the counter. Reading address N has no affect on the counter, but reading address N-1 resets the counter after read operation.
2. Address range 100-17F located in 128x8. GRA Address range 180-1BF located in 64x8 GRA.
3. The 64-byte J1 path trace processing uses the 16 byte addresses of 16 byte J1 path trace to map a full 64 byte space.

3.23.7.1 ROFmid

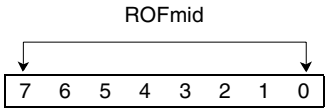
Read-on-the-fly registers.

Length 8 bits

Type Read Only

Framer Address 800

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ROFmid(7-0)	Read-on-the-fly register, most significant byte.

3.23.7.2 B1BITCNT

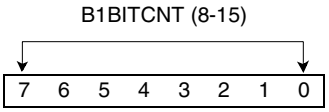
Number of BIP-8 B1 bit errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 804/805

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B1BITCNT(8-15)	BIP-8 B1 bit error counter, least significant byte.

3.23.7.3 B1BITCNTTh11

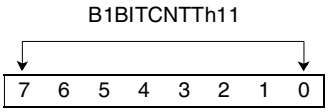
Threshold for number of BIP-8 B1 bit errors.

Length 8 bits

Type Read/Write

Framer Address 807

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B1BITCNTTh11(7-0)	Threshold for BIP-8 B1 bit error counter, most significant byte.

3.23.7.4 B1BITCNTTh12

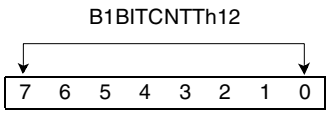
Threshold for number of BIP-8 B1 bit errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 806

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B1BITCNTTh12(7-0)	Threshold for BIP-8 B1 bit error error counter, least significant byte.

3.23.7.5 B1BLKCNT

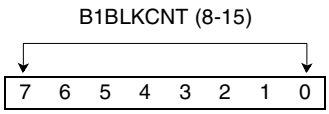
Number of BIP-8 B1 block errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 808/809

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B1BLKCNT(8-15)	BIP-8 B1 block error counter, least significant byte.

3.23.7.6 B1BLKCNTTh11

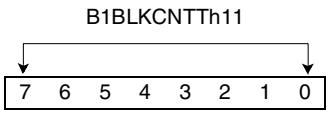
Threshold for number of BIP-8 B1 block errors.

Length 8 bits

Type Read/Write

Framer Address 80B

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B1BLKCNTTh11(7-0)	Threshold for BIP-8 B1 block error counter, most significant byte.

3.23.7.7 B1BLKCNTTh12

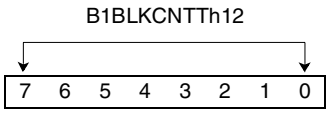
Threshold for number of BIP-8 B1 block errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 80A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B1BLKCNTTh12(7-0)	Threshold for BIP-8 B1 block error counter, least significant byte.

3.23.7.8 B2BITCNT

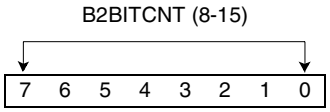
Number of BIP-24 B2 bit errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 80C/80D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B2BITCNT(8-15)	BIP-24 B2 bit error counter, least significant byte.

3.23.7.9 B2BITCNTTh11

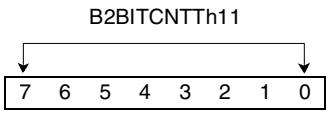
Degradation threshold for number of BIP-24 B2 bit errors.

Length 8 bits

Type Read/Write

Framer Address 80F

Power On Reset Value x‘4E’



Bit(s)	Name	Description
7-0	B2BITCNTTh11(7-0)	Degradation threshold for BIP-24 B2 bit error counter, most significant byte.

3.23.7.10 B2BITCNTTh12

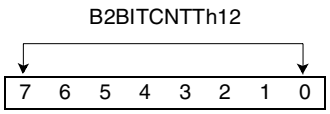
Degradation threshold for number of BIP-24 B2 bit errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 80E

Power On Reset Value x‘20’



Bit(s)	Name	Description
7-0	B2BITCNTTh12(7-0)	Degradation threshold for BIP-24 B2 bit error counter, least significant byte.

3.23.7.11 B2BITCNTTh21

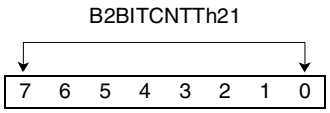
Failure threshold for number of BIP-24 B2 bit errors.

Length 8 bits

Type Read/Write

Framer Address 811

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B2BITCNTTh21(7-0)	Failure threshold for BIP-24 B2 bit error counter, most significant byte.

3.23.7.12 B2BITCNTTh22

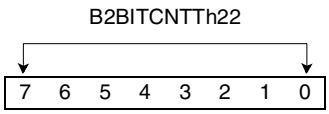
Failure threshold for number of BIP-24 B2 bit errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 810

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B2BITCNTTh22(7-0)	Failure threshold for BIP-24 B2 bit error counter, least significant byte.

3.23.7.13 B2BLKCNT

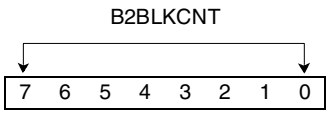
Number of BIP-24 B2 block errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 812/813

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B2BLKCNT(8-15)	BIP-24 B2 block error counter, least significant byte.

3.23.7.14 B2BLKCNTTh11

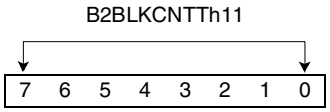
Degradation threshold for number of BIP-24 B2 block errors.

Length 8 bits

Type Read/Write

Framer Address 815

Power On Reset Value x‘4E’



Bit(s)	Name	Description
7-0	B2BLKCNTTh11(7-0)	Degradation threshold for BIP-24 B2 block error counter, most significant byte.

3.23.7.15 B2BLKCNTTh12

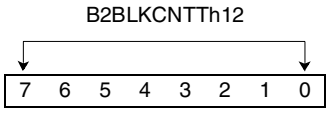
Degradation threshold for number of BIP-24 B2 block errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 814

Power On Reset Value x‘20’



Bit(s)	Name	Description
7-0	B2BLKCNTTh12(7-0)	Degradation threshold for BIP-24 B2 block error counter, least significant byte.

3.23.7.16 B2BLKCNTTh21

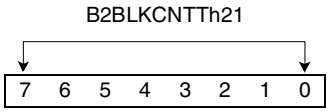
Failure threshold for number of BIP-24 B2 block errors.

Length 8 bits

Type Read/Write

Framer Address 817

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B2BLKCNTTh21(7-0)	Failure threshold for BIP-24 B2 block error counter, most significant byte.

3.23.7.17 B2BLKCNTTh22

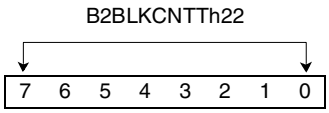
Failure threshold for number of BIP-24 B2 block errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 816

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B2BLKCNTTh22(7-0)	Failure threshold for BIP-24 B2 block error counter, least significant byte.

3.23.7.18 B3BITCNT

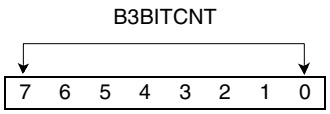
Number of BIP-8 B3 bit errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 818/819

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B3BITCNT(8-15)	BIP-8 B3 bit error counter, least significant byte.

3.23.7.19 B3BITCNTTh11

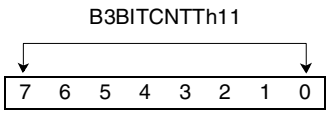
Threshold for number of BIP-8 B3 bit errors.

Length 8 bits

Type Read/Write

Framer Address 81B

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B3BITCNTTh11(7-0)	Threshold for BIP-8 B3 bit error counter, most significant byte.

3.23.7.20 B3BITCNTTh12

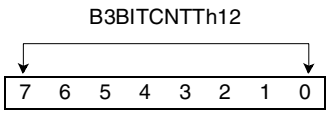
Threshold for number of BIP-8 B3 bit errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 81A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B3BITCNTTh12(7-0)	Threshold for BIP-8 B3 bit error counter, least significant byte.

3.23.7.21 B3BLKCNT

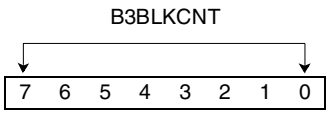
Number of BIP-8 B3 block errors counted since last counter reset (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 81C/81D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B3BLKCNT(8-15)	BIP-8 B3 block error counter, least significant byte.

3.23.7.22 B3BLKCNTTh11

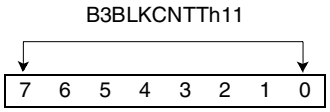
Threshold for number of BIP-8 B3 block errors.

Length 8 bits

Type Read/Write

Framer Address 81F

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	B3BLKCNTTh11(7-0)	Threshold for BIP-8 B3 block error counter, most significant byte.

3.23.7.23 B3BLKCNTTh12

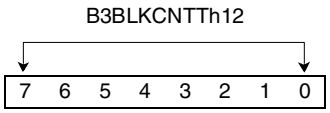
Threshold for number of BIP-8 B3 block errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 81E

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	B3BLKCNTTh12(7-0)	Threshold for BIP-8 B3 block error counter, least significant byte.

3.23.7.24 MSREICNT

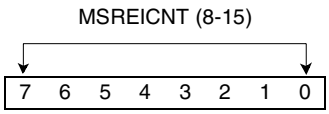
Multiplex Section Remote Error Indication counter (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 820/821

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	MSREICNT(8-15)	Multiplex Section Remote Error Indication counter, least significant byte.

3.23.7.25 MSREICNTTh11

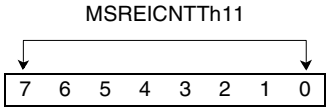
Threshold for number of Multiplex Section Remote Errors.

Length 8 bits

Type Read/Write

Framer Address 823

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	MSREICNTTh11(7-0)	Threshold for Multiplex Indication counter Section Remote Error, most significant byte.

3.23.7.26 MSREICNTTh12

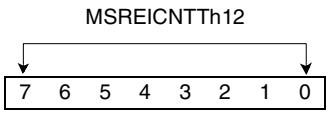
Threshold for number of Multiplex Section Remote Errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 822

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	MSREICNTTh12(7-0)	Threshold for Multiplex Indication counter Section Remote Error, least significant byte.

3.23.7.27 HPREICNT

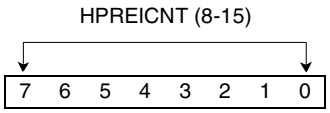
Higher-order Path Remote Error Indication counter (16-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 824/825

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	HPREICNT(8-15)	Higher-order Path Remote Error Indication counter, least significant byte.

3.23.7.28 HPREICNTTh11

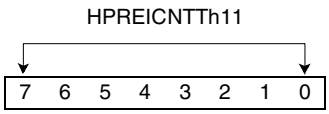
Threshold for number of Higher-order Path Remote Errors.

Length 8 bits

Type Read/Write

Framer Address 827

Power On Reset Value x‘7D’



Bit(s)	Name	Description
7-0	HPREICNTTh11(7-0)	Threshold for Higher-order Path Remote Error Indication counter, most significant byte.

3.23.7.29 HPREICNTTh12

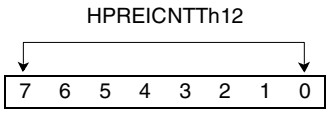
Threshold for number of Higher-order Path Remote Errors. Threshold overstep leads to an interrupt request.

Length 8 bits

Type Read/Write

Framer Address 826

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	HPREICNTTh12(7-0)	Threshold for Higher-order Path Remote Error Indication counter, least significant byte.

3.23.7.30 PJ_EVCNT

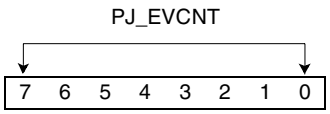
Positive Justification Event counter (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 828/829

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	PJ_EVCNT(7-0)	Positive Justification Event counter.

3.23.7.31 NJ_EVCNT

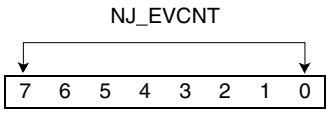
Negative Justification Event counter (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 82A/82B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	NJ_EVCNT(7-0)	Negative Justification Event counter.

3.23.7.32 ND_EVCNT

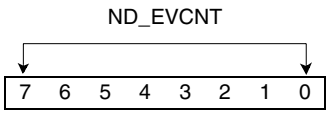
New Data Event counter (eight-bit counter). Overflow leads to an interrupt request.

Length 8 bits

Type Read Only

Framer Address 82C/82D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-0	ND_EVCNT(7-0)	New Data Event counter.

3.23.7.33 CntEn1

Counter On/Off control register #1 for OFP_Rx.

For each bit position:

0 = Counter is disabled.

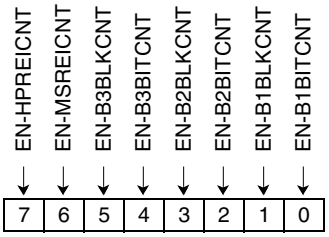
1 = Counter is enabled.

Length 8 bits

Type Read/Write

Framer Address 802

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	EN-HPREICNT	Higher-order Path Remote Error Indication counter enable.
6	EN-MSREICNT	Multiplex Section Remote Error Indication counter enable.
5	EN-B3BLKCNT	BIP-8 B3 block error counter enable.
4	EN-B3BITCNT	BIP-8 B3 bit error counter enable.
3	EN-B2BLKCNT	BIP-24 B2 block error counter enable.
2	EN-B2BITCNT	BIP-24 B2 bit error counter enable.
1	EN-B1BLKCNT	BIP-8 B1 block error counter enable.
0	EN-B1BITCNT	BIP-8 B1 bit error counter enable.

3.23.7.34 CntEn2

Counter On/Off control register #2 for OFP_Rx.

For each bit position:

0 = Counter is disabled.

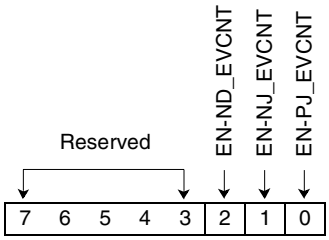
1 = Counter is enabled.

Length 8 bits

Type Read/Write

Framer Address 803

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-3	Reserved	Reserved.
2	EN-ND_EVCNT	New Data Event counter enable.
1	EN-NJ_EVCNT	Negative Justification Event counter enable.
0	EN-PJ_EVCNT	Positive Justification Event counter enable.

3.23.7.35 Reset Register (RESET)

Reset/Halt chiplet control register. This register is preset automatically to the default value by the reset signal ResOT coming from GPPINT chiplet.

For each bit position:

0 = Reset/Halt not active.

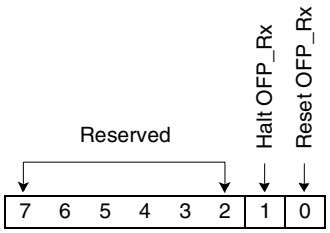
1 = Reset/Halt active.

Length 8 bits

Type Read/Write

Framer Address 830

Power On Reset Value x‘01’



Bit(s)	Name	Description
7-2	Reserved	Reserved.
1	Halt OFP_Rx	Halt (freeze) OFP_Rx chiplet.
0	Reset OFP_Rx	Reset (disable) OFP_Rx chiplet.

3.23.7.36 STAT1

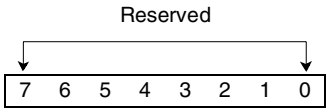
Status register #1 of the chiplet. OFP_Rx Mode status information. This is an event latch register.

Length 8 bits

Type

Framer Address 833

Power On Reset Value -



Bit(s)	Name	Description
7-0	Reserved	Reserved.

3.23.7.37 STAT2

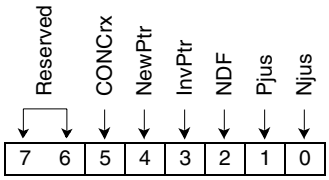
Status register #2 of the chiplet. AU pointer status information of OFP_Rx. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 834

Power On Reset Value



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	CONCrx	Concatenation indication received.
4	NewPtr	Valid New Pointer received.
3	InvPtr	Invalid Pointer received.
2	NDF	NDF received.
1	Pjus	Positive frequency justification received.
0	Njus	Negative frequency justification received.

3.23.7.38 STAT3

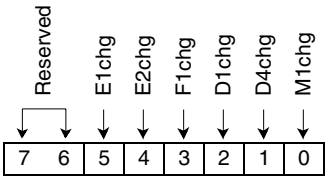
Status register #3 of the chiplet. Section Overhead (SOH) status of OFP_Rx. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 835

Power On Reset Value



Bit(s)	Name	Description
7-6	Reserved	Reserved.
5	E1chg	Orderwire channel E1 content changed.
4	E2chg	Orderwire channel E2 content changed.
3	F1chg	User communication channel F1 content changed.
2	D1chg	D1-D3 communication channel content changed.
1	D4chg	D4-D12 communication channel content changed.
0	M1chg	Number of bit blocks in error changed.

3.23.7.39 STAT4

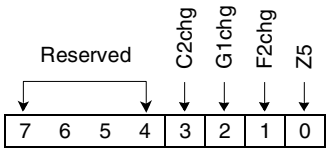
Status register #4 of the chiplet. Path Overhead (POH) status of OFP_Rx. This is an event latch register.

Length 8 bits

Type Read/Write

Framer Address 836

Power On Reset Value



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	C2chg	Payload composition indication changed.
2	G1chg	Path status indication changed.
1	F2chg	User communication channel F2 content changed.
0	Z5	Z5 content changed.

3.23.7.40 MainIRQ

This register is used to indicate fatal interrupt events and point to user IRQ registers with active requests.

For each bit position:

0 = No interrupt request pending.

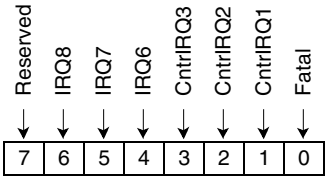
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 838

Power On Reset Value



Bit(s)	Name	Description
7	Reserved	Reserved.
6	IRQ8	Active request in IRQ8 register.
5	IRQ7	Active request in IRQ7 register.
4	IRQ6	Active request in IRQ6 register.
3	CntrIRQ3	Active request in CntrIRQ3 register.
2	CntrIRQ2	Active request in CntrIRQ2 register.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.7.41 M_MainIRQ

This register is used to mask pending interrupt requests. A masked request will not generate an outgoing IRQ to the GPPINT.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

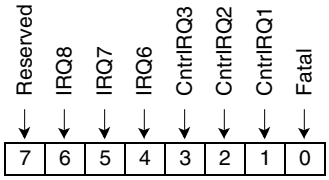
1 = The corresponding pending request bit activates signal IRQOR to GPPINT.

Length 8 bits

Type Read/Write

Framer Address 839

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	Reserved	Reserved.
6	IRQ8	Active request in IRQ8 register.
5	IRQ7	Active request in IRQ7 register.
4	IRQ6	Active request in IRQ6 register.
3	CntrIRQ3	Active request in CntrIRQ3 register.
2	CntrIRQ2	Active request in CntrIRQ2 register.
1	CntrIRQ1	Active request in CntrIRQ1 register.
0	Fatal	Fatal event occurred.

3.23.7.42 CntrIRQ1

Register #1 to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

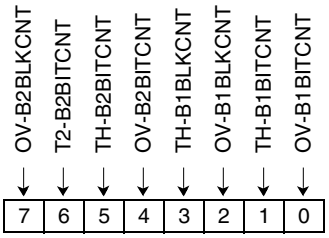
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 83A

Power On Reset Value



Bit(s)	Name	Description
7	OV-B2BLKCNT	Overflow BIP-24 B2 block error counter.
6	T2-B2BITCNT	Failure threshold overstep BIP-24 B2 bit error counter.
5	TH-B2BITCNT	Degradation threshold overstep BIP-24 B2 bit error counter.
4	OV-B2BITCNT	Overflow BIP-24 B2 bit error counter.
3	TH-B1BLKCNT	Threshold overstep BIP-8 B1 block error counter.
2	OV-B1BLKCNT	Overflow BIP-8 B1 block error counter.
1	TH-B1BITCNT	Threshold overstep BIP-8 B1 bit error counter.
0	OV-B1BITCNT	Overflow BIP-8 B1 bit error counter.

3.23.7.43 M_CntrIRQ1

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

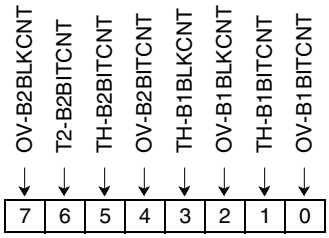
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 83B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	OV-B2BLKCNT	Overflow BIP-24 B2 block error counter.
6	T2-B2BITCNT	Failure threshold overstep BIP-24 B2 bit error counter.
5	TH-B2BITCNT	Degradation threshold overstep BIP-24 B2 bit error counter.
4	OV-B2BITCNT	Overflow BIP-24 B2 bit error counter.
3	TH-B1BLKCNT	Threshold overstep BIP-8 B1 block error counter.
	2OV-B1BLKCNT	Overflow BIP-8 B1 block error counter.
1	TH-B1BITCNT	Threshold overstep BIP-8 B1 bit error counter.
0	OV-B1BITCNT	Overflow BIP-8 B1 bit error counter.

3.23.7.44 CntrIRQ2

Register #2 to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

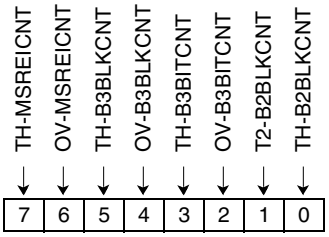
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 83C

Power On Reset Value



Bit(s)	Name	Description
7	TH-MSREICNT	Threshold overstep Multiplex Section Remote Error Indication counter.
6	OV-MSREICNT	Overflow Multiplex Section Remote Error indication counter.
5	TH-B3BLKCNT	Threshold overstep BIP-8 B3 block error counter.
4	OV-B3BLKCNT	Overflow BIP-8 B3 block error counter.
3	TH-B3BITCNT	Threshold overstep BIP-8 B3 bit error counter.
2	OV-B3BITCNT	Overflow BIP-8 B3 bit error counter.
1	T2-B2BLKCNT	Failure threshold overstep BIP-24 B2 block error counter.
0	TH-B2BLKCNT	Degradation threshold overstep BIP-24 B2 block error counter.

3.23.7.45 M_CntrIRQ2

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

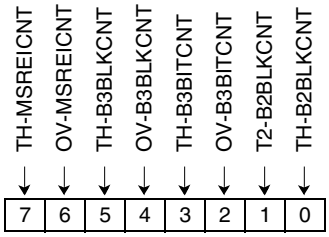
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 83D

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	TH-MSREICNT	Threshold overstep Multiplex Section Remote Error Indication counter.
6	OV-MSREICNT	Overflow Multiplex Section Remote Error indication counter.
5	TH-B3BLKCNT	Threshold overstep BIP-8 B3 block error counter.
4	OV-B3BLKCNT	Overflow BIP-8 B3 block error counter.
3	TH-B3BITCNT	Threshold overstep BIP-8 B3 bit error counter.
2	OV-B3BITCNT	Overflow BIP-8 B3 bit error counter.
1	T2-B2BLKCNT	Failure threshold overstep BIP-24 B2 block error counter.
0	TH-B2BLKCNT	Degradation threshold overstep BIP-24 B2 block error counter.

3.23.7.46 CntrIRQ3

Register #3 to indicate active counter interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

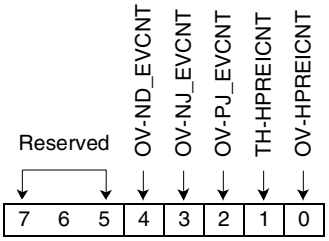
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 83E

Power On Reset Value



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	OV-ND_EVCNT	Overflow New Data event counter.
3	OV-NJ_EVCNT	Overflow Negative Justification event counter.
2	OV-PJ_EVCNT	Overflow Positive Justification event counter.
1	TH-HPREICNT	Threshold overstep Higher-order Path Remote Error indication counter.
0	OV-HPREICNT	Overflow HPR error indication counter.

3.23.7.47 M_CntrIRQ3

This register is used to mask pending counter interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

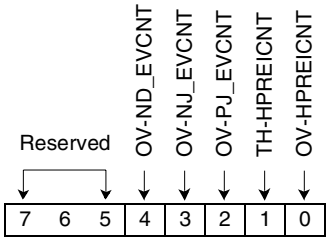
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 83F

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-5	Reserved	Reserved.
4	OV-ND_EVCNT	Overflow New Data event counter.
3	OV-NJ_EVCNT	Overflow Negative Justification event counter.
2	OV-PJ_EVCNT	Overflow Positive Justification event counter.
1	TH-HPREICNT	Threshold overstep Higher-order Path Remote Error indication counter.
0	OV-HPREICNT	Overflow HPR error indication counter.

3.23.7.48 IRQ6

This register is used to indicate active user interrupt requests of this chiplet.

For each bit position:

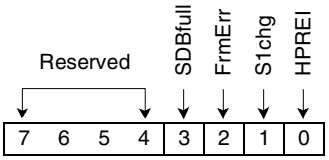
0 = No interrupt request pending.
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 840

Power On Reset Value



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	SDBfull	SDB_Rx FIFO full.
2	FrmErr	Interrupt from ORxAUG FSM.
1	S1chg	Synchronization status changed.
0	HPREI	Higher-order Path Remote Error Indication.

3.23.7.49 M_IRQ6

This register is used to mask pending user interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

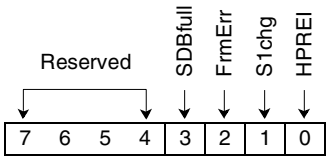
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 841

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	SDBfull	SDB_Rx FIFO full.
2	FrmErr	Interrupt from ORxAUG FSM.
1	S1chg	Synchronization status changed.
0	HPREI	Higher-order Path Remote Error Indication.

3.23.7.50 IRQ7

This register is used to indicate active user interrupt requests of this chiplet.

For each bit position:

0 = No interrupt request pending.

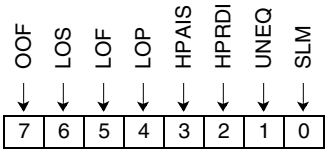
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 842

Power On Reset Value



Bit(s)	Name	Description
7	OOF	Out of frame alarm.
6	LOS	Loss of signal alarm.
5	LOF	Loss of frame alarm.
4	LOP	Loss of pointer alarm.
3	HPAIS	Higher-order path AIS.
2	HPRDI	Higher-order path RDI.
1	UNEQ	Unequipped signal.
0	SLM	Signal label mismatch alarm.

3.23.7.51 M_IRQ7

This register is used to mask pending user interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

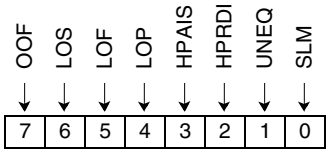
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 843

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	OOF	Out of frame alarm.
6	LOS	Loss of signal alarm.
5	LOF	Loss of frame alarm.
4	LOP	Loss of pointer alarm.
3	HPAIS	Higher-order path AIS.
2	HPRDI	Higher-order path RDI.
1	UNEQ	Unequipped signal.
0	SLM	Signal label mismatch alarm.

3.23.7.52 IRQ8

This register is used to indicate active user interrupt requests of this chiplet.

For each bit position:

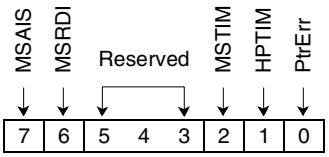
0 = No interrupt request pending.
1 = Interrupt request pending.

Length 8 bits

Type Read/Write

Framer Address 844

Power On Reset Value



Bit(s)	Name	Description
7	MSAIS	Multiplex Section AIS.
6	MSRDI	Multiplex Section RDI.
5-3	Reserved	Reserved.
2	MSTIM	Multiplex Section trace identifier mismatch.
1	HPTIM	Higher-order path trace identifier mismatch.
0	PtrErr	Pointer processing error.

3.23.7.53 M_IRQ8

This register is used to mask pending user interrupt requests.

For each bit position:

0 = The corresponding pending request bit is masked (DEFAULT).

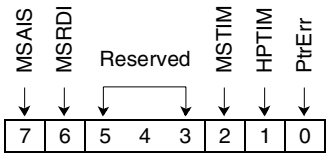
1 = The corresponding pending request bit activates the pointer bit in MainIRQ register.

Length 8 bits

Type Read/Write

Framer Address 845

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	MSAIS	Multiplex Section AIS.
6	MSRDI	Multiplex Section RDI.
5-3	Reserved	Reserved.
2	MSTIM	Multiplex Section trace identifier mismatch.
1	HPTIM	Higher-order path trace identifier mismatch.
0	PtrErr	Pointer processing error.

3.23.7.54 CONF1

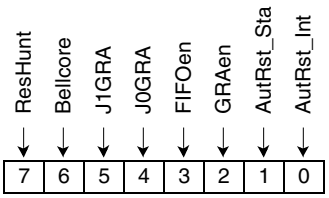
Configuration register #1. General OFP_Rx configuration signals.

Length 8 bits

Type Read/Write

Framer Address 848

Power On Reset Value x‘3F’



Bit(s)	Name	Description
7	ResHunt	0 Hunt free running. 1 Reset Hunt to PIM.
6	Bellcore	0 Operate according to ITU standard. 1 Operate according to Bellcore specification.
5	J1GRA	0 Do not write J1 section trace to GRA. 1 Write J1 section trace to GRA.
4	J0GRA	0 Do not write J0 section trace to GRA. 1 Write J0 section trace to GRA.
3	FIFOen	0 Do not write C4 payload to FIFO. 1 Write C4 payload to FIFO.
2	GRAen	0 Do not write SOH/POH info to GRA. 1 Write received SOH/POH info to GRA.
1	AutRst_Sta	0 No action on read access. 1 Auto-reset status register upon read access.
0	AutRst_Int	0 No action on read access. 1 Auto-reset interrupt request registers upon read access.

3.23.7.55 CONF2

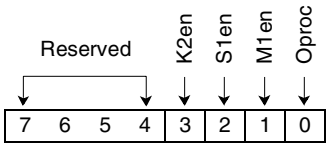
Configuration register #2. SOH processing configuration signals.

Length 8 bits

Type Read/Write

Framer Address 849

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	K2en	0 Disable K2 AIS processing. 1 Enable K2 AIS processing.
2	S1en	0 Disable S1 synchronization status processing. 1 Enable S1 synchronization status processing.
1	M1en	0 Disable M1 REI processing. 1 Enable M1 REI processing.
0	J0proc	0 Disable J0 section trace processing. 1 Enable J0 section trace processing.

3.23.7.56 CONF3

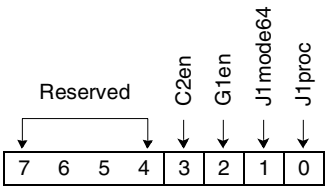
Configuration register #3. POH byte processing configuration signals.

Length 8 bits

Type Read/Write

Framer Address 84A

Power On Reset Value x‘00’



Bit(s)	Name	Description
7-4	Reserved	Reserved.
3	C2en	0 Disable C2 signal label processing. 1 Enable C2 signal label processing.
2	G1en	0 Disable G1 path status processing. 1 Enable G1 path status processing.
1	J1mode64	0 16-byte J1 trace. 1 64-byte J1 trace.
0	J1proc	0 Disable J1 path trace processing. 1 Enable J1 path trace processing.

3.23.7.57 CONF4

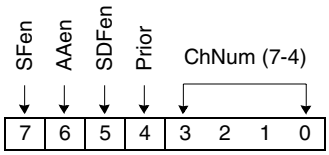
Configuration register #4. APS processing configuration signals.

Length 8 bits

Type Read/Write

Framer Address 84B

Power On Reset Value x‘00’



Bit(s)	Name	Description
7	SFen	0 Disable SF K2 MS_RDI processing. 1 Enable SF K2 MS_RDI processing.
6	AAen	0 Disable automatic Alarm processing for K2. 1 Enable automatic Alarm processing for K2.
5	SDFen	0 Disable automatic SDF K1 processing. 1 Enable automatic SDF K1 processing.
4	Prior	Priority level.
3-0	ChNum(7-4)	Channel Number.

3.23.7.58 CONF7

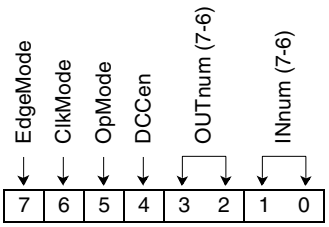
Configuration register #7. Miscellaneous OFP_Rx configuration signals.

Length 8 bits

Type Read/Write

Framer Address 84E

Power On Reset Value x‘20’



Bit(s)	Name	Description
7	EdgeMode	0 Active falling edge. 1 Active rising edge.
6	ClkMode	0 Continuous clock mode. 1 Strobed clock mode.
5	OpMode	0 DCC 1 channel selected. 1 DCC 2 channel selected.
4	DCCen	0 Disable DCC processing. 1 Enable DCC processing.
3-2	OUTnum(7-6)	Number of µs for in-frame to out-of-frame transition.
1-0	INnum(7-6)	Number of µs for out-of-frame to in-frame transition.

3.23.7.59 CONF8

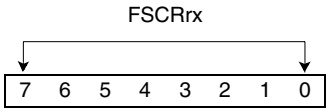
Configuration register #8. Pattern register signals.

Length 8 bits

Type Read/Write

Framer Address 84F

Power On Reset Value x‘FE’



Bit(s)	Name	Description
7-0	FSCRrx(7-0)	Frame descrambling reload pattern.

3.23.7.60 CONF9

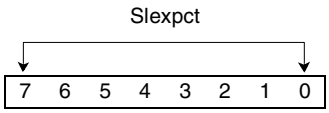
Configuration register #9. Pattern register signals.

Length 8 bits

Type Read/Write

Framer Address 850

Power On Reset Value x‘13’



Bit(s)	Name	Description
7-0	Slexpct(7-0)	Expected signal label.

4. Physical Description and Signal Definitions

Figure 36: Package Diagram

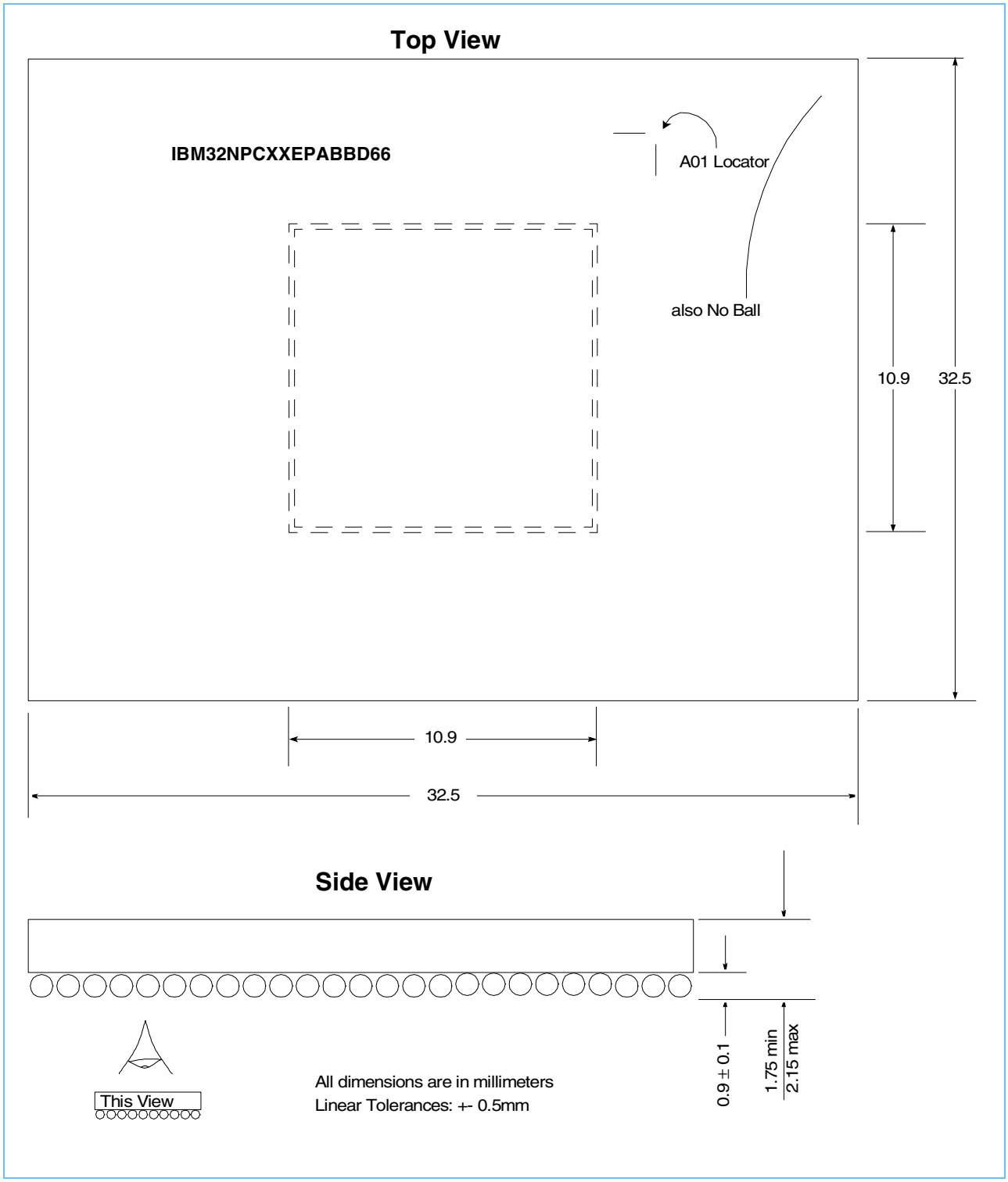
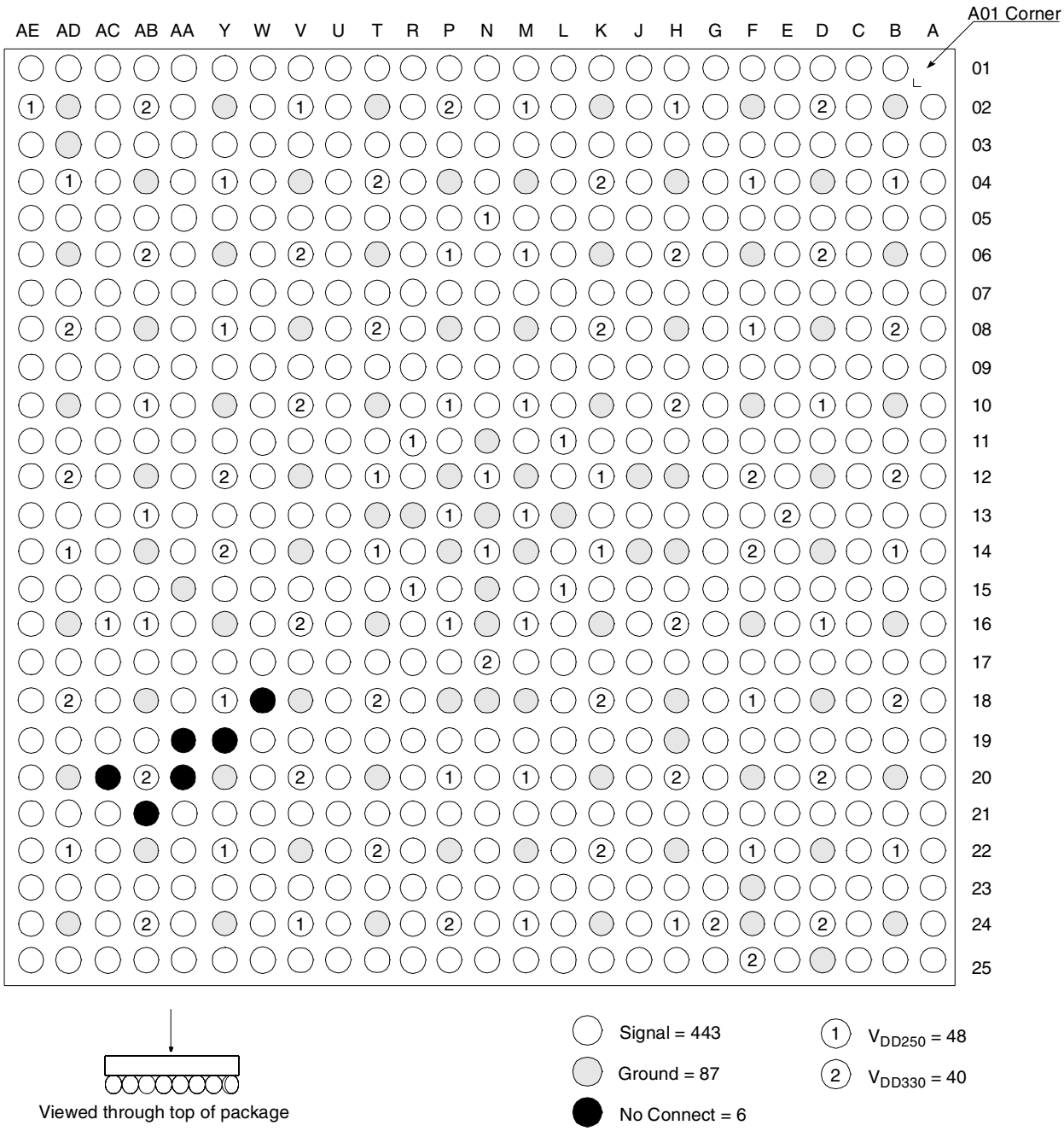


Figure 37: Pinout Viewed from Above BSM - 32 x 32mm CBGA at 1.27mm pitch



Note: For illustrative purposes only. Refer to IBM ASIC SA-12E Databook available from your IBM representative.

Table 38: Signal Pin Listing By Signal Name (Page 1 of 5)

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
BIST0DI1	0W01	K	CMDATA(0)	0M09	C	CMDATA(36)	0G06	C
CM0CS(0)	AD17	C	CMDATA(1)	0N03	C	CMDATA(37)	0G07	C
CM0CS(1)	0Y15	C	CMDATA(2)	0N02	C	CMDATA(38)	0E04	C
CM0CS(2)	AE16	C	CMDATA(3)	0L02	C	CMDATA(38)	0E04	C
CM0CS(3)	AE15	C	CMDATA(4)	0L03	C	CMSYNCAS(0)	0U15	C
CM0DQM(0)	0U14	C	CMDATA(5)	0L09	C	CMSYNCAS(1)	AC17	C
CM0DQM(1)	AB15	C	CMDATA(6)	0M03	C	CMSYNRAS(0)	AE18	C
CM0DQM(2)	AE14	C	CMDATA(7)	0L04	C	CMSYNRAS(1)	AA17	C
CM0DQM(3)	AC14	C	CMDATA(8)	0L08	C	CMWE(0)	0W13	C
CMADDR(0)	0W02	C	CMDATA(9)	0K03	C	CMWE(1)	AA13	C
CMADDR(1)	0U03	C	CMDATA(10)	0L05	C	CTS	0P07	T
CMADDR(2)	0R08	C	CMDATA(11)	0L06	C	DSR	0W03	O
CMADDR(3)	0U02	C	CMDATA(12)	0J02	C	DTR	AA05	O
CMADDR(4)	0T05	C	CMDATA(13)	0L07	C	ENSTATE(0)	0C24	A
CMADDR(5)	0U04	C	CMDATA(14)	0L10	C	ENSTATE(1)	0B25	A
CMADDR(6)	0R07	C	CMDATA(15)	0K05	C	ENSTATE(2)	0E24	A
CMADDR(7)	0T03	C	CMDATA(16)	0J05	C	ENSTATE(3)	AA24	A
CMADDR(8)	0R06	C	CMDATA(17)	0H01	C	ENSTATE(4)	AB25	A
CMADDR(9)	0N09	C	CMDATA(18)	0J03	C	ENSTATE(5)	AD25	A
CMADDR(10)	0R05	C	CMDATA(19)	0K09	C	ENSTATE(6)	AC24	A
CMADDR(11)	0P03	C	CMDATA(20)	0J04	C	ENSTATE(7)	AD23	A
CMADDR(12)	0R03	C	CMDATA(21)	0J07	C	ENSTATE(8)	AE25	A
CMADDR(13)	0R04	C	CMDATA(22)	0H03	C	ENSTATE(9)	AE22	A
CMADDR(14)	0R02	C	CMDATA(23)	0K07	C	ENSTATE(10)	AE24	A
CMADDR(15)	0N04	C	CMDATA(24)	0G02	C	ENSTATE(11)	AD21	A
CMADDR(16)	0N07	C	CMDATA(25)	0F01	C	ENSTATE(12)	AE04	A
CMADDR(17)	0N08	C	CMDATA(26)	0J09	C	ENSTATE(13)	AD05	A
CMADDR(18)	0M11	C	CMDATA(27)	0H05	C	ENSTATE(14)	AE01	A
CMADDR(19)	0N10	C	CMDATA(28)	0J06	C	ENSTATE(15)	AC02	A
CMADDR(20)	0N06	C	CMDATA(29)	0G04	C	ENSTATE(16)	AD01	A
CMCLK(0)	0J01	B	CMDATA(30)	0F03	C	ENSTATE(17)	AB01	A
CMCLK(1)	0K01	B	CMDATA(31)	0J08	C	ENSTATE(18)	AA02	A
CMCLK(2)	0L01	B	CMDATA(32)	0G05	C	ENSTATE(19)	0B01	A
CMCLK(3)	0M01	B	CMDATA(33)	0H07	C	ENSTATE(20)	0E02	A
CMCLK(4)	0N01	B	CMDATA(34)	0D03	C	ENSTATE(21)	0D01	A
CMCLKE	AD13	C	CMDATA(35)	0F05	C	ENSTATE(22)	0C02	A

Table 38: Signal Pin Listing By Signal Name (Page 2 of 5)

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
ENSTATE(23)	0B03	A	ENSTATE(60)	0C25	K	FYRSCLK	0J24	DA
ENSTATE(24)	0A02	A	ENSTATE(61)	0C23	K	$\overline{\text{FYRSCLK}}$	0J25	DA
ENSTATE(25)	0A04	A	ENSTATE(62)	0A23	K	FYRSDAT	0M23	DA
ENSTATE(26)	0B05	A	ENSTATE(63)	0A21	K	$\overline{\text{FYRSDAT}}$	0M25	DA
ENSTATE(27)	0A22	A	$\overline{\text{FY0EMP}}$	0L17	N	FYRSOC	0R24	L
ENSTATE(28)	0B21	A	$\overline{\text{FY0FUL}}$	0J23	N	FYTADR(0)	0N20	G
ENSTATE(29)	0A25	A	$\overline{\text{FY0RENB}}$	0H25	I	FYTADR(1)	0N21	G
ENSTATE(30)	0B23	A	$\overline{\text{FY0TENB}}$	0J21	I	FYTADR(2)	0T25	G
ENSTATE(31)	0A24	A	FYDISCRD	0K21	L	FYTADR(3)	0N22	G
ENSTATE(32)	0N23	J	FYDTCT	0L18	N	FYTADR(4)	0N24	G
ENSTATE(33)	0R22	J	FYRADR(0)	0L19	G	FYTCA	0N25	L
ENSTATE(34)	0R19	J	FYRADR(1)	0L20	G	FYTDAT(0)	0F21	J
ENSTATE(35)	0U22	J	FYRADR(2)	0K25	G	FYTDAT(1)	0K17	J
ENSTATE(36)	0T21	J	FYRADR(3)	0L25	G	FYTDAT(2)	0G20	J
ENSTATE(37)	0U24	J	FYRADR(4)	0L21	G	FYTDAT(3)	0G21	J
ENSTATE(38)	0R18	J	FYRCA	0L22	L	FYTDAT(4)	0E22	J
ENSTATE(39)	0U23	J	FYRDAT(0)	AA23	T	FYTDAT(5)	0J18	J
ENSTATE(40)	0W24	J	FYRDAT(1)	0W25	T	FYTDAT(6)	0D23	J
ENSTATE(41)	0V23	J	FYRDAT(2)	0W23	T	FYTDAT(7)	0G22	J
ENSTATE(42)	0V25	J	FYRDAT(3)	AC21	T	FYTDAT(8)	0J19	G
ENSTATE(43)	0T19	J	FYRDAT(4)	AA21	T	FYTDAT(9)	0J20	G
ENSTATE(44)	0R17	J	FYRDAT(5)	0P21	T	FYTDAT(10)	0H21	G
ENSTATE(45)	0R16	J	FYRDAT(6)	0M21	T	FYTDAT(11)	0M15	G
ENSTATE(46)	0U20	J	FYRDAT(7)	0E21	T	FYTDAT(12)	0K19	G
ENSTATE(47)	0U21	J	FYRDAT(8)	0C21	T	FYTDAT(13)	0H23	G
ENSTATE(48)	0V21	J	FYRDAT(9)	AE19	T	FYTDAT(14)	0L16	G
ENSTATE(49)	0W22	J	FYRDAT(10)	AC19	T	FYTDAT(15)	0J22	G
ENSTATE(50)	AA01	K	FYRDAT(11)	0P19	T	FYTEOP	0R21	H
ENSTATE(51)	AC01	K	FYRDAT(12)	0M19	T	FYTMOD	0P17	H
ENSTATE(52)	AC03	K	FYRDAT(13)	0C19	T	FYTPAR(0)	0P15	J
ENSTATE(53)	AE03	K	FYRDAT(14)	AA14	T	FYTPAR(1)	0N19	J
ENSTATE(54)	AE05	K	FYRDAT(15)	0W14	T	FYTSCLK	0T23	DA
ENSTATE(55)	AE21	K	FYREOP	0L23	L	$\overline{\text{FYTSCLK}}$	0R25	DA
ENSTATE(56)	AE23	K	FYRMOD	0L24	L	FYTSDAT	0P23	DB
ENSTATE(57)	AC23	K	FYRPAR(0)	0K23	N	$\overline{\text{FYTSDAT}}$	0P25	DB
ENSTATE(58)	AC25	K	FYRPAR(1)	0M17	N	FYTSOC	0U25	G
ENSTATE(59)	AA25	K	FYRRDB	0R23	N	FYTWRB	0R20	N

Table 38: Signal Pin Listing By Signal Name (Page 3 of 5)

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
IBDINH1	0E05	Q	PAD(1)	0F13	D	PAD64(38)	0B07	D
IBDINH2	0A03	R	PAD(2)	0L14	D	PAD64(39)	0F07	D
IBDRINH	0C01	U	PAD(3)	0G13	D	PAD64(40)	0D07	D
$\overline{\text{JTAG0RST}}$	0G12	T	PAD(4)	0H13	D	PAD64(41)	0G09	D
JTAGTCK	0E12	T	PAD(5)	0J13	D	PAD64(42)	0F09	D
JTAGTDI	0E14	T	PAD(6)	0K13	D	PAD64(43)	0E08	D
JTAGTDO	0A07	K	PAD(7)	0D13	D	PAD64(44)	0J10	D
JTAGTMS	0G14	T	PAD(8)	0B13	D	PAD64(45)	0G08	D
JTCOMPLY	0C03	M	PAD(9)	0A13	D	PAD64(46)	0H09	D
LEAKTST	0A05	S	PAD(10)	0C15	D	PAD64(47)	0G10	D
$\overline{\text{MACK64}}$	0C10	D	PAD(11)	0D15	D	PAD64(48)	0C08	D
$\overline{\text{MDEVSEL}}$	0E16	D	PAD(12)	0A16	D	PAD64(49)	0K11	D
$\overline{\text{MEXTPMEVENT}}$	0G15	N	PAD(13)	0C14	D	PAD64(50)	0D09	D
$\overline{\text{MFRAME}}$	0C17	D	PAD(14)	0A14	D	PAD64(51)	0J11	D
$\overline{\text{MGNT}}$	0C22	D	PAD(15)	0E15	D	PAD64(52)	0C09	D
MHALTPPC	0U19	N	PAD(16)	0J15	D	PAD64(53)	0A08	D
$\overline{\text{MINT2}}$	0J16	D	PAD(17)	0K15	D	PAD64(54)	0E09	D
$\overline{\text{MINTA}}$	0J17	D	PAD(18)	0G16	D	PAD64(55)	0E10	D
$\overline{\text{MIRDY}}$	0H15	D	PAD(19)	0H17	D	PAD64(56)	0H11	D
$\overline{\text{MPCIRST}}$	AA03	E	PAD(20)	0G18	D	PAD64(57)	0G11	D
MPEGCLK	0C07	T	PAD(21)	0F17	D	PAD64(58)	0A09	D
$\overline{\text{MPERR}}$	0C16	D	PAD(22)	0E17	D	PAD64(59)	0B09	D
$\overline{\text{MPLLRESET}}$	AA12	V	PAD(23)	0E18	D	PAD64(60)	0F11	D
$\overline{\text{MPMEVENT}}$	0Y25	F	PAD(24)	0C18	D	PAD64(61)	0A10	D
$\overline{\text{MREQ}}$	0D21	D	PAD(25)	0A18	D	PAD64(62)	0A11	D
$\overline{\text{MREQ64}}$	0D11	D	PAD(26)	0G19	D	PAD64(63)	0E11	D
$\overline{\text{MSERR}}$	0A15	D	PAD(27)	0E20	D	$\overline{\text{PB0EPRM}}$	0V17	N
$\overline{\text{MSTOP}}$	0D17	D	PAD(28)	0F19	D	$\overline{\text{PB0PHY1}}$	AC22	N
$\overline{\text{MTRDY}}$	0B17	D	PAD(29)	0E19	D	$\overline{\text{PB0PHY2}}$	AB19	N
NC	AA20		PAD(30)	0C20	D	PBADDR16	0W17	N
NC	0W18		PAD(31)	0A20	D	PBADDR17	0Y17	N
NC	AA19		PAD64(32)	0C04	D	PBALE1	AA18	N
NC	AB21		PAD64(33)	0D05	D	PBALE2	0U16	N
NC	0Y19		PAD64(34)	0A06	D	PBDATA(0)	0W21	J
NC	AC20		PAD64(35)	0C06	D	PBDATA(1)	0U18	J
$\overline{\text{NSELFT}}$	AC05	T	PAD64(36)	0E06	D	PBDATA(2)	0W20	J
PAD(0)	0C13	D	PAD64(37)	0E07	D	PBDATA(3)	0V19	J

Table 38: Signal Pin Listing By Signal Name (Page 4 of 5)

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
PBDATA(4)	AB23	J	PMADDR(0)	AA04	C	PMDATA(10)	0W11	C
PBDATA(5)	0Y21	J	PMADDR(1)	0W06	C	PMDATA(11)	AB09	C
PBDATA(6)	0W19	J	PMADDR(2)	0Y05	C	PMDATA(12)	AA10	C
PBDATA(7)	AA22	J	PMADDR(3)	0T09	C	PMDATA(13)	AD09	C
PBINTRA	AE20	N	PMADDR(4)	0V07	C	PMDATA(14)	0V11	C
PBPHYRST	AD19	N	PMADDR(5)	0R10	C	PMDATA(15)	AC09	C
PBRDRDY	0W16	N	PMADDR(6)	0W05	C	PMDATA(16)	AD07	C
PBRNWRT	AC18	N	PMADDR(7)	0U08	C	PMDATA(17)	AC08	C
PBSCLK	0T15	N	PMADDR(8)	AB03	C	PMDATA(18)	AE08	C
PBSDATA	AB17	J	PMADDR(9)	0R09	C	PMDATA(19)	0W10	C
PCBE(0)	0B15	D	PMADDR(10)	0Y03	C	PMDATA(20)	0U11	C
PCBE(1)	0A17	D	PMADDR(11)	0Y01	C	PMDATA(21)	0T11	C
PCBE(2)	0B19	D	PMADDR(12)	0U07	C	PMDATA(22)	0Y09	C
PCBE(3)	0D19	D	PMADDR(13)	0W04	C	PMDATA(23)	AA09	C
PCBE64(4)	0A12	D	PMADDR(14)	0V05	C	PMDATA(24)	AA08	C
PCBE64(5)	0C12	D	PMADDR(15)	0U05	C	PMDATA(25)	AB07	C
PCBE64(6)	0L12	D	PMADDR(16)	0U06	C	PMDATA(26)	0W09	C
PCBE64(7)	0C11	D	PMADDR(17)	0P11	C	PMDATA(27)	AE06	C
PCICLK	0G25	PLL	PMADDR(18)	0P09	C	PMDATA(28)	AC06	C
PDBLCLK	0Y23	N	PMADDR(19)	0T07	C	PMDATA(29)	0U10	C
PFFCFG(0)	0G01	T	PMADDR(20)	0V03	C	PMDATA(30)	0U09	C
PFFCFG(1)	0G03	T	PMCLK(0)	0P01	B	PMDATA(31)	0Y07	C
PFFCFG(2)	0C05	T	PMCLK(1)	0R01	B	PMDATA(32)	AA07	C
PFFOSC	0E03	T	PMCLK(2)	0T01	B	PMDATA(33)	0V09	C
PIDSEL	0G17	D	PMCLK(3)	0U01	B	PMDATA(34)	AA06	C
PINTCLK	0T17	N	PMCLK(4)	0V01	B	PMDATA(35)	0W08	C
PLLTUNE(0)	0G23	P	PMCLKE	AC11	C	PMDATA(36)	AB05	C
PLLTUNE(1)	0E23	P	PMDATA(0)	AB11	C	PMDATA(37)	0W07	C
$\overline{\text{PM0CS}}$(0)	0R14	C	PMDATA(1)	AE10	C	PMDATA(38)	AC04	C
$\overline{\text{PM0CS}}$(1)	AC15	C	PMDATA(2)	AE12	C	$\overline{\text{PMSYNCAS}}$(0)	0V15	C
$\overline{\text{PM0CS}}$(2)	AD15	C	PMDATA(3)	AC12	C	$\overline{\text{PMSYNCAS}}$(1)	AA16	C
$\overline{\text{PM0CS}}$(3)	AE13	C	PMDATA(4)	AA11	C	$\overline{\text{PMSYNRAS}}$(0)	0W15	C
$\overline{\text{PM0DQM}}$(0)	0Y13	C	PMDATA(5)	0U12	C	$\overline{\text{PMSYNRAS}}$(1)	AE17	C
$\overline{\text{PM0DQM}}$(1)	0V13	C	PMDATA(6)	AE09	C	$\overline{\text{PMWE}}$(0)	0R12	C
$\overline{\text{PM0DQM}}$(2)	0U13	C	PMDATA(7)	0Y11	C	$\overline{\text{PMWE}}$(1)	AC13	C
$\overline{\text{PM0DQM}}$(3)	AD11	C	PMDATA(8)	AE11	C	PPAR	0F15	D
PM66EN	0A19	E	PMDATA(9)	AC10	C	PPAR64	0B11	D

Table 38: Signal Pin Listing By Signal Name (Page 5 of 5)

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
PPLLOUT	0U17	J	RTS	0M07	O	TESTM	0E01	W
PPLLTI	0W12	V	RXCLK	AE07	T	TXCLK	AC07	T
PVDDA	0E25	PLL	RXD	0M05	T	TXD	0P05	O

Table 39: 2.5V V_{DD} Pins

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
VDD2500	0B04	Y	VDD2516	0M06	Y	VDD2532	0T12	Y
VDD2501	0B14	Y	VDD2517	0M10	Y	VDD2533	0T14	Y
VDD2502	0B22	Y	VDD2518	0M13	Y	VDD2534	0V02	Y
VDD2503	0D10	Y	VDD2519	0M16	Y	VDD2535	0V24	Y
VDD2504	0D16	Y	VDD2520	0M20	Y	VDD2536	0Y04	Y
VDD2505	0F04	Y	VDD2521	0M24	Y	VDD2537	0Y08	Y
VDD2506	0F08	Y	VDD2522	0N05	Y	VDD2538	0Y18	Y
VDD2507	0F18	Y	VDD2523	0N12	Y	VDD2539	0Y22	Y
VDD2508	0F22	Y	VDD2524	0N14	Y	VDD2540	AB10	Y
VDD2509	0H02	Y	VDD2525	0P06	Y	VDD2541	AB13	Y
VDD2510	0H24	Y	VDD2526	0P10	Y	VDD2542	AB16	Y
VDD2511	0K12	Y	VDD2527	0P13	Y	VDD2543	AC16	Y
VDD2512	0K14	Y	VDD2528	0P16	Y	VDD2544	AD04	Y
VDD2513	0L11	Y	VDD2529	0P20	Y	VDD2545	AD14	Y
VDD2514	0L15	Y	VDD2530	0R11	Y	VDD2546	AD22	Y
VDD2515	0M02	Y	VDD2531	0R15	Y	VDD2547	AE02	Y

Table 40: 3.3V V_{DD} Pins

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
VDD3300	0B08	Z	VDD3314	0H16	Z	VDD3328	0V10	Z
VDD3301	0B12	Z	VDD3315	0H20	Z	VDD3329	0V16	Z
VDD3302	0B18	Z	VDD3316	0K04	Z	VDD3330	0V20	Z
VDD3303	0D02	Z	VDD3317	0K08	Z	VDD3331	0Y12	Z
VDD3304	0D06	Z	VDD3318	0K18	Z	VDD3332	0Y14	Z
VDD3305	0D20	Z	VDD3319	0K22	Z	VDD3333	AB02	Z
VDD3306	0D24	Z	VDD3320	0N17	Z	VDD3334	AB06	Z
VDD3307	0E13	Z	VDD3321	0P02	Z	VDD3335	AB20	Z
VDD3308	0F12	Z	VDD3322	0P24	Z	VDD3336	AB24	Z
VDD3309	0F14	Z	VDD3323	0T04	Z	VDD3337	AD08	Z
VDD3310	0F25	Z	VDD3324	0T08	Z	VDD3338	AD12	Z
VDD3311	0G24	Z	VDD3325	0T18	Z	VDD3339	AD18	Z
VDD3312	0H06	Z	VDD3326	0T22	Z			
VDD3313	0H10	Z	VDD3327	0V06	Z			

Table 41: Ground Pins

Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element	Signal Name	Grid Position	Library Element
GND00	0B02	X	GND29	0K02	X	GND58	0T16	X
GND01	0B06	X	GND30	0K06	X	GND59	0T20	X
GND02	0B10	X	GND31	0K10	X	GND60	0T24	X
GND03	0B16	X	GND32	0K16	X	GND61	0V04	X
GND04	0B20	X	GND33	0K20	X	GND62	0V08	X
GND05	0B24	X	GND34	0K24	X	GND63	0V12	X
GND06	0D04	X	GND35	0L13	X	GND64	0V14	X
GND07	0D08	X	GND36	0M04	X	GND65	0V18	X
GND08	0D12	X	GND37	0M08	X	GND66	0V22	X
GND09	0D14	X	GND38	0M12	X	GND67	0Y02	X
GND10	0D18	X	GND39	0M14	X	GND68	0Y06	X
GND11	0D22	X	GND40	0M18	X	GND69	0Y10	X
GND12	0D25	X	GND41	0M22	X	GND70	0Y16	X
GND13	0F02	X	GND42	0N11	X	GND71	0Y20	X
GND14	0F06	X	GND43	0N13	X	GND72	0Y24	X
GND15	0F10	X	GND44	0N15	X	GND73	AA15	X
GND16	0F16	X	GND45	0N16	X	GND74	AB04	X
GND17	0F20	X	GND46	0N18	X	GND75	AB08	X
GND18	0F23	X	GND47	0P04	X	GND76	AB12	X
GND19	0F24	X	GND48	0P08	X	GND77	AB14	X
GND20	0H04	X	GND49	0P12	X	GND78	AB18	X
GND21	0H08	X	GND50	0P14	X	GND79	AB22	X
GND22	0H12	X	GND51	0P18	X	GND80	AD02	X
GND23	0H14	X	GND52	0P22	X	GND81	AD03	X
GND24	0H18	X	GND53	0R13	X	GND82	AD06	X
GND25	0H19	X	GND54	0T02	X	GND83	AD10	X
GND26	0H22	X	GND55	0T06	X	GND84	AD16	X
GND27	0J12	X	GND56	0T10	X	GND85	AD20	X
GND28	0J14	X	GND57	0T13	X	GND86	AD24	X

Table 42: Library Element Definitions (Page 1 of 2)

Element Name	Instances	Description	V_{IL} (V)		V_{IH} (V)		I_{IL} (@0V) Max	I_{IH} (@V_{DD}) Max	V_{OH} (V) Min	V_{OL} (V) Min	I_{OH} (mA) Min	I_{OL} (mA) Min	Note
			Min	Max	Min	Max							
A	86	-5.0V-Tolerant PCI Non-Test Three-state CIO	0.0	0.8	2.0	5.5	>0	<0	2.4	0.5	-	-	
B	14	-3.3V LVTTL Test 35 Ohm Three-State CIO	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	2.4	0.4	13.0/ 12.0	9.0	
C	51	-3.3V LVTTL Non-Test 35 Ohm Three-State CIO	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	2.4	0.4	13.0/ 12.0	9.0	
D	3	-3.3V LVTTL Test 50 Ohm Three-State CIO w/Pull-up	0.0	0.8	2.0	V_{DD}+ 0.6	-250µA	0	2.4	0.4	10.0	7.0	
E	16	-3.3V LVTTL Non-Test 50 Ohm Three-State CIO w/Pull-up	0.0	0.8	2.0	V_{DD}+ 0.6	-250µA	0	2.4	0.4	10.0	7.0	
F	4	-3.3V LVTTL Test 50 Ohm Three-State CIO	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	2.4	0.4	10.0	7.0	
G	52	-3.3V LVTTL Non-Test 50 Ohm Three-State CIO	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	2.4	0.4	10.0	7.0	
H	77	-5.0V-Tolerant LVTTL Non-Test 50 Ohm Three-State CIO	0.0	0.8	2.0	5.5	0	0	2.4	0.4	13.0/ 12.0	9.0	
J	3	-5.0V-Tolerant LVTTL Non-Test 50 Ohm Three-State CIO w/Pull-down	0.0	0.8	2.0	5.5	0	400µA	2.4	0.4	10.0	7.0	
K	8	-5.0V-Tolerant LVTTL Test 50 Ohm Three-State CIO w/Pull-up	0.0	0.8	2.0	5.5	-250µA	0	2.4	0.4	10.0	7.0	
L	13	-5.0V-Tolerant LVTTL Non-Test 50 Ohm Three-State CIO w/Pull-up	0.0	0.8	2.0	5.5	-250µA	0	2.4	0.4	10.0	7.0	
M	12	-5.0V-Tolerant LVTTL Non-Test 50 Ohm Three-State CIO	0.0	0.8	2.0	5.5	0	0	2.4	0.4	10.0	7.0	
N	3	-3.3V STI Non-Test Differential Receiver	-0.5	V_{REF} +0.5	V_{REF} +0.5	V_{DDQ} +0.3	0	0	-	-	-	-	1
P	1	-3.3V STI Non-Test Differential Driver	V_{OH} minimum voltage: V_{DDQ} = -0.4V V_{OL} maximum voltage = 0.4V								10.0	7.0	1
Q	1	-3.3V LVTTL Test DI1 Receiver w/Pull-up	0.0	0.8	2.0	V_{DD}+ 0.6	0	400µA	-	-	-	-	
R	1	-3.3V LVTTL Test DI2 Receiver w/Pull-up	0.0	0.8	2.0	V_{DD}+ 0.6	0	400µA	-	-	-	-	
S	4	-3.3V LVTTL Test Receiver w/Pull-up	0.0	0.8	2.0	V_{DD}+ 0.6	0	400µA	-	-	-	-	

1. V_{REF} = Differential Input Voltage. V_{DDQ} = Output Supply Voltage.

Table 42: Library Element Definitions (Page 2 of 2)

Element Name	Instances	Description	V_{IL} (V)		V_{IH} (V)		I_{IL} (@0V) Max	I_{IH} (@V_{DD}) Max	V_{OH} (V) Min	V_{OL} (V) Min	I_{OH} (mA) Min	I_{OL} (mA) Min	Note
			Min	Max	Min	Max							
T	1	-3.3V LVTTL Test RI Receiver	0.0	0.8	2.0	V_{DD}+ 0.6	0	400µA	-	-	-	-	
V	1	-5.0V-Tolerant LVTTL Test LT w/Pull-up	0.0	0.8	2.0	5.5	0	400µA	-	-	-	-	
W	23	-5.0V-Tolerant LVTTL Test Receiver w/Pull-up	0.0	0.8	2.0	5.5	0	400µA	-	-	-	-	
X	2	-5.0V-Tolerant LVTTL Test Receiver	0.0	0.8	2.0	5.5	0	0	-	-	-	-	
Z	4	-3.3V Non-Test 20 Ohm	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	2.4	0.4	23.0/ 12.0	16.0	
PLL	3	PLL (Phase Locked Loop that Connects at I/O Pads)	0.0	0.8	2.0	V_{DD}+ 0.6	0	0	-	-	-	-	

1. V_{REF} = Differential Input Voltage. V_{DDQ} = Output Supply Voltage.

5. AC Timing Characteristics

Table 43: I/O PCI Bus Timing (Page 1 of 2)

Description	Min	Max	Units
PCICLK High to PAD(31:0)	2	6	ns
PCICLK High to PPAR	2	6	ns
PCICLK High to PCBE(3:0)	2	6	ns
PCICLK High to $\overline{\text{MFRAME}}$	2	6	ns
PCICLK High to $\overline{\text{MTRDY}}$	2	6	ns
PCICLK High to $\overline{\text{MIRDY}}$	2	6	ns
PCICLK High to $\overline{\text{MSTOP}}$	2	6	ns
PCICLK High to $\overline{\text{MDEVSEL}}$	2	6	ns
PCICLK High to $\overline{\text{MREQ}}$	2	6	ns
PCICLK High to $\overline{\text{MPERR}}$	2	6	ns
PCICLK High to $\overline{\text{MSERR}}$	2	6	ns
PCICLK High to $\overline{\text{MINTA}}$	2	6	ns
PCICLK High to $\overline{\text{MINT2}}$	2	6	ns
PCICLK High to $\overline{\text{MREQ64}}$	2	6	ns
PCICLK High to PPAR64	2	6	ns
PCICLK High to PAD64(63:32)	2	6	ns
PCICLK High to MACK64	2	6	ns
$\overline{\text{MFRAME}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MFRAME}}$ to PCICLK Hold	0	—	ns
PCBE(3:0) to PCICLK Setup	3	—	ns
PCBE(3:0) to PCICLK Hold	0	—	ns
PAD(31:0) to PCICLK Setup	3	—	ns
PAD(31:0) to PCICLK Hold	0	—	ns
PPAR to PCICLK Setup	3	—	ns
PPAR to PCICLK Hold	0	—	ns
$\overline{\text{MPERR}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MPERR}}$ to PCICLK Hold	0	—	ns
PIDSEL to PCICLK Setup	3	—	ns
PIDSEL to PCICLK Hold	0	—	ns
$\overline{\text{MDEVSEL}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MDEVSEL}}$ to PCICLK Hold	0	—	ns
$\overline{\text{MTRDY}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MTRDY}}$ to PCICLK Hold	0	—	ns
$\overline{\text{MIRDY}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MIRDY}}$ to PCICLK Hold	0	—	ns

Table 43: I/O PCI Bus Timing (Page 2 of 2)

Description	Min	Max	Units
$\overline{\text{MSTOP}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MSTOP}}$ to PCICLK Hold	0	—	ns
$\overline{\text{MGNT}}$ to PCICLK Setup	3	—	ns
$\overline{\text{MGNT}}$ to PCICLK Hold	0	—	ns
PCBE64(7:4) to PCICLK Setup	3	—	ns
PCBE64(7:4) to PCICLK Hold	0	—	ns

Table 44: Memory Timing

Description	Min	Max	Units
CMCLK High to CMADDR (20:0)	1	5.5	ns
CMCLK High to $\overline{\text{CMSYNRAS}}$ (1:0)	1	5.5	ns
CMCLK High to $\overline{\text{CMSYNCAS}}$ (1:0)	1	5.5	ns
CMCLK High to $\overline{\text{CM0DQM}}$ (3:0)	1	5.5	ns
CMCLK High to $\overline{\text{CM0CS}}$ (3:0)	1	5.5	ns
CMCLK High to $\overline{\text{CMWE}}$ (1:0)	1	5.5	ns
CMCLK High to CMCLKE	1	5.5	ns
CMCLK High to CMDATA (38:0) - Write	1	5.5	ns
CMDATA (38-0) TO CMCLK Setup - Read	2.1	—	ns
CMDATA (38-0) TO CMCLK Hold - Read	1.5	—	ns
PMCLK High to PMADDR (20:0)	1	5.5	ns
PMCLK High to $\overline{\text{PMSYNRAS}}$ (1:0)	1	5.5	ns
PMCLK High to $\overline{\text{PMSYNCAS}}$ (1:0)	1	5.5	ns
PMCLK High to $\overline{\text{PM0DQM}}$ (3:0)	1	5.5	ns
PMCLK High to $\overline{\text{PM0CS}}$ (3:0)	1	5.5	ns
PMCLK High to $\overline{\text{PMWE}}$ (1:0)	1	5.5	ns
PMCLK High to PMCLKE	1	5.5	ns
PMCLK High to PMDATA (38:0) - Write	1	5.5	ns
PMDATA (38-0) TO PMCLK Setup - Read	2.1	—	ns
PMDATA (38-0) TO PMCLK Hold - Read	1.5	—	ns

Table 45: NPBUS Timing

Description	Min	Max	Units
PINTCLK High to PBDATA(7:0)	2	6	ns
PINTCLK High to PBDATAP	2	6	ns
PINTCLK High to PBRNWRT	2	6	ns
PINTCLK High to PBRDRDY	2	6	ns
PINTCLK High to PBADDR(15:0)	2	6	ns
PBDATA(7:0) to PINTCLK Setup	15	—	ns
PBDATA(7:0) to PINTCLK Hold	0	—	ns
PBDATAP to PINTCLK Setup	15	—	ns
PBDATAP to PINTCLK Hold	0	—	ns
PBRDRDY to PINTCLK Setup	15	—	ns
PBRDRDY to PINTCLK Hold	0	—	ns
PBRNWRT to PINTCLK Setup	15	—	ns
PBRNWRT to PINTCLK Hold	0	—	ns

Table 46: PHY Timing

Description	Min	Max	Units
FYTWRB High to FYTDAT(15:0)	2	10	ns
FYTWRB High to FYTPAR(1:0)	2	10	ns
FYTWRB High to FYTSOC, $\overline{\text{FY0TENB}}$, FYTMOD, FYTEOP, FYTADR(4:0)	2	10	ns
FYTCA to FYTWRB Setup	3	—	ns
FYTCA to FYTWRB Hold	1	—	ns
$\overline{\text{FY0FUL}}$ to FYTWRB Setup	3	—	ns
$\overline{\text{FY0FUL}}$ to FYTWRB Hold	1	—	ns
FYRRDB High to $\overline{\text{FY0RENB}}$, FYRADR(4:0)	2	10	ns
FYRDAT(15:0) to FYRRDB Setup	3	—	ns
FYRDAT(15:0) to FYRRDB Hold	1	—	ns
FYRPAR(1:0) to FYRRDB Setup	3	—	ns
FYRPAR(1:0) to FYRRDB Hold	1	—	ns
FYRSOC to FYRRDB Setup	3	—	ns
FYRSOC to FYRRDB Hold	1	—	ns
$\overline{\text{FY0FUL}}$ to FYRRDB Setup	3	—	ns
$\overline{\text{FY0FUL}}$ to FYRRDB Hold	1	—	ns
$\overline{\text{FY0EMP}}$ to FYRRDB Setup	3	—	ns
$\overline{\text{FY0EMP}}$ to FYRRDB Hold	1	—	ns
FY0DISCRD to FYRRDB Setup	3	—	ns
FY0DISCRD to FYRRDB Hold	1	—	ns
FYDTCT to FYRRDB Setup	3	—	ns
FYDTCT to FYRRDB Hold	1	—	ns
FYRCA to FYRRDB Setup	3	—	ns
FYRCA to FYRRDB Hold	1	—	ns
FYRMOD to FYRRDB Setup	3	—	ns
FYRMOD to FYRRDB Hold	1	—	ns
FYREOP to FYRRDB Setup	3	—	ns
FYREOP to FYRRDB Hold	1	—	ns

Figure 38: SDRAM Read Cycle (1 of 2)

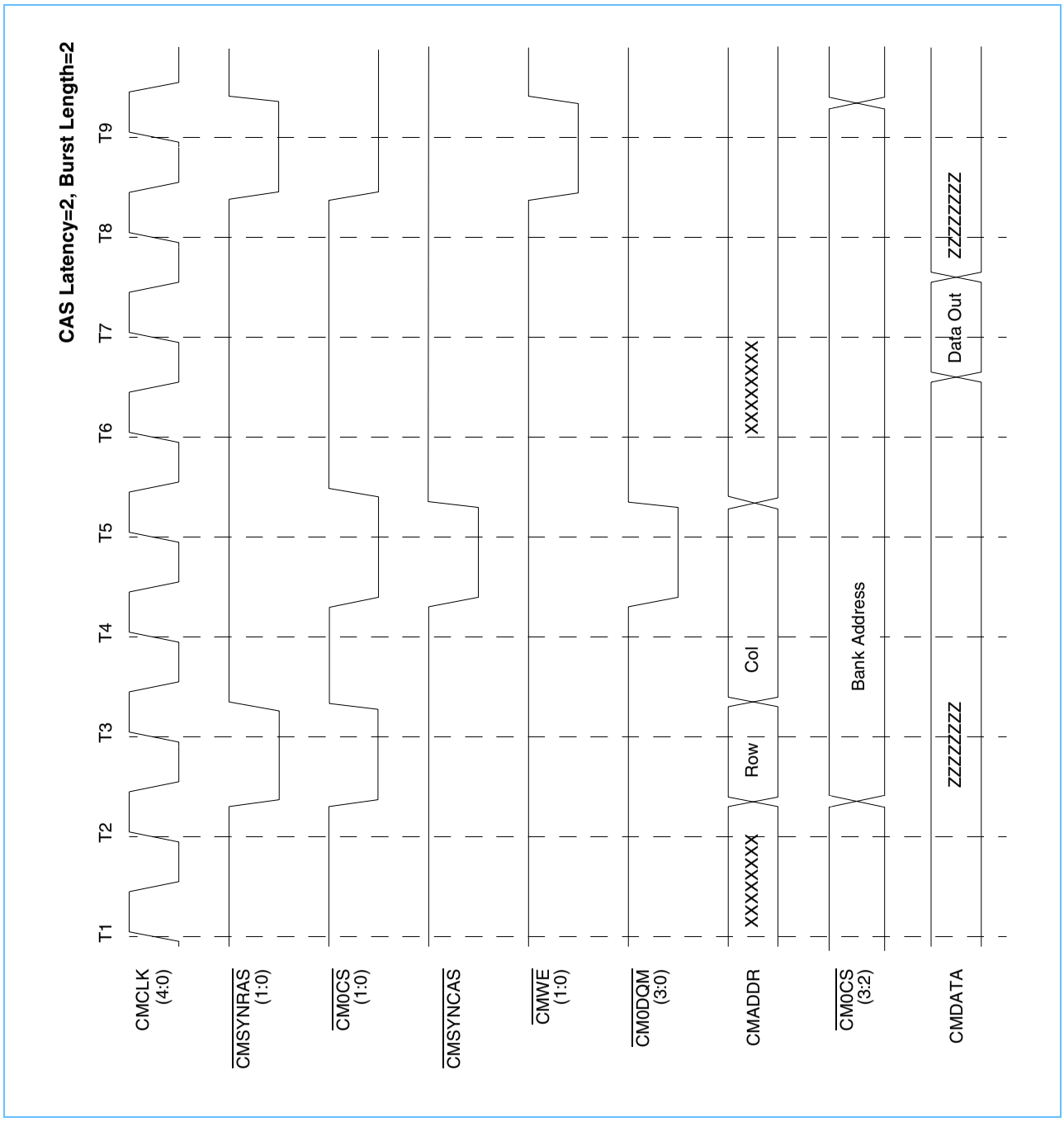


Figure 39: SDRAM Read Cycle (2 of 2)

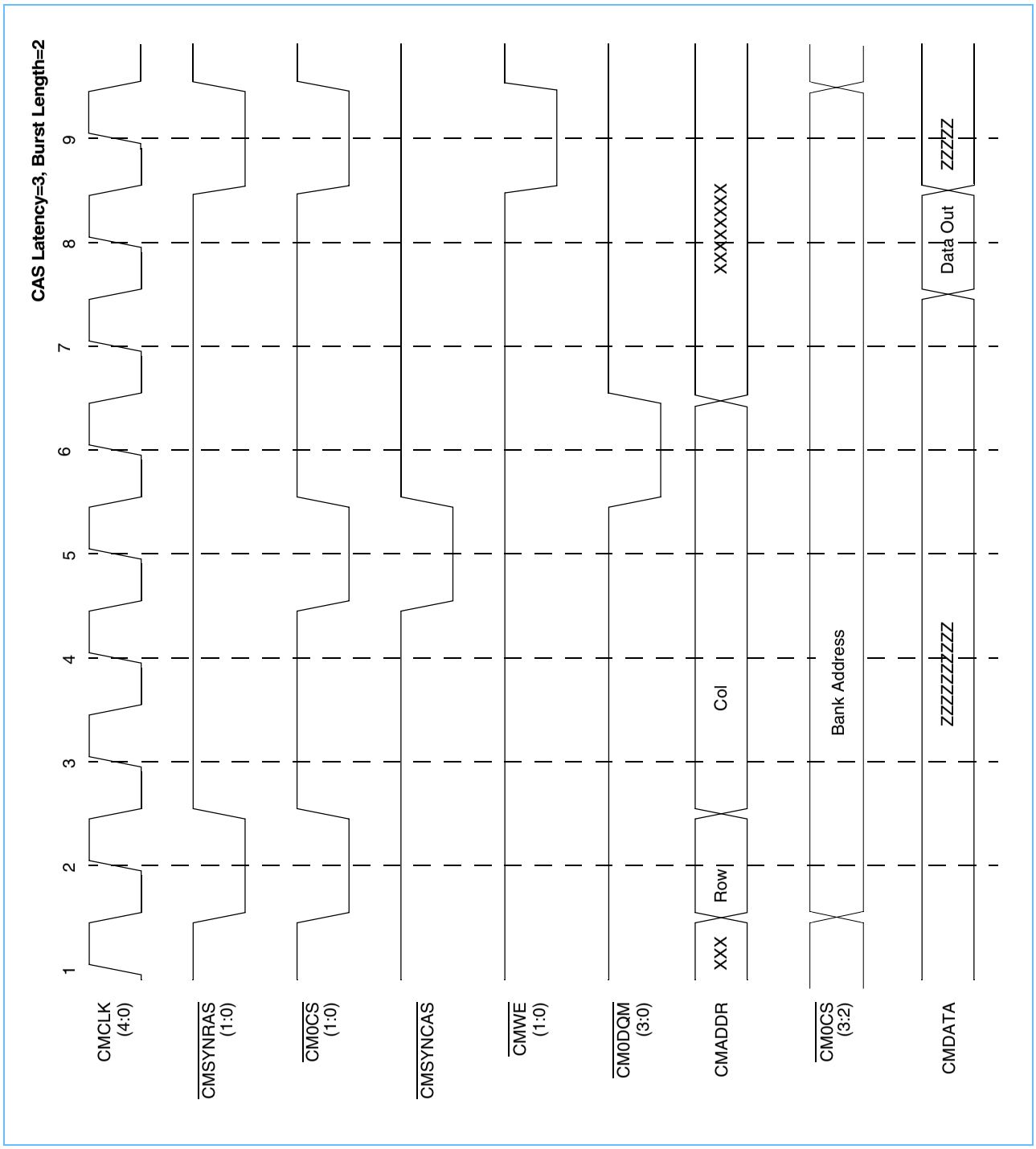


Figure 40: SDRAM Write Cycle (1 of 2)

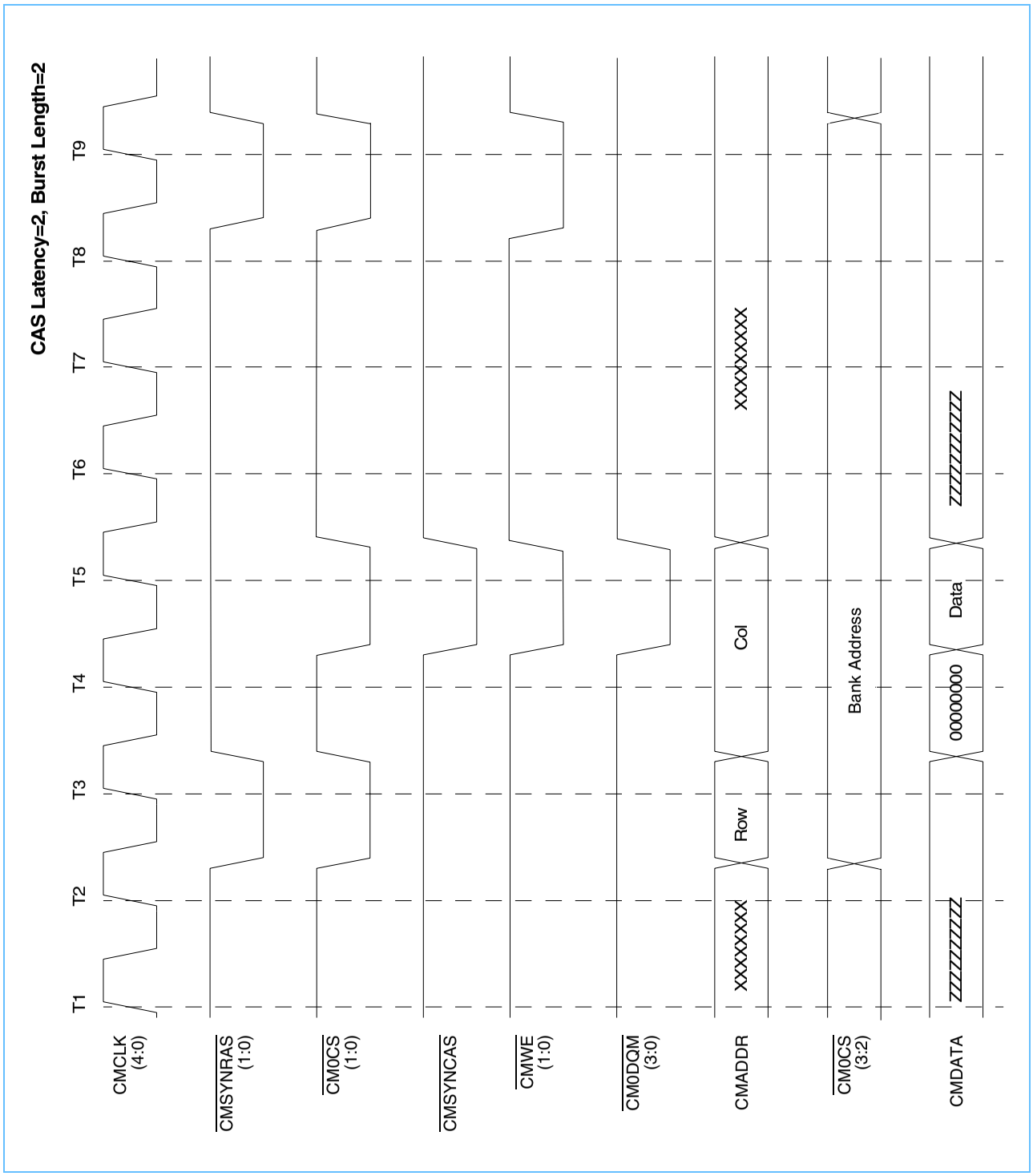


Figure 41: SDRAM Write Cycle (2 of 2)

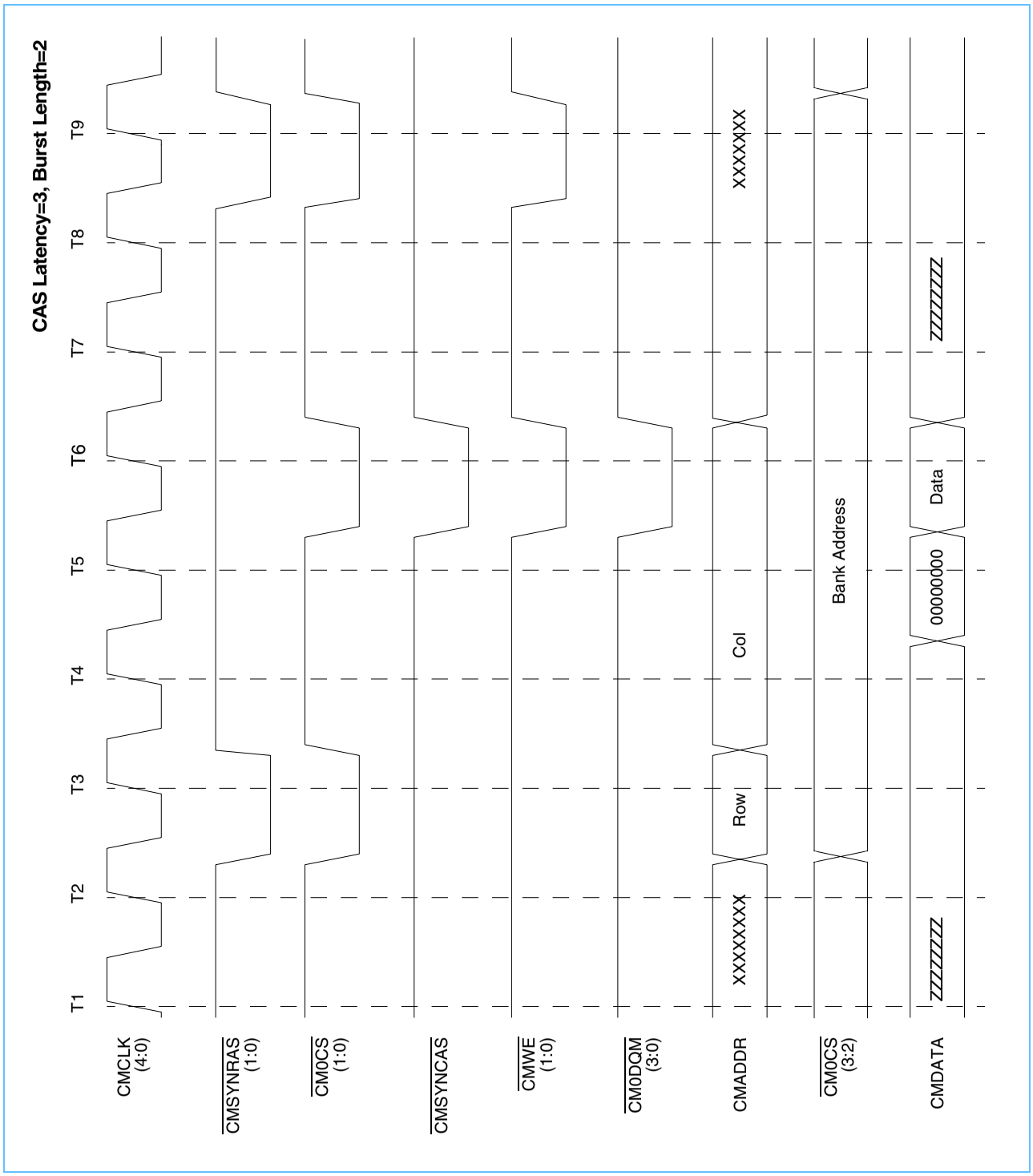


Figure 42: SDRAM Write of 64-byte Burst with CAS Latency=2

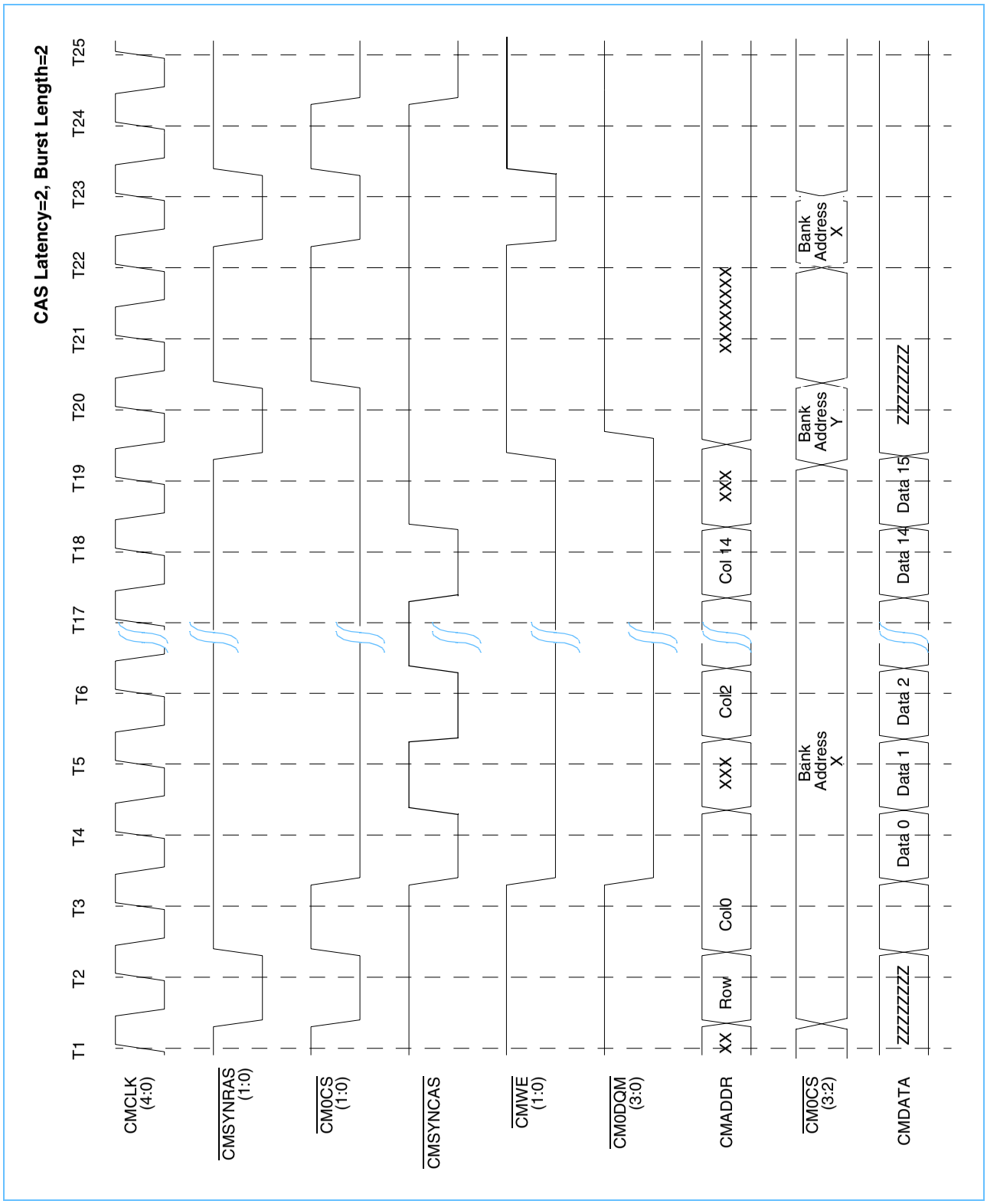
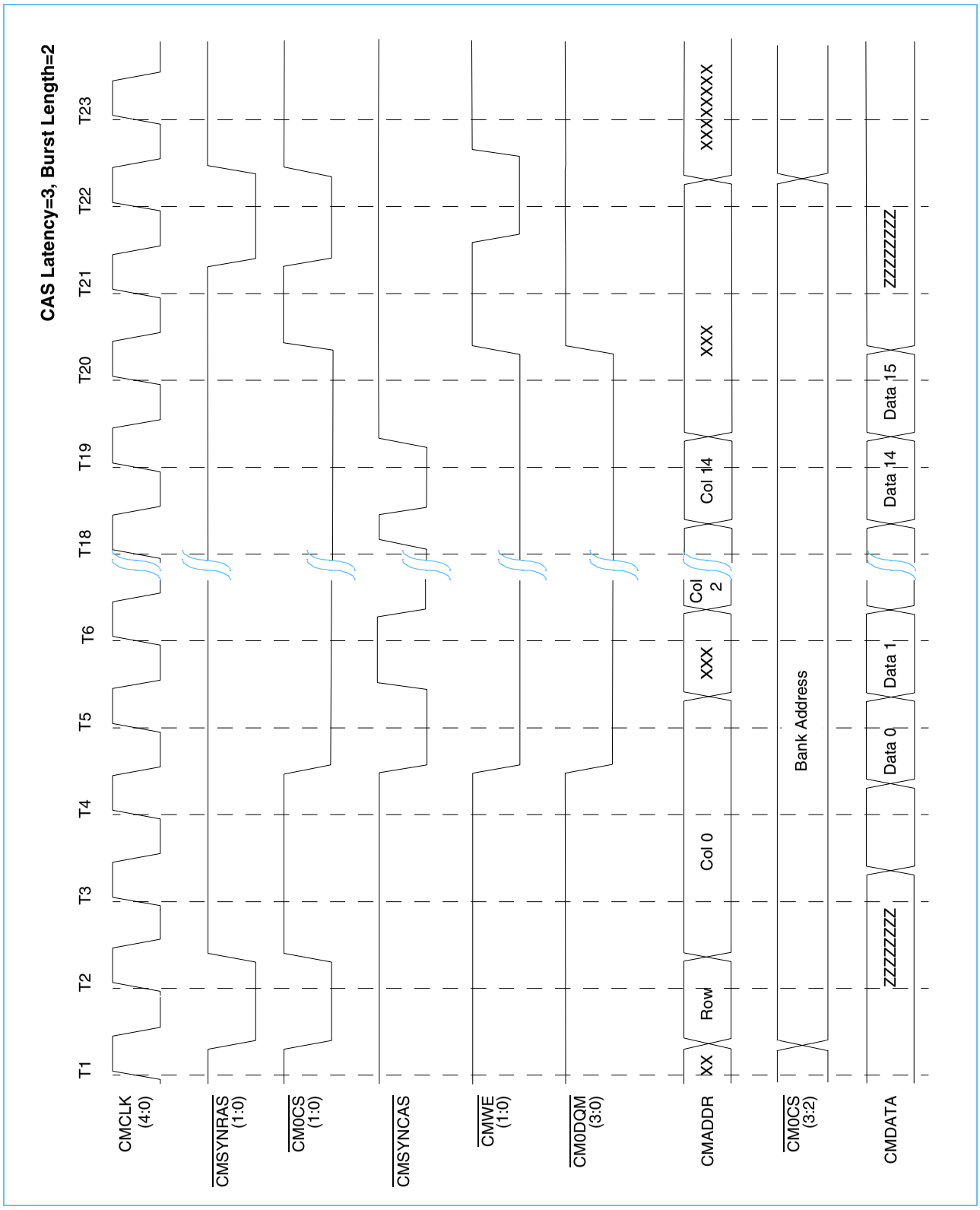


Figure 43: SDRAM Write of 64-byte Burst with CAS Latency=3



5.1 SRAM Timing Diagrams

Figure 44: SRAM Read Cycle

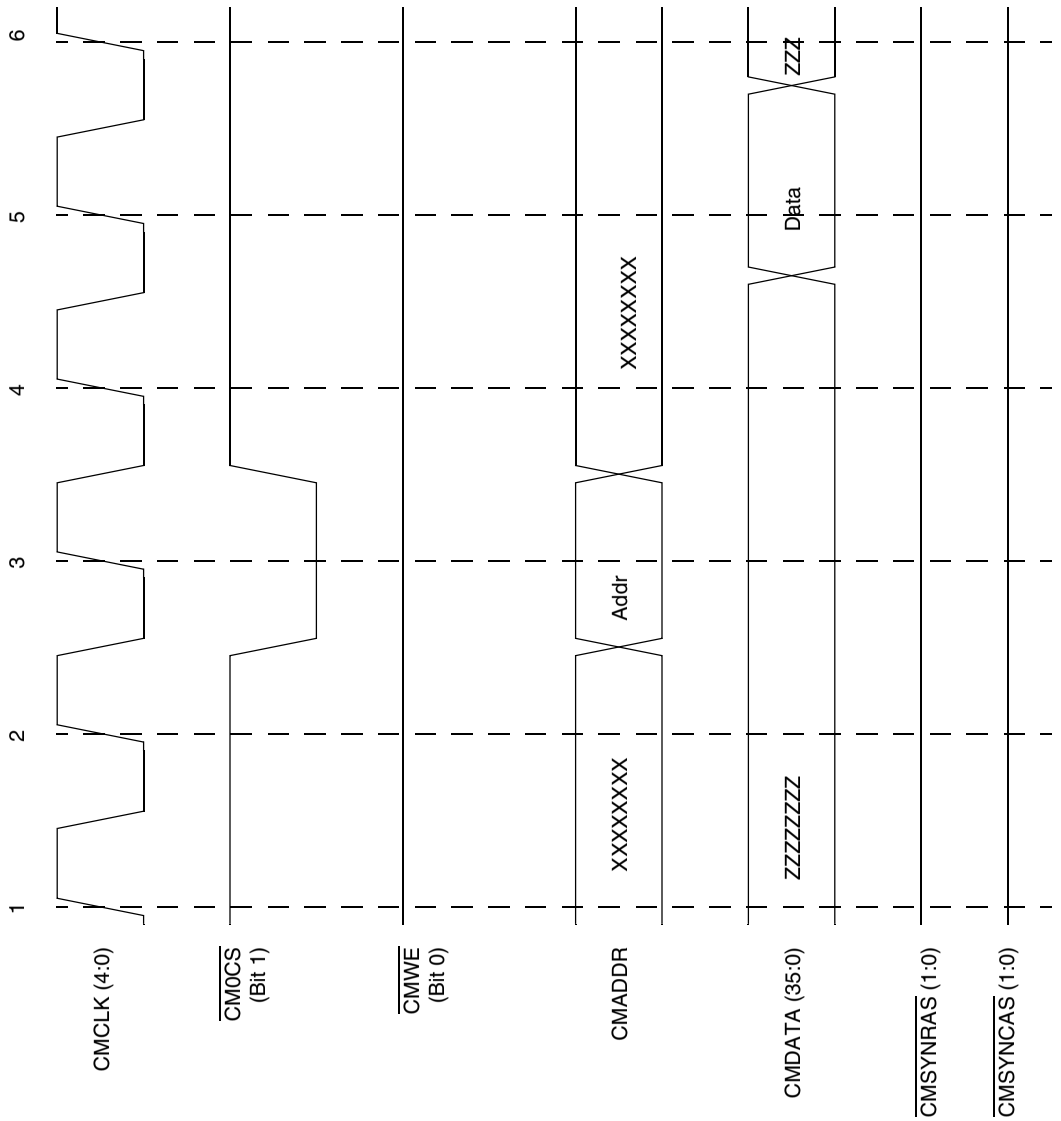


Figure 45: SRAM Write Cycle

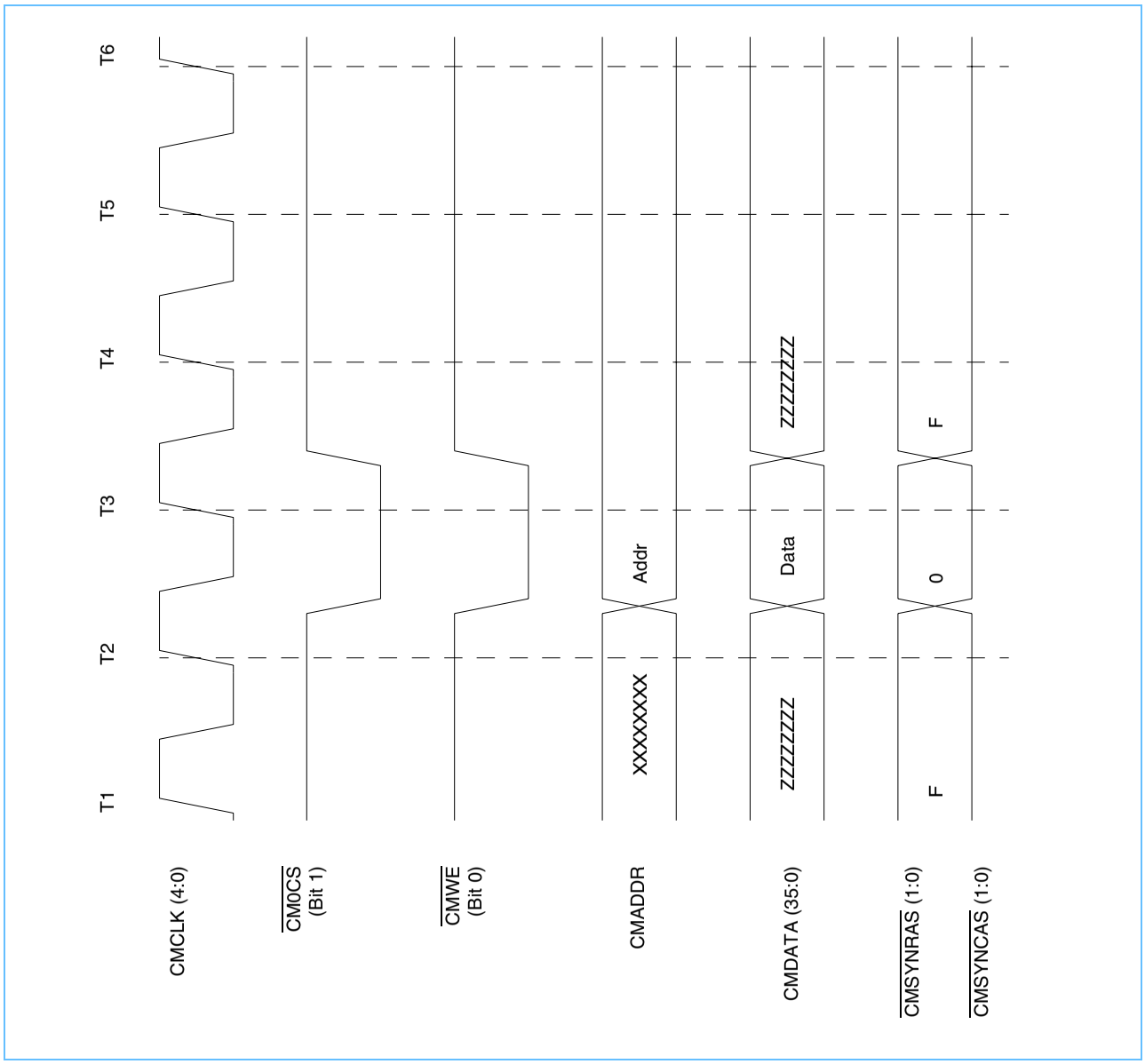


Figure 46: SRAM Read Cycle with Byte Enables

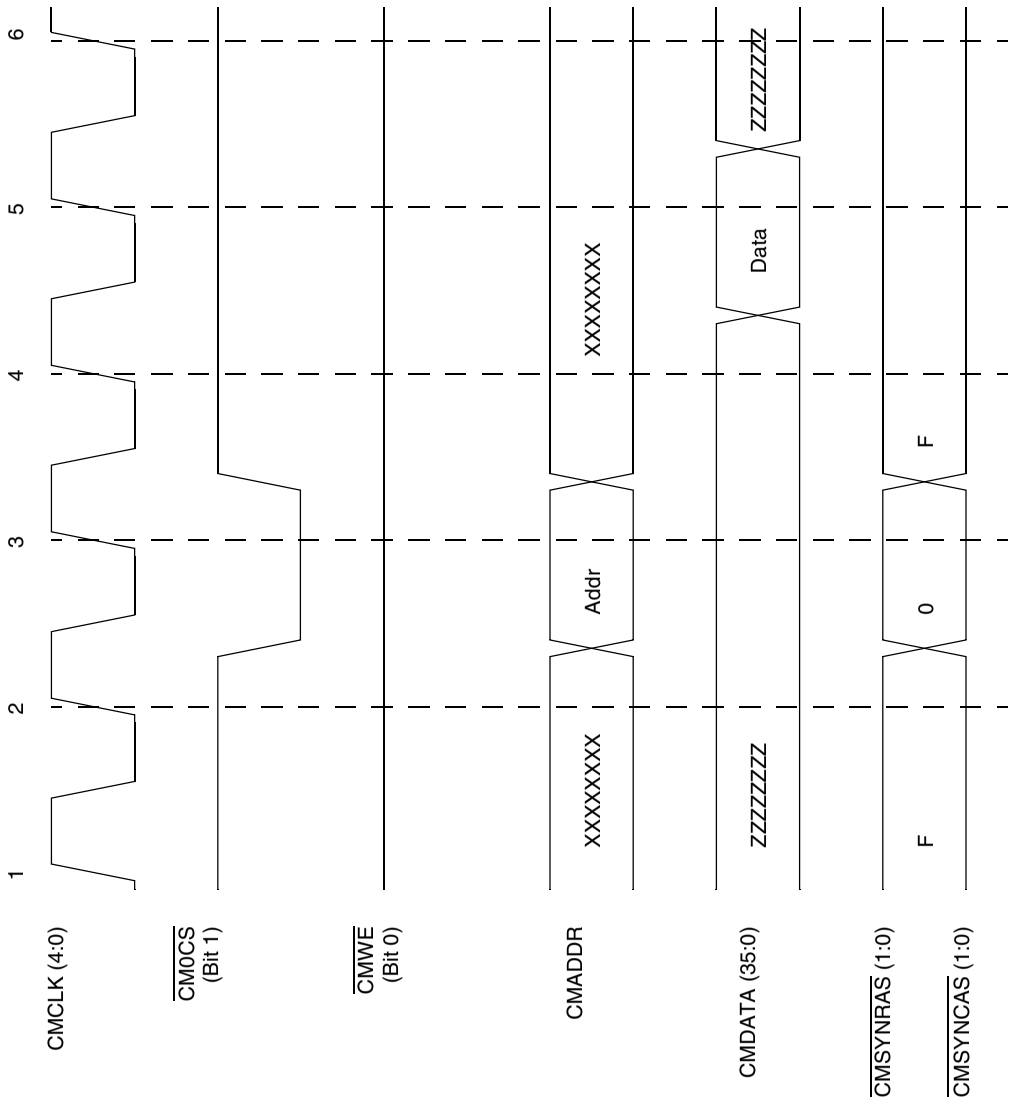
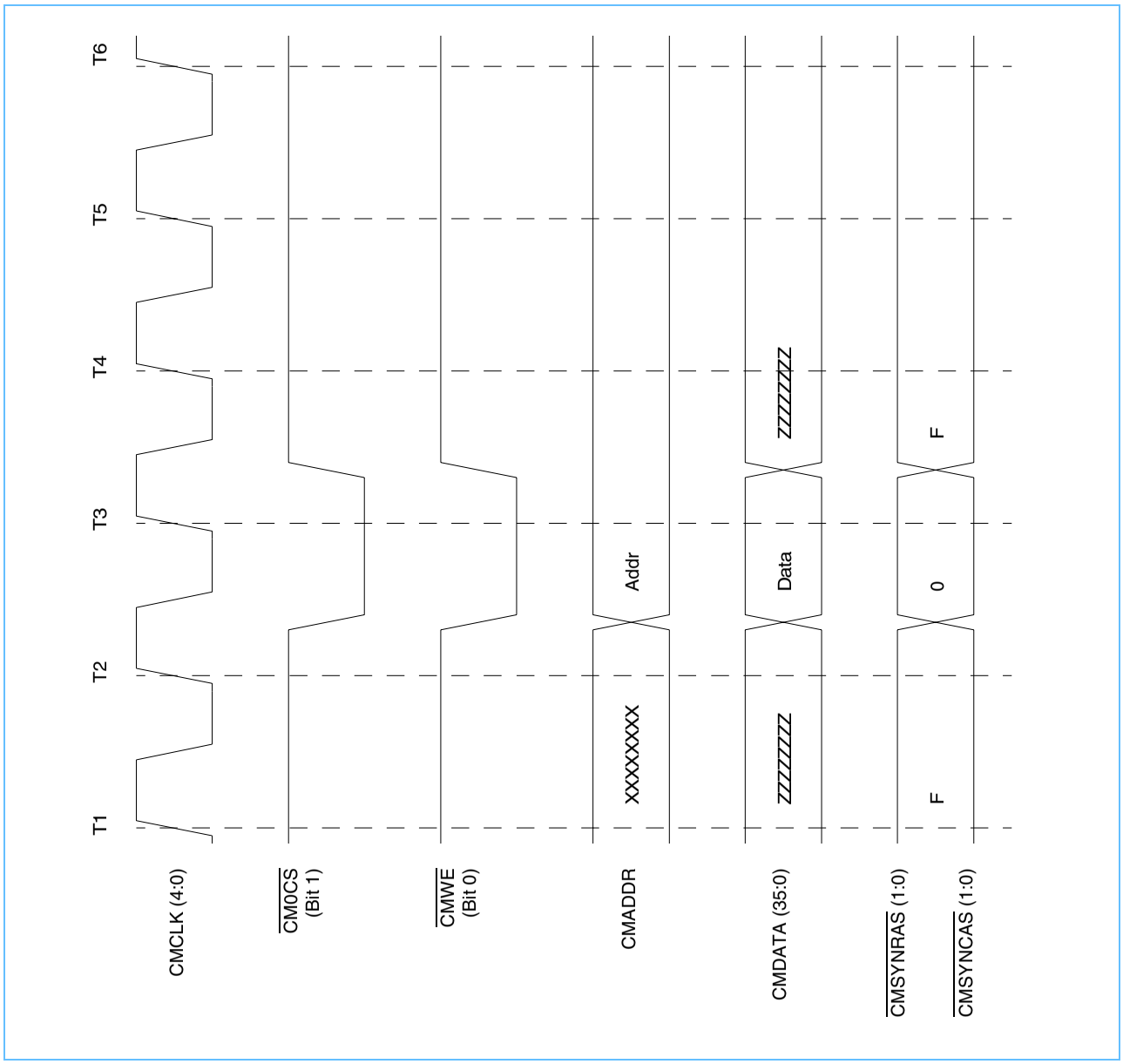


Figure 47: SRAM Write Cycle with Byte Enables



5.2 EPROM Timing Diagrams

Figure 48: Parallel EPROM Read

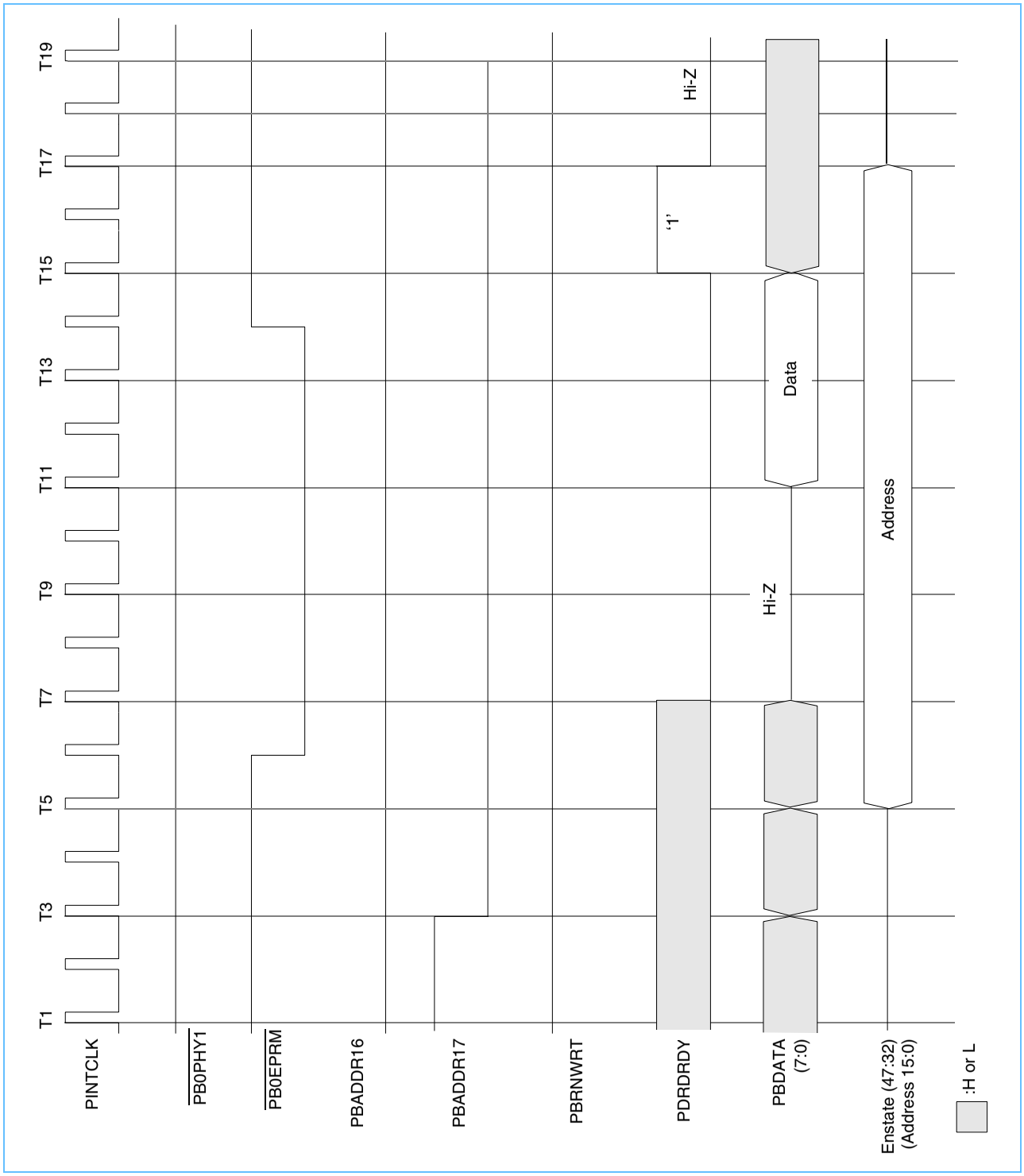


Figure 49: Parallel EPROM Write

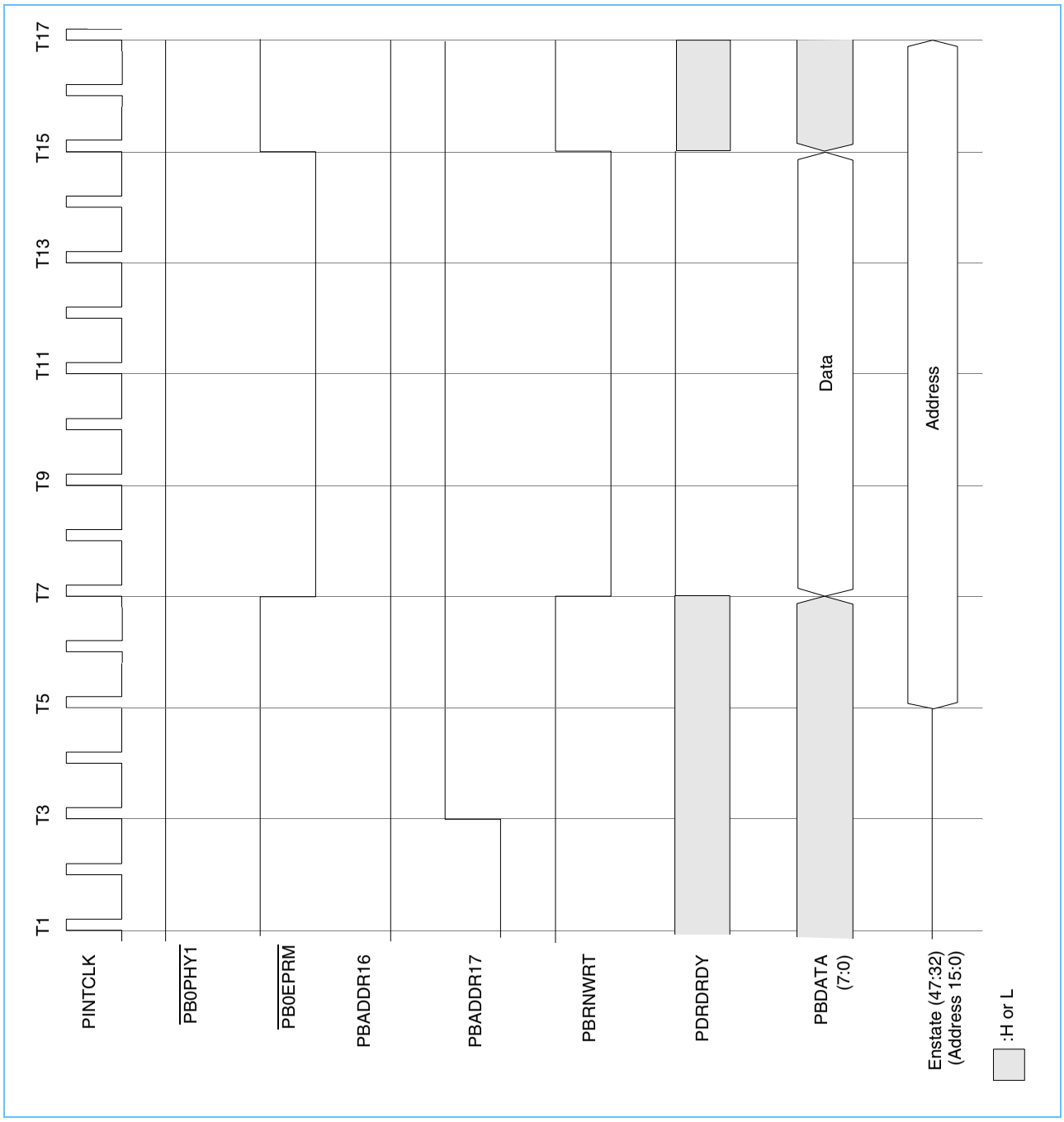


Figure 50: Serial EPROM Read

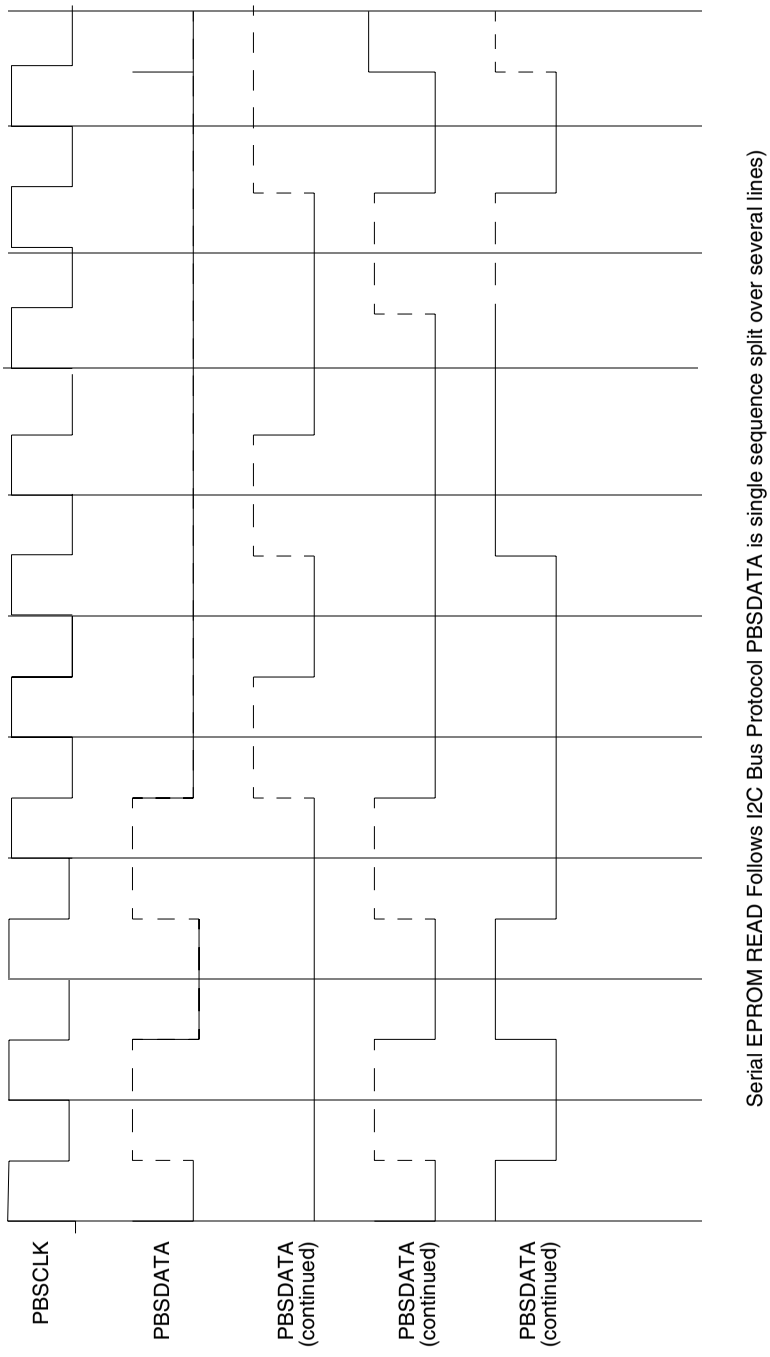
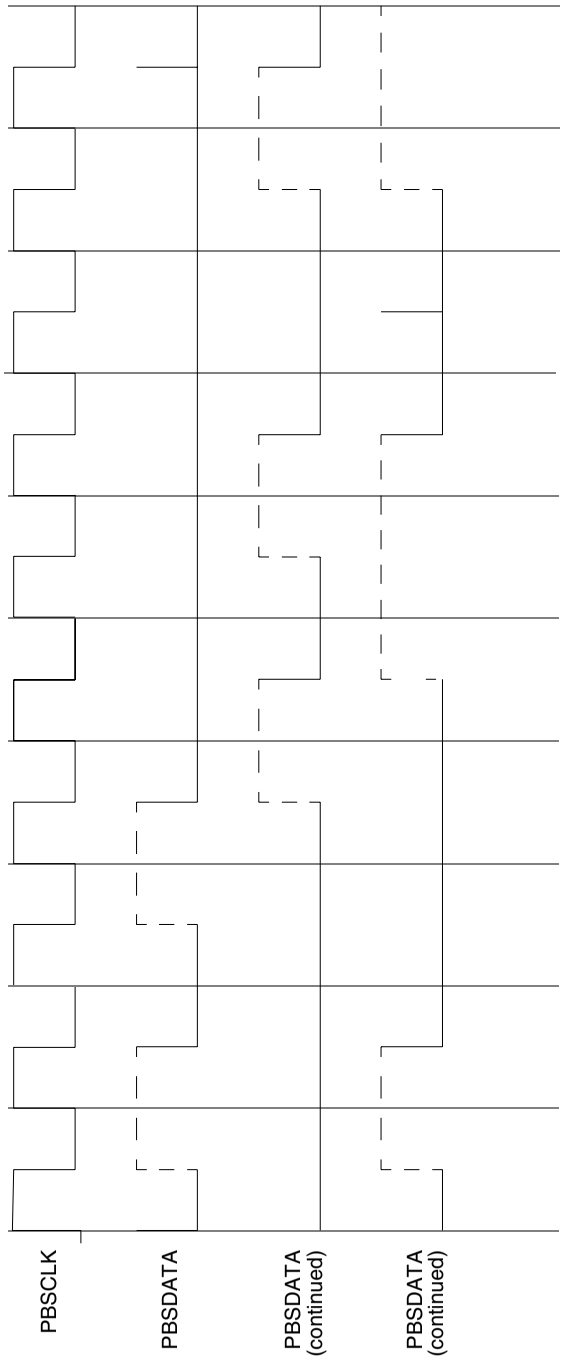


Figure 51: Serial EPROM Write



5.3 PHY Timing Diagrams

Figure 52: PHY Read

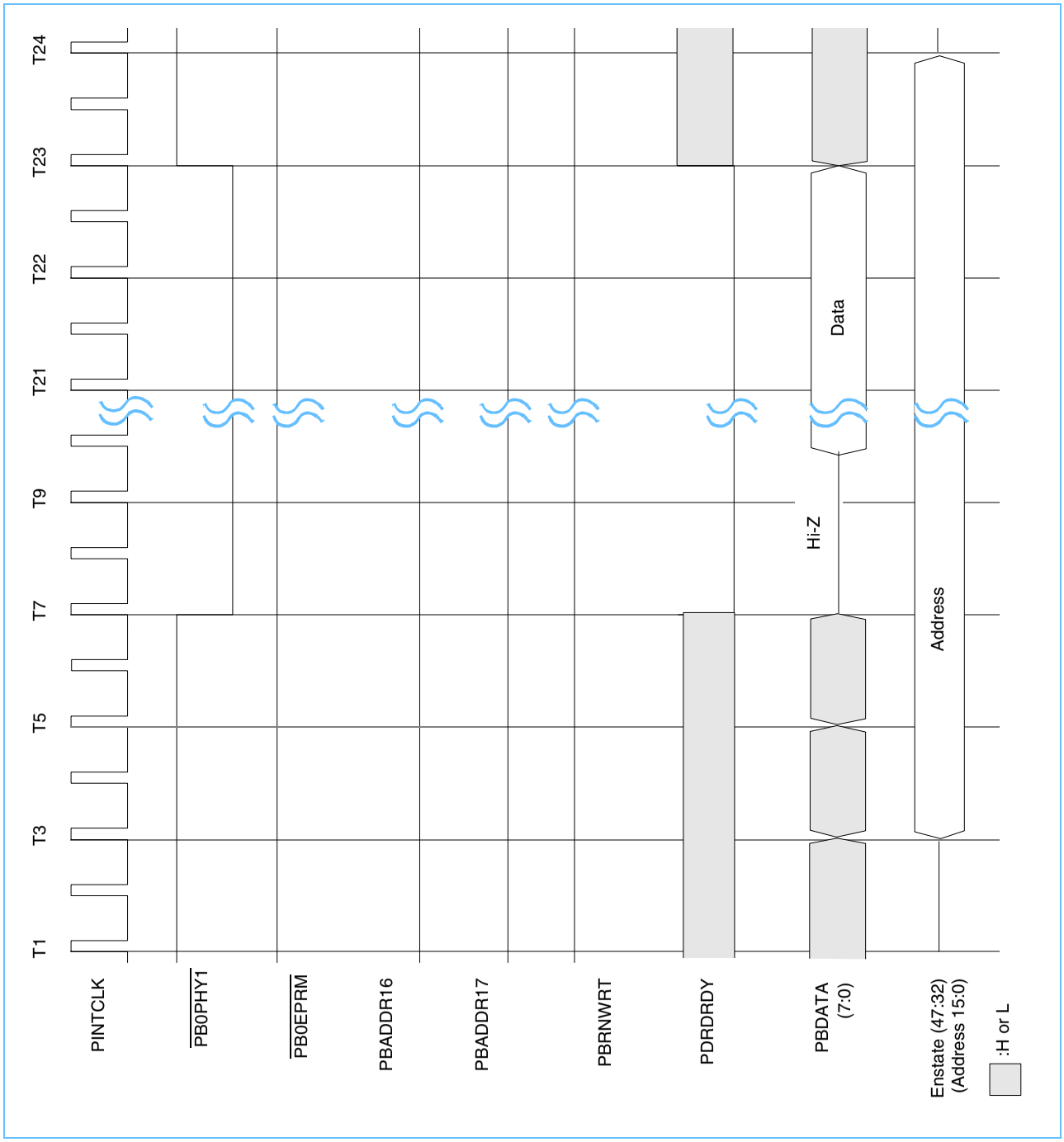
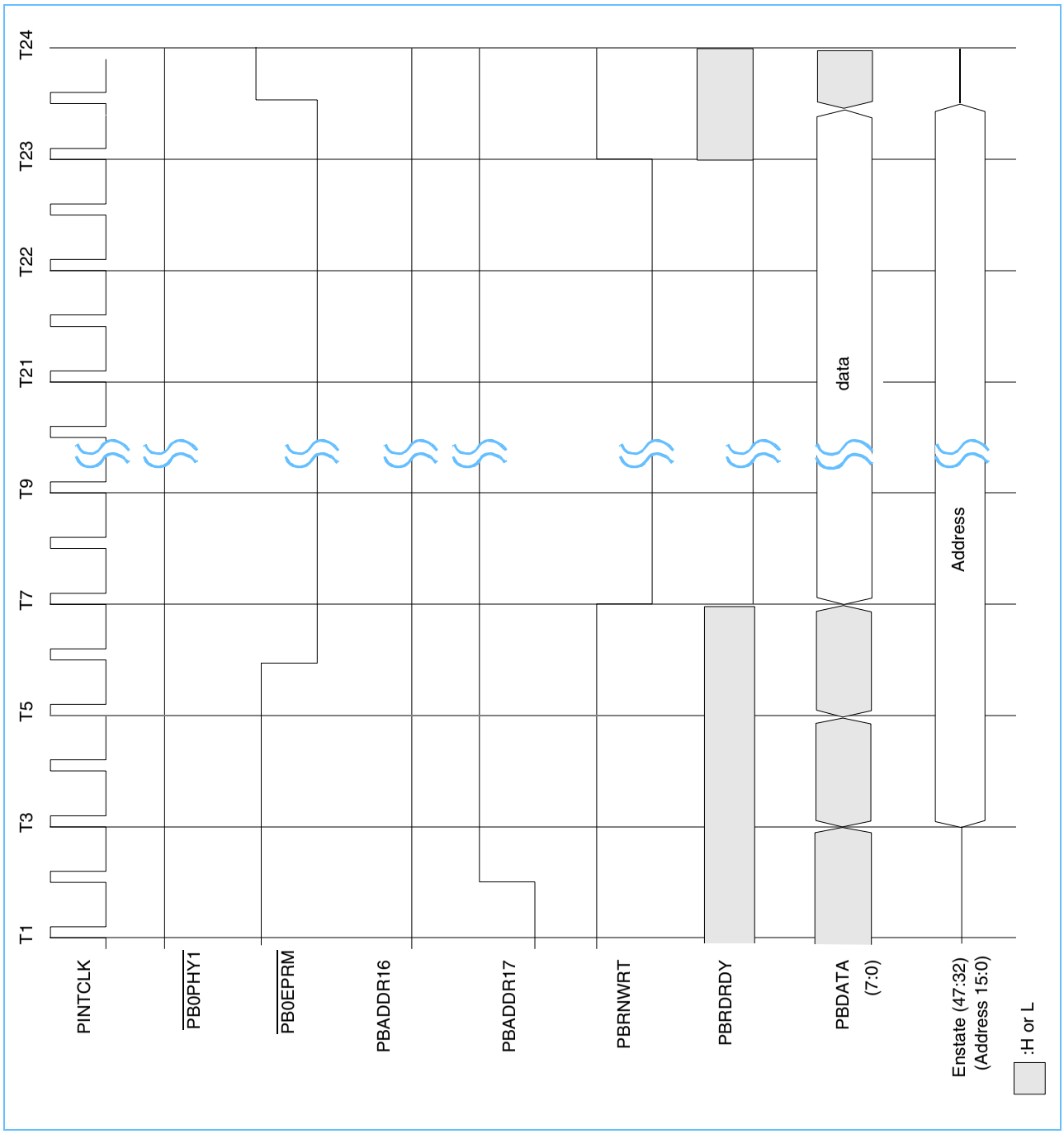


Figure 53: PHY Write



6. Electrical Ratings

Table 47: Absolute Maximum Ratings

Parameter	Rating	Unit	Note
Supply Voltage, V_{DD250}	2.3 to 2.7	V	1
Supply Voltage, V_{DD330}	3.0 to 3.6	V	1
Storage Temperature	-65 to 150	°C	1
Ambient Temperature with Power Applied	-40 to 100	°C	1

1. These are the maximum ratings that can be applied to the device without damage. The device function and specifications are valid only within the Recommended Operating Conditions.

Table 48: Recommended Operating Conditions

Parameter	Rating	Unit
Junction Temperature	0 to 85	°C
Supply Voltage, V_{DD250}, with respect to Ground	2.6 ± 2%	V
Supply Voltage, V_{DD330}, with respect to Ground	3.3 ± 5%	V

Table 49: Power Dissipation

Parameter	Rating	Unit
V_{DD250} (nominal)	6	W
V_{DD330} (nominal)	2	W

Table 50: DC Electrical Characteristics I (Page 1 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
V_{IL}	**Input Low Voltage**				
	A B C	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO	-.06	0.7	V
	D E F G H I J K L M N O p Q R S T U V W PLL	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Phase Locked Loop that Connects at I/O Pads	-0.6	0.8	V
	X Y Z	Programmable Ground Programmable V_{DD250} Programmable V_{DD330}	-	-	

Table 50: DC Electrical Characteristics I (Page 2 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
V_{IH}	**Input High Voltage**				
	A	2.5V CMOS Non-Test 35 Ohm Three-State CIO	1.7	V_{DD} +0.6	V
	D E	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO	2	5.5	V
	B C F G H I J K L M N O P Q R S T U V W PLL	2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Phase Locked Loop that Connects at I/O Pads	2	V_{DD} 2 + 0.6	V
	X Y Z	Programmable Ground Programmable V_{DD250} Programmable V_{DD330}	-	-	-

Table 50: DC Electrical Characteristics I (Page 3 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
$I_{IL\ (@0V)}$	**Input Low Current**				
	A B C F G H J K L M Q R S T U V PLL	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver Phase Locked Loop that Connects at I/O Pads		0	µA
	I N O P W	3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down		-250	µA
	D E	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO		>0	µA
	X Y Z	Programmable Ground Programmable V_{DD250} Programmable V_{DD330}		-	-

Table 50: DC Electrical Characteristics I (Page 4 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
I_{IH} ($@V_{DD}$)	**Input High Current**				
	A B C F G I J K N O P W PLL	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Phase Locked Loop that Connects at I/O Pads		0	µA
	H L M Q R S T U V	3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver		400uA	µA
	D E	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO		<0	µA
	X Y Z	Programmable Ground Programmable V_{DD250} Programmable V_{DD330}		-	–

Table 50: DC Electrical Characteristics I (Page 5 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
V_{OH}	**Output High Voltage**				
	A B C	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO	2		V
	D E F G H I J K L M N O p	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	2.4		V
	Q R S T U V W X Y Z PLL	3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Programmable Ground Programmable V_{DD250} ProgrammableV_{DD330} Phase Locked Loop that Connects at I/O Pads	-		V

Table 50: DC Electrical Characteristics I (Page 6 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
V_{OL}	**Output Low Voltage**				
	A B C F G H I J K L M N O p	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO 3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	0.4		V
	D E	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO	0.5		V
	Q R S T U V W X Y Z PLL	3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Programmable Ground Programmable V_{DD250} Programmable V_{DD330} Phase Locked Loop that Connects at I/O Pads	-		V

Table 50: DC Electrical Characteristics I (Page 7 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
I_{OH}	**Output High Current**				
	P	3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	09/19		mA
	A C	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO	10/18		mA
	J K L M N O	3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	12/19		mA
	B	2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO	19/18		mA
	G H I	3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	19/19		mA
	F	3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec)	40/19		mA
	D E Q R S T U V W X Y Z PLL	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Programmable Ground Programmable V_{DD250} Programmable V_{DD330} Phase Locked Loop that Connects at I/O Pads	-		mA

Table 50: DC Electrical Characteristics I (Page 8 of 8)
($0°C \leq T_A \leq 85°C$; $V_{DD250} = 2.5V \pm 0.2V$, $V_{DD330} = 3.3V \pm 0.3V$)

Symbol	Library Element	Parameter and Conditions	Min	Max	Units
I_{OL}	**Output Low Current**				
	G H I	3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 35 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	12/19		mA
	A C	2.5V CMOS Non-Test 35 Ohm Three-State CIO 2.5V CMOS (3.3V Protected) Nontest 35 Ohm Three-State CIO	13/18		mA
	F	3.3V LVTTL Nontest 20 Ohm Three-State CIO (3.3V Rec)	25/19		mA
	B	2.5V CMOS (3.3V Protected) Nontest 20 Ohm Three-State CIO	26/18		mA
	P	3.3V LVTTL Test 65 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	6/19		mA
	J K L M N O	3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Down 3.3V LVTTL Nontest 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up 3.3V LVTTL Test 50 Ohm Three-State CIO (3.3V Rec) w/Pull-Up	8/19		mA
	D E Q R S T U V W X Y Z PLL	3.3V/5V-Tolerant PCI Nontest Three-State CIO 3.3V/5V-Tolerant PCI Test Three-State CIO 3.3V LVTTL Test DI1 Receiver w/Pull-Up 3.3V LVTTL Test DI2 Receiver w/Pull-Up 3.3V LVTTL Leakage Test Receiver w/Pull-Up 3.3V LVTTL Test Receiver w/Pull-Up 3.3V LVTTL Test RI/TT Receiver 3.3V LVTTL Test Receiver 3.3V LVTTL Test Reference Enable (TE) Receiver w/Pull-Down Programmable Ground Programmable V_{DD250} Programmable V_{DD330} Phase Locked Loop that Connects at I/O Pads	-		mA
V_{ICM}	**Differential Common Mode Voltage**				
	DA	Low-Voltage Diff Signals Wide Common Mode Receiver with Terminator	-		
	DB	2.5V STI Non-Test Differential Driver	1.25+-0.2		
V_{DDS}	**Driver Output Differential Voltage Swing**				
	DA	Low-Voltage Diff Signals Wide Common Mode Receiver with Terminator	-		
	DB	2.5V STI Non-Test Differential Driver	1.0+-0.2		

7. Application Notes: Data Structures

These structures reside in Control Memory for each of the logical channels that are set up for transmission or reception.

7.1 Packet Header

Each packet buffer consists of two parts. The first part is the control information used by the PNR. The second portion of the packet buffer is used to hold the actual packet data. The following figures show the structure of the transmit and receive packet headers:

Figure 54: Transmit Packet Header Structure

```
struct tx_min_packhead {          struct tx_packhead {
    bit32 next_buffer;                bit32 next_buffer;
    bit8  AAL5_user_byte1;            bit8  AAL5_user_byte;
    bit8  buffer_offset;              bit8  buffer_offset;
    bit16 buffer_length;              bit16 buffer_length;
    bit25 lc_address;                 bit25 lc_address;
    bit1  EFCI_status;                bit1  EFCI_status;
    bit1  reserved;                   bit1  reserved;
    bit1  dma_on_xmit;                bit1  dma_on_xmit;
    bit1  generate_CRC10;             bit1  generate_CRC10;
    bit1  free_on_xmit;               bit1  free_on_xmit;
    bit1  queue_on_xmit;              bit1  queue_on_xmit;
    bit1  cell_loss_priority;         bit1  cell_loss_priority;
    };                                bit32 dma_desc_addr;

                                      bit16  AAL5_user_byte1_2;
                                      bit16  reserved
                                      };
```

The minimum transmit packet header size (and transmit offset) is x'C' bytes.

Figure 55: Receive Packet Header Structure

```
struct rx_packhead {
    bit32 rx_label_flags;

    bit8  AAL5_user_byte1;
    bit8  buffer_offset;
    bit16 buffer_length;

    bit25 lc_address;
    bit1  EFCI_status;
    bit5  reserved;
    bit1  cell_loss_priority;

    bit32 optional_words[7];

    };
```

See *3.14.6.8: RXAAL Packet Header Configuration* on page 335 for available word choices and definitions.

Figure 56: Receive Packet Definitions

```
// aal 5 definition
struct rx_label flags {
    bit16 rx_label;
    bit2  ip_chksm_flags;
    bit2  proto_chksm_flags;
    bit1  toobig_status;
    bit1  memchk_status;
    bit1  fabort_status;
    bit1  badlen_status;
    bit1  badcpi_status;
    bit1  badcrc_status;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  route_status;
    bit1  error_status;
    bit1  done_status;
    };
```

```
// raw definition
struct rx_label flags {
    bit16 rx_label;
    bit2  reserved;
    bit2  reserved;
    bit1  toobig_status;
    bit1  memchk_status;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  badcrc_status;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  route_status;
    bit1  error_status;
    bit1  done_status;
    };
```

```
// packet mode definition
struct rx_label flags {
    bit16 rx_label;
    bit2  ip_chksm_flags;
    bit2  proto_chksm_flags;
    bit1  toobig_status;
    bit1  memchk_status;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  reserved;
    bit1  route_status;
    bit1  error_status;
    bit1  done_status;
    };
```

The minimum receive packet offset is x'C' bytes. When the optional fields are enabled, the receive packet offset increases and should be set appropriately in the receive LCD. See *3.14.6.8: RXAAL Packet Header Configuration* on page 335 for available word choices and definitions.

Table 51: Transmit and Receive Packet Header Field Descriptions (Page 1 of 3)

Field Name	Field Description
next_buffer	This field is used by the hardware to chain buffers together on queues. It contains the address of the next buffer if one exists. For transmit buffers allocated in virtual memory, this field is written by the hardware with a distinctive pattern ('zzzzzBAD'x) where zzzzz is the offset of the failure when a write operation was not able to complete due to a shortage of the real buffers needed to map into the virtual address space. This field can be checked after all buffer write operations and the appropriate recovery actions are taken immediately, or when a buffer that has had a write failure is enqueued to CSKED (an event will be generated and the buffer will not be processed by CSKED). A status bit also exists in the BCACH status register indicating that a write to virtual memory has failed. With cache performance in mind, this status bit could be checked first; if it is not set, there is no need to access the header of the packet. **Note:** This automatic error recovery mechanism results in the restriction that this first four bytes of a transmit packet must never be written via programmed IO or DMA during preparation for transmission. If this field is written by a software or DMA operation, the automatic error detection will not work properly and undesirable results are likely.
AAL5_user_byte1	On transmit, this field contains the value to be sent in the user byte in the last cell of an AAL5 packet, if INTST is configured for one user byte. On receive, this field contains the user byte from the AAL5 trailer, if INTST is configured for one user byte. When not configured for AAL5, this field is redefined. The two most significant bits contain the drop number. When in packet mode, the low five bits of this byte contain the number of bytes dropped due to the dropN-Bytes field in the LCD.
dma_on_xmit	If this bit is set, a DMA descriptor address placed in the packet header (offset x'C') will be queued for execution.
generate_CRC10	If this bit is set, CRC10 will be generated over the cell(s) in this packet.
free_on_xmit	If this bit is set, the buffer will be freed after the transmission completes.
queue_on_xmit	If this bit is set, the buffer will be queued on the transmit complete queue after the transmission completes.
EFCT_status	This bit is used on both transmit and receive: Transmit: If this bit is set, the EFCI bit in the ATM cell header will be set for each cell in this packet. Receive: This bit contains the ORed EFCI bits across all the cells that comprised this packet if this LCD is using AAL5.

Table 51: Transmit and Receive Packet Header Field Descriptions (Page 2 of 3)

Field Name	Field Description
cell_loss_priority	This bit is used on both transmit and receive: Transmit: If this bit is set, the cell loss priority bit in the ATM cell header will be set for each cell in this packet Receive: This bit contains the ORed cell loss priority bits across all the cells that comprised this packet if this LCD is using AAL5.
buffer_offset	This field contains the offset into the buffer where the data starts.
buffer_length	This field contains the length of the packet.
lc_address	This is the address of the logical connection descriptor on which this packet was received.
rx_atm_header	On reception, the four-byte ATM header (no HEC) is copied from the first and last cell into this area. This is an optional header word.
AAL5_user_byte2 (tx)	This field contains the value to be sent in the user bytes, one and two, in the last cell of an AAL5 packet if INTST is configured for two-user byte. The normal one-byte AAL5 user byte field is not used.
AAL5_user_byte2 (rx)	This field contains the AAL5 user bytes, one and two, in the last cell of an AAL5 packet if INTST is configured for two-user byte. The normal one-byte AAL5 user byte field is not filled in. This is an optional packet header word.
rx_label	This field is written with “RA” in ASCII (x’5241’) to signal that this buffer was used by RAALL.
ip_chksm_flags	This field contains the IP checksum status if enabled. The possible values are: 00 Not checked 01 Good 10 Bad 11 Unknown
proto_chksm_flags	This field contains the protocol checksum status if enabled. The possible values are: 00 Not checked 01 Good 10 Bad 11 Unknown
toobig_status	Indicates the current packet exceeded the maximum packet size.
memchk_status	Indicates the current packet had a memory check (real size exceeded or virtual error).
fabort_status	Indicates the current packet was aborted (AAL5 forward abort).
badlen_status	Indicates the current packet had a bad AAL5 length in the trailer.
badcpi_status	Indicates the current packet had a bad AAL5 CPI field (not zero).
badcrc_status	Indicates the current packet had a bad AAL5 CRC.
route_status	This bit is written when the packet is completed if it is internally routed.
error_status	This bit is written when the packet is completed if an error condition occurs.
done_status	This bit is written when the packet is completed. It can be used when thresholding.
host_data	This is an optional word that can be copied from the LCD to the packet header.
VBA	This is the PNR virtual buffer address of the current receive buffer. This is an optional packet header word.
TxQueueLenH/M/L	These words provide the current transmit queue length. See *3.14.6.7: RXAAL Transmit Queue Length Compression Configuration* on page 334 for more information on the format of these words. These are optional packet header words.
start_timestamp	A timestamp can be inserted in the packet header when the packet is started. The timestamp is sourced from the RXQUE timestamp register. The location of this timestamp is important so it is not overwritten when the packet is completed. For this reason, it should be the last word in the packet header. This is an optional header word.

Table 51: Transmit and Receive Packet Header Field Descriptions (Page 3 of 3)

Field Name	Field Description
end_timestamp	A timestamp can be inserted in the packet header when the packet is started. The timestamp is sourced from the RXQUE timestamp register. This is an optional header word.
dma_desc_addr	If the dma_on_xmit bit is set in the packet header, this field contains the address of the DMA descriptor that will be queued when transmission is complete.

7.2 General LCD

Figure 57: Logical Channel Data Structure

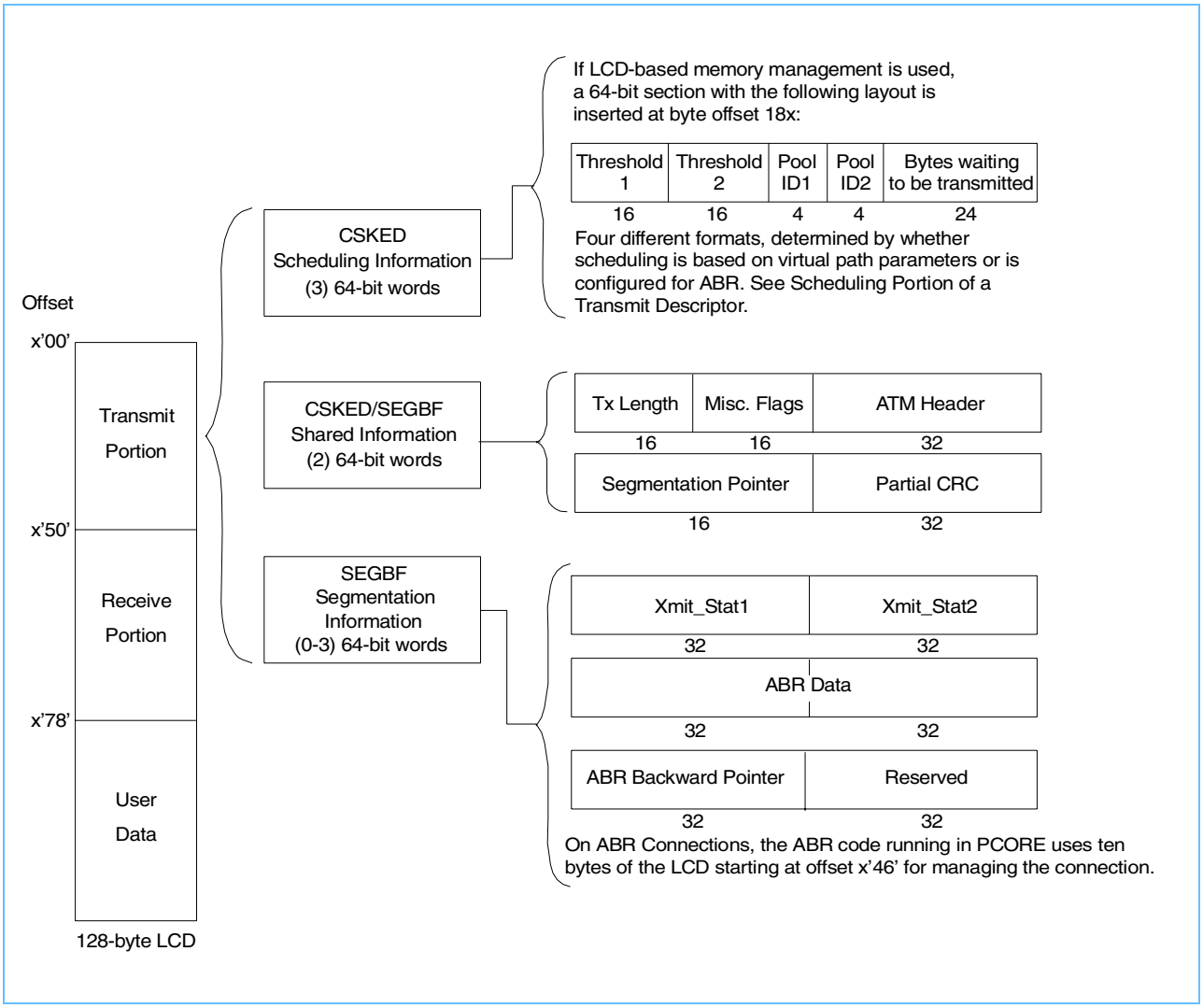


Figure 58: General LCD Layout

```
struct lcd_struct {
    tx_lcd_struct  tx_lcd ;              // transmit portion of the lc descriptor
    bit8  fill[N] ;                      // the fill area depends on the type of tx lcd
    rx_lcd_struct  rx_lcd ;              // receive portion of the lc descriptor
} ;
```

7.3 Transmit LCD Data Structures

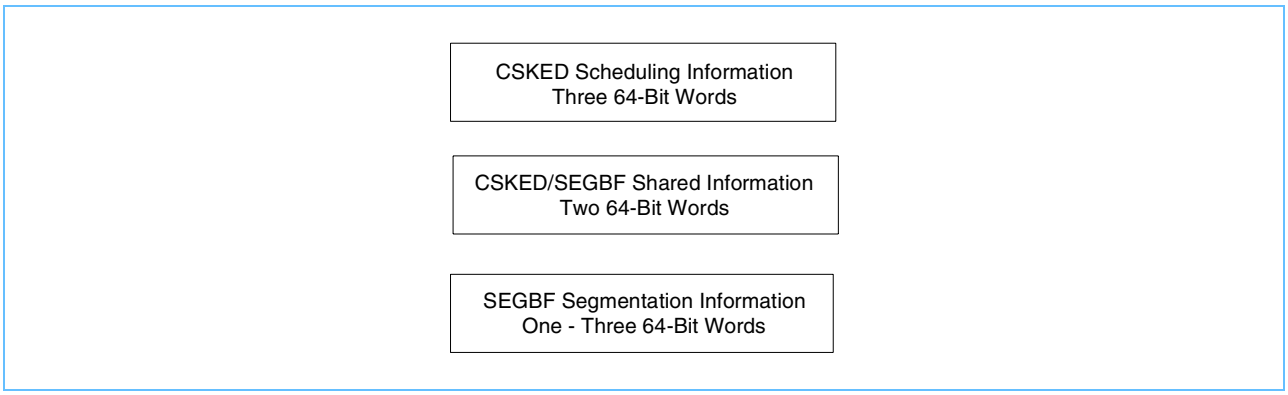
Figure 57 on page 677 and Figure 60 on page 679 show the layout of the transmit portion of a Logical Channel Descriptor. When initializing an LCD, any locations that are not written to a specific value should be initialized to zeros. Fields that typically need to be initialized to a non-zero value are flagged with a # in the structure below.

Note: This is only one possible layout of the transmit portion of the LCD. Some field locations vary and are further defined later in this section.

Care must be taken when updating fields in the LCD and then immediately causing the updated fields to be accessed by other PNR entities. For example, it is possible, although not likely, under the right conditions, for a normal LCD update followed by a SEGBF cell enqueue operation to actually execute in reverse order. This is due to PNR internal priority levels and could result in SEGBF fetching the LCD data before it has been updated to the new value. For this reason, it is highly advisable to use the LCD update mechanism in section *3.14: Cell/Packet Reassembly (REASM)* on page 301.

The transmit portion of the LCD can be subdivided into three distinct parts based on which chip functions or entities access that particular part of the LCD. The first three 64-bit words are scheduling related and are accessed only by CSKED. The next two 64-bit words (four if using switch fabric header) are related to both scheduling and segmentation and are accessed and shared by both CSKED and SEGBF. The words following these shared locations are related only to segmentation and are accessed only by SEGBF. The number of 64-bit words in this portion of the LCD can vary from one to three. The actual number being used in an LCD is determined by the segmentation processor code entry point field of that LCD. The following figure is the layout of the entire transmit portion of the LCD.

Figure 59: Overall Transmit LCD Layout



The three 64-bit words containing CSKED scheduling information can have four different formats depending upon whether scheduling is based on virtual path parameters or is configured for ABR.

If LCD-based memory management is used, a 64-bit section is inserted at byte offset x‘18’.

On ABR connections, the ABR code running in PCORE will use ten bytes of the LCD for managing the connection, starting at offset x’46’ in the LCD.

Figure 60: Scheduling Portion of a Transmit Descriptor

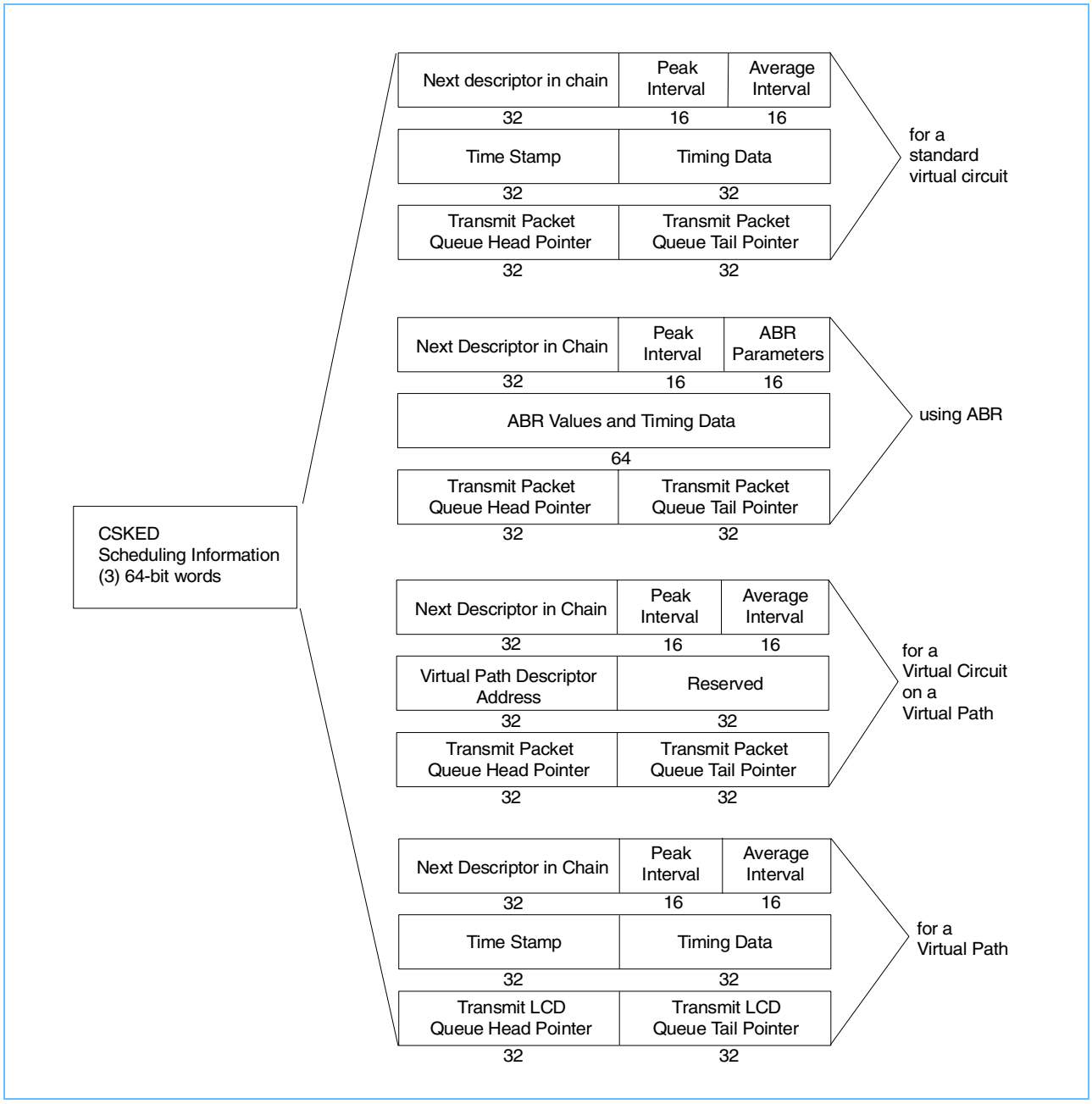


Figure 61: Transmit Logical Channel Descriptor Structure

```
.
typedef struct {
    bit32 next_lcd;
    bit16 #peak_interval;
    bit16 #average_interval;

    bit32 #timestamp;
    bit11 Reserved;
    bit1  remove_lcd;
    bit1  lc_on_timewheel;
    bit3  #alter_sched;
    bit2  #transmit_priority;
    bit1  #max_resolution;
    bit3  #max_burst_mult;
    bit10 #max_burst_value;

    bit26 head_packet_pointer;
    bit1  free_on_xmit;
    bit1  queue_on_xmit;
    bit1  conn_suss;
    bit1  #drop;
    bit26 tail_packet_pointer;
    bit6  reserved;

    bit16 transmit_length;
    bit8  buffer_offset;

    bit2  xmt_cmp_evt_mod;
    bit2  reserved;
    bit4  seg_prc_Entry_point;

    bit32 #ATM_header;

    bit32 segmentation_pointer;
    bit32 current_CRC;

    bit32 xmit_stat1;
    bit32 xmit_stat2;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 62: Transmit Logical Path Descriptor Structure

```
.
typedef struct {

    bit32 next_lcd;
    bit16 #peak_interval;
    bit16 #average_interval;

    bit32 #timestamp;
    bit11 Reserved;
    bit1  remove_lcd;
    bit1  lc_on_timewheel;
    bit3  #alter_sched;
    bit2  #transmit_priority;
    bit1  #max_resolution;
    bit3  #max_burst_mult;
    bit10 #max_burst_value;

    bit26 forward_LCD_pointer;
    bit6  reserved;

    bit26 backwared_LCD_pointer;
    bit6  reserved;


} tx_lpd_struct, *tx_lpd_struct_ptr;
```

Figure 63: Redefinition of Transmit Logical Channel Descriptor for Connections Sharing (Logical Path Bandwidth)

```
typedef struct {
    bit32 next_lcd;
    bit32 reserved;

    bit32 lcd_pointer;
    bit11 reserved;
    bit1  remove_lcd;
    bit1  lc_on_timewheel;
    bit3  #alter_sched;
    bit2  #transmit_priority;
    bit14 reserved;

    bit26 head_packet_pointer;
    bit1  free_on_transmit;
    bit1  queue_on_transmit;
    bit1  dma_on_transmit;
    bit1  conn_suss;
    bit2  #drop;
    bit26 tail_packet_pointer;
    bit6  reserved;

    bit16 transmit_length;
    bit8  buffer_offset;
    bit2  xmt_cmp_evt_mod;
    bit2  reserved;
    bit4  seg_prc_Entry_point;
    bit32 #ATM_header;

    bit32 segmentation_pointer;
    bit32 current_CRC;

    bit32 xmit_stat1;
    bit32 xmit_stat2;


} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 64: Redefinition of Shared and Segmentation Portion of Transmit LCD for ABR

```
typedef struct {
    bit16 transmit_length;
    bit8  buffer_offset;

    bit2  xmt_cmp_evt_mod;
    bit2  reserved;
    bit4  seg_prc_Entry_point;

    bit32 #ATM_header;

    bit32 segmentation_pointer;
    bit32 current_CRC;

    bit32 xmit_stat1;
    bit32 xmit_stat2;


    bit16 reserved;
    bit16 explicit_rate;
    bit16 current_rate;
    bit16 minimum_rate;

    bit32 backward_ptr;

    bit32 reserved;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Owing to the use of certain LCD fields, a connection running ABR cannot be set up for segmentation AAL types x'6' (fixed-sized blocking) or x'7' (MPEG-2 assist).

Figure 65: Redefinition of Segmentation Portion of Transmit LCD for Fixed Size AAL5 Blocking (segmentation type x'6')

```
typedef struct {

    bit16 transmit_length;
    bit8  buffer_offset;

    bit2  xmt_cmp_evt_mod;
    bit2  reserved;
    bit4  seg_prc_Entry_point;

    bit32 #ATM_header;

    bit32 segmentation_pointer;
    bit32 current_CRC;

    bit32 xmit_stat1;
    bit32 xmit_stat2;

    bit8  #Packets_per_AAL5_frame;
    bit8  #Blocking_size (4 bytes x'2F' for MPEG-2);
    bit8  Current_transport_stream_packet;
    bit8  Current_Blocking_Count (4 bytes);
    bit32 reserved;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 66: Redefinition of Segmentation Portion of Transmit LCD for MPEG2 (Segmentation type x'7')

```
typedef struct {

    bit16 transmit_length;
    bit8  buffer_offset;

    bit2  xmt_cmp_evt_mod;
    bit2  reserved;
    bit4  seg_prc_Entry_point;

    bit32 #ATM_header;

    bit32 segmentation_pointer;
    bit32 current_CRC;

    bit32 xmit_stat1
    bit32 xmit_stat2

    bit8  #Packets_per_AAL5_frame;
    bit8  #Blocking_size (4 bytes x'2F' for MPEG-2);
    bit8  Current_transport_stream_packet;
    bit8  Current_Blocking_Count (4 bytes);
    bit32 reserved;

    bit32 reserved;
    bit32 reserved;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 67: Redefinition of Scheduling Portion of Transmit LCD for ABR

```
typedef struct {
    bit32 next_lcd;
    bit16 #peak_interval;
    bit3  #Nrm;
    bit3  #Trm;
    bit10 #Tadtf;

    bit8  #Nc;
    bit8  #Ncrm;
    bit16 Reserved;
    bit11 Tlrm1;
    bit1  remove_lcd;
    bit1  lc_on_timewheel;
    bit3  #alter_sched;
    bit2  #transmit_priority;
    bit1  #max_resolution;
    bit13 Tlrm2;

    bit26 head_packet_pointer;
    bit1  free_on_xmit;
    bit1  queue_on_xmit;
    bit4  reserved;
    bit26 tail_packet_pointer;
    bit6  reserved;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 68: Redefinition of Scheduling Portion of Transmit LCD for Timers

```
typedef struct {
    bit32 next_lcd;
    bit32 #timer_period;

    bit32 #timestamp;
    bit12 reserved;
    bit1  lc_on_timewheel;
    bit1  reserved;
    bit2  #timer_type;
    bit2  #transmit_priority;
    bit1  #max_resolution;
    bit13 reserved;

    bit32 #dma_desc_addr;
    bit32 reserved;

} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 69: Definition of LCD-Based Memory Management of Transmit LCD

```
typedef struct {
    bit16 #threshold_1;
    bit16 #threshold_2;
    bit4  #pool_id1;
    bit4  #pool_id2;
    bit24 #bytes_queued;
} tx_lcd_struct, *tx_lcd_struct_ptr;
```

Figure 70: Definition of ABR Code Variables

```
typedef struct {
    bit8  #CRM;
    bit8  #iCDF;
    bit16 #iMCR;
    bit16 #PCR;
    bit8  #iRDF;
    bit8  #iRIF;
    bit16 #ICR;
} tx_lcd_struct, *tx_lcd_struct_ptr;
```

7.3.1 Field Definitions

The following is a detailed description of the fields listed above. This data structure should be initialized at connection setup but not modified while transmission is occurring on the connection.

Table 52: Transmit LCD Field Definitions (Page 1 of 5)

Field Name	Needs to be initialized to a non-zero value?	Field Description
next_lcd	No	This field is used by the hardware to chain LCDs together on queues. It contains the address of the next LCD if one exists.
peak_interval	Yes	This field contains the minimum spacing allowed between consecutive cells on this connection. This spacing is expressed in cell times. A connection that can transmit every cell time would have a value of ‘1’ for this field. In frame-based mode, the average portion of the bandwidth used by a connection will be 1/(peak interval)
average_interval	Yes	This field contains the minimum average spacing allowed between cells transmitted on this connection. It is the inverse of the Sustainable Cell Rate. The value for this field is expressed in cell times. In frame-based mode, this field should be set equal to the peak interval times the maximum packet size divided by 64.
Nrm	Yes	This field specifies the maximum number of cells a source may send for each forward RM cell. Number of cells = (2**Nrm)+1.
Trm	Yes	This field provides an upper bound on the time between forward RM cells for an active source. Time = 100•(2**-Trm) msec.
Tadtf	Yes	The ACR Decrease Time Factor is the time permitted between sending RM cells before the rate is decreased to ICR. Time = Tadtf• 0.01 sec.
Nc	Yes	This field is used as a counter to determine when PNR cells have been sent. It should be initialized at connection setup time to ‘0’.
Ncrm	Yes	This field is used as a counter to determine when CRM RM cells have been sent. It should be initialized at connection setup time to CRM.

Table 52: Transmit LCD Field Definitions (Page 2 of 5)

Field Name	Needs to be initialized to a non-zero value?	Field Description
timestamp	Yes	This field contains a timestamp used by the hardware to determine if transmit opportunity credits exist and if the Burst Tolerance has been exceeded. It should be initialized at connection setup time to the value in the current timeslot counter.
Tlrm1 & 2	No	These fields are used by the hardware to determine when the last RM cell was sent. They should be initialized to '0'.
lc_on_timewheel	Yes	This field indicates if the LCD is currently queued to the timewheel. It should be initialized to '0'.
remove_lcd	Yes	If this bit is set, the LCD will be removed from the time wheel at next transmission opportunity. It should be initialized to '0'.
alter_sched	Yes	These encoding bits alter the scheduling of cells on a Virtual Circuit (VC) 000 Normal Scheduling — Scheduling is not altered. 001 VC on VP — This VC is contained on a virtual path and will share the VP bandwidth after one packet is sent. The scheduling parameters are contained in the descriptor for the virtual path that is pointed to by the Virtual Path Descriptor Address field in this LCD. 010 MPEG-2 Scheduling — The cells being sent out on this connection are monitored for a Peak Cell Rate (PCR). If a PCR is found, the AAL5 packet is terminated at the end of the MPEG-2 frame and the last cell is scheduled to go out at the time specified in the PCR. 011 Packet-based scheduling — Packets will be scheduled at the average interval and cells within the packet will be scheduled at the peak interval. This is useful for sending information where variably-sized packets need to be sent at regular intervals. 100 ABR scheduling — This VC will send Resource Management cells and adjust its transmission rate according to the behaviors specified in the ATM Forum Traffic Management Specification, Version 4.0. 101 Fair VC on VP — This VC is contained on a virtual path and will share the VP bandwidth after one cell is sent. The scheduling parameters are contained in the descriptor for the virtual path which is pointed to by the Virtual Path Descriptor Address field in this LCD. 110 Reserved — For MPEG-2 scheduling. 111 Reserved
transmit_priority	Yes	This field specifies the priority of transmission on this connection: 0=high, 1=medium, 2=low.
max_resolution	Yes	If this bit is set, the lower eight bits of the average interval and peak interval parameters contain a fractional component. This allows a finer resolution for scheduling. For example, for a peak interval of 1.5 time units, the value written to the peak_interval field should be x'0180'. If this bit is set, the initial value of timestamp should contain the current timeslot counter shifted 16 bits to the left.

Table 52: Transmit LCD Field Definitions (Page 3 of 5)

Field Name	Needs to be initialized to a non-zero value?	Field Description
max_burst_mult	Yes	The values in this field and the next field are used to limit the number of cells that can be transferred at the peak rate. The max_burst_value will be multiplied by four to the power of the value in this field to yield the maximum credit time. This time is expressed in cell times and represents the time it would take to acquire the maximum number of cell credits. This maximum credit time should equal the maximum number of cells that can be transferred at the peak rate (MBS) times the difference between the average and intervals. Maximum credit time = MBS * (AI-PI) where MBS = maximum burst size, AI = average interval, and PI = peak interval. MBS must be at least one to transmit at peak rate. If MBS is not at least one, the peak interval should be set to the average interval.
max_burst_value	Yes	The value in this field will be multiplied by four to the power of the value in the max_burst_mult field to yield the maximum credit time.
head_packet_pointer	No	This field is used to chain buffers to LCDs.
tail_packet_pointer	No	This field is used to chain buffers to LCDs.
transmit_length	No	This field contains the length of the currently transmitted packet.
free_on_xmit	No	This bit is set if the header of the currently transmitted packet has specified that the packet is to be freed after transmission.
queue_on_xmit	No	This bit is set if the header of the currently transmitted packet has specified that the packet is to be queued after transmission.
dma_on_xmit	No	This bit is set if the header of the currently transmitted packet has specified that a DMA descriptor is to be queued after transmission.
conn_suss	No	This bit is used on ABR connections to suspend transmission. It should be initialized to ‘0’.
drop	No	These two bits are used to indicate which physical drop will be used for this connection. Traffic can be scheduled on up to four drops.
buffer_offset	No	This field contains the offset into the buffer that the transmit data starts.
xmt_cmp_evt_mod	No	This two-bit field can optionally (based on a bit in the SEGBF control register) be logically ORed with bits 8-7 of a transmit complete buffer event when it is generated by the segmentation logic. This field will only be ORed when buffer address events are being generated. It will have no affect when LCD addresses are being enqueued when a transmit complete event occurs.
seg_prc_Entry_point	Yes	This four-bit field is loaded into the instruction pointer for both the LCD update processor and the cell generation processor when a cell opportunity occurs for the LCD. The value loaded into this field defines what type of cell will be generated by the segmentation logic. Possible types include raw 48- and 52-byte cells, AAL5 cells, switch bound cells (48-byte payload), extended switch bound cells (54-byte payload), and frame-based cells. The actual values that are associated with each type of cell will be defined at a later time.
ATM_header	Yes	This field contains the first four bytes of the ATM header.
segmentation_pointer	No	This field contains a pointer to the next data to be transmitted. In normal operation, this field is initialized by the cell scheduler when a new frame is queued for segmentation.
current_CRC	No	This field contains the CRC as it is being built.
Current_Blocking_Count	No	This eight-bit field contains the current count of four-byte values that have been assembled into cells and sent out on this LCD for all fix block or MPEG AAL types. Other than initialization, this field should only be accessed by the hardware.
Fixed_Blocking_size	Yes	This eight-bit field should be initialized by the software to contain the number of four-byte values that constitute a packet. For MPEG2, this register should be set to x’2F’ (4•x’2F’ = 188 byte transport stream packet).

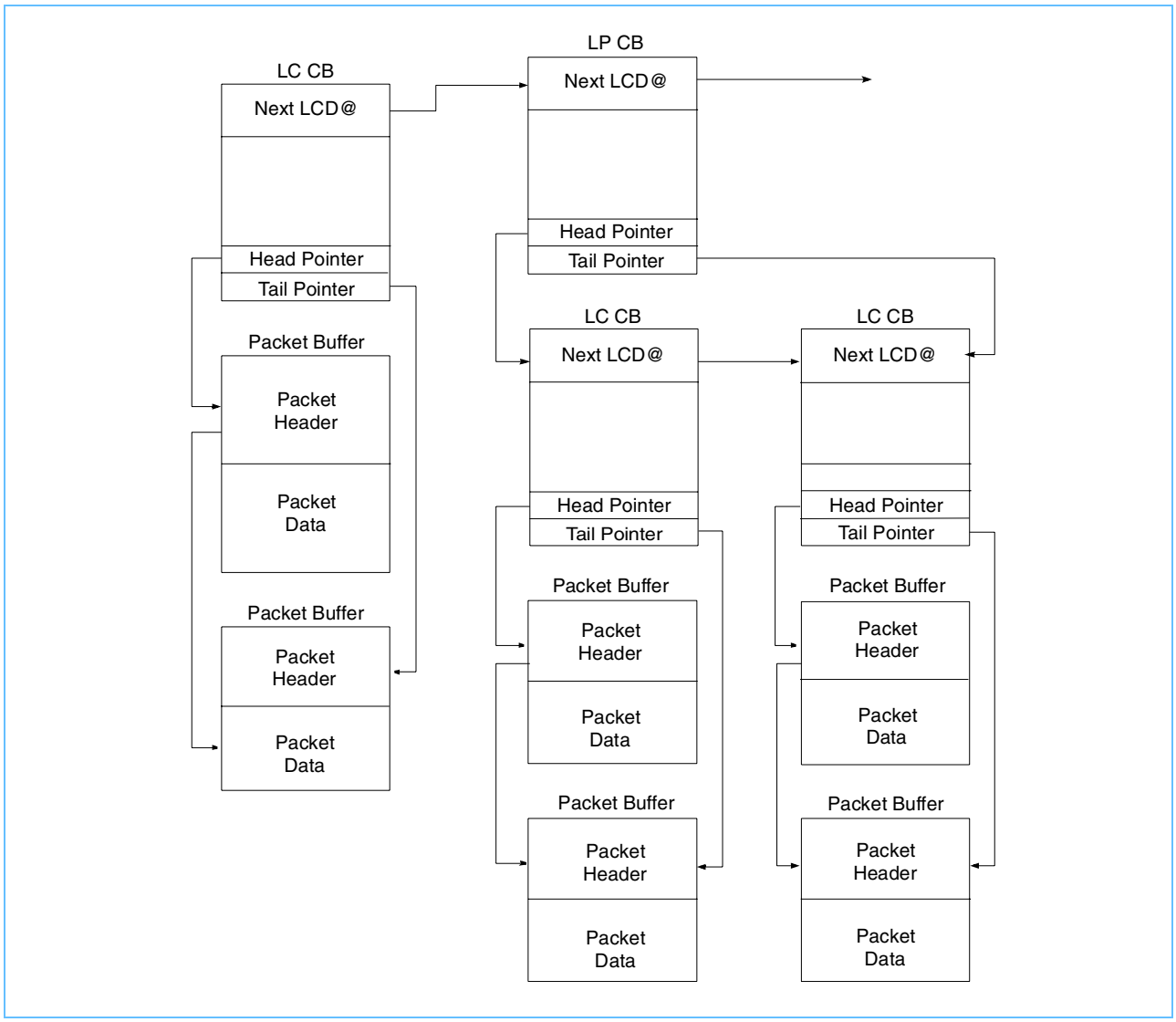
Table 52: Transmit LCD Field Definitions (Page 4 of 5)

Field Name	Needs to be initialized to a non-zero value?	Field Description
Current_transport_stream_packet	No	This eight-bit field contains the number of the current transport stream packet that is being segmented. Other than initialization, this field should only be accessed by the hardware.
Packets_per_AAL5_frame	Yes	This eight-bit field should be initialized by the software to indicate how many packets should be concatenated into an AAL5 frame.
explicit_rate	No	This 16-bit field contains the explicit cell rate as defined for ABR traffic on this LCD.
current_rate	No	This 16-bit field contains the current cell rate as defined for ABR traffic on this LCD.
minimum_rate	No	This 16-bit field contains the minimum cell rate as defined for ABR traffic on this LCD.
backward_ptr	No	When software needs to send a backward RM cell, this 32-bit field should be updated with the address of a buffer that contains the desired backward RM cell. After the segmentation logic transmits the cell, this field is cleared by the hardware.
xmit_stat1	No	This 32-bit field contains a count of one of three things: the total number of user cells that have been sent on this LCD, the total number of bytes that have been sent on this LCD, or the total number of frames that have been sent on this LCD. This field should zeroed when the connection is initialized. An event will be generated when this count wraps.
xmit_stat2	No	This 32-bit field contains a count of one of three things: the total number of user cells that have been sent on this LCD, the total number of bytes that have been sent on this LCD, or the total number of frames that have been sent on this LCD. This field should be zeroed when the connection is initialized. An event will be generated when this count wraps.
threshold_1&2	No	These fields are compared to the upper 24 bits of the bytes_queued field to determine when a threshold is crossed and the POOL ID for the received LCD should be changed.
pool_id1&2	No	These fields are used to change the POOL ID when a threshold is crossed.
bytes_queued	No	This field is used to keep track of the number of bytes queued for transmission on this LCD.
timer_type	Yes	These encoded bits determine the time of timer: 00 Relative non-periodic timer — The expiration time will be in one timer period. The timer will not be scheduled again automatically. 01 Relative periodic timer — The expiration time will be in one timer period. The timer will be automatically scheduled again. 10 Absolute non-periodic timer — The timer will expire at the time specified by the timestamp field. The timer will not be automatically scheduled again. 11 Absolute periodic timer — The timer will expire at the time specified by the timestamp field. The timer will be scheduled again, automatically, using the time specified in the timer_period field.
timer_period	Yes	This field specifies the number of timeslots before the timer expires.
dma_desc_addr	Yes	The DMA descriptor pointed to by this field will be queued for execution when the timer expires.
CRM	No	Missing RM cell count. CRM limits the number of forward RM cells that may be sent in the absence of received backward RM cells. CDF is written to the NCRM field whenever a backward RM cell is detected.

Table 52: Transmit LCD Field Definitions (Page 5 of 5)

Field Name	Needs to be initialized to a non-zero value?	Field Description
iCDF	No	Cutoff Decrease Factor (CDF) controls the decrease in ACR associated with CRM. CDF is zero or a power of 2 value in the range of 1/64 to 1. iCDF represents the power of 2 that is in the denominator of CDF. CDF = 1/(2**iCDF) so iCDF = log (base 2) of 1/CDF. Range = 1 to 6. A zero value for CDF should be represented as x'FF' for iCDF.
iMCR	No	This is the reciprocal of the Minimum Cell Rate (MCR). MCR is represented in the ABR Rate format. iMCR needs to be an integer representing the interval between cells, in units of timeslots per cell. The following formula illustrates the conversion from MCR to iMCR. iMCR = 1/(MCR) * 53 * 8 * (TSP/CI*(2**23)). The Timeslot Prescalar (TSP) is defined by the CSKED Timeslot Prescalar Register. The clock interval (CI) is determined by the CRSET Clock Control Register. With the TSP set to one timeslot per cell transmission time, iMCR =1 for a full bandwidth, 2 for a half bandwidth, etc.
PCR	No	The Peak Cell Rate (PCR) is the cell rate that the source may never exceed. PCR should be in the ABR Rate format.
iRDF	No	Rate Decrease Factor (RDF) controls the decrease in the cell transmission rate. RDF is a power of 2 value in the range of 1/32,768 to 1. iRDF represents the power of 2 that is in the denominator of RDF. RDF = 1/(2**iRDF) so iRDF = log (base 2) of 1/RDF. Range = 1 to 15.
iRIF	No	Rate Increase Factor (RIF) controls the increase in the cell transmission rate. RIF is a power of 2 value in the range of 1/32,768 to 1. iRIF represents the power of 2 that is in the denominator of RIF. RIF = 1/(2**iRIF) so iRIF = log (base 2) of 1/RIF. Range = 1 to 15.
ICR	No	The Initial Cell Rate is the rate at which a source should send initially and after an idle period. ICR should be in the ABR Rate format.

Figure 71: Transmit Data Structure Linkage



7.4 Receive LCD Data Structure and Modes

The format of the receive LCD structure depends on which AAL is being configured and which options are used. It also depends on whether TCP/IP checksum verification has been enabled. When TCP/IP checksum verification is enabled, 16 additional bytes are added to the LCD format. TCP/IP checksum is enabled in the *REASM Mode Register*. The following are the basic layouts of the receive LCD:

Figure 72: Basic Receive LCD Layout

```
struct BasicRxLcd {
    bit32 packedInfo;
    bit32 crcState;

    bit32 misc;
    bit32 buffPtr;

    bit32 stat0;
    bit32 stat1;

    bit32 hostData;
    bit32 misc2;


    bit32 reserved;
    bit32 reserved;
    bit32 reserved;
    bit32 reserved;

};

struct ipWrd0  {;
    bit32  ipWrd0;
        bit4  frameType;
        bit6  skipCount;
        bit6  reserved;
        bit16 reserved;
};
```

```
struct BasicRxLcdIP {
     bit32 packedInfo;
     bit32 crcState;

     bit32 ipWrd0;
     bit32 ipWrd1;
     bit32 ipWrd2;
     bit32 ipWrd3;

     bit32 misc;
     bit32 buffPtr;


     bit32 stat0;
     bit32 stat1;

     bit32 hostData;
     bit32 misc2;

};
```

The basic layout is the same for all LCD types. Only the packed Info and misc fields vary between the different LCD types. The following sections detail the receive LCD and the differences from the basic layout for each major option.

Figure 73: Raw LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;          // 0000 - raw
    bit2  ppMode;           // 00   - normal
    bit2  state;            // 00->down 01->idle/enabled

    bit1  reserved;         // set to zero
    bit1  reserved;         // set to zero
    bit1  reserved;         // set to zero
    bit1  size;             // 1->52 byte cell 0->48 byte cell
    bit1  storeCrc10;
    bit3  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 reserved;
};
```

A raw LCD allows raw ATM cells to be received with no reassembly. The user can select to receive 52- or 48-byte cells. The packet header may or may not contain the ATM header. The cell data is then placed after the packet header at the configured receive offset. The 52-byte mode stores the entire cell minus the HEC, and the 48-byte mode stores only the ATM cell payload. Optional CRC-10 checking is available in raw modes.

Figure 74: Raw Routed LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;       // 0000 - raw
    bit2  ppMode;        // 01   - routed
    bit2  state;         // 00->down 01->idle/enabled

    bit1  reserved;      // set to zero
    bit1  reserved;      // set to zero
    bit1  reserved;      // set to zero
    bit1  size;          // 1->52 byte cell 0->48 byte cell
    bit1  reserved;
    bit3  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 routedLcd;
};
```

A raw routed LCD receives data in the same way that a raw LCD does. Once received, the cell buffer is routed internally to the scheduler and rescheduled for transmission. Normally, when a cell is received, the receive LCD address is written into the packet header and the buffer is surfaced to the user. When a cell is routed, the routedLcd field is used to fill in the LCD address in the packet header. This allows cells to be routed out the transmit interface with the same or different VPI/VCI.

The low order bits in the routedLcd field should be set correctly to free the buffer on transmission. These bits correspond to the flag bits in the packet header. Raw routing is also called forwarded or fast forward mode.

Figure 75: Raw Routed Early Drop LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;         // 0001 - raw early drop
    bit2  ppMode;          // 01   - routed
    bit2  state;           // 00->down 01->idle/enabled 11->error

    bit1  reserved;        // set to zero
    bit1  reserved;        // set to zero
    bit1  reserved;        // set to zero
    bit1  size;            // 1->52 byte cell 0->48 byte cell
    bit4  finalPoolId;     // pool id

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 routedLcd;
};
```

A raw routed early drop LCD receives data in the same way that a raw LCD does. Once received, the cell buffer is then routed internally to the scheduler and rescheduled for transmission. Normally when a cell is received, the receive LCD address is written into the packet header and the buffer is surfaced to the user. When a cell is routed, the routedLcd field is used to fill in the LCD address in the packet header. This allows cells to be routed out the transmit interface with the same or different VP/VC.

This mode should only be used when the routed cell stream is actually an AAL5 packet stream. In this mode, a cell being dropped due to resource causes the LCD to go into error mode until the cell that contains the user indicate (UIND) bit is received. All cells received in error mode are dropped, except the final cell which is forwarded. This conserves bandwidth while maintaining the AAL5 integrity. The finalPoolId provides a second poolid for the final cells to use to be sure that these final cells are always forwarded even when resources are low. The finalPoolId is only used if no buffers are available in the normal pool.

The low order bits in the routedLcd field should be set correctly to free the buffer on transmit. These bits correspond to the flag bits in the packet header.

This is also called forwarded or fast forward mode.

Figure 76: Raw Scatter/Cut-Through LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;       // 0000 - raw
    bit2  ppMode;        // 10   - scatter/cut through
    bit2  state;         // 00->down 01->idle/enabled

    bit1  reserved;      // set to zero
    bit1  reserved;      // set to zero
    bit1  reserved;      // set to zero
    bit1  size;          // 1->52 byte cell 0->48 byte cell
    bit1  storeCrc10;
    bit1  reserved;
    bit2  cutThruSel;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 reserved;
};
```

A raw scatter/cut-through LCD receives data in the same way that a raw LCD does. Once received, the cutThruSel field is used to select one of four configurations. Each configuration specifies a receive queue and a DMA queue. The cut-through selector is used to select a cut-through/scatter configuration. The DMA descriptor is then built using the cell buffer address and the data length and the flags specified in the cut-through configuration. After being built, it is enqueued to the DMA queue specified. If there is no DMA descriptor available, then a no descriptor event is enqueued.

Figure 77: AAL5 LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;// 0101 - aal5
    bit2  ppMode;          // 00   - normal
    bit2  state;           // 00->down 01->idle/enabled 10->reasm 11->error

    bit1  reserved;        // set to zero
    bit1  rtoTest;         // set to zero
    bit1  rtoEnable;
    bit1  tmpCLP;
    bit1  tmpCongestion;
    bit3  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 reserved;
};
```

An AAL5 LCD allows AAL5 packets to be received with no special processing.

Figure 78: AAL5 Routed LCD Layout

```
struct Packed {
    bit4  aalType;       // 0101 - aal5
    bit2  ppMode;        // 01   - routed
    bit2  state;         // 00->down 01->idle/enabled 10->reasm 11->error

    bit1  reserved;      // set to zero
    bit1  rtoTest;       // set to zero
    bit1  rtoEnable;
    bit1  tmpCLP;
    bit1  tmpCongestion;
    bit3  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit32 routedLcd;
};
```

An AAL5 Routed LCD allows AAL5 packets to be received. Once received, the packet buffer is then routed internally to the scheduler and rescheduled for transmission. Normally when a packet is received, the receive LCD address is written into the packet header and the buffer is surfaced to the user. When a packet is routed, the routedLcd field is used to fill in the LCD address in the packet header. This allows packets to be routed out the transmit interface with the same or different VP/VC.

The low order bits in the routedLcd field should be set correctly to free the buffer on transmission. These bits correspond to the flag bits in the packet header.

AAL5 routing is also called forwarded or fast forward mode.

Note: Non-user data cells are terminated.

Figure 79: AAL5 Cut-Through/Scatter Mode LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4   aalType;                  // 0101 - aal 5
    bit2   ppMode;                   // 10   - scatter
    bit2   state;                    // 00->down 01->idle/enabled 10->reasm 11->error

bit1   reserved;                     // set to zero
    bit1   rtoTest;                  // set to zero
    bit1   rtoEnable;
    bit1   tmpCLP;
    bit1   tmpCongestion;
    bit1   reserved;
    bit2   cutThruSel;

bit4   rxqNum;
    bit4   rxPoolId;
    bit8   rxOffset;
};

struct Misc {
    bit6  numDesc;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 oamMask;
};

struct Misc2 {
    bit5  reserved;
    bit1  useCrcNumHead;
    bit10 numHeadBytes;
    bit16 reserved;
};
```

Figure 80: Packet LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;       // 0111 - packet
    bit2  ppMode;        // 00   - normal
    bit2  state;         // 00->down 01->idle/enabled 10->reasm 11->error

    bit1  reserved;      // set to zero
    bit1  rtoTest;       // set to zero
    bit1  rtoEnable;
    bit5  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 reserved;
};

struct Misc2 {
    bit5  dropNBytes;
    bit11 reserved;
    bit16 reserved;
};
```

A packet LCD allows packets from the POS-PHY to be received with no special processing. The header-Thresh can be used to allow packet header thresholding events to be surfaced.

Figure 81: Packet Routed LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;         // 0111 - packet
    bit2  ppMode;          // 01   - routed
    bit2  state;           // 00->down 01->idle/enabled 10->reasm 11->error

    bit1  reserved;        // set to zero
    bit1  rtoTest;         // set to zero
    bit1  rtoEnable;
    bit5  reserved;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  reserved;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 reserved;
};

struct Misc2 {
    bit32 routedLcd;
};
```

A packet routed LCD allows packets to be received from the POS-PHY. Once received, the packet buffer is then routed internally to the scheduler and rescheduled for transmission. Normally, when a packet is received, the receive LCD address is written into the packet header and the buffer is surfaced to the user. When a packet is routed, the routedLcd field is used to fill in the LCD address in the packet header. This allows packets to be routed out the transmit interface with the same or different LCD.

The low order bits in the routedLcd field should be set correctly to free the buffer on transmit. These bits correspond to the flag bits in the packet header.

This is also called forwarded or fast forward mode.

Figure 82: Packet Cut-Through Scatter Mode LCD Packed and Miscellaneous Field Layouts

```
struct Packed {
    bit4  aalType;       // 0111 - aal5
    bit2  ppMode;        // 10   - scatter
    bit2  state;         // 00->down 01->idle/enabled 10->reasm 11->error

    bit1  reserved;      // set to zero
    bit1  rtoTest;       // set to zero
    bit1  rtoEnable;
    bit3  reserved;
    bit2  cutThruSel;

    bit4  rxqNum;
    bit4  rxPoolId;
    bit8  rxOffset;
};

struct Misc {
    bit6  numDesc;
    bit2  packHeadSel;
    bit8  reserved;
    bit16 reserved;
};

struct Misc2 {
    bit5  dropNBytes;
    bit1  useCrcNumHead;
    bit10 numHeadBytes;
    bit16 reserved;
};
```

7.5 LCD Field Definitions

The following are the definitions of the LCD fields, grouped by major function. All reserved fields should be set to zero.

Table 53: Common Field Definitions

Field Name	Field Description	Note
aalType	Specifies the AAL for this LCD. The following are the valid values: 0000 Raw Mode 0001 Raw Mode - Early Drop 0101 AAL5 0110 AAL5 - 54-Byte Mode 0111 Packet	1
ppMode	Specifies the post processing mode for this LCD. The following are the valid values: 00 Normal 01 Routed 10 Scatter/Cut-Through 11 Reserved	1
state	This specifies the reassembly state for this LCD. This field is used by the PNR, but in order to receive cells, an LCD must be initialized to idle state. The following are the valid values: 00 Down State 01 Idle State 10 Reassembling State 11 Error State	1
cutThruSel	Specifies a cut-through configuration. The cut-through configuration specifies a receive queue to get a descriptor from, a DMA queue to enqueue the descriptor to, and a set of cut-through flags.	1
rxqNum	Specifies to which receive queue normal events should be posted. Note: some events may be routed to the error queue based on your RXQUE setup.	1
rxPoolId	Specifies which POOL ID should be used when getting buffers for received packets.	1
rxOffset	Specifies the offset into the PNR buffer where the received packet should be placed. A value of ‘0’ is equivalent to 256 bytes.	1
stat0	LC statistic word zero. Default counts the total users cells with CLP=0 received on this LC. For accurate counts, this should be initialized to zero.	1
stat1	LC statistic word one. Default counts the total users cells received on this LC. For accurate counts, this should be initialized to ‘0’.	1
hostData	If enabled, the contents of this field are placed in packet of each received packet for this LCD. One use of this is to place a correlator to a host-specific data structure for this LCD.	1
ipWrd0-3	When TCP/IP Verification is enabled, these words are used by the PNR to store state between cells for the TCP/IP verification process. The frameType field specifies an offset for the checksum nanoprogram. This field is used to jump to a specific algorithm to find the IP header. The skipCount field allows the user to specify a fixed amount that is always skipped before looking for the IP header using the specified algorithm. The remainder of the words should be initialized to ‘0’.	1

1. Software should set up this field.

Table 54: Raw Mode Field Definitions

Field Name	Field Description	Note
size	This field specifies how many bytes are stored when cell is received: 01 52-Byte cell (no HEC) 00 48-Byte cell	1
storeCrc10	When set, the CRC-10 state bit is written into the packet header. A '1' is written in the error status bit in word 0 if a bad CRC-10 is detected.	1
routedLcd	When routing cells, this field is used to fill in the LCD field of the packet header. This allows the user to dynamically route cells back out the interface using a different LCD. The user should be sure to set the free on transmit bit in this field as if it were in a packet header.	1

1. Software should set up this field.

Table 55: Packet/AAL5 Field Definitions

Field Name	Field Description	Note
rtoTest	This is the reassembly timeout processing test-and-set bit. It is used by the PNR but should be initialized to '0'.	1
rtoEnable	If set, reassembly processing is enabled for this LC, if the LC is running AAL5.	1
tmpCLP	Used by the PNR to track the current state of the ORed CLP bit for the current AAL5 packet. This field should be set to '0' at initialization. After initialization, the PNR maintains this field.	1
tmpCongestion	Used by the PNR to track the current state of the ORed congestion bit for the current AAL5 packet. This field should be set to '0' at initialization time.	1
headerThresh	Specifies how much data should be received before poping a packet start event. If it is set to '0', only complete packet events will be popped.	1
buffPtr	This field is used by the PNR, but should be initialized to zero by software. This field is used to track the current packet under reassembly.	1
crcState	This field is used by the PNR to maintain the CRC residue as the current packet is reassembled. It should be initialized to '0'.	
routedLcd	When routing cells, this field is used to fill in the LCD field of the packet header. This allows the user to dynamically route cells back out the interface using a different LCD. The user should be sure to set the free on transmit bit in this field as if it were in a packet header.	1
cutThruThresh	Used to determine how much cut-through data is DMAed.	1
dmaedHeader	This is used by the PNR for cut-through Mode 7 processing. This should be initialized to '0'.	1
numDesc	This is used by thePNR for scatter processing, and should be initialized to '0'.	1
packHeadSel	Specifies which packet header should be used for this connection. See *3.14.6.8: RXAAL Packet Header Configuration* on page 335 for more information.	1
oamMask	Specifies how OAM traffic should be filtered. See *3.14.1.1: ATM OAM Cell Processing* on page 303 for more information.	
useCrcNumHead	When set, specifies that receive CRC will determine how many bytes to use for numHeadBytes. This is useful when a connection is carrying IP traffic, and the TCP/IP header lengths can be determined.	1
numHeadBytes	Specifies how many bytes of data should be kept with the packet header when DMAing the final DMA list for a completed scatter packet. Must be less than the page size.	1
dropNBytes	Allows 0-31 bytes of packet data to be dropped from the beginning of the packet on POS-PHY networks.	1

1. Software should set up this field.

Revision Log

Rev.	Description
8/31/99	Initial release (00).
3/31/00	First revision (01). Updated content to describe IBM Processor for Network Resources Version 2.6 (IBM32NPCXXEPABBD66). • In the COMET/PAKIT entities, the memory controller no longer supports burst length 1 for SDRAM; only burst length 2 is supported. The SDRAM RAS to CAS delay T_{RCD} becomes programmable with the new revision. • In the CJTAG entity, the JTAG revision ID changed from x'44103049' to x'14700049'. • In the CRSET entity, bits 3-0 of the CRSET Control Register are now reserved. • In the DMAQS entity, bits 31-30 and 27-24 of the DMAQS Upper Bound/Properites Registers are no longer reserved. • In the POOLS entity, the definition of bit 18 of the POOLS control register has changed. • In the INTST entity, the power on reset value of the INTST Debug States Control register has changed. The decode of bits 7-0 of this register have also changed. • In the PCINT entity, the power on reset value of the PCI revision ID in PCINT Config Word 2 register has changed to reflect the new revision of the PNR. The PCI class code also stored in PCINT Config Word 2 register can now be modified by software. • Updated Pin Signal Lists. Reorganized the databook as follows: • Separated COBRA, RS-232, and PPOCM registers from their former locations within the PCORE section and moved them into their own sections. • Moved former Data Flow section into *7: Application Notes: Data Structures* on page 673. • Moved Physical Description from before I/O Definitions to after Register Descriptions. • Added DC Electrical Characteristics.
5/10/00	Second revision (02). In *3.15 Receive Queues (RXQUE)*, added three events to *Table 19: Event Summary and Routing Information* (x'3F', x'6E', and x'6F'0. Corrected numbering of fourth level headings. In *7. Application Notes: Data Structures*, changed all third-level headings to figures. Updated *Contents* and *List of Figures*. In *4. Physical Description and Signal Definitions*, improved pinout and signal pin list, added tables for VDD and ground pins, and added table defining library elements. Corrected many minor formatting and typographical flaws.
5/22/00	Third revision (03). Corrected part number for IBM Processor for Network Resources Version 2.61 to IBM32NPCXX1EPABBD66.
7/13/00	Fourth revision (04). Corrected type designation of *3.6.5 COMET/PAKIT Lock Enable Register*. In *3.12.17 Debugging Register Access*, added three registers: *LCD Cache LCD Address Registers*, *LCD Cache State Machine Variables Register*, and *LCD Cache LRU State Register*. In *3.14.6.13 RXAAL Scatter/Cut Through Info Registers*, correctly divided Scatter/Cut Through Info Register 1 and Scatter/Cut Through Info Register 2. In RXQUE Events, added *3.15.3.9: RXAAL Picoprocessor Generated Events* on page 361. Renumbered former sections 3.15.4 - 3.15.10 (lists of RXQUE events, by category) to be fourth level entries below *3.15.3 RXQUE Events*. In *7.2 General LCD*, corrected Figure 57. Added die dimensions to *Figure 36: Package Diagram*. Corrected shading of Ground pins in *Figure 37: Pinout Viewed from Above*.
7/2700	Fifth revision (05). Changed product number from IBM32NPCXX1EPABBD66 to IBM32NPCXX1EPABBE66.
8/14/00	Sixth revision (06). In *2. Input/Output Definitions* Table 12 on page 31, corrected RXCLK definition.