



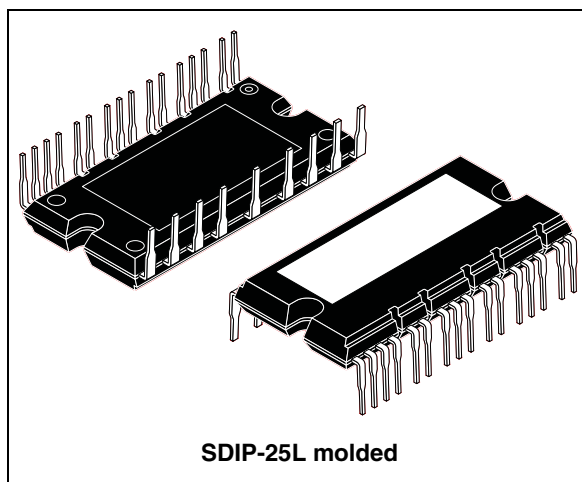
STGIPS20K60

IGBT intelligent power module (IPM)
17 A - 600 V - SDIP-25L molded

Preliminary data

Features

- 17 A, 600 V 3-phase IGBT inverter bridge including control ICs for gate driving and free-wheeling diodes
- 3.3 V, 5 V, 15 V CMOS/TTL inputs comparators with hysteresis and pull down / pull up resistors
- Internal bootstrap diode
- Dead time and interlocking function
- $V_{CE(sat)}$ negative temperature coefficient
- Short-circuit rugged IGBTs
- Undervoltage lockout
- Smart shutdown function
- Comparator for fault protection against over temperature and overcurrent
- DBC fully isolated package
- Isolation rating of 2500 Vrms/min



short-circuit rugged IGBT system technology. Please refer to dedicated technical note TN0107 for mounting instructions.

Applications

- 3-phase inverters for motor drives
- Home appliances, such as washing machines, refrigerators, air conditioners

Description

The new intelligent power module developed by STMicroelectronics provides a compact, high performance AC motor drive for a simple and rugged design. It mainly targets low power inverters for applications such as home appliances and air conditioners. It combines ST proprietary control ICs with the most advanced

Table 1. Device summary

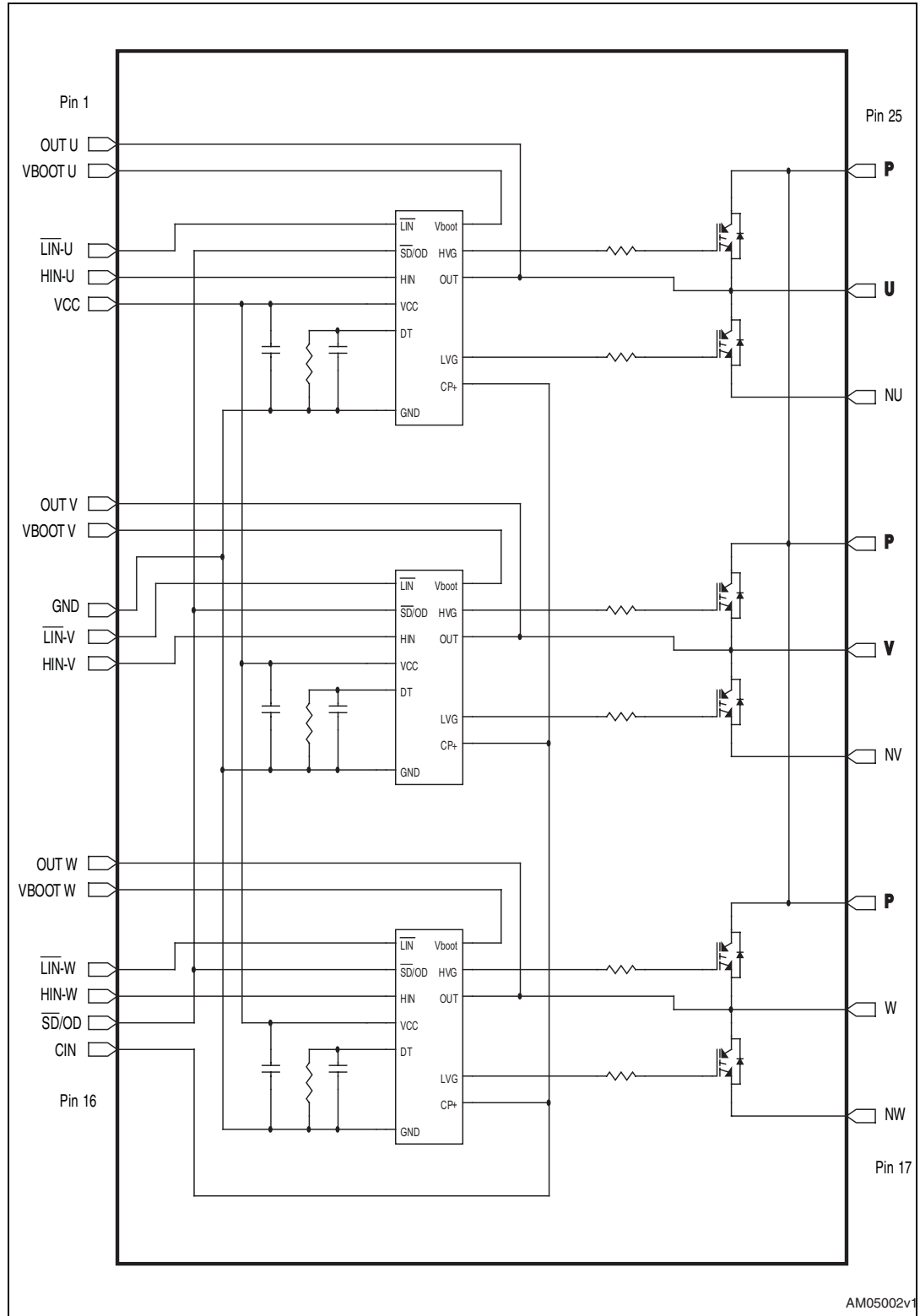
Order code	Marking	Package	Packaging
STGIPS20K60	GIPS20K60	SDIP-25L molded	Tube

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1 Internal block diagram and pin configuration

Figure 1. Internal block diagram

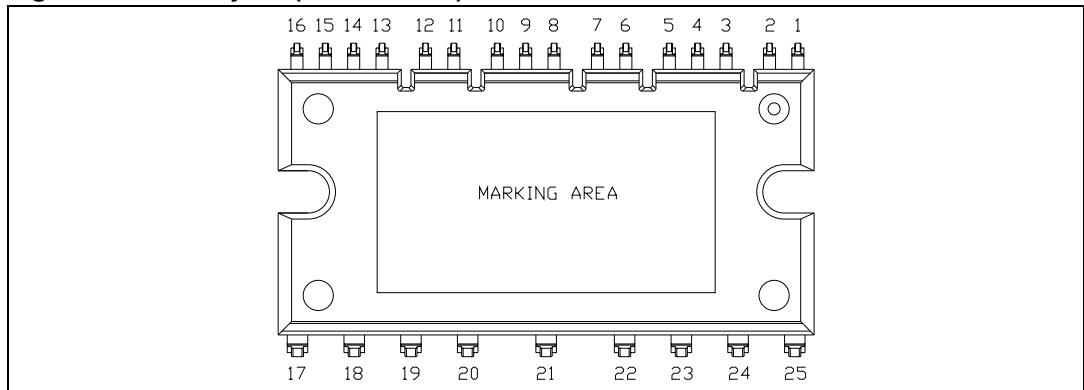


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Table 2. Pin description

Pin n°	Symbol	Description
1	OUT _U	High-side reference output for U phase
2	V _{bootU}	Bootstrap voltage for U phase
3	$\overline{\text{LIN}}_{\text{U}}$	Low-side logic input for U phase
4	HIN _U	High-side logic input for U phase
5	V _{CC}	Low voltage power supply
6	OUT _V	High-side reference output for V phase
7	V _{boot V}	Bootstrap voltage for V phase
8	GND	Ground
9	$\overline{\text{LIN}}_{\text{V}}$	Low-side logic input for V phase
10	HIN _V	High-side logic input for V phase
11	OUT _W	High-side reference output for W phase
12	V _{boot W}	Bootstrap voltage for W phase
13	$\overline{\text{LIN}}_{\text{W}}$	Low-side logic input for W phase
14	HIN _W	High-side logic input for W phase
15	$\overline{\text{SD}} / \text{OD}$	Shutdown logic input (active low) / open-drain (comparator output)
16	CIN	Comparator input
17	N _W	Negative DC input for W phase
18	W	W phase output
19	P	Positive DC input
20	N _V	Negative DC input for V phase
21	V	V phase output
22	P	Positive DC input
23	N _U	Negative DC input for U phase
24	U	U phase output
25	P	Positive DC input

Figure 2. Pin layout (bottom view)



2 Absolute maximum ratings

Table 3. Inverter part

Symbol	Parameter	Value	Unit
V_{PN}	Supply voltage applied between P - N_U , N_V , N_W	450	V
$V_{PN(surge)}$	Supply voltage (surge) applied between P - N_U , N_V , N_W	500	V
V_{CES}	Collector emitter voltage ($V_{IN}^{(1)} = 0$)	600	V
$\pm I_C^{(2)}$	Each IGBT continuous collector current at $T_C = 25^\circ\text{C}$	17	A
$\pm I_{CP}^{(3)}$	Each IGBT pulsed collector current	40	A
P_{TOT}	Each IGBT total dissipation at $T_C = 25^\circ\text{C}$	42	W
t_{scw}	Short circuit withstand time, $V_{CE} = 0.5 V_{(BR)CES}$ $T_J = 125^\circ\text{C}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$	5	μs

1. Applied between HIN_i , \overline{LIN}_i and GND for $i = U, V, W$
2. Calculated according to the iterative formula:

$$I_C(T_C) = \frac{T_{j(max)} - T_C}{R_{thj-c} \times V_{CE(sat)(max)}(T_{j(max)}, I_C(T_C))}$$

3. Pulse width limited by max junction temperature

Table 4. Control part

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between OUT_U , OUT_V , OUT_W - GND	$V_{boot} - 21$ to $V_{boot} + 0.3$	V
V_{CC}	Low voltage power supply	-0.3 to +21	V
V_{CIN}	Comparator input voltage	-0.3 to $V_{CC} + 0.3$	V
V_{boot}	Bootstrap voltage applied between $V_{boot\ i} - OUT_i$ for $i = U, V, W$	-0.3 to 620	V
V_I	Logic input voltage	-0.3 to 15	V
V_{OD}	Open-drain voltage	-0.3 to 15	V
dV_{OUT}/dt	Allowed output slew rate	50	V/ns

Table 5. Total system

Symbol	Parameter	Value	Unit
V_{OUT}	Output voltage applied between U, V, W - GND	450	V
V_{ISO}	Isolation withstand voltage applied between each pin and heatsink plate (AC voltage, $t = 60\text{ sec.}$)	2500	V
T_J	Operating junction temperature	-40 to 125	$^\circ\text{C}$

Table 6. Thermal data

Symbol	Parameter	Value	Unit
R_{thJC}	Thermal resistance junction-case single IGBT	2.4	°C/W
	Thermal resistance junction-case single diode	5	°C/W

3 Electrical characteristics

($T_J = 25\text{ °C}$ unless otherwise specified)

Table 7. Inverter part

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
$V_{CE(sat)}$	Collector-emitter saturation voltage	$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 12\text{ A}$	-	2.2	2.75	V
		$V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \div 5\text{ V}$, $I_C = 12\text{ A}$, $T_J = 125\text{ °C}$	-	1.8		
I_{CES}	Collector-cut off current ($V_{IN}^{(1)} = 0$ "logic state")	$V_{CE} = 600\text{ V}$, $V_{CC} = V_{Boot} = 15\text{ V}$	-		100	μA
V_F	Diode forward voltage	$V_{IN}^{(1)} = 0$ "logic state", $I_C = 12\text{ A}$	-	1.9		V
High-side inductive load						
t_{on}	Turn-on time	$V_{PN} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \leftrightarrow 5\text{ V}$, $I_C = 12\text{ A}$ (see Figure 3)	-	TBD	-	ns
$t_{c(on)}$	Crossover time (on)		-	TBD	-	
t_{off}	Turn-off time		-	TBD	-	
$t_{c(off)}$	Crossover time (off)		-	TBD	-	
t_{rr}	Reverse recovery time		-	TBD	-	
E_{on}	Turn-on switching losses		-	TBD	-	μJ
E_{off}	Turn-off switching losses		-	TBD	-	
Low-side inductive load						
t_{on}	Turn-on time	$V_{PN} = 300\text{ V}$, $V_{CC} = V_{boot} = 15\text{ V}$, $V_{IN}^{(1)} = 0 \leftrightarrow 5\text{ V}$, $I_C = 12\text{ A}$ (see Figure 3)	-	TBD	-	ns
$t_{c(on)}$	Crossover time (on)		-	TBD	-	
t_{off}	Turn-off time		-	TBD	-	
$t_{c(off)}$	Crossover time (off)		-	TBD	-	
t_{rr}	Reverse recovery time		-	TBD	-	
E_{on}	Turn-on switching losses		-	TBD	-	μJ
E_{off}	Turn-off switching losses		-	TBD	-	

1. Applied between HIN_i , $\overline{LIN_i}$ and GND for $i = U, V, W$

Note: t_{ON} and t_{OFF} include the propagation delay time of the internal drive. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the internally given gate driving condition.

3.1 Control part

Table 8. Low voltage power supply

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{CC_hys}	V _{CC} UV hysteresis		1.2	1.5		V
V _{CC_thON}	V _{CC} UV turn ON threshold		11.5	12.0		V
V _{CC_thOFF}	V _{CC} UV turn OFF threshold		10	10.5		V
I _{qccu}	Undervoltage quiescent supply current	V _{CC} = 10 V SD = 5 V; LIN = 5 V; and HIN = GND; CP+ = GND		350	450	μA
I _{qcc}	Quiescent current	V _{CC} = 15 V SD = 5 V; LIN = 5 V; and HIN = GND; CP+ = GND		2	3.5	mA
V _{ref}	Internal reference voltage		0.5	0.54	0.58	mV

Table 9. Bootstrapped voltage

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{BS_hys}	V _{BS} UV hysteresis		1.2	1.5		V
V _{BS_thON}	V _{BS} UV turn ON threshold		10.6	11.5		V
V _{BS_thOFF}	V _{BS} UV turn OFF threshold		9.0	10.0		V
I _{QBSU}	Undervoltage V _{BS} quiescent current	V _{BS} = 10 V SD = 5 V; LIN and HIN = 5 V; CP+ = GND		70	110	μA
I _{QBS}	V _{BS} quiescent current	V _{BS} = 15 V SD = 5 V; LIN and HIN = 5 V; CP+ = GND		150	210	μA
R _{DS(on)} ⁽¹⁾	Bootstrap driver on resistance	LVG ON		120		Ω

1. R_{DS(on)} is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{boot1}) - (V_{CC} - V_{boot2})}{I_{boot1}(V_{CC}, V_{boot1}) - I_{boot2}(V_{CC}, V_{boot2})}$$

Table 10. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{il}	Low logic level voltage				0.8	V
V_{ih}	High logic level voltage		2.25			V
I_{HINh}	HIN logic "1" input bias current	HIN = 15 V		175	260	μ A
I_{HINl}	HIN logic "0" input bias current	HIN = 0 V			1	μ A
I_{LINl}	\overline{LIN} logic "0" input bias current	\overline{LIN} = 0 V		6	20	μ A
I_{LINh}	\overline{LIN} logic "1" input bias current	\overline{LIN} = 15 V			1	μ A
I_{SDh}	\overline{SD} logic "1" input bias current	\overline{SD} = 15 V		120	300	μ A
I_{SDl}	\overline{SD} logic "0" input bias current	\overline{SD} = 0 V			3	μ A
Dt	Dead time	see Figure 4		600		ns

Table 11. Sense comparator characteristics ($V_{CC} = 15$ V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{io}	Input bias current	$V_{CP+} = 1$ V	-		3	μ A
V_{ol}	Open-drain low-level output voltage	$I_{od} = -3$ mA	-		0.5	V
t_{d_comp}	Comparator delay	\overline{SD}/OD pulled to 5 V through 100 k Ω resistor	-	90	130	ns
SR	Slew rate	$C_L = 180$ pF; $R_{pu} = 5$ k Ω	-	60		V/ μ sec

Table 12. Truth table

Input			Output	
\overline{SD}	\overline{LIN}	HIN	LVG	HVG
L	X	X	L	L
H	H	L	L	L
H	L	H	L	L
H	L	L	H	L
H	H	H	L	H

Note: X: don't care

3.2 Waveforms definitions

Figure 3. Switching time definition

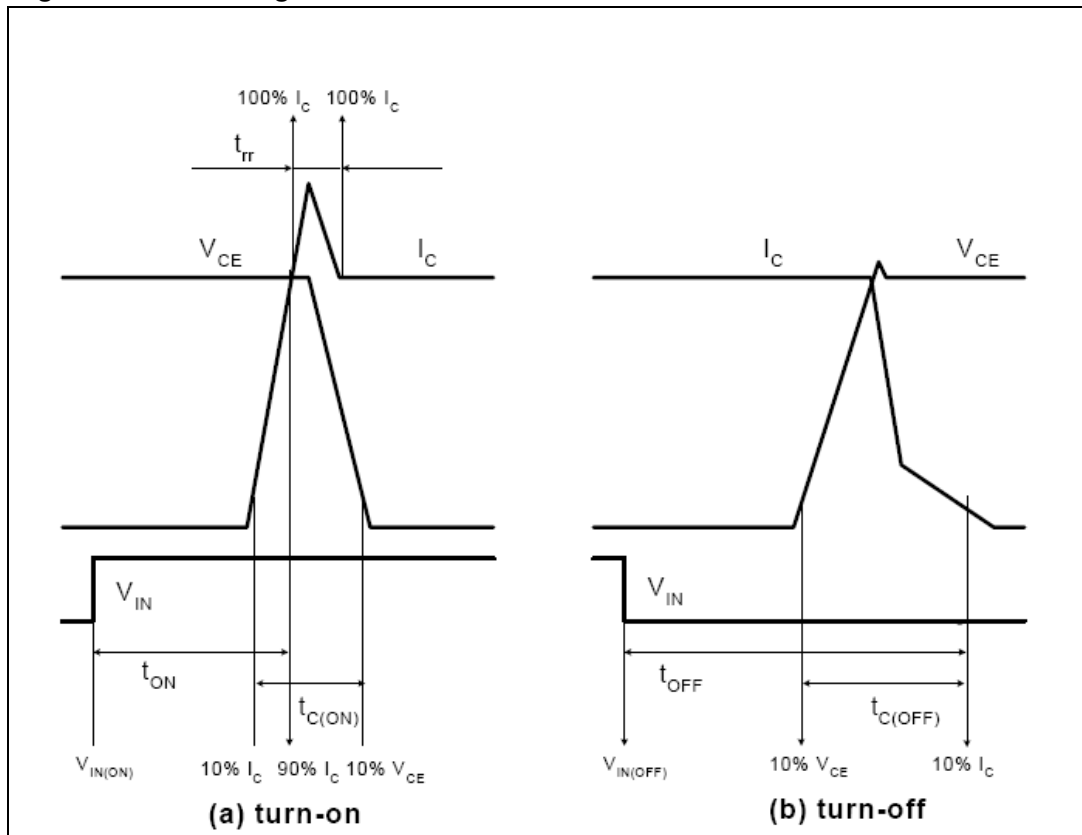
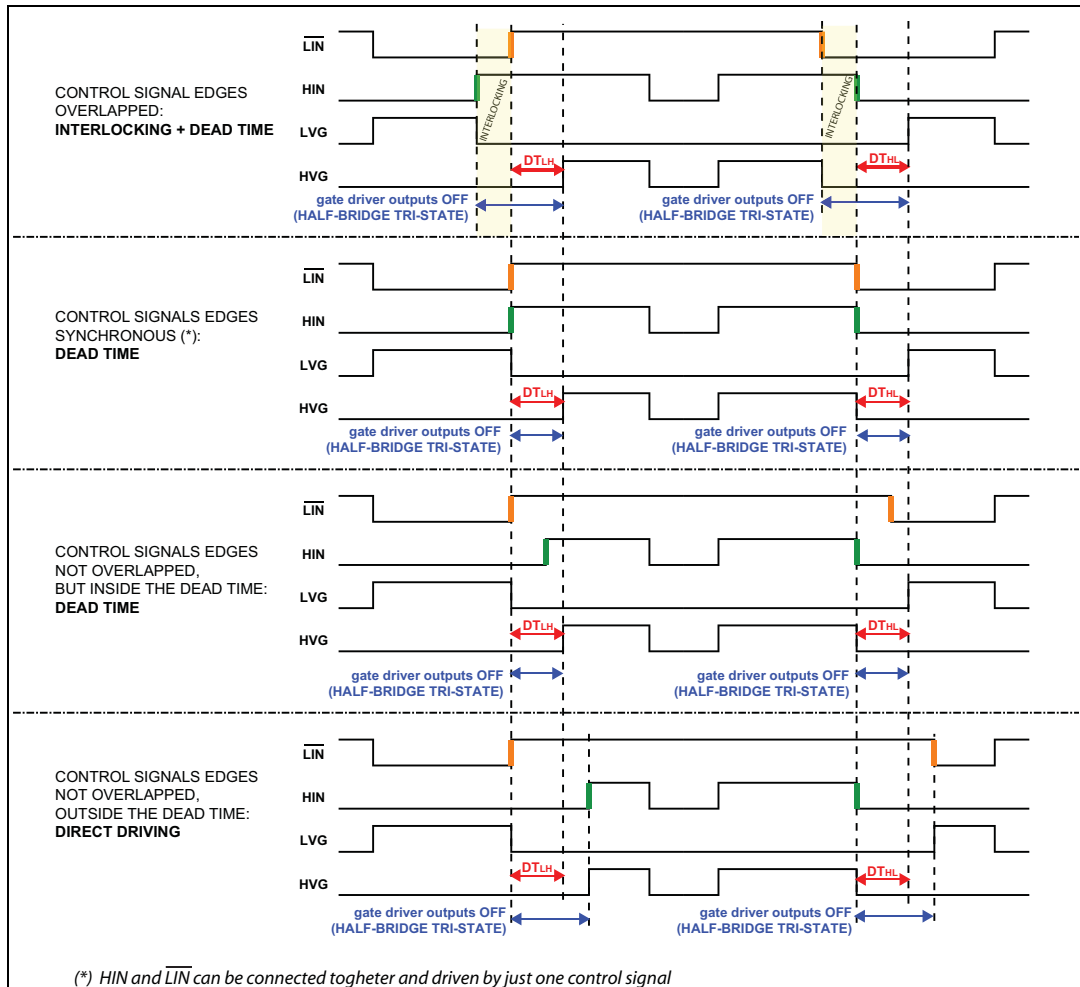


Figure 4. Dead time and interlocking waveforms definitions



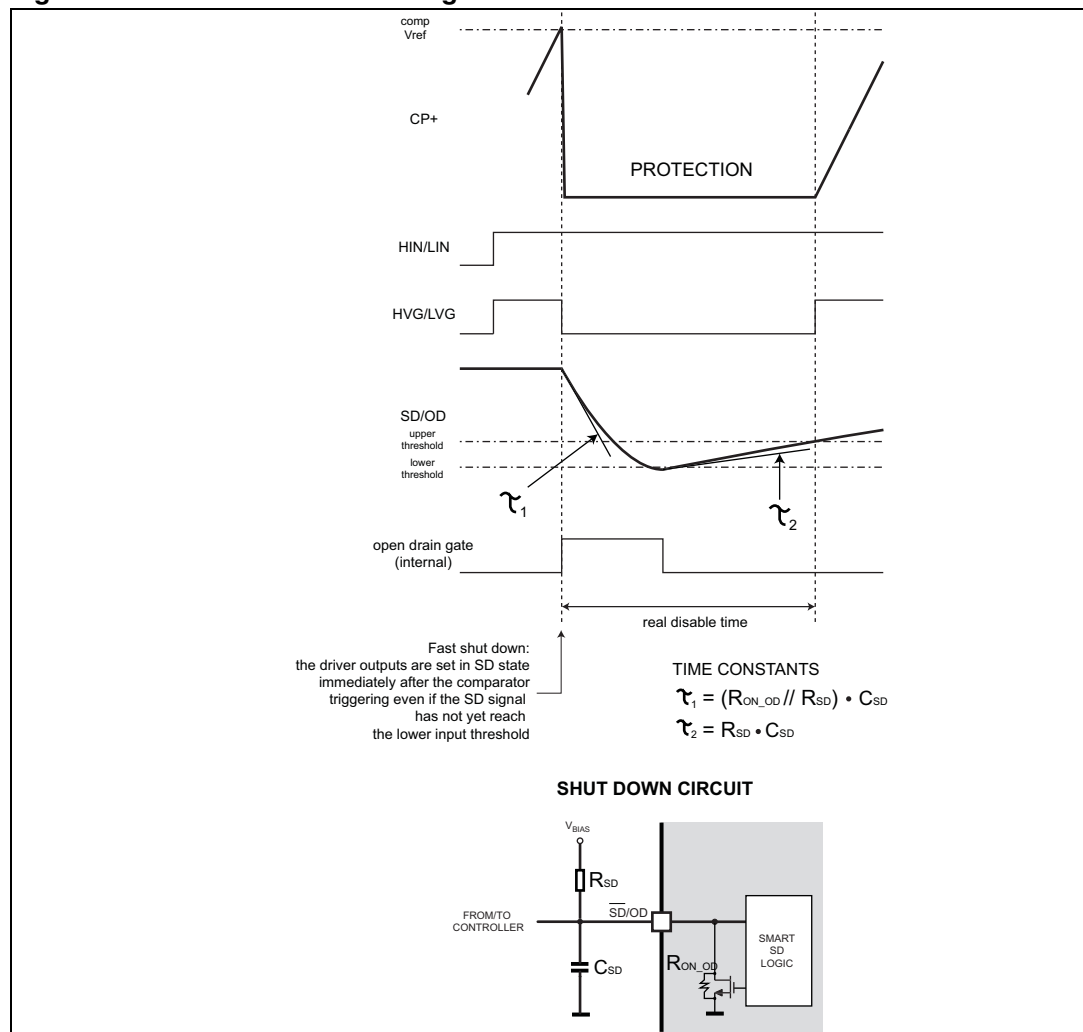
4.1 Recommendations

- To prevent the input signals oscillation, the wiring of each input should be as short as possible.
- By integrating an application specific type HVIC inside the module, direct coupling to MCU terminals without any opto-coupler is possible.
- Each capacitor should be located as nearby the pins of IPM as possible.
- Low inductance shunt resistors should be used for phase leg current sensing.
- Electrolytic bus capacitors should be mounted as close to the module bus terminals as possible. Additional high frequency ceramic capacitor mounted close to the module pins will further improve performance.
- The \overline{SD} signal should be pulled up to 5 V / 3.3 V with an external resistor (see [Section 5: Smart shutdown function](#) for detailed info).

5 Smart shutdown function

The STGIPS14K60 integrates a comparator for fault sensing purposes. The comparator non-inverting input (CIN) can be connected to an external shunt resistor in order to implement a simple over-current protection function. When the comparator triggers, the device is set in shutdown state and both its outputs are set to low-level leading the half-bridge in tri-state. In the common overcurrent protection architectures the comparator output is usually connected to the shutdown input through a RC network, in order to provide a mono-stable circuit, which implements a protection time that follows the fault condition. Our smart shutdown architecture allows to immediately turn-off the output gate driver in case of overcurrent, the fault signal has a preferential path which directly switches off the outputs. The time delay between the fault and the outputs turn-off is no more dependent on the RC values of the external network connected to the shutdown pin. At the same time the internal logic turns on the open-drain output and holds it on until the shutdown voltage goes below the logic input lower threshold. Finally the smart shutdown function provides the possibility to increase the real disable time without increasing the constant time of the external RC network.

Figure 6. Smart shutdown timing waveforms



6 Package mechanical data

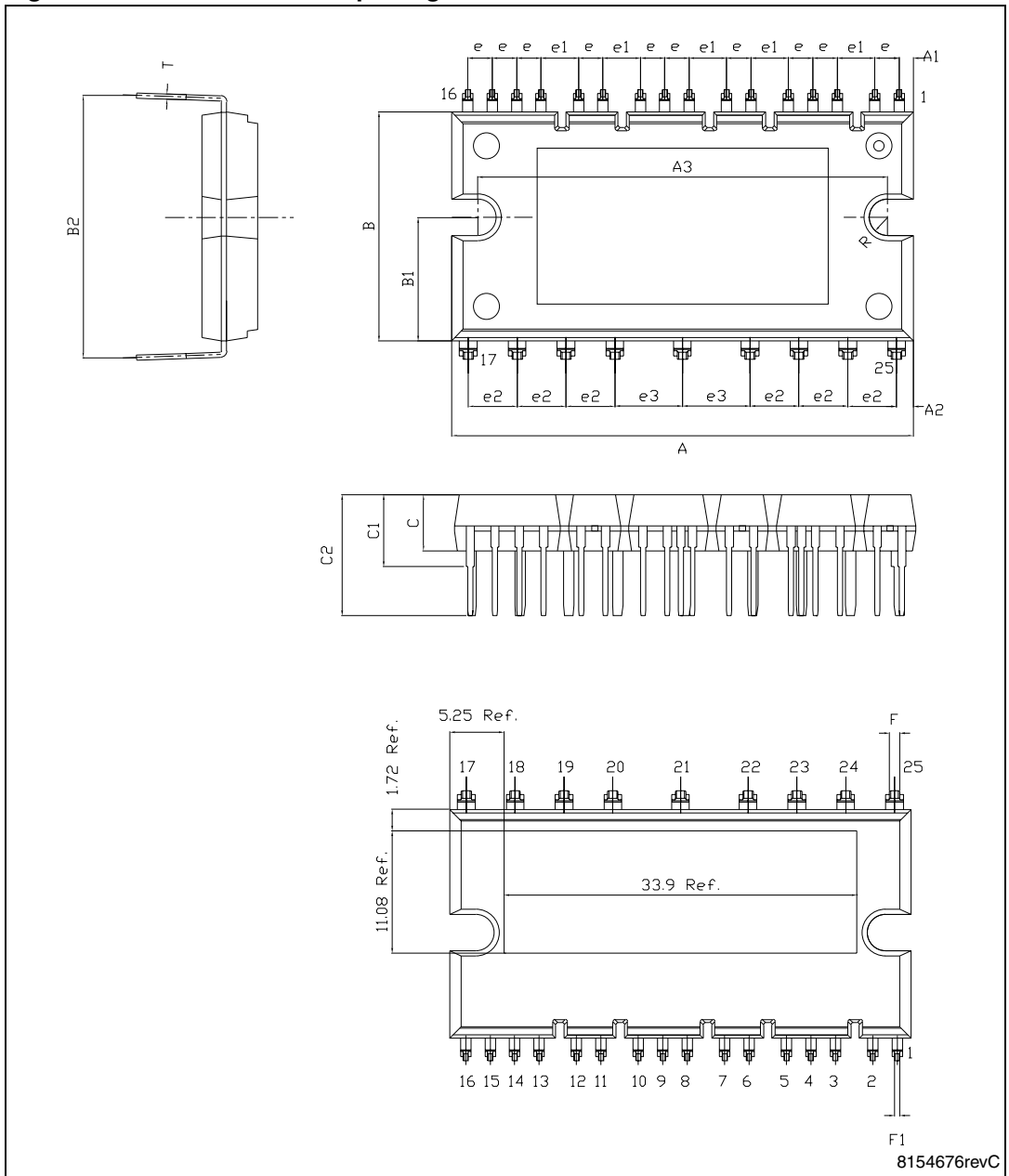
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Please refer to dedicated technical note TN0107 for mounting instructions.

Table 13. SDIP-25L molded package mechanical data

Dim.	(mm.)		
	Min.	Typ.	Max.
A	44	-	44.8
A1	0.95	-	1.75
A2	1.2	-	2
A3	39	-	39.8
B	21.6	-	22.4
B1	11.45	-	12.25
B2	24.83	-	25.63
C	5	-	5.8
C1	6.4	-	7.4
C2	11.1	-	12.1
e	1.95	-	2.75
e1	3.2	-	4
e2	4.3	-	5.1
e3	6.1	-	6.9
F	0.8	-	1.2
F1	0.3	-	0.7
R	3	-	4
T	0.4	-	0.7

Figure 7. SDIP-25L molded package mechanical data



7 Revision history

Table 14. Document revision history

Date	Revision	Changes
10-Aug-2009	1	Initial release

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