CMOS LOW VOLTAGE GATE ARRAY

DESCRIPTION

The SLA600L Series is a master slice CMOS gate array developed as a low voltage version of the SLA6000 Series. It covers 500 to 6,200 gates, the gate capacity range that is most demanded in the gate array market. Operating on low voltage, the SLA600L LSI can be applied to portable products. The SLA600L Series incorporates all of the advantages that ordinary gate arrays can provide, such as quick development and high system reliability. Changing the delay value of the SLA6000 Series MSI library enables the user to utilize all macro cells so that an SLA600L gate array system can be designed with the same technique as the SLA6000 Series.

FEATURES

- Eight items cover the wide range of scale from 513 to 6,206 gates.
- Operating voltage 1.8 to 3.5V
- Applicable to portable products
- Input/output CMOS compatible
- Even small orders for LSI will be accepted.
- Speedy development and delivery
- Delay time (V_{DD} = 3V, Ta = 25°C) ..... Internal gate 4ns
  Input buffer ..... 5 to 8ns
  Output buffer ..... 10 to 16ns

SLA600L SERIES

Parameter \ Series	SLA605L	SLA608L	SLA614L	SLA617L	SLA627L	SLA633L	SLA643L	SLA662L
Gates (2-input NAND)	513	820	1,394	1,746	2,667	3,312	4,342	6,206
Technology	Si-CMOS 2 LAYER METALLIZATION							
I/O level	CMOS							
Delay factor	Maximum delay (V_{DD}=1.8V, Ta=70 degrees C) is 4.66 x typical delay of the SLA6000 Series. Minimum delay (V_{DD}=3.5V, Ta=0 degrees C) is 0.88 x typical delay of the SLA6000 Series.							
Total ports for I/O (Terminals only for input port)	48	60	74	82	100	110	126	154
	(6)	(6)	(6)	(6)	(6)	(6)	(6)	(8)
Output mode	Normal, Open-drain, 3-state, Bi-directional							

ABSOLUTE MAXIMUM RATINGS

(Vss=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	- 0.3 to 7.0	V
Input voltage	V_I	- 0.3 to V_{DD}+0.3	V
Output voltage	V_O	- 0.3 to V_{DD}+0.3	V
Storage temperature	T_{stg}	- 65 to l50	°C

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}		1.8	—	3.5	V
Operating temperature	T_{opr}		0	—	70	°C

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3V, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply current	I_{DD}	Standby	—	2	—	μA
High level output current	I_{OH}	V_{DD} = 3V V_{OH}=V_{DD} -0.4	—	2	—	mA
Low level output current	I_{OL}	V_{DD} = 3V V_{OL} = V_{SS} +0.4	—	4	—	mA
High level input voltage	V_{IH}	V_{DD} = 3V	2.4	—	—	V
Low level input voltage	V_{IL}	V_{DD} = 3V	—	—	0.6	V
Input leakage current	I_{LI}		- 1	—	1	μA

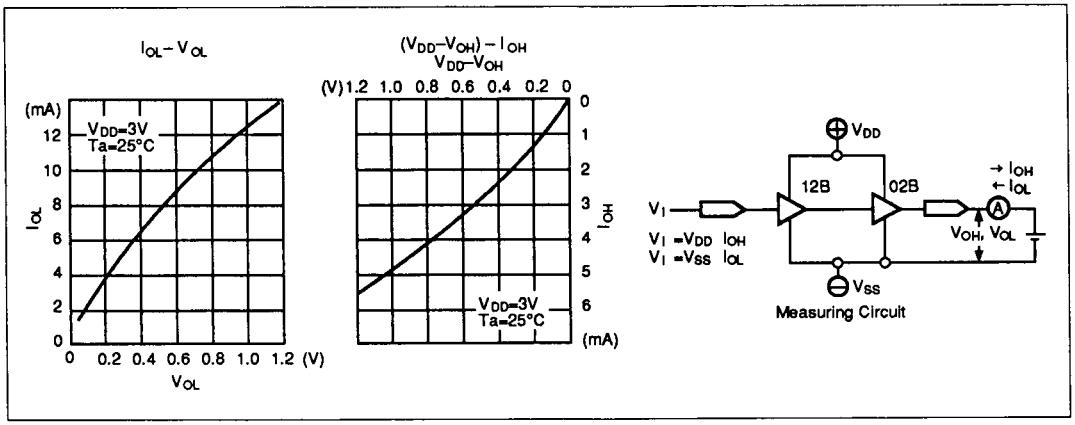
PACKAGE LIST

Type	Pin No.	Pkg.name	SLA605L	SLA608L	SLA614L	SLA617L	SLA627L	SLA633L	SLA643L	SLA662L
Plastic DIP	14pin	C14	A	A						
	16pin	C16	A	A						
	18pin	C18	A	A						
	24pin	C24	A	A	A	A				
	28pin	C28	A	A	A	A	A			
	40pin	C40	A	A	A	A	A	F		
	42pin	C42	A	A	A	A	A	F		
Plastic FP	44pin	F44-2		A	A	A	F			
	46pin	F46-5	A	A	A	A	A	A	A	
	60pin	F60-2	A	A	A	A	A	F		
	60pin	F60-5	A	A	A	A	A	A	A	
	80pin	F80-5			A	A	A	A	A	
	100pin	F100-5				A	A	A	A	
Ceramic FP	148pin	H148						A	A	A
Plastic SOP	24pin	M24	A	A	A					
	28pin	M28-2		A	A					
Plastic shrink Dip	28pin	S28		A						
	42pin	S42								
	64pin	S64			A	A	A			
Ceramic PGA	64pin	P64			A	A	A	A		
	72pin	P72				A	A	A		
	132pin	P132					A	A	A	A
PLCC	44pin	J44	A	A	A	A	A	A	A	
	68pin	J68			A	A	A	A	A	A
	84pin	J84				A	A	A	A	A

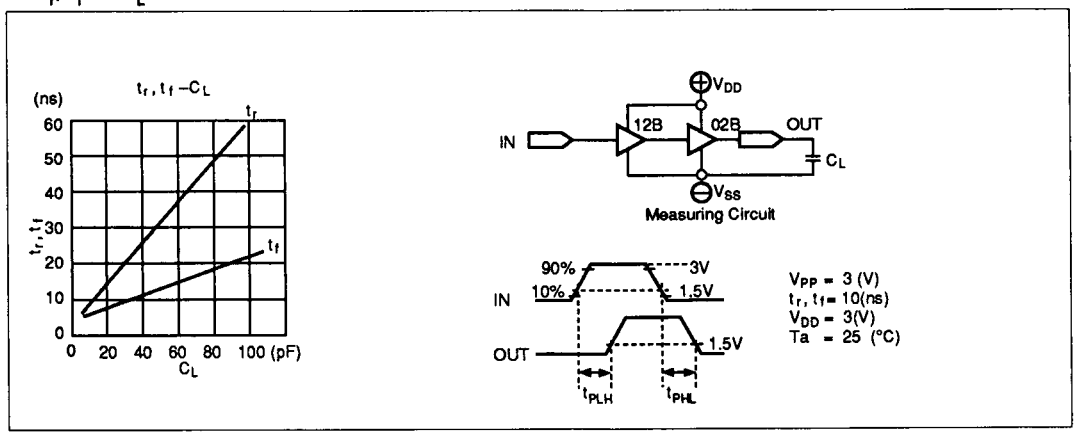
A: Available F: Under development

■ PERFORMANCE CURVES

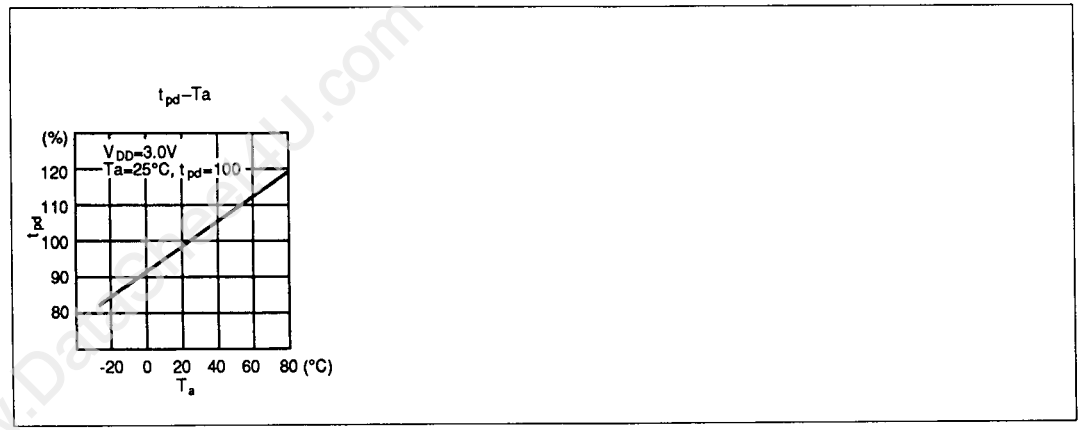
● Output Current



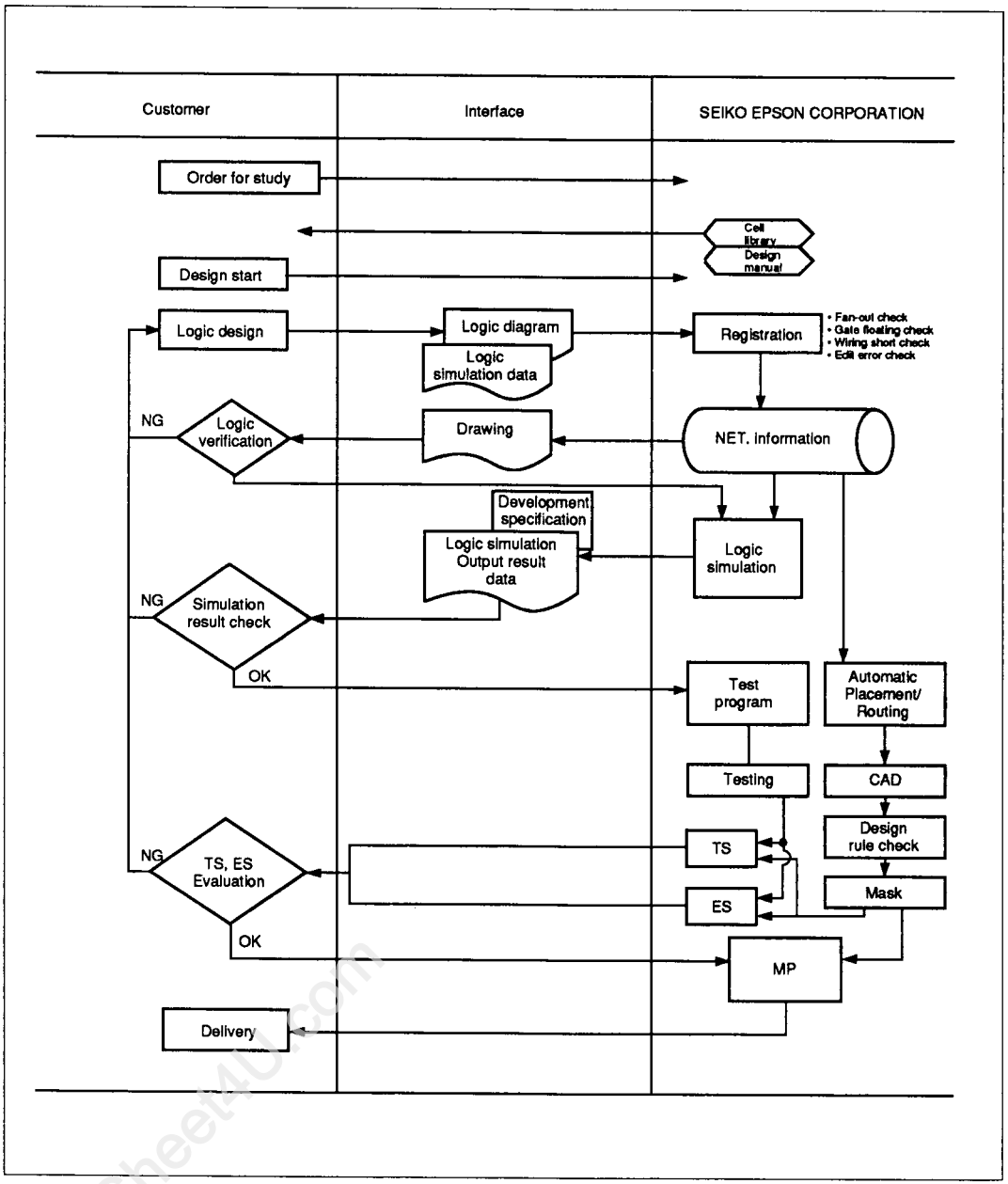
● t_r, t_f — C_L



● Delay Time



GATE ARRAY DESIGN FLOW



NOTE: Values in the properties table are specified as Max or Min according to the comparison on the numerical coordinate.
NOTE: All specification of this device are subject to change without notice.