C167CR-xC
Step GA

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Microcontrollers

C166 Family

16-Bit Single-Chip Microcontroller

C167CR-xC, Bare Die, Step GA

Data Sheet 1999-11 (Bare Die Delivery)

C167CR-xC (Bare Die Delivery) Revision History:	1999-11, Step GA
Previous Versions:	1999-11 (Step FA) 10.97 (Step BA) 05.97 (Step BA)

Page	Subjects (Changes compared to step BA)
2	Derivative table updated
4 - 12	Pad Configuration updated (figure and table) [1]
14, 15	Representation of parameters updated
16	Chip outline adapted
17	Wafer characteristics adapted

[1] Pad coordinates have changed compared to step FA.

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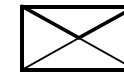

Edition 1999-11

Published by Infineon Technologies AG,
St.-Martin-Strasse 53
D-81541 München

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C166 Family of C167CR-xC
High-Performance CMOS 16-Bit Microcontrollers

Preliminary
C167CR-xC 16-Bit Microcontroller

- High Performance 16-bit CPU with 4-Stage Pipeline
  - 80 ns Instruction Cycle Time at 25/ MHz CPU Clock
  - 400 ns Multiplication (16 × 16 bit), 800 ns Division (32 / 16 bit)
  - Enhanced Boolean Bit Manipulation Facilities
  - Additional Instructions to Support HLL and Operating Systems
  - Register-Based Design with Multiple Variable Register Banks
  - Single-Cycle Context Switching Support
  - 16 MBytes Total Linear Address Space for Code and Data
  - 1024 Bytes On-Chip Special Function Register Area
- 16-Priority-Level Interrupt System with 56 Sources, Sample-Rate down to 40 ns
- 8-Channel Interrupt-Driven Single-Cycle Data Transfer Facilities via Peripheral Event Controller (PEC)
- Clk. Generation via on-chip PLL (1:1.5/2/2.5/3/4/5), via prescaler or via direct clk. inp.
- On-Chip Memory Modules
  - 2 KBytes On-Chip Internal RAM (IRAM)
  - 2 KBytes On-Chip Extension RAM (XRAM)
  - 32 KBytes On-Chip Mask ROM optional
- On-Chip Peripheral Modules
  - 16-Channel 10-bit A/D Converter with Programmable Conversion Time down to 7.8 µs
  - Two 16-Channel Capture/Compare Units
  - 4-Channel PWM Unit
  - Two Multi-Functional General Purpose Timer Units with 5 Timers
  - Two Serial Channels (Synchronous/Asynchronous and High-Speed-Synchronous)
  - On-Chip CAN Interface (Rev. 2.0B active) with 15 Message Objects (Full CAN / Basic CAN)
- Up to 16 MBytes External Address Space for Code and Data
  - Programmable External Bus Characteristics for Different Address Ranges
  - Multiplexed or Demultiplexed External Address/Data Buses with 8-Bit or 16-Bit Data Bus Width
  - Five Programmable Chip-Select Signals
  - Hold- and Hold-Acknowledge Bus Arbitration Support
- Idle and Power Down Modes
- Programmable Watchdog Timer and Oscillator Watchdog
- Up to 111 General Purpose I/O Lines, partly with Selectable Input Thresholds and Hysteresis

- Supported by a Large Range of Development Tools like C-Compilers, Macro-Assembler Packages, Emulators, Evaluation Boards, HLL-Debuggers, Simulators, Logic Analyzer Disassemblers, Programming Boards
- On-Chip Bootstrap Loader

Ordering Information

Table 1 Bare Die Ordering Information

Type	Ordering Code	Wafers	Function
SAK-C167CR-LC	Q67120-C2227	Whole	16-bit microcontroller with 2*2 KByte RAM, on-chip CAN Temperature range -40 to +125 °C
SAK-C167CR-4RC	Q67120-D....	Whole	16-bit microcontroller with 32 KByte ROM 2*2 KByte RAM, on-chip CAN Temperature range -40 to +125 °C
SAK-C167CR-LC	Q67120-C2226	Sawn	16-bit microcontroller with 2*2 KByte RAM, on-chip CAN Temperature range -40 to +125 °C

Note: The ordering codes for Mask-ROM versions are defined for each product after verification of the respective ROM code.

For simplicity all versions are referred to by the term **C167CR-xC** throughout this document.

Introduction

The C167CR-xC derivatives are high performance derivatives of the Infineon C166 Family of full featured single-chip CMOS microcontrollers. They combine high CPU performance (up to 12.5 million instructions per second) with high peripheral functionality and enhanced IO-capabilities. They also provide clock generation via PLL and various on-chip memory modules like program ROM, internal RAM, and extension RAM.

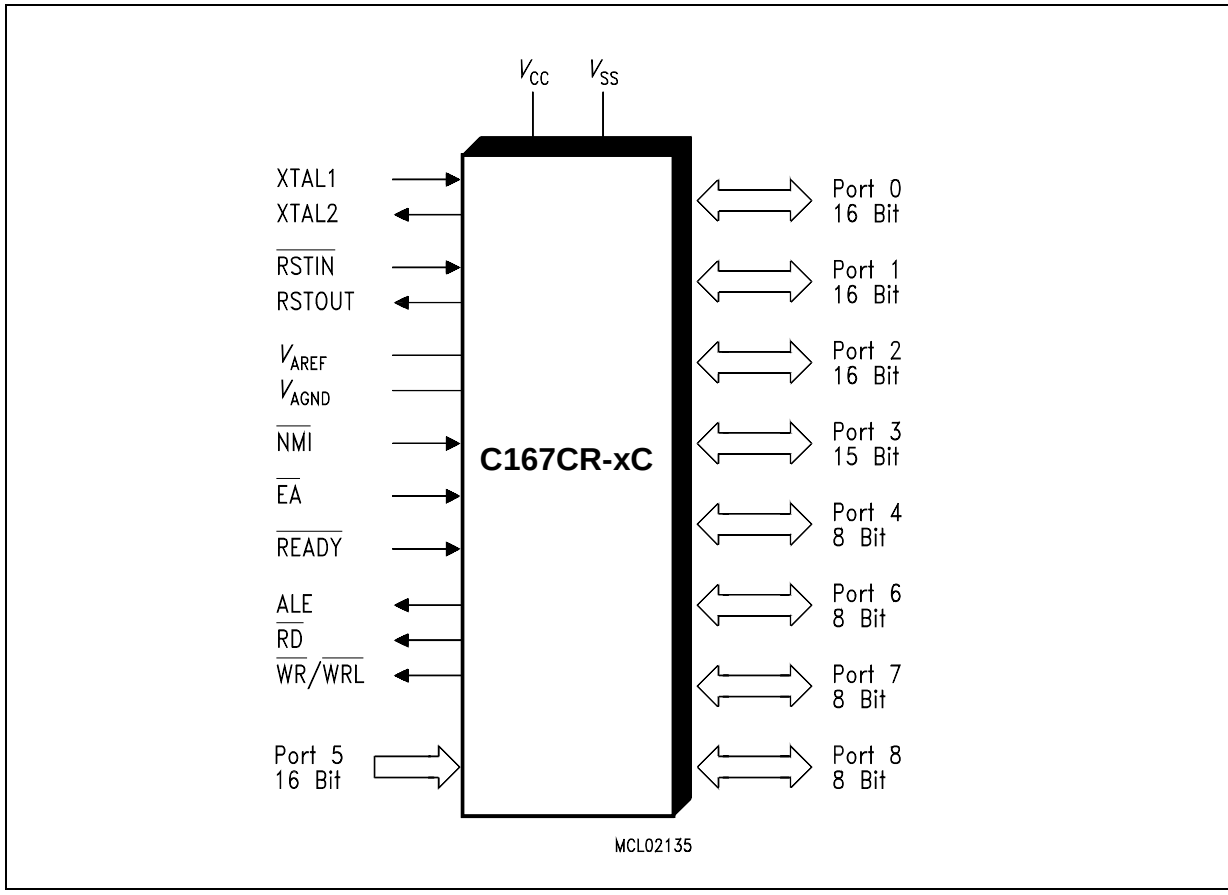

Figure 1 Logic Symbol

Pad Configuration

(top view)

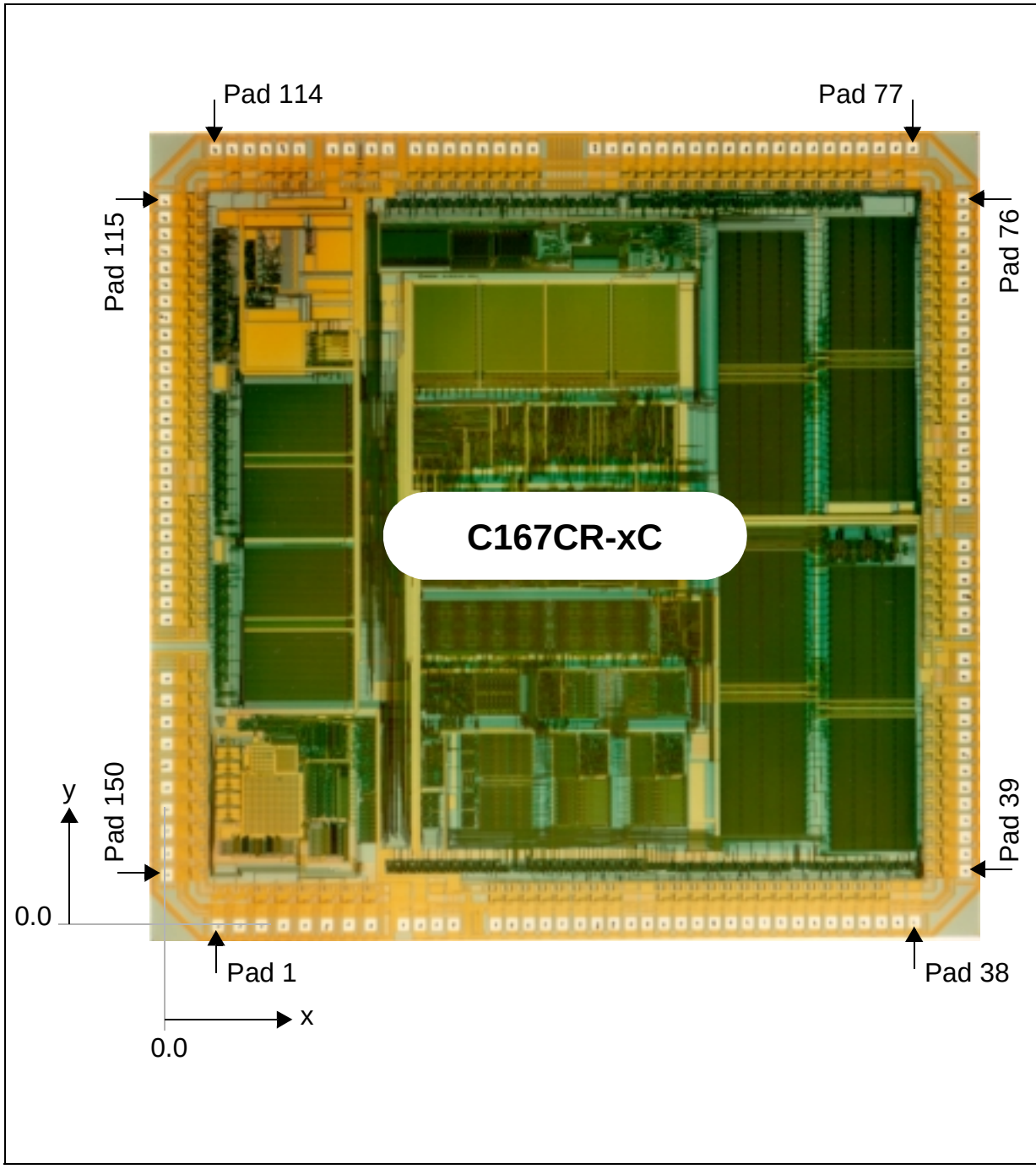

Figure 2

Table 2 Pad Definitions and Functions

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
V_{AREF}	1	-	380	0	Reference voltage for the A/D converter.
V_{AGND}	2	-	543	0	Reference ground for the A/D converter.
P5.10	3	I	705	0	Port 5 input, analog input AN10, external up/down T6EUD.
P5.11	4	I	868	0	Port 5 input, analog input AN11, external up/down T5EUD.
P5.12	5	I	1030	0	Port 5 input, analog input AN12, timer input T6IN.
P5.13	6	I	1193	0	Port 5 input, analog input AN13, timer input T5IN.
P5.14	7	I	1356	0	Port 5 input, analog input AN14, external up/down T4EUD.
P5.15	8	I	1518	0	Port 5 input, analog input AN15, external up/down T2EUD.
V_{SS}	9	-	1715	0	Digital Ground.
V_{SS}	10	-	1840	0	Digital Ground.
V_{DD}	11	-	1965	0	Digital Supply Voltage.
V_{DD}	12	-	2090	0	Digital Supply Voltage.
P2.0	13	I/O	2403	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC0IO.
P2.1	14	I/O	2528	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC1IO.
P2.2	15	I/O	2653	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC2IO.
P2.3	16	I/O	2779	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC3IO.
P2.4	17	I/O	2904	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC4IO.
P2.5	18	I/O	3038	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC5IO.
P2.6	19	I/O	3163	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC6IO.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P2.7	20	I/O	3289	0	Port 2 input/output (open drain, sp. threshold), Capture-Input/Compare-Output CC7IO.
V_{SS}	21	-	3414	0	Digital Ground.
V_{DD}	22	-	3539	0	Digital Supply Voltage.
P2.8	23	I/O	3664	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC8IO, Fast Interrupt EX0IN.
P2.9	24	I/O	3789	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC9IO, Fast Interrupt EX1IN.
P2.10	25	I/O	3914	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC10IO, Fast Interrupt EX2IN.
P2.11	26	I/O	4039	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC11IO, Fast Interrupt EX3IN.
P2.12	27	I/O	4164	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC12IO, Fast Interrupt EX4IN.
P2.13	28	I/O	4289	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC13IO, Fast Interrupt EX5IN.
P2.14	29	I/O	4414	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC14IO, Fast Interrupt EX6IN.
P2.15	30	I/O	4540	0	Port 2 input/output (open drain, sp. threshold), Capt. Input/Comp. Output CC15IO, Fast Interrupt EX7IN, Timer T7 input T7IN.
P3.0	31	I/O	4665	0	Port 3 input/output (open drain, sp. threshold), Timer T0 Input T0IN.
P3.1	32	I/O	4790	0	Port 3 input/output (open drain, sp. threshold), Timer T6 Toggle Latch Output T6OUT.
P3.2	33	I/O	4915	0	Port 3 input/output (open drain, sp. threshold), CAPREL Capture Input CAPIN.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P3.3	34	I/O	5045	0	Port 3 input/output (open drain, sp. threshold), Timer T3 Toggle Latch Output T3OUT.
P3.4	35	I/O	5179	0	Port 3 input/output (open drain, sp. threshold), Timer T3 ext.up/down T3EUD.
P3.5	36	I/O	5318	0	Port 3 input/output (open drain, sp. threshold), Timer T4 Input T4IN.
V_{SS}	37	-	5462	0	Digital Ground.
V_{DD}	38	-	5587	0	Digital Supply Voltage.
P3.6	39	I/O	5967	380	Port 3 input/output (open drain, sp. threshold), Timer T3 Input T3IN.
P3.7	40	I/O	5967	505	Port 3 input/output (open drain, sp. threshold), Timer T2 Input T2IN.
P3.8	41	I/O	5967	649	Port 3 input/output (open drain, sp. threshold), SSC Master-Rec./Slave-Transmit I/O MRST.
P3.9	42	I/O	5967	788	Port 3 input/output (open drain, sp. threshold), SSC Master-Transmit/Slave-Rec. O/I MTSR.
P3.10	43	I/O	5967	922	Port 3 input/output (open drain, sp. threshold), ASC0 Clock/Data Output (Asyn./Syn.) T×D0.
P3.11	44	I/O	5967	1052	Port 3 input/output (open drain, sp. threshold), ASC0 Data Input (Asyn.) or I/O (Syn.) R×D0.
P3.12	45	I/O	5967	1177	Port 3 input/output (open drain, sp. threshold).
	46	O	5967	1302	High Byte Enable $\overline{BHE}$, High Byte Write Strobe $\overline{WRH}$.
P3.13	47	I/O	5967	1427	Port 3 input/output (open drain, sp. threshold), SSC Master(Slave) Clock Output(Input) SCLK.
P3.15	48	I/O	5967	1552	Port 3 input/output (open drain, sp. threshold).
	49	O	5967	1678	System Clock Output (=CPU Clock) CLKOUT.
V_{DD}	50	-	5967	1897	Digital Supply Voltage.
V_{SS}	51	-	5967	2022	Digital Ground.
OWE	52	I	5967	2248	Osc. Watchdog Enable, disables OWD when low, should be high or NC during normal op.
P4.0	53	I/O	5967	2373	Port 4 input/output, Segment Address Line A16.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P4.1	54	I/O	5967	2498	Port 4 input/output, Segment Address Line A17.
P4.2	55	I/O	5967	2623	Port 4 input/output, Segment Address Line A18.
P4.3	56	I/O	5967	2748	Port 4 input/output, Segment Address Line A19.
P4.4	57	I/O	5967	2873	Port 4 input/output, Segment Address Line A20.
P4.5	58	I/O	5967	3113	Port 4 input/output, Segment Address Line A21, CAN Receive Data Input CAN_RxD.
P4.6	59	I/O	5967	3238	Port 4 input/output, Segment Address Line A22 CAN Transmit Data Output CAN_TxD.
P4.7	60	I/O	5967	3363	Port 4 input/output, Segment Address Line A23.
V_{DD}	61	-	5967	3488	Digital Supply Voltage.
V_{SS}	62	-	5967	3613	Digital Ground.
$\overline{RD}$	63	O	5967	3738	External Memory Read Strobe $\overline{RD}$.
$\overline{WR}(\overline{L})$	64	O	5967	3863	External Memory Write(Low) Strobe $\overline{WR}$ ($\overline{WRL}$).
$\overline{READY}$	65	I	5967	3988	Ready Input.
ALE	66	O	5967	4114	Address Latch Enable Output.
$\overline{EA}$	67	I	5967	4239	External Access Enable pin.
P0L.0	68	I/O	5967	4364	PORT0 input/output, Address/Data Line AD0.
P0L.1	69	I/O	5967	4489	PORT0 input/output, Address/Data Line AD1.
P0L.2	70	I/O	5967	4614	PORT0 input/output, Address/Data Line AD2.
P0L.3	71	I/O	5967	4739	PORT0 input/output, Address/Data Line AD3.
P0L.4	72	I/O	5967	4869	PORT0 input/output, Address/Data Line AD4.
P0L.5	73	I/O	5967	5003	PORT0 input/output, Address/Data Line AD5.
P0L.6	74	I/O	5967	5142	PORT0 input/output, Address/Data Line AD6.
P0L.7	75	I/O	5967	5286	PORT0 input/output, Address/Data Line AD7.
P0H.0	76	I/O	5967	5411	PORT0 input/output, Address/Data Line AD8.
V_{DD}	77	-	5587	5791	Digital Supply Voltage.
ROM 128K	78	I	5462	5791	ROM size-select input, must be connected to V_{SS}. (connected to V_{DD} in the C167CR-16RM)
V_{SS}	79	-	5318	5791	Digital Ground.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P0H.1	80	I/O	5179	5791	PORT0 input/output, Address/Data Line AD9.
P0H.2	81	I/O	5045	5791	PORT0 input/output, Address/Data Line AD10.
P0H.3	82	I/O	4915	5791	PORT0 input/output, Address/Data Line AD11.
P0H.4	83	I/O	4790	5791	PORT0 input/output, Address/Data Line AD12.
P0H.5	84	I/O	4665	5791	PORT0 input/output, Address/Data Line AD13.
P0H.6	85	I/O	4540	5791	PORT0 input/output, Address/Data Line AD14.
P0H.7	86	I/O	4414	5791	PORT0 input/output, Address/Data Line AD15.
P1L.0	87	I/O	4289	5791	PORT1 input/output, Address Line A0.
P1L.1	88	I/O	4164	5791	PORT1 input/output, Address Line A1.
P1L.2	89	I/O	4039	5791	PORT1 input/output, Address Line A2.
P1L.3	90	I/O	3914	5791	PORT1 input/output, Address Line A3.
P1L.4	91	I/O	3789	5791	PORT1 input/output, Address Line A4.
P1L.5	92	I/O	3664	5791	PORT1 input/output, Address Line A5.
P1L.6	93	I/O	3539	5791	PORT1 input/output, Address Line A6.
P1L.7	94	I/O	3414	5791	PORT1 input/output, Address Line A7.
V_{DD}	95	-	3289	5791	Digital Supply Voltage.
V_{SS}	96	-	3163	5791	Digital Ground.
P1H.0	97	I/O	2779	5791	PORT1 input/output, Address Line A8.
P1H.1	98	I/O	2654	5791	PORT1 input/output, Address Line A9.
P1H.2	99	I/O	2529	5791	PORT1 input/output, Address Line A10.
P1H.3	100	I/O	2404	5791	PORT1 input/output, Address Line A11.
P1H.4	101	I/O	2279	5791	PORT1 input/output, Addr. Line A12, Capt. Input CC24.
P1H.5	102	I/O	2154	5791	PORT1 input/output, Addr. Line A13, Capt. Input CC25.
P1H.6	103	I/O	2029	5791	PORT1 input/output, Addr. Line A14, Capt. Input CC26.
P1H.7	104	I/O	1904	5791	PORT1 input/output, Addr. Line A15, Capt. Input CC27.
V_{DD}	105	-	1685	5791	Digital Supply Voltage.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
XTAL2	106	O	1560	5791	Output of the oscillator amplifier circuit.
XTAL1	107	I	1396	5791	Input to oscillator amplifier and internal clock generator.
V_{SS}	108	-	1271	5791	Digital Ground.
$\overline{\text{RSTIN}}$	109	I/O	1052	5791	Reset Input with Schmitt-Trigger characteristics, output in bidirectional reset mode.
$\overline{\text{RST OUT}}$	110	O	922	5791	Internal Reset Indication Output.
$\overline{\text{NMI}}$	111	I	788	5791	Non-Maskable Interrupt Input.
V_{SS}	112	-	649	5791	Digital Ground.
$\overline{\text{XP1\_EN}}$	113	I	505	5791	CAN module enable input, must be connected to V_{SS}. (connected to V_{DD} in the C167SR-xy)
V_{DD}	114	-	380	5791	Digital Supply Voltage.
P6.0	115	I/O	0	5411	Port 6 input/output, Chip Select 0 Output $\overline{\text{CS0}}$.
P6.1	116	I/O	0	5286	Port 6 input/output, Chip Select 1 Output $\overline{\text{CS1}}$.
P6.2	117	I/O	0	5142	Port 6 input/output, Chip Select 2 Output $\overline{\text{CS2}}$.
P6.3	118	I/O	0	5003	Port 6 input/output, Chip Select 3 Output $\overline{\text{CS3}}$.
P6.4	119	I/O	0	4869	Port 6 input/output, Chip Select 4 Output $\overline{\text{CS4}}$.
P6.5	120	I/O	0	4739	Port 6 input/output, External Hold Request Input $\overline{\text{HOLD}}$.
P6.6	121	I/O	0	4614	Port 6 input/output, External Hold Acknowledge Output $\overline{\text{HLDA}}$.
P6.7	122	I/O	0	4489	Port 6 input/output, Bus Request Output $\overline{\text{BREQ}}$.
P8.0	123	I/O	0	4364	Port 8 input/output, Capt.-Input/Comp.-Output CC16IO.
P8.1	124	I/O	0	4239	Port 8 input/output, Capt.-Input/Comp.-Output CC17IO.
P8.2	125	I/O	0	4114	Port 8 input/output, Capt.-Input/Comp.-Output CC18IO.
P8.3	126	I/O	0	3988	Port 8 input/output, Capt.-Input/Comp.-Output CC19IO.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P8.4	127	I/O	0	3863	Port 8 input/output, Capt.-Input/Comp.-Output CC20IO.
P8.5	128	I/O	0	3738	Port 8 input/output, Capt.-Input/Comp.-Output CC21IO.
P8.6	129	I/O	0	3613	Port 8 input/output, Capt.-Input/Comp.-Output CC22IO.
P8.7	130	I/O	0	3488	Port 8 input/output, Capt.-Input/Comp.-Output CC23IO.
V_{DD}	131	-	0	3363	Digital Supply Voltage.
V_{SS}	132	-	0	3238	Digital Ground.
P7.0	133	I/O	0	3113	Port 7 input/output, (open drain, sp. threshold), PWM Channel Output POUT0.
P7.1	134	I/O	0	2988	Port 7 input/output, (open drain, sp. threshold), PWM Channel Output POUT1.
P7.2	135	I/O	0	2863	Port 7 input/output, (open drain, sp. threshold), PWM Channel Output POUT2.
P7.3	136	I/O	0	2737	Port 7 input/output, (open drain, sp. threshold), PWM Channel Output POUT3.
P7.4	137	I/O	0	2612	Port 7 input/output, (open drain, sp. threshold), Capt.-Input/Comp.-Output CC28IO.
P7.5	138	I/O	0	2487	Port 7 input/output, (open drain, sp. threshold), Capt.-Input/Comp.-Output CC29IO.
P7.6	139	I/O	0	2362	Port 7 input/output, (open drain, sp. threshold), Capt.-Input/Comp.-Output CC30IO.
P7.7	140	I/O	0	2237	Port 7 input/output, (open drain, sp. threshold), Capt.-Input/Comp.-Output CC31IO.
P5.0	141	I	0	1843	Port 5 input, analog input AN0.
P5.1	142	I	0	1681	Port 5 input, analog input AN1.
P5.2	143	I	0	1518	Port 5 input, analog input AN2.
P5.3	144	I	0	1356	Port 5 input, analog input AN3.
P5.4	145	I	0	1193	Port 5 input, analog input AN4.
P5.5	146	I	0	1030	Port 5 input, analog input AN5.

Table 2 Pad Definitions and Functions (continued)

Symbol	Pad Num	In / Out	Position [µm]		Function
			x	y	
P5.6	147	I	0	868	Port 5 input, analog input AN6.
P5.7	148	I	0	705	Port 5 input, analog input AN7.
P5.8	149	I	0	543	Port 5 input, analog input AN8.
P5.9	150	I	0	380	Port 5 input, analog input AN9.

Note: All V_{SS} pads and all V_{DD} pads must be connected to the system ground and the power supply, respectively.
The pad definitions and locations in this table are only valid for the indicated device and design step.

Handling Of Unconnected Pads

Signal input stages may generate undesired switching noise and cross-current when left open. Respect the following precautions for unconnected (not bonded) pads:

Table 3 Precautions for Unconnected Pads

Pad Type	Recommended Action	Related Pads
Power Supply	*Always connect!*	V_{DD}, V_{SS}, V_{AREF}, V_{AGND}
Standard IO pads	Switch to output	PORT0, PORT1, P2, P3, P4, P6, P7, P8
Input port pads	Disable input stages via P5DIDIS	P5
Double-bond ports	Connect port pad (45, 48), if the alternate output (46, 49) is used. [1)]	P3.12 (45/46), P3.15 (48/49)
Configuration lines	*Always connect!*	$\overline{\text{EA}}$, ROM128K, $\overline{\text{XP1\_EN}}$
Required control lines	*Always connect!*	XTAL1, $\overline{\text{RSTIN}}$, $\overline{\text{NMI}}$
Optional control lines	Can be left open	OWE, $\overline{\text{RD}}$, $\overline{\text{WR}}$($\overline{\text{L}}$), $\overline{\text{READY}}$, ALE, $\overline{\text{RSTOUT}}$

[1)] Port pad is input in this case! If the port pad is used, the corresponding alternate output pad may be left open.

Functional Description

As the standard packaged devices are made from this silicon the C167CR-xC dies provide exactly the same functionality and behaviour. Also the DC characteristics and AC characteristics are compatible with those of the packaged devices.

For a description of the functionality and the DC and AC parameters please refer to the following documents (or later versions thereof):

- C167CR Data Sheet 1999-10
- C167 Derivatives User's Manual Version 2.1

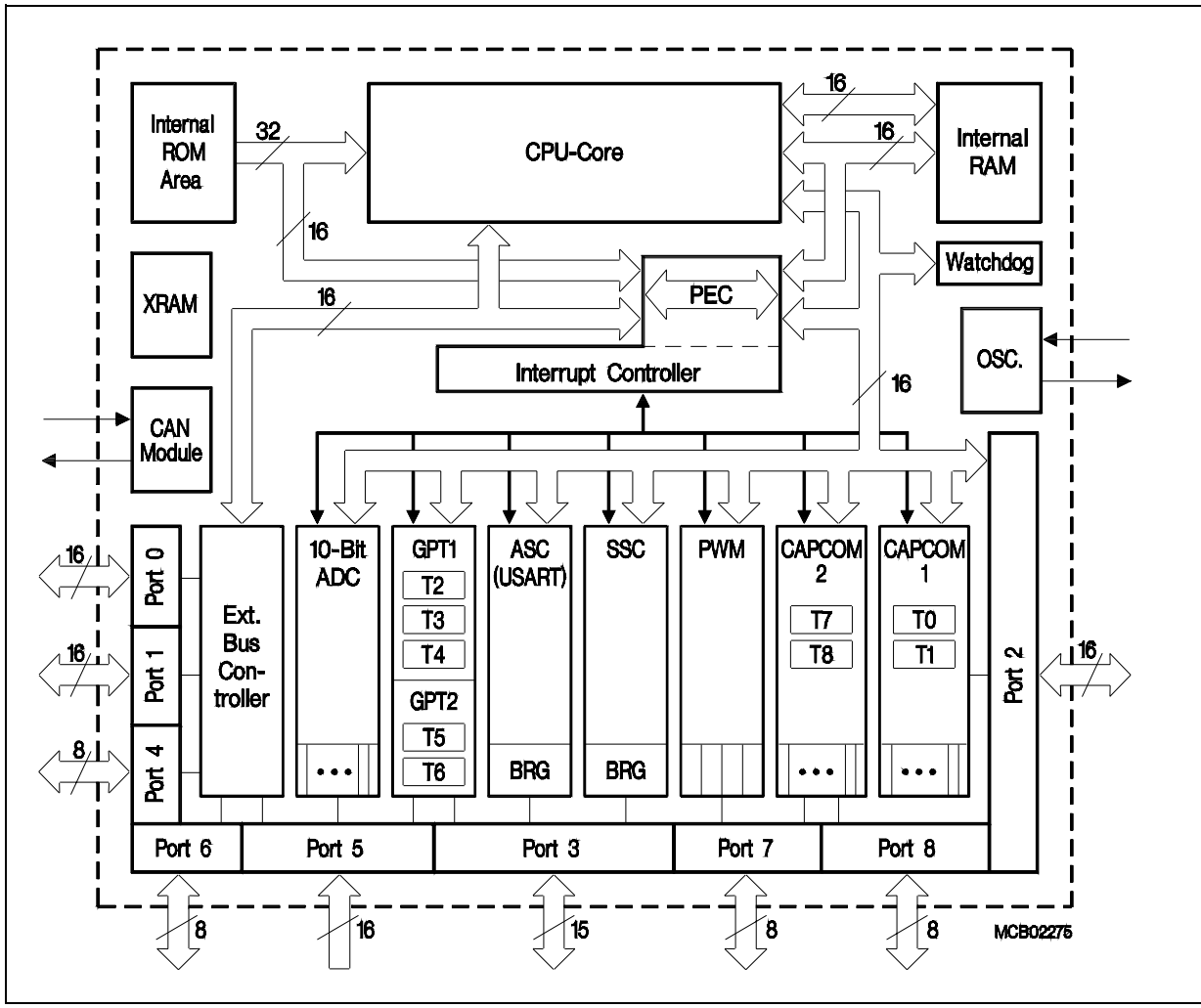

Figure 3 Block Diagram

Absolute Maximum Ratings

Table 4 Absolute Maximum Rating Parameters

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Storage temperature	T_{ST}	-65	150	°C	
Junction temperature	T_J	-40	150	°C	under bias
Voltage on V_{DD} pins with respect to ground (V_{SS})	V_{DD}	-0.5	6.5	V	
Voltage on any pin with respect to ground (V_{SS})	V_{IN}	-0.5	V_{DD}+0.5	V	
Input current on any pin during overload condition		-10	10	mA	
Absolute sum of all input currents during overload condition		-	|100|	mA	

Note: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
During absolute maximum rating overload conditions (V_{IN}>V_{DD} or V_{IN}<V_{SS}) the voltage on V_{DD} pins with respect to ground (V_{SS}) must not exceed the values defined by the absolute maximum ratings.

Operating Conditions

The following operating conditions must not be exceeded in order to ensure correct operation of the C167CR-xC.

The operating conditions for the C167CR-xC are identical with the conditions for the packaged parts. Please refer to the mentioned data sheets.

Note: Temperature specifications refer to the carrier side of the die (T_D).

Storage Conditions

The C167CR-xC dies may be stored for a certain time under the conditions described below.

Table 5 Bare Die Storage Conditions and Duration

Packing	Environment	Temperature	Rel. Humidity	Storage Time
Vacuum pack	Air	15...30 °C	< 60 %	< 4 Months

Chip Outline

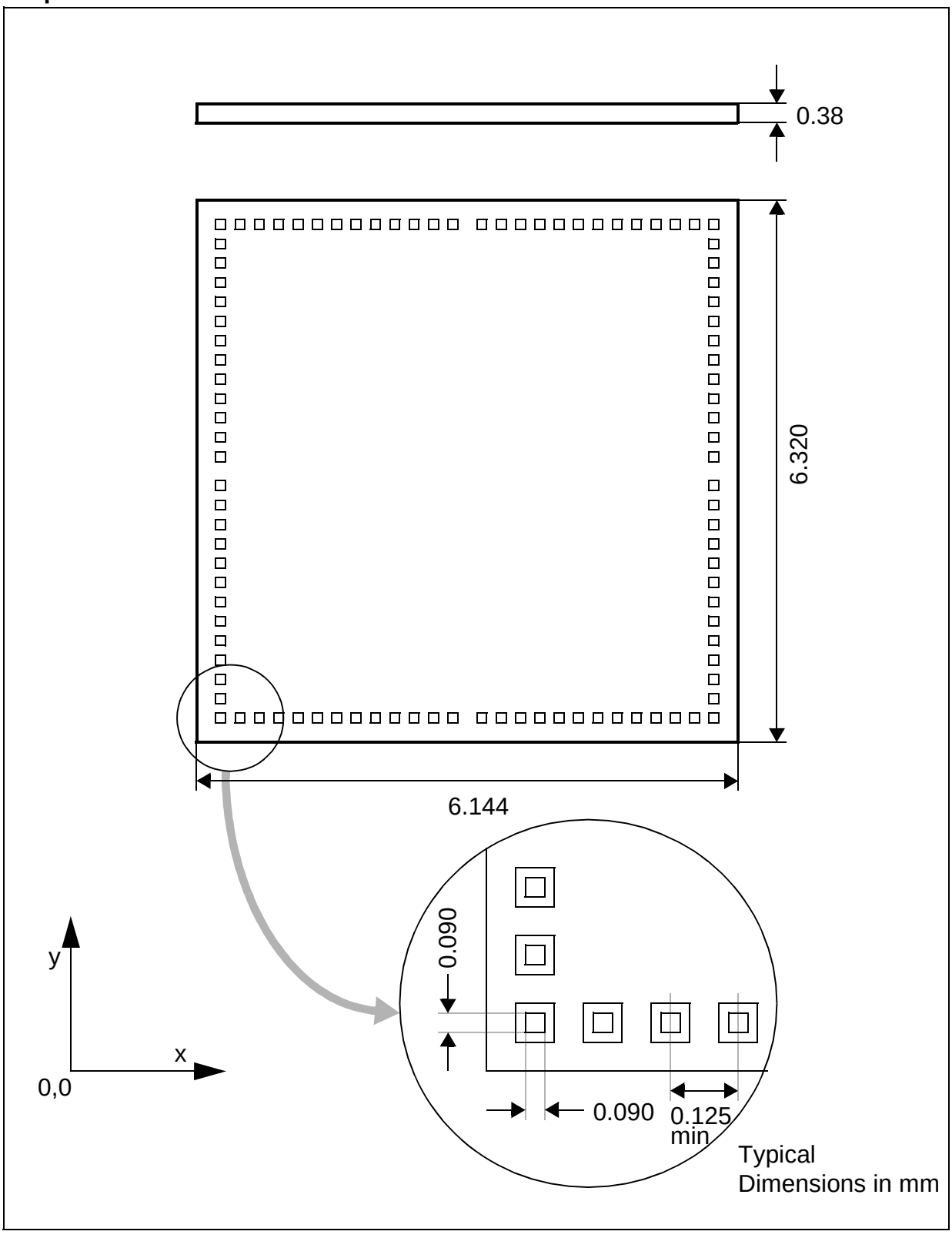

Figure 4

Table 6 Wafer Characteristics

Item	Characteristic
Chips per wafer	373 (geometrically)
Metallization layers	2
Metallization material	AlCu
Metallization thickness	Met1: 400 nm, Met2: 800 nm
Metallization barrier material	Ti
Metallization isolation	SOG-CMP
Metallization material on pads	AlSiCu (Al 98.5% - SI 1% - Cu 0.5%)
Passivation	Oxide (310 nm) + nitride (510 nm), polyimid
Backside metallization	None (silicon)
Inkdot diameter	1.0-1.3 typical

The wafers are glued to a plastic tape which is fixed within a plastic ring (see figure below).
Wafers can be shipped in one piece or sawn into individual dies.

*Note: Please refer also to the document "**Bare Die Packing Information**".*

Wafer Outline

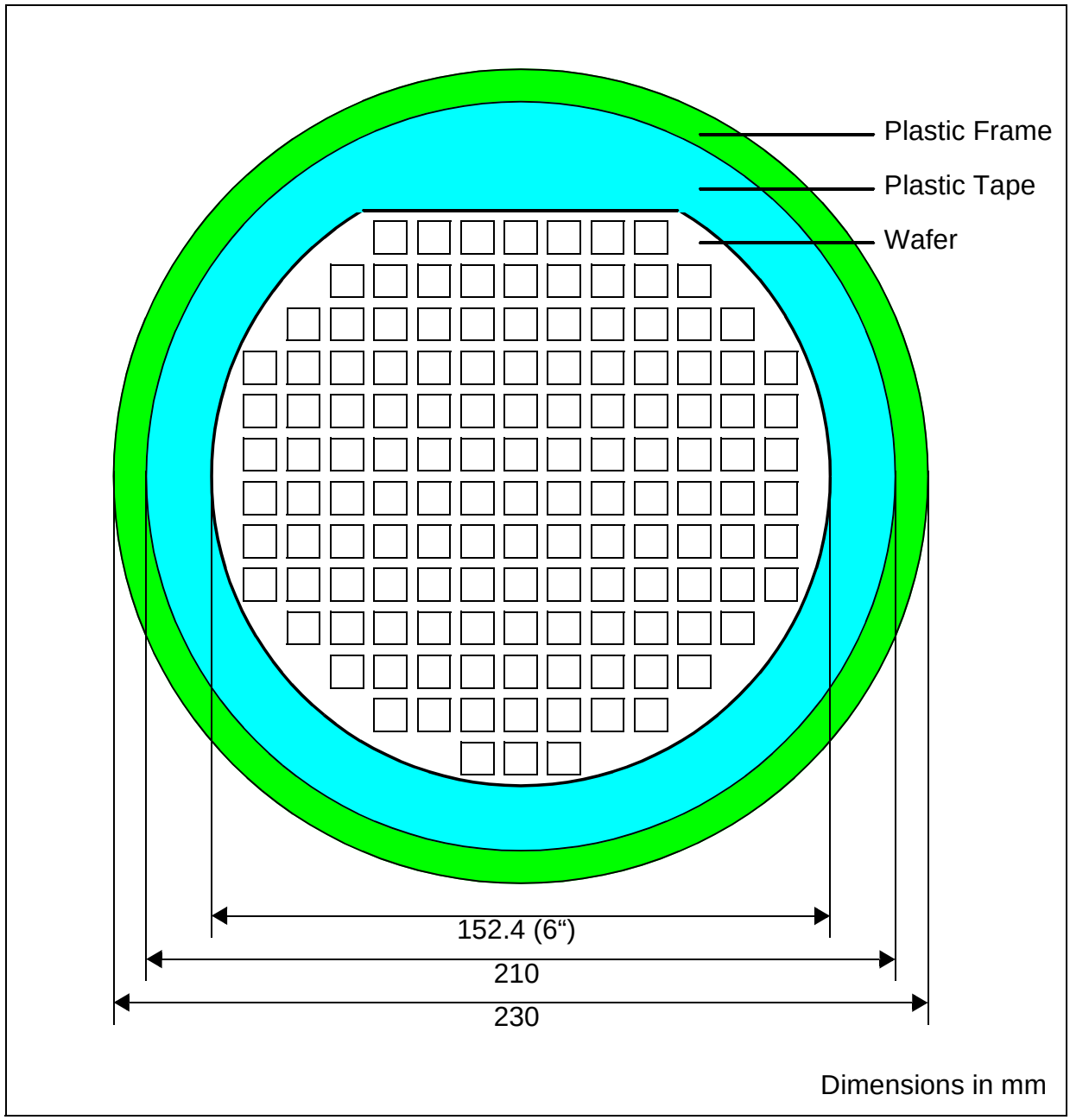

Figure 5

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