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L64715
Two-Error Correcting
BCH Encoder-Decoder

Description

The L64715 implements the forward error correction, bit filling and synchronization scheme specified in ITU-TSS (formerly CCITT) recommendation H.261. The forward error correcting code is a 2-error correcting BCH code. The device contains both an encoder and a decoder for full duplex operation.

The device processes blocks of 512 bits. Each block consists of a 511-bit BCH codeword and a single internally generated or user supplied frame bit. The encoder appends 18 bits of redundant check bits to every 493 bits of message to form the BCH codeword. The message consists of either 493 bits of data or a fill indicator bit and 492 bits of data or a fill indicator and 492 fill bits.

The BCH decoder can correct up to two errors per codeword. The number of errors that have been corrected is reported for channel characterization.

When internal framing and synchronization is selected, the encoder appends a single framing bit, as specified in ITU-TSS recommendation H.261, to each BCH codeword. The decoder will automatically detect the synchronization pattern to determine the codeword boundary. External synchronization can also be provided, in which the codeword boundary for the decoder is provided externally.

The device can be programmed to operate with or without bit filling. When the fill mode is selected, the first message bit is used to indicate if the rest of the message has been filled or contains data.

Sustained encoded bit rates of up to 30 Mbits per second are supported for both the encoder and decoder in full duplex mode.
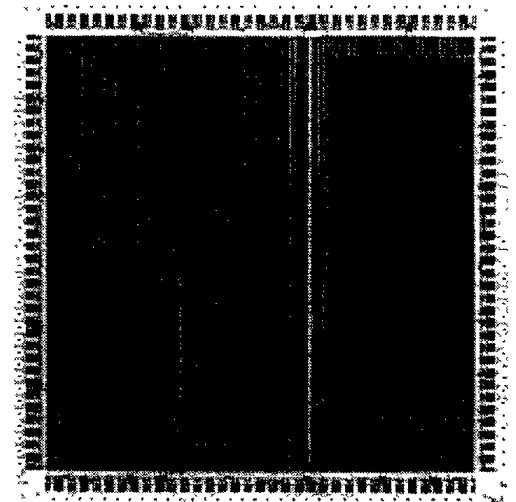
L64715 Chip

Features

- Codeword size of 511 bits
- Corrects up to two bits of errors per codeword
- Separate encoder and decoder for full duplex operation
- Optional synchronization and bit filling
- Compatible with ITU-TSS H.261 requirements
- 30 MHz data rate for decoder and encoder
- Internal BCH decoding buffers
- 44-pin PLCC (Plastic Leaded Chip Carrier) package

May 1994

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Pin Listing and Description

ECLK
Encoder system clock. Controls all encoder system functions at LOW to HIGH transitions.

EDI
Encoder data input. The data bits of the message to be encoded are input on this pin. Depending on the state of FMODE and FILL, up to 493 data bits per block will be latched on EDI and encoded.

EIMS
Input which indicates the start of encoder input message. A HIGH on EIMS indicates that the first of the 493 message bits is currently on the EDI pin.

EDO
Encoder data output. The output block consisting of the codeword and frame bits is output on the EDO pin. The data and external framing bits are passed from the EDI pin with a delay of four cycles. The encoder inserts the 18 check bits. In addition, a frame bit and/or fill bits are inserted when the appropriate modes are selected.

EOMS
Output which indicates the start of encoder output message. A HIGH on EOMS indicates that the first of the 493 bits of messages in a codeword is on the EDO signal. EOMS is delayed from EIMS by four clock cycles.

DCLK
Decoder system clock. Controls all decoder system functions at LOW to HIGH transitions.

DDI
Decoder data input. Each codeword of 511 contiguous bits is followed by a frame bit.

DIMS
This input signal is used to reset the internal synchronizer by going HIGH for at least two DCLK cycles. In the external synchronization mode, it indicates the start of decoder input message. A HIGH on DIMS indicates that the first of the 493 bits of message in a codeword is on the DDI pin.

DDO
Decoder data output. The block input on the DDI pin is processed and output on the DDO pin 534 cycles later. Up to two errors within the codeword will be corrected in the output, while all other bits in the block will be passed directly to DDO without change.

DOMS
Output which indicates the start of decoder output message. A HIGH on DOMS indicates that the first of the 493 bits of messages in a codeword will appear on the DDO signal in the following clock cycle. DOMS is delayed from DIMS (in external synchronization mode) by 534 clock cycles.

DDV
Decoder data valid output signal. A HIGH on DDV indicates that the data on DDO is a useful data bit. DDV is HIGH during the message portion of the block except that it will go LOW when the output bit corresponds to either a fill indicator bit or a fill bit (FMODE HIGH).

SMODE
Synchronization mode select input. When HIGH, indicates that the device operates in the internal synchronization mode. In this case, an ITU-TSS framing bit is automatically appended after the last redundant check bit. When LOW, it indicates that the device operates in the external synchronization mode. In this case, only the redundant check bits are generated internally by the encoder. When SMODE is HIGH, the decoder will automatically detect the framing sequence to determine the BCH code boundary.

FMODE
Fill mode select input. When HIGH, it indicates that the device operates in the internal bit filling mode. In this case, the first message bit of the block is used to indicate if the remaining data bits are valid or fill bits. When LOW, FMODE indicates that all of the 493 message bits can be used for data. SMODE must be HIGH when FMODE is HIGH.

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Pin Listing and Description
(Continued)

FILL
Fill indicator input. Used by the encoder when FMODE is HIGH and latched when EIMS is HIGH. If FMODE and FILL are HIGH, the first message bit is set to ZERO and all remaining message bits are filled with ONEs. If FMODE is HIGH and FILL is LOW, the first message bit is set to ONE and all remaining message bits are set from the EDI pin. This pin is ignored when FMODE is LOW.

NERR.0, NERR.1
NERR is a 2-bit output flag which indicates the number of errors being corrected or detected in the corresponding output codeword. When there are more than two errors within a codeword, these bits may not reflect the true number of errors.

SYNFD
In the internal synchronization mode, a HIGH on SYNFD indicates the successful detection of three consecutive periods of the synchronization sequence (00011011). SYNFD can be ignored in the external synchronization mode.

RESET, TEST
LSI Logic internal input test pins. Should be left unconnected or set LOW by the user.

RTEST, STEST, TESTO
LSI Logic internal output test pins. Should be left unconnected by the user.

Pin Description Summary

Pin	No. of Pins	I/O	Description
ECLK	1	I	Encoder clock
EDI	1	I	Encoder data input
EIMS	1	I	Encoder input message start
EDO	1	O	Encoder data output
EOMS	1	O	Encoder output message start
DCLK	1	I	Decoder clock
DDI	1	I	Decoder data input
DIMS	1	I	Decoder input message start
DDO	1	O	Decoder data output
DOMS	1	O	Decoder output message start
DDV	1	O	Decoder data valid
SMODE	1	I	Sync mode select pin
FMODE	1	I	Fill mode select pin
FILL	1	I	Fill indicator input
NERR.0-NERR.1	2	O	Number of errors corrected
SYNFD	1	O	Sync detected
RESET, TEST	2	I	LSI test inputs
RTEST, STEST, TESTO	3	O	LSI test outputs

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Block Diagram　　　　**BCH Encoder-Decoder**
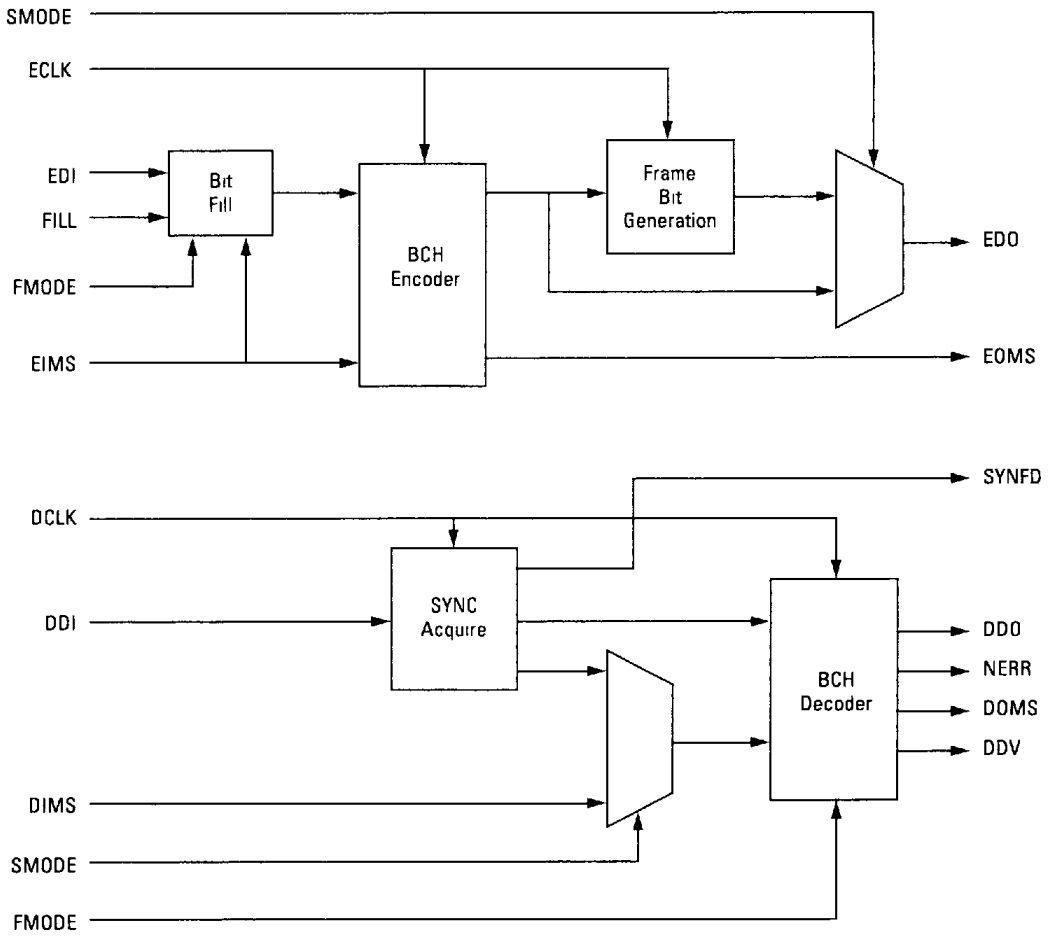
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BCH Encoder-Decoder

Architecture

The L64715 has two main sections, the encoder side and the decoder side, running on two separate clocks for independent full duplex operation.

The encoder section consists of the bit filling logic, the BCH encoder and the frame bit generation circuitry. The bit filling logic will automatically insert the fill indicator and fill bits into the message as specified by the FMODE and FILL pins. The BCH encoder accepts a single-bit stream of data and encodes it using the generator polynomial $g(x) = (x^9 + x^4 + 1)(x^9 + x^6 + x^4 + x^3 + 1)$. It appends 18 redundant check bits to 493 message bits to form a codeword of 511 bits. The codeword boundary is provided by the EIMS signal. In the internal synchronization mode, the frame bit generation circuitry appends a framing bit to the end of each codeword to form a synchronization frame of 512 bits as shown in Figure 1.
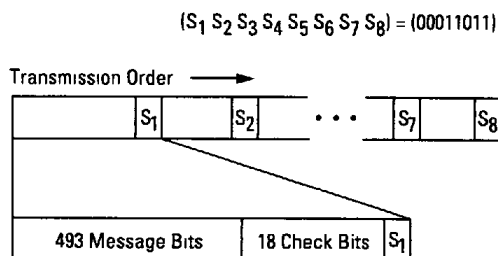
$$(S_1\ S_2\ S_3\ S_4\ S_5\ S_6\ S_7\ S_8) = (00011011)$$

Figure 1. Message Frame

The decoder section consists of the synchronization acquisition circuitry and the BCH decoder.

In the internal synchronization mode, the frame boundary is established by the synchronization acquisition circuitry. It looks for three consecutive periods of the synchronization sequence (00011011) formed by the framing bits. Once it detects the occurrence of this 24-bit pattern, the SYNFD signal goes HIGH, and the decoder acquires synchronization. Based on its acquired notion of the codeword boundary, the decoder can predict the value of the next upcoming framing bit. The SYNFD signal remains HIGH so long as the upcoming framing bit matches its expected value. When the matching is unsuccessful, the SYNFD signal goes LOW and the synchronization process starts to look for the 24-bit pattern again. Between the time the SYNFD signal goes LOW, and the next successful detection of the 24-bit pattern, the decoder will continue to use its old notion of the codeword boundary. The synchronization acquisition time is less than the ITU-TSS requirement of 34,000 bits. In the external synchronization mode, the frame boundary is provided by the DIMS signal.

The BCH decoder corrects up to two bits of error in a codeword of 511 bits and outputs the result on the DDO signal. The number of errors corrected or detected in the output codeword is indicated by the 2-bit output flag NERR. When NERR is equal to three (NERR.0 = NERR.1 = 1), it indicates that the decoder detects the occurrence of at least three errors in the codeword. In this case, the input codeword data are left unchanged. When NERR is less than three, it represents the number of errors being corrected in the output codeword.
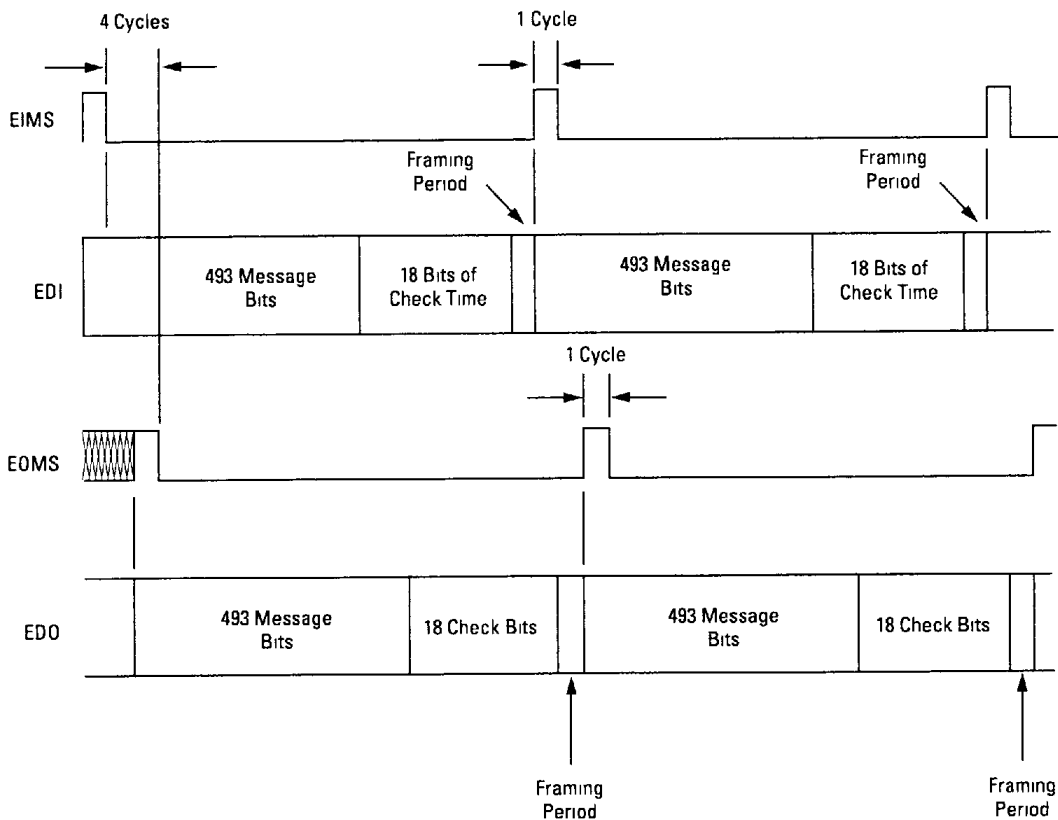
The NERR signal may be used for gathering error statistics on the channel. It should be noted, however, that with greater than two errors in the codeword, NERR will not always indicate three or more errors.

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Functional Timing Diagrams

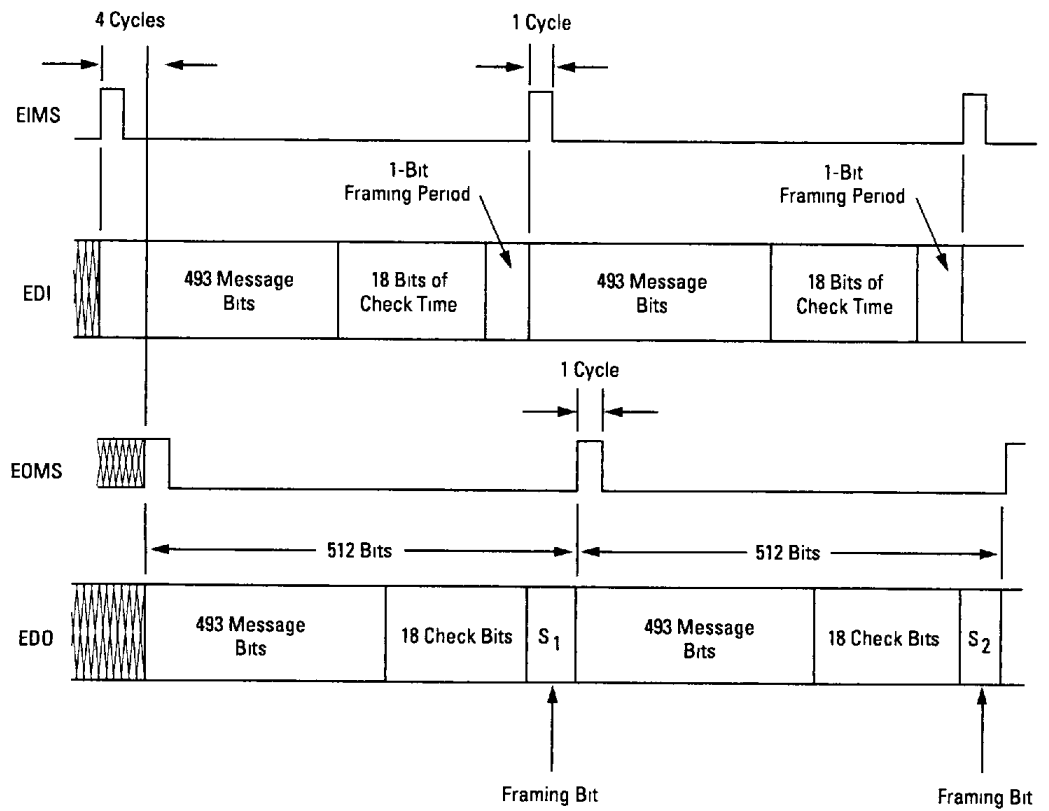**Encoder Functional Timing External Synchronization (SMODE LOW)**

FMODE must be LOW. For this case, all 493 message bits are set by the user via the EDI pin.

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Functional Timing Diagrams (Continued)

Encoder Functional Timing Internal Synchronization (SMODE HIGH)

When FMODE is LOW, all 493 message bits are set by the user via the EDI pin. If the internal fill mode is selected (FMODE HIGH), then the first bit of the 493 output message bits will be set to zero if FILL is HIGH (when EIMS is HIGH) and the remaining 492 output message bits will be set to one. If FILL is LOW during EIMS HIGH and FMODE is HIGH, the first message bit is set HIGH and the remaining message bits are set according to the data on the EDI pin.

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**Functional Timing
Diagrams
(Continued)**

Decoder Functional Timing External Synchronization (SMODE LOW)

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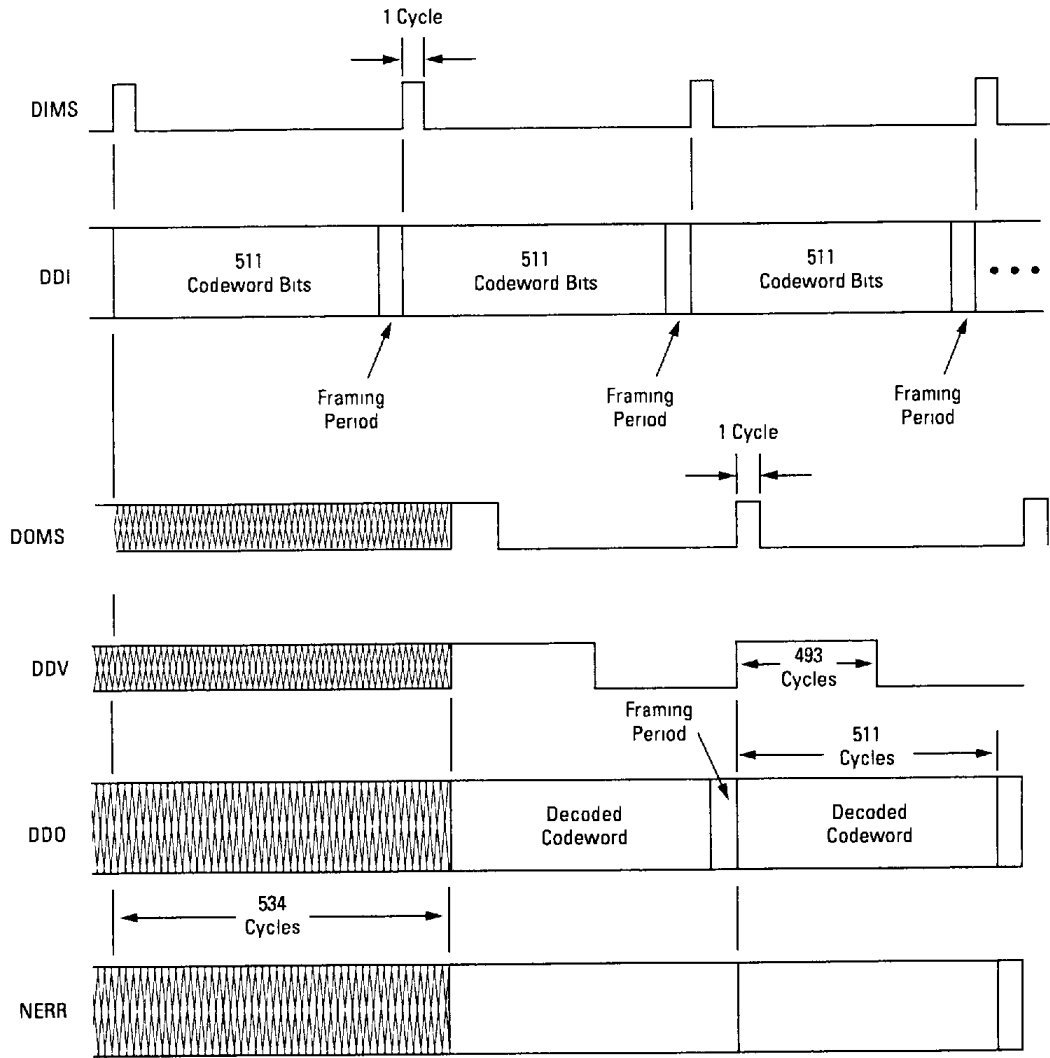
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Functional Timing Diagrams (Continued)

Decoder Functional Timing Internal Synchronization (SMODE HIGH)
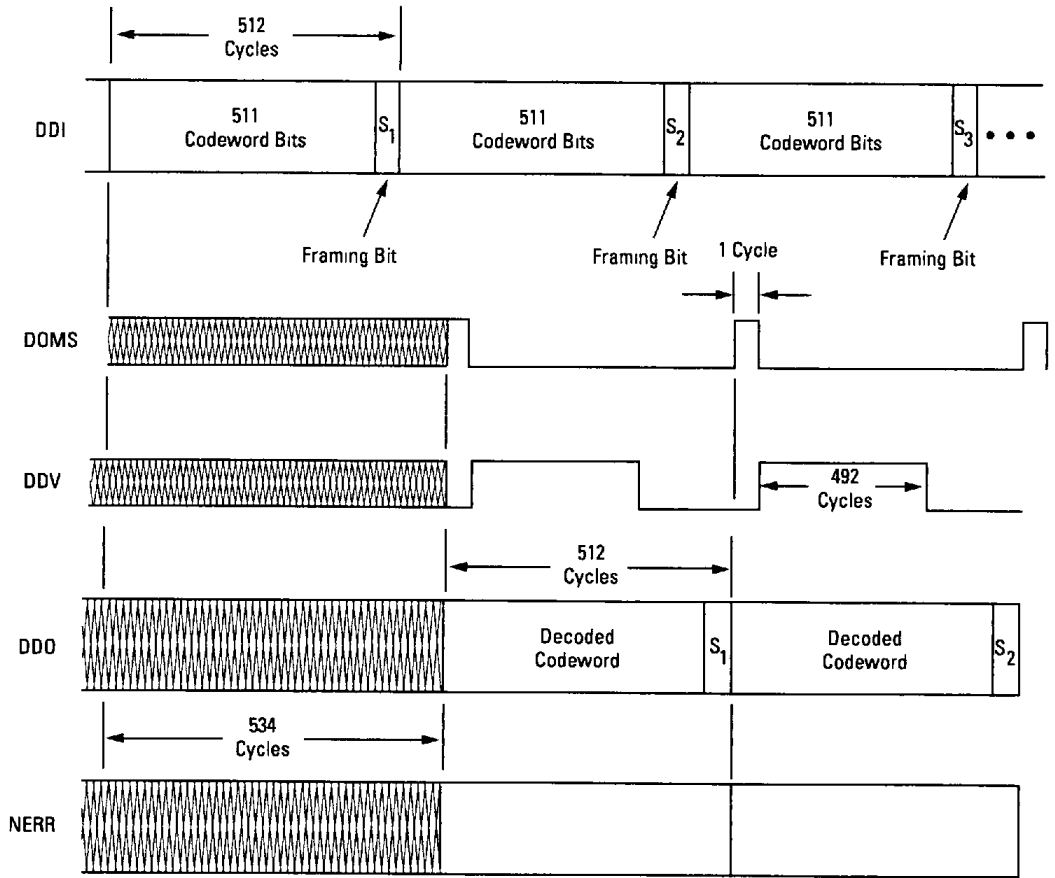
DDV is shown for the case in which FMODE is HIGH. IF FMODE is HIGH, DDV will go HIGH for 492 cycles only when the first message bit is ONE. Otherwise, DDV will be LOW for the entire block. If FMODE is LOW, DDV will always go HIGH for 493 cycles when the decoded message bits are output.

To initialize the synchronizer, DIMS should be HIGH for at least two DCLK cycles and then remain LOW. This will force the device to begin searching for the framing pattern and to indicate that synchronization has not been achieved.

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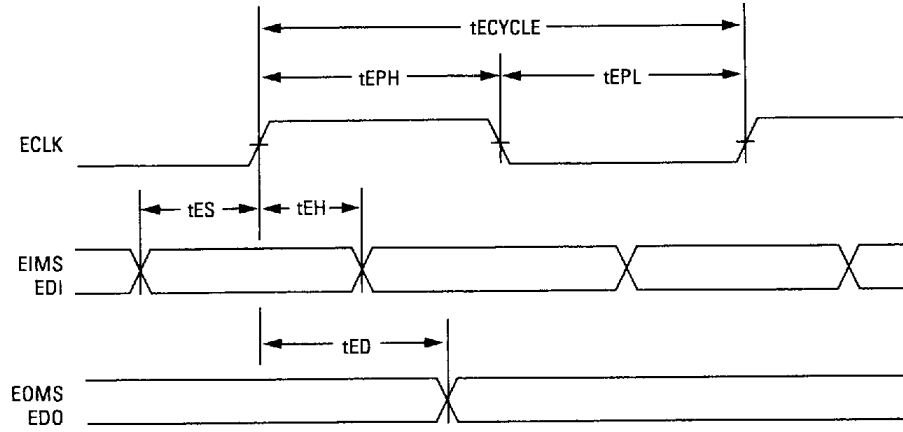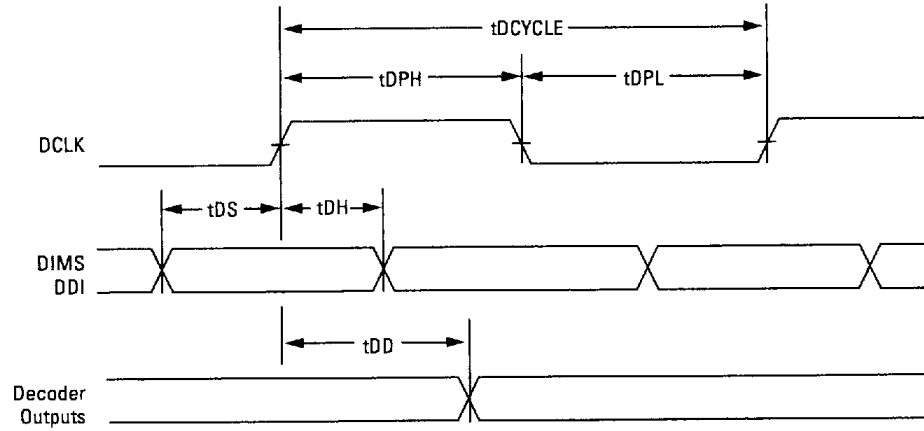**BCH Encoder-Decoder**

AC Timing
Waveforms

Encoder Section

Decoder Section

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AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64715-30 Min	L64715-30 Max
tECYCLE	ECLK cycle time	33	
tEPH	ECLK pulse width, HIGH	15	
tEPL	ECLK pulse width, LOW	15	
tES	EIMS, EDI, FILL input setup time	10	
tEH	EIMS, EDI, FILL input hold time	0	
tED	EOMS, EDO output delay*		22
tDCYCLE	DCLK cycle time	33	
tDPH	DCLK pulse width, HIGH	15	
tDPL	DCLK pulse width, LOW	15	
tDS	DIMS, DDI input setup time	10	
tDH	DIMS, DDI input hold time	0	
tDD	Decoder output delay*		22

Notes:
1. All times are in ns.
2. * – Output loading = 50 pF.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-40 to +125	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Commercial range	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition	Min	Typ	Max	Units
VIL	Low level input voltage				0.8	V
VIH	High level input voltage	0°C ≤ TA ≤ 70°C	2.0			V
IIN	Input current	VIN = VDD	10		120	μA
VOH	High level output voltage	IOH = -4 mA	2.4	4.5		V
VOL	Low level output voltage	IOL = 4 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD	15		130	mA
		VDD = Max, VO = 0V	-5		-100	mA
IDDQ	Quiescent supply current	VIN = VDD or VSS			10	mA
IDD	Operating supply current[3]	tCYCLE = 25 ns		100		mA
CIN	Input capacitance	Any input		5		pF
COUT	Output capacitance	Any input		10		pF

Notes:
1. Commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. For 40 MHz device.

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L64715 Package Pin Information (44-Pin PLCC, by Pin Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
1	VDD	12	VSS	24	VDD	35	VDD
2	VSS	14	EDI	25	ECLK	36	STEST
3	DDI	15	EIMS	26	SMODE	37	NERR.1
4	DIMS	16	EDO	27	FMODE	38	NERR.0
6	VDD	17	EOMS	28	VSS	39	VSS
7	VSS	18	VSS	29	VDD	40	VDD
8	DDO	19	VDD	30	SYNFD	42	RESET
9	DOMS	20	TEST	31	TESTO	44	DCLK
10	DDV	21	FILL	32	RTEST		
11	VDD	23	VSS	34	VSS		

L64715 Package Pin Information (44-Pin PLCC, by Signal Name)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
44	DCLK	17	EOMS	20	TEST	12	VSS
3	DDI	21	FILL	31	TESTO	18	VSS
8	DDO	27	FMODE	1	VDD	2	VSS
10	DDV	38	NERR 0	11	VDD	23	VSS
4	DIMS	37	NERR 1	19	VDD	28	VSS
9	DOMS	42	RESET	24	VDD	34	VSS
25	ECLK	32	RTEST	29	VDD	39	VSS
14	EDI	26	SMODE	35	VDD	7	VSS
16	EDO	36	STEST	40	VDD		
15	EIMS	30	SYNFD	6	VDD		

Note Pins 5, 13, 22, 33, 41, 43, are not used

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Pinout Diagram

```
        6  5  4  3  2 │1│44 43 42 41 40
     7                              39
     8                              38
     9                              37
    10                              36
    11                              35
    12         Top View             34
    13                              33
    14                              32
    15                              31
    16                              30
    17                              29
       18 19 20 21 22 23 24 25 26 27 28
```
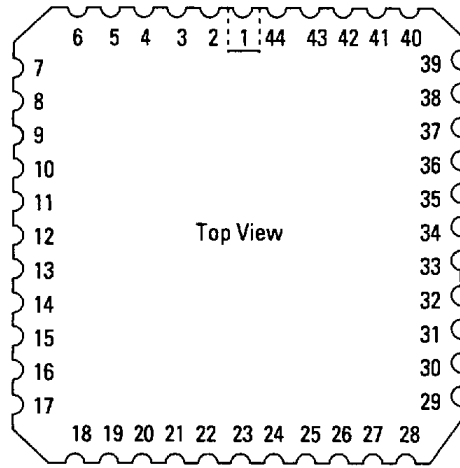
Packaging

44-Pin Plastic Leaded Chip Carrier: See MF Package in Package Selector Guide

Ordering Information

L64715　　J　　C　　-XX

- Speed MHz

- Temperature Range/Flow Option
  C = Commercial (0°C to 70°C)

- Package Code
  J = 44-Pin Plastic Leaded Chip Carrier

- Device Type
  Two-Error Correcting BCH Encoder-Decoder

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