ADE-203-373 (Z)

HM5118165A/AL Series

1,048,576-word × 16-bit Dynamic Random Access Memory

HITACHI

Preliminary
Rev. 0.0
Mar. 20, 1995

The Hitachi HM5118165A/AL is a CMOS dynamic RAM organized 1,048,576-word × 16-bit. It employs the most advanced CMOS technology for high performance and low power. The HM5118165A/AL offers Extended Data Out (EDO) Page Mode as a high speed access mode.

Feature

- Single 5.0 V (± 10%)
- High speed
  - Access time
    70 ns/ 80 ns (max)
- Low power dissipation
  - Active mode
    825 mW/715 mW (max)
  - Standby mode 11 mW (max)
    0.83 mW (max) (L-version)
- EDO page mode capability
- Long refresh period
  - 1024 refresh cycles : 16 ms
    :128 ms (L-version)
- 4 variations of refresh
  - $\overline{\text{RAS}}$-only refresh
  - $\overline{\text{CAS}}$-before-$\overline{\text{RAS}}$ refresh
  - Hidden refresh
  - Self refresh (L-version)
- 2$\overline{\text{CAS}}$-byte control
- Battery backup operation (L-version)

Ordering Information

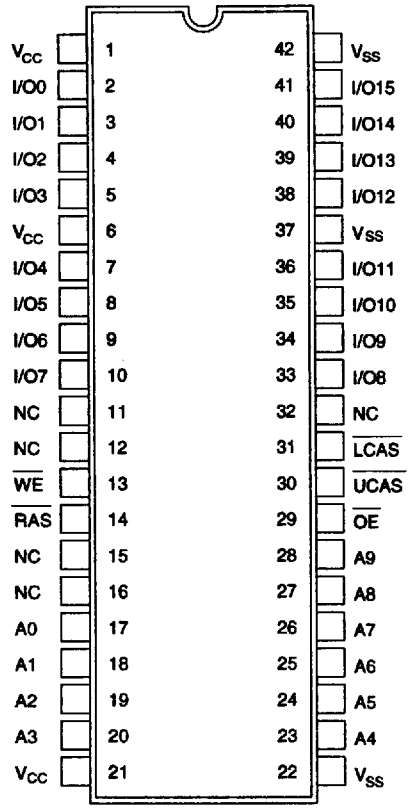
Type No.	Access time	Package
HM5118165AJ-7	70 ns	400-mil, 42-pin plastic SOJ (CP-42D)
HM5118165AJ-8	80 ns	
HM5118165ALJ-7	70 ns	
HM5118165ALJ-8	80 ns	
HM5118165ATT-7	70 ns	400-mil, 50-pin plastic TSOP II (TTP-50/44DC)
HM5118165ATT-8	80 ns	
HM5118165ALTT-7	70 ns	
HM5118165ALTT-8	80 ns	

Preliminary: This document contains information on a new product. Specifications and information contained herein are subject to change without notice.

This specification is fully compatible with the 16-Mbit DRAM specifications from TEXAS INSTRUMENTS.

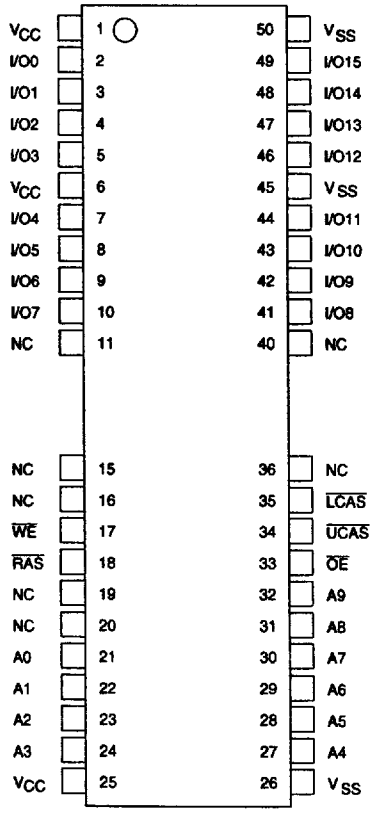
$\overline{RAS}$	Row address strobe

HM5118165AJ/ALJ Series



(Top view)

HM5118165ATT/ALTT Series



(Top view)

$\overline{UCAS}$, $\overline{LCAS}$	Column address strobe
$\overline{WE}$	Read/Write enable
$\overline{OE}$	Output enable

Pin Arrangement

Pin Description

Pin name	Function
A0 to A9	Address input
A0 to A9	Refresh address input
I/O0 to I/O15	Data input/data output

Pin name	Function
V_{CC}	Power supply (+ 5.0 V)
V_{SS}	Ground
NC	No connection

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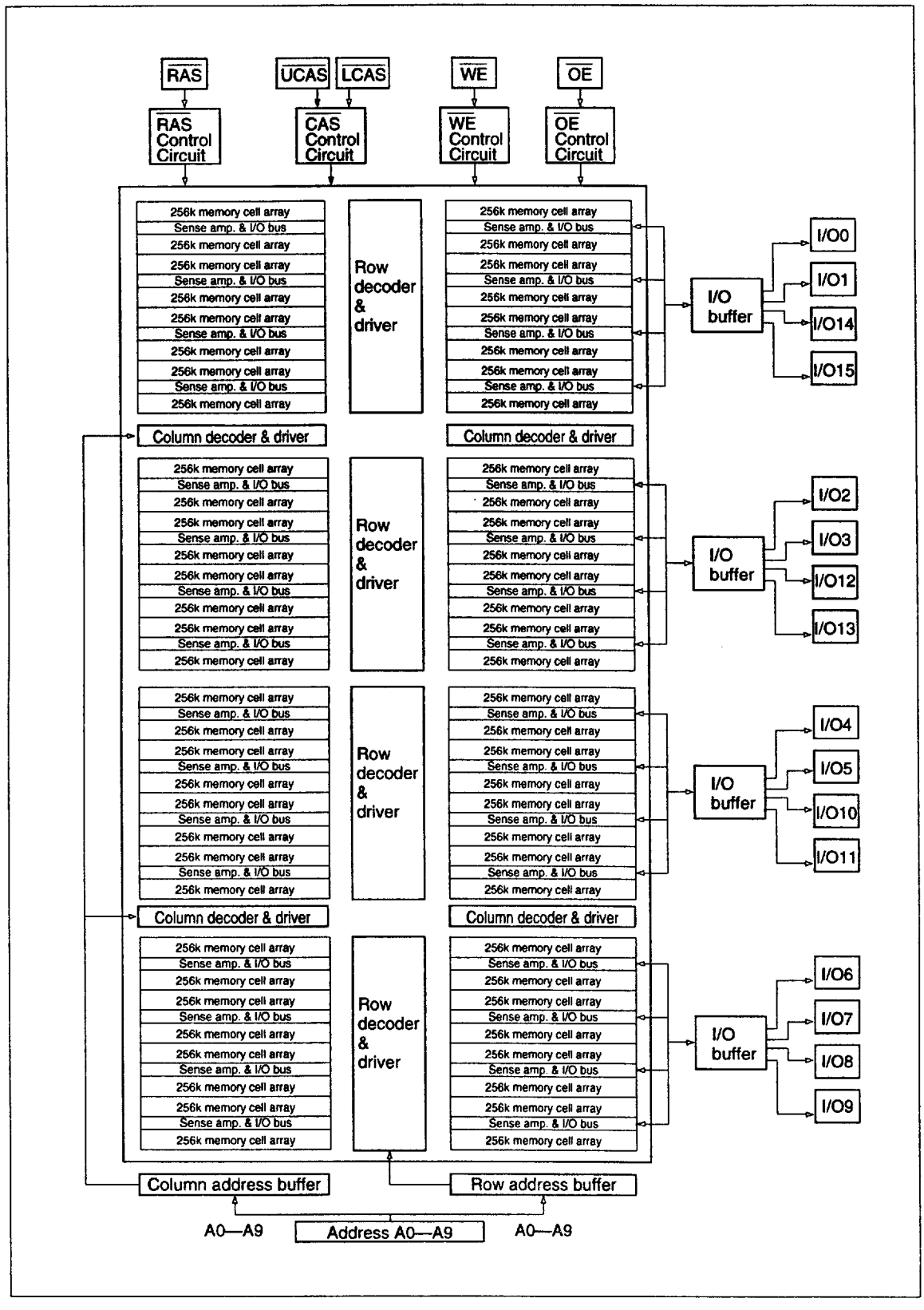

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Truth Table

Inputs					I/O			
$\overline{RAS}$	$\overline{LCAS}$	$\overline{UCAS}$	$\overline{WE}$	$\overline{OE}$	I/O0 – I/O7	I/O8 – I/O15	Operation	Notes
H	H	H	H	H	High-Z	High-Z	Standby	1, 3
L	H	H	H	H	High-Z	High-Z	Refresh	1, 3
L	L	H	H	L	Dout	High-Z	Lower byte read	1, 3
L	H	L	H	L	High-Z	Dout	Upper byte read	1, 3
L	L	L	H	L	Dout	Dout	Word read	1, 3
L	L	H	L	H	Din	Don't care	Lower byte write	1, 2, 3
L	H	L	L	H	Don't care	Din	Upper byte write	1, 2, 3
L	L	L	L	H	Din	Din	Word write	1, 2, 3
L	L	L	H	H	High-Z	High-Z		1, 3
H to L	L	H	–	–	High-Z	High-Z	CBR refresh or Self refresh	1, 3
H to L	H	L	–	–	High-Z	High-Z		
H to L	L	L	–	–	High-Z	High-Z		

Notes: 1. H: High(inactive) L: Low(active)
2. $t_{WCS} \geq 0$ ns Early write cycle
   $t_{WCS} < 0$ ns Delayed write cycle
3. Mode is determined by the OR function of the $\overline{UCAS}$ and $\overline{LCAS}$. (Mode is set by the earliest of $\overline{UCAS}$ and $\overline{LCAS}$ active edge and reset by the latest of $\overline{UCAS}$ and $\overline{LCAS}$ inactive edge.) However write OPERATION and output HIZ control are done independently by each $\overline{UCAS}$, $\overline{LCAS}$.
   ex. if $\overline{RAS}$ = H to L, $\overline{LCAS}$ = L, $\overline{UCAS}$ = H, then $\overline{CAS}$-before-$\overline{RAS}$ refresh cycle is selected.

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to V_{SS}	V_T	–1.0 +7.0	V
Supply voltage relative to V_{SS}	V_{CC}	–1.0 +7.0	V
Short circuit output current	Iout	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	–55 to +125	°C

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Recommended DC Operating Conditions (Ta = 0 to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input high voltage	V_{IH}	2.4	—	6.5	V	1
Input low voltage	V_{IL}	−1.0	—	0.8	V	1

Note : 1. All voltage referred to V_{SS}

DC Characteristics (Ta = 0 to +70°C, V_{CC} = 5.0 V ± 10%, V_{SS} = 0 V)

		HM5118165A/AL						
		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test condition	Notes
Operating current	I_{CC1}	—	150	—	130	mA	t_{RC} = min	1, 2
Standby current	I_{CC2}	—	2	—	2	mA	TTL interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ = V_{IH}, Dout = High-Z	
		—	1	—	1	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} −0.2V Dout = High-Z	
Standby current (L-version)		—	0.15	—	0.15	mA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS}$ ≥ V_{CC} −0.2V Dout = High-Z	
$\overline{RAS}$-only refresh current	I_{CC3}	—	150	—	130	mA	t_{RC} = min	2
Standby current	I_{CC5}	—	5	—	5	mA	$\overline{RAS}$ = V_{IH} $\overline{UCAS}$, $\overline{LCAS}$ = V_{IL} Dout = enable	1
$\overline{CAS}$-before-$\overline{RAS}$ refresh current	I_{CC6}	—	150	—	130	mA	t_{RC} = min	
EDO page mode current	I_{CC7}	—	165	—	150	mA	t_{HPC} = min	1,3
Battery back up operating current (Stand by with CBR refresh) (L-version)	I_{CC10}	—	0.5	—	0.5	mA	CMOS interface Dout = High-Z CBR refresh: t_{RC} = 125 µs t_{RAS} ≤ 0.3 µs	

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DC Characteristics (cont.)

		HM5118165A/AL						
		-7		-8				
Parameter	Symbol	Min	Max	Min	Max	Unit	Test condition	Notes
Self refresh mode current (L-version)	I_{CC11}	—	300	—	300	µA	CMOS interface $\overline{RAS}$, $\overline{UCAS}$, $\overline{LCAS} \leq 0.2V$ Dout = High-Z	
Input leakage current	I_{LI}	–10	10	–10	10	µA	0 V ≤ Vin ≤ 7 V	
Output leakage current Dout = disable	I_{LO}	–10	10	–10	10	µA	0 V ≤ Vout ≤ 7 V	
Output high voltage	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	V	High Iout = –2 mA	
Output low voltage	V_{OL}	0	0.4	0	0.4	V	Low Iout = 2 mA	

Notes : 1. I_{CC} depends on output load condition when the device is selected. I_{CC} max is specified at the output open condition.
2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.
3. Address can be changed once or less while $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$

Capacitance (Ta = 25°C, V_{CC} = 5.0 V ± 10%)

Parameter	Symbol	Typ	Max	Unit	Notes
Input capacitance (Address)	C_{I1}	—	5	pF	1
Input capacitance (Clocks)	C_{I2}	—	7	pF	1
Output capacitance (Data-in, Data-out)	$C_{I/O}$	—	7	pF	1, 2

Notes : 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{UCAS}$ and $\overline{LCAS} = V_{IH}$ to disable Dout.

AC Characteristics (Ta = 0 to +70°C, V_{CC} = 5 V ± 10%, V_{SS} = 0 V)*1, *2, *3, *19

Test Conditions

- Input rise and fall time: 2 ns
- Input levels: V_{IL} = 0 V, V_{IH} = 3.0 V
- Input timing reference levels: 0.8 V, 2.4 V
- Output timing reference levels: 0.8 V, 2.0 V
- Output Load: 1 TTL gate + C_L (100 pF) (Including scope and jig)

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Read, Write, Read-Modify-Write and Refresh Cycles (Common parameters)

		HM5118165A/AL					
		-7		-8			
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Unit**	**Notes**
Random read or write cycle time	t_{RC}	124	–	144	—	ns	
$\overline{RAS}$ precharge time	t_{RP}	50	—	60	—	ns	
$\overline{CAS}$ precharge time	t_{CP}	13	—	15	—	ns	
$\overline{RAS}$ pulse width	t_{RAS}	70	10000	80	10000	ns	
$\overline{CAS}$ pulse width	t_{CAS}	13	10000	15	10000	ns	
Row address setup time	t_{ASR}	0	—	0	—	ns	
Row address hold time	t_{RAH}	10	—	10	—	ns	
Column address setup time	t_{ASC}	0	—	0	—	ns	
Column address hold time	t_{CAH}	13	—	15	—	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	20	45	20	53	ns	4
$\overline{RAS}$ to column address delay time	t_{RAD}	15	35	15	40	ns	5
$\overline{RAS}$ hold time	t_{RSH}	18	—	20	—	ns	
$\overline{CAS}$ hold time	t_{CSH}	58	—	68	—	ns	
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	5	—	5	—	ns	
$\overline{OE}$ to Din delay time	t_{OED}	18	—	20	—	ns	6
$\overline{OE}$ delay time from Din	t_{DZO}	0	—	0	—	ns	7
$\overline{CAS}$ delay time from Din	t_{DZC}	0	—	0	—	ns	7
Transition time (rise and fall)	t_T	2	50	2	50	ns	8

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Read Cycle

		HM5118165A/AL					
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Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Access time from $\overline{RAS}$	t_{RAC}	—	70	—	80	ns	9, 10
Access time from $\overline{CAS}$	t_{CAC}	—	18	—	20	ns	10, 11, 18
Access time from address	t_{AA}	—	35	—	40	ns	10, 12, 18
Access time from $\overline{OE}$	t_{OEA}	—	18	—	20	ns	10
Read command setup time	t_{RCS}	0	—	0	—	ns	
Read command hold time to $\overline{CAS}$	t_{RCH}	5	—	5	—	ns	13
Read command hold time from $\overline{RAS}$	t_{RCHR}	70	—	80	—	ns	
Read command hold time to $\overline{RAS}$	t_{RRH}	0	—	0	—	ns	13
Column address to $\overline{RAS}$ lead time	t_{RAL}	35	—	40	—	ns	
Column address to $\overline{CAS}$ lead time	t_{CAL}	23	—	28	—	ns	
$\overline{CAS}$ to output in low-Z	t_{CLZ}	0	—	0	—	ns	
Output data hold time	t_{OH}	3	—	3	—	ns	
Output data hold time from $\overline{OE}$	t_{OHO}	3	—	3	—	ns	
Output buffer turn-off time	t_{OFF}	—	15	—	15	ns	14
Output buffer turn-off to $\overline{OE}$	t_{OEZ}	—	15	—	15	ns	14
$\overline{CAS}$ to Din delay time	t_{CDD}	18	—	20	—	ns	6
Output data hold time from $\overline{RAS}$	t_{OHR}	3	—	3	—	ns	
Output buffer turn-off time to $\overline{RAS}$	t_{OFR}	—	15	—	15	ns	
Output buffer turn-off to $\overline{WE}$	t_{WEZ}	—	15	—	15	ns	
$\overline{WE}$ to Din delay time	t_{WED}	18	—	20	—	ns	
$\overline{RAS}$ to Din delay time	t_{RDD}	18	—	20	—	ns	

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Write Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write command setup time	t_{WCS}	0	—	0	—	ns	15
Write command hold time	t_{WCH}	13	—	15	—	ns	
Write command pulse width	t_{WP}	10	—	10	—	ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	13	—	15	—	ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	13	—	15	—	ns	
Data-in setup time	t_{DS}	0	—	0	—	ns	16
Data-in hold time	t_{DH}	13	—	15	—	ns	16

Read-Modify-Write Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read-modify-write cycle time	t_{RWC}	175	—	199	—	ns	
$\overline{RAS}$ to $\overline{WE}$ delay time	t_{RWD}	95	—	107	—	ns	15
$\overline{CAS}$ to $\overline{WE}$ delay time	t_{CWD}	43	—	47	—	ns	15
Column address to $\overline{WE}$ delay time	t_{AWD}	60	—	67	—	ns	15
$\overline{OE}$ hold time from $\overline{WE}$	t_{OEH}	18	—	20	—	ns	

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Refresh Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{CAS}$ setup time (CBR refresh cycle)	t_{CSR}	5	—	5	—	ns	
$\overline{CAS}$ hold time (CBR refresh cycle)	t_{CHR}	10	—	10	—	ns	
$\overline{WE}$ setup time (CBR refresh cycle)	t_{WRP}	0	—	0	—	ns	
$\overline{WE}$ hold time (CBR refresh cycle)	t_{WRH}	10	—	10	—	ns	
$\overline{RAS}$ precharge to $\overline{CAS}$ hold time	t_{RPC}	0	—	0	—	ns	

EDO Page Mode Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode cycle time	t_{HPC}	30	—	35	—	ns	26
EDO page mode $\overline{RAS}$ pulse width	t_{RASP}	—	100000	—	100000	ns	17
Access time from $\overline{CAS}$ precharge	t_{CPA}	—	40	—	45	ns	10, 18
$\overline{RAS}$ hold time from $\overline{CAS}$ precharge	t_{CPRH}	40	—	45	—	ns	
Outoput data hold time from $\overline{CAS}$ low	t_{DOH}	5	—	5	—	ns	10, 18
$\overline{CAS}$ hold time referred $\overline{OE}$	t_{COL}	13	—	15	—	ns	
$\overline{CAS}$ to $\overline{OE}$ setup time	t_{COP}	5	—	5	—	ns	
Read command hold time from $\overline{CAS}$ precharge	t_{RCHC}	40	—	45	—	ns	

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EDO Page Mode Read-Modify-Write Cycle

		HM5118165A/AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
EDO page mode read-modify-write cycle time	t_{HPRWC}	90	—	99	—	ns	
$\overline{WE}$ delay time from $\overline{CAS}$ precharge	t_{CPW}	62	—	69	—	ns	15

Refresh

Parameter	Symbol	Max	Unit	Note
Refresh period	t_{REF}	16	ms	1024 cycles

Self-Refresh Mode

		HM5118165AL					
		-7		-8			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
$\overline{RAS}$ pulse width (self refresh)	t_{RASS}	100	—	100	—	µs	
$\overline{RAS}$ precharge time (self refresh)	t_{RPS}	130	—	150	—	ns	
$\overline{CAS}$ hold time (self refresh)	t_{CHS}	–50	—	–50	—	ns	

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Notes:
1. AC measurements assume t_T = 2 ns.
2. An initial pause of 200 µs is required after power up followed by a minimum of eight initialization cycles (any combination of cycles containing $\overline{RAS}$-only refresh or $\overline{CAS}$-before-$\overline{RAS}$ refresh).
3. Only row address is indispensable on address A8, A9.
4. Operation with the t_{RCD} (max) limit insures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only; if $t_{RCD} \geq t_{RAD}$ (max) + t_{AA} (max) – t_{CAC} (max), then access time is controlled exclusively by t_{CAC}.
5. Operation with the t_{RAD} (max) limit insures that t_{RAC} (max) can be met, t_{RAD} (max) is specified as a reference point only; if t_{RAD} is greater than the specified t_{RAD} (max) limit, then access time is controlled exclusively by tAA.
6. Either t_{OED} or t_{CDD} must be satisfied.
7. Either t_{DZO} or t_{DZC} must be satisfied.
8. V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} (min) and V_{IL} (max).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \leq t_{RAD}$ (max). If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
10. Measured with a load circuit equivalent to 1 TTL loads and 100 pF.
11. Assumes that $t_{RCD} \geq t_{RAD}$ (max) + t_{AA}(max) – t_{CAC} (max) and $t_{RAD} \leq t_{RAD}$ (max).
12. Assumes that $t_{RCD} \leq t_{RCD}$ (max) and $t_{RAD} \geq t_{RAD}$ (max).
13. Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
14. t_{OFF} (max) and t_{OEZ} (max) define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
15. t_{WCS}, t_{RWD}, t_{CWD}, t_{AWD} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}$ (min), $t_{CWD} \geq t_{CWD}$ (min), and $t_{AWD} \geq t_{AWD}$ (min), or $t_{CWD} \geq t_{CWD}$ (min), $t_{AWD} \geq t_{AWD}$ (min) and $t_{CPW} \geq t_{CPW}$ (min), the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
16. These parameters are referred to $\overline{UCAS}$ and $\overline{LCAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.
17. t_{RASP} defines $\overline{RAS}$ pulse width in EDO page mode cycles.
18. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CPA}.
19. In delayed write or read-modify-write cycles, $\overline{OE}$ must disable output buffer prior to applying data to the device. After $\overline{RAS}$ is reset, if $t_{OEH} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEH} \leq t_{CWL}$, invalid data will be out at each I/O.
20. When both $\overline{LCAS}$ and $\overline{UCAS}$ go low at the same time, all 16-bits data are written into the device. $\overline{LCAS}$ and $\overline{UCAS}$ cannot be staggered within the same write/read cycles.
21. All the V_{CC} and V_{SS} pins shall be supplied with the same voltages.
22. t_{ASC}, t_{CAH}, t_{RCS}, t_{RCH}, t_{WCS}, t_{WCH}, t_{CSR} and t_{RPC} are determined by the earlier falling edge of $\overline{UCAS}$ or $\overline{LCAS}$.
23. t_{CRP}, t_{CHR}, t_{ACP} and t_{CPW} are determined by the later rising edge of $\overline{UCAS}$ or $\overline{LCAS}$.
24. t_{CWL}, t_{DH}, t_{DS} and t_{CHS} should be satisfied by both $\overline{UCAS}$ and $\overline{LCAS}$.
25. t_{CPN} and t_{CP} are determined by the time that both $\overline{UCAS}$ and $\overline{LCAS}$ are high.
26. t_{HPC} (min) can be achieved during a series of EDO page mode write cycles or EDO page mode read cycles. If both write and read operation are mixed in a EDO page mode $\overline{RAS}$ cycle (EDO page mode mix cycle (1), (2)), minimum value of $\overline{CAS}$ cycle (t_{CAS} + t_{CP} + 2t_T) becomes greater than the specified t_{HPC} (min) value.The value of CAS cycle time of mixed EDO page mode is shown in EDO page mode mix cycle (1) and (2).
27. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade V_{IH} min/V_{IL} max level.
28. Please do not use t_{RASS} timing, 10 µs ≤ t_{RASS} ≤ 100 µs. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq$ 100 µs, then $\overline{RAS}$ precharge time should use t_{RPS} instead of t_{RP}.

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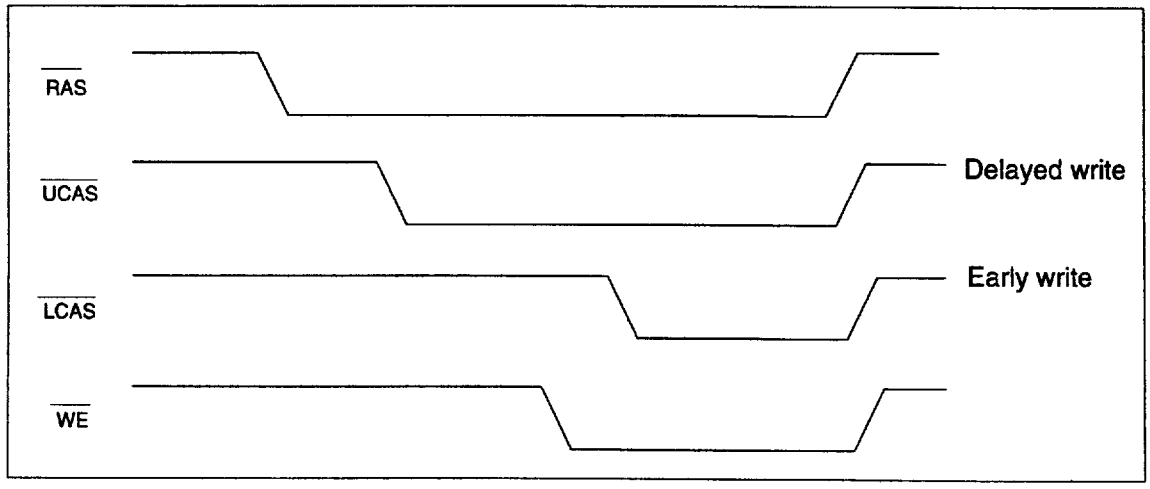
29. If you use distributed CBR refresh mode with 15.6 µs interval in normal read/write cycle, CBR refresh should be executed within 15.6 µs immediately after exiting from and before entering into self refresh mode.
30. If you use $\overline{RAS}$ only refresh or CBR burst refresh mode in normal read/write cycle, 1024 cycles of distributed CBR refresh with 15.6 µs interval should be executed within 16 ms immediately after exiting from and before entering into the self refresh mode.
31. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self fresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

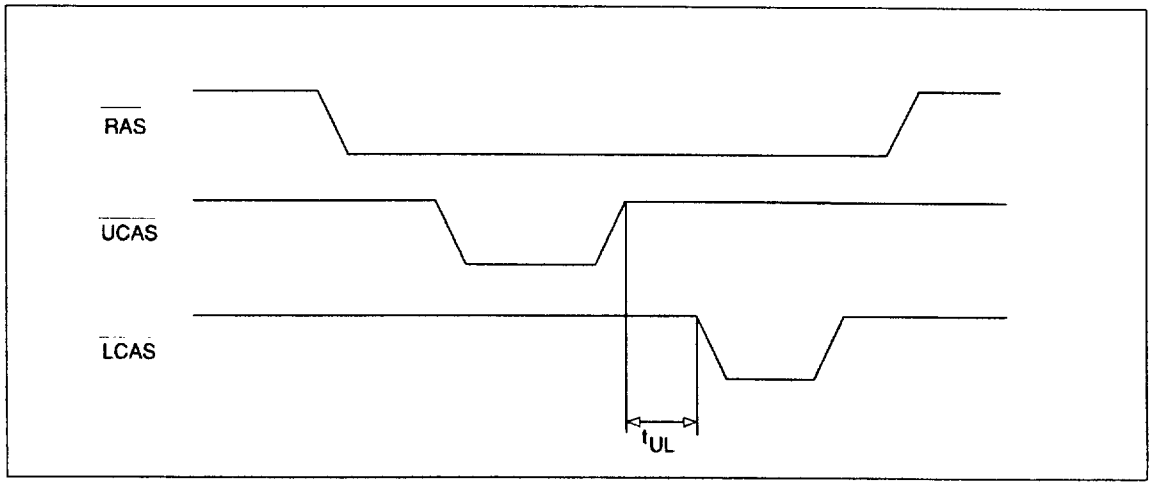
Notes concerning 2$\overline{CAS}$ control

Please do not separate the $\overline{UCAS}$/$\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}$/$\overline{LCAS}$ are allowed under the following conditions.

(1) Each of the $\overline{UCAS}$/$\overline{LCAS}$ should satisfy the timing specifications individually.
(2) Different operation mode for upper/lower byte is not allowed; such as following.



(3) Closely separated upper/lower byte control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, EDO page mode can be performed.



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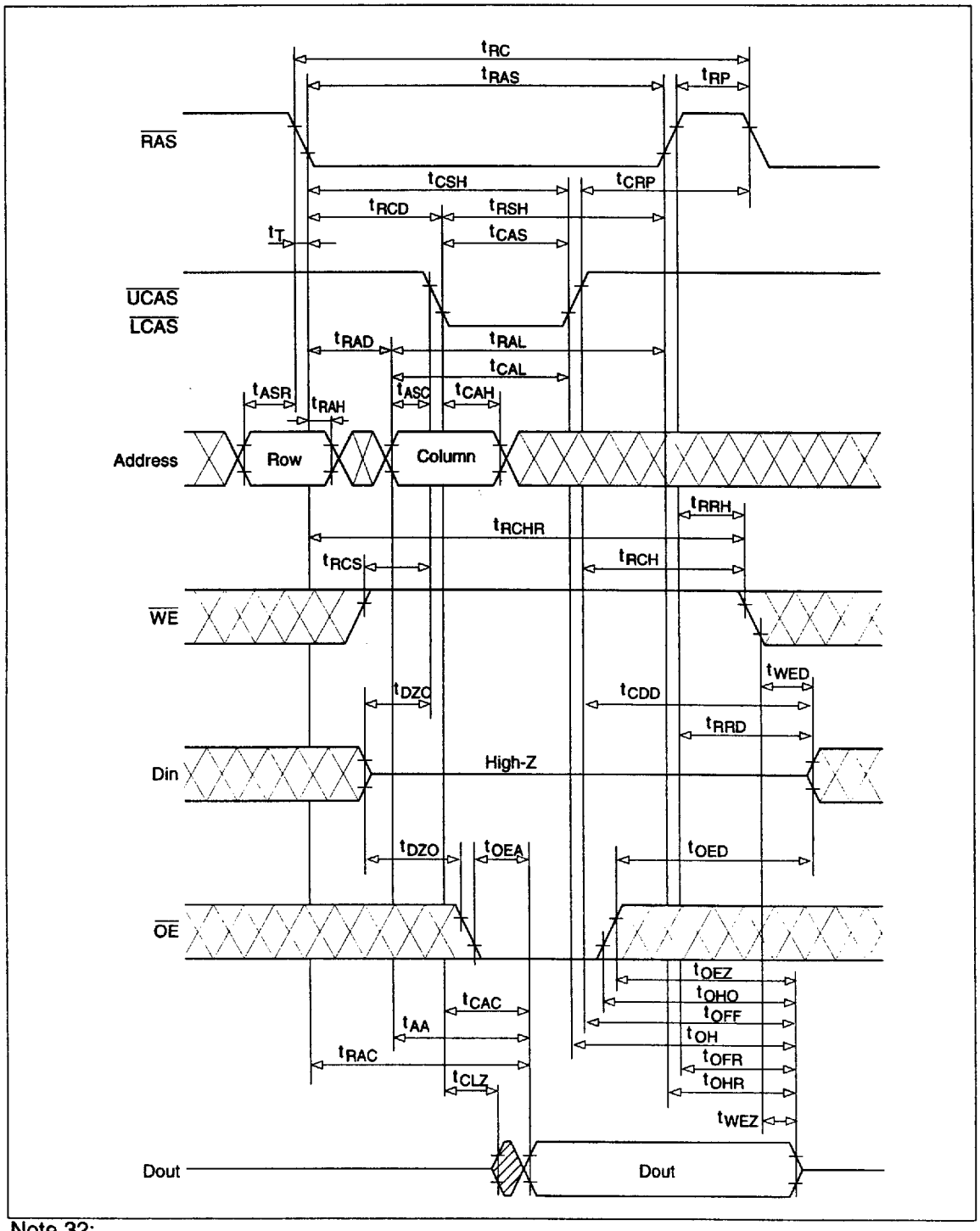
Timing Waveforms*32

Read Cycle



Note 32:

H or L (H: V_{IH} (min) ≤ V_{IN} ≤ V_{IH} (max), L: V_{IL} (min) ≤ V_{IN} ≤ V_{IL} (max))

Invalid Dout

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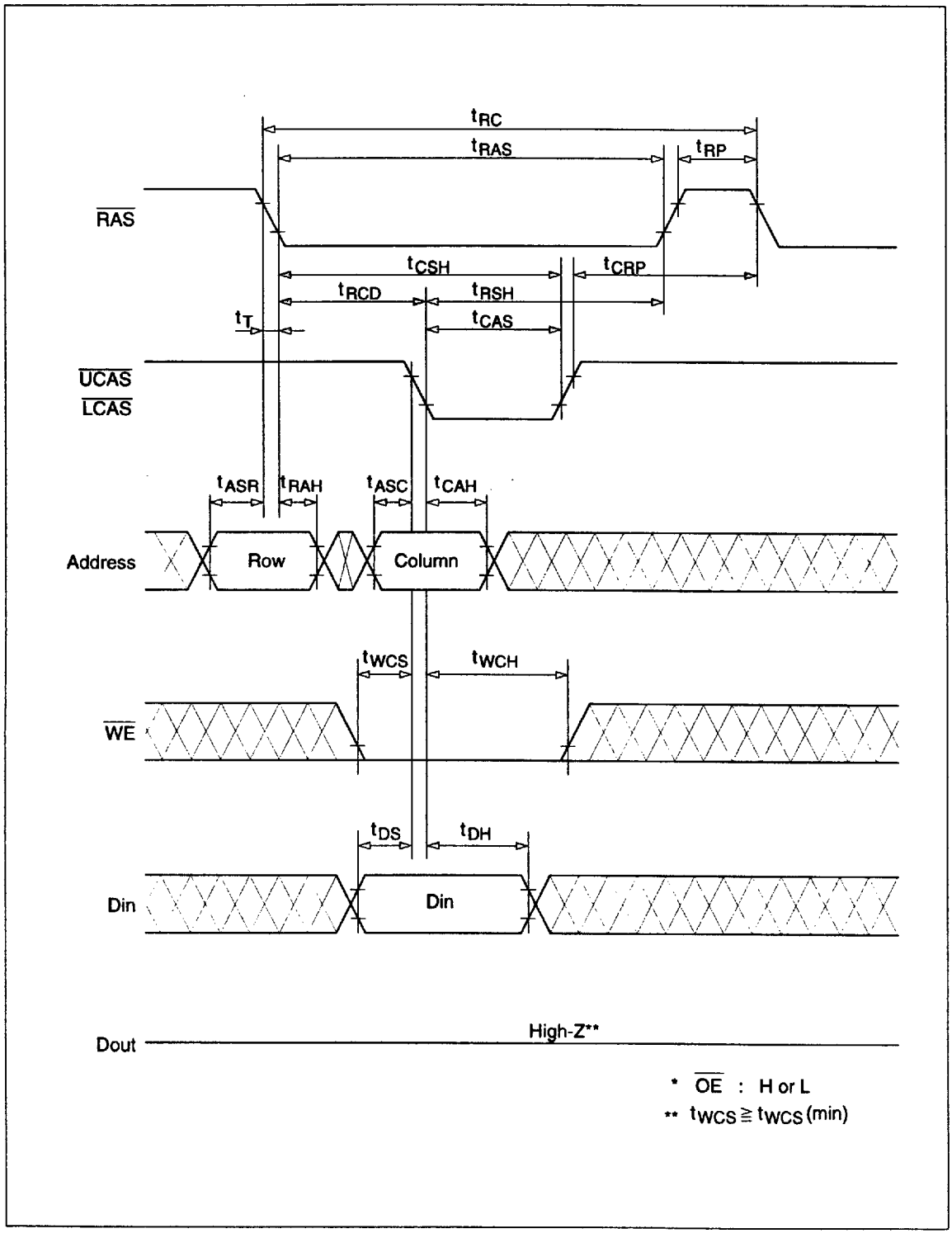
Early Write Cycle



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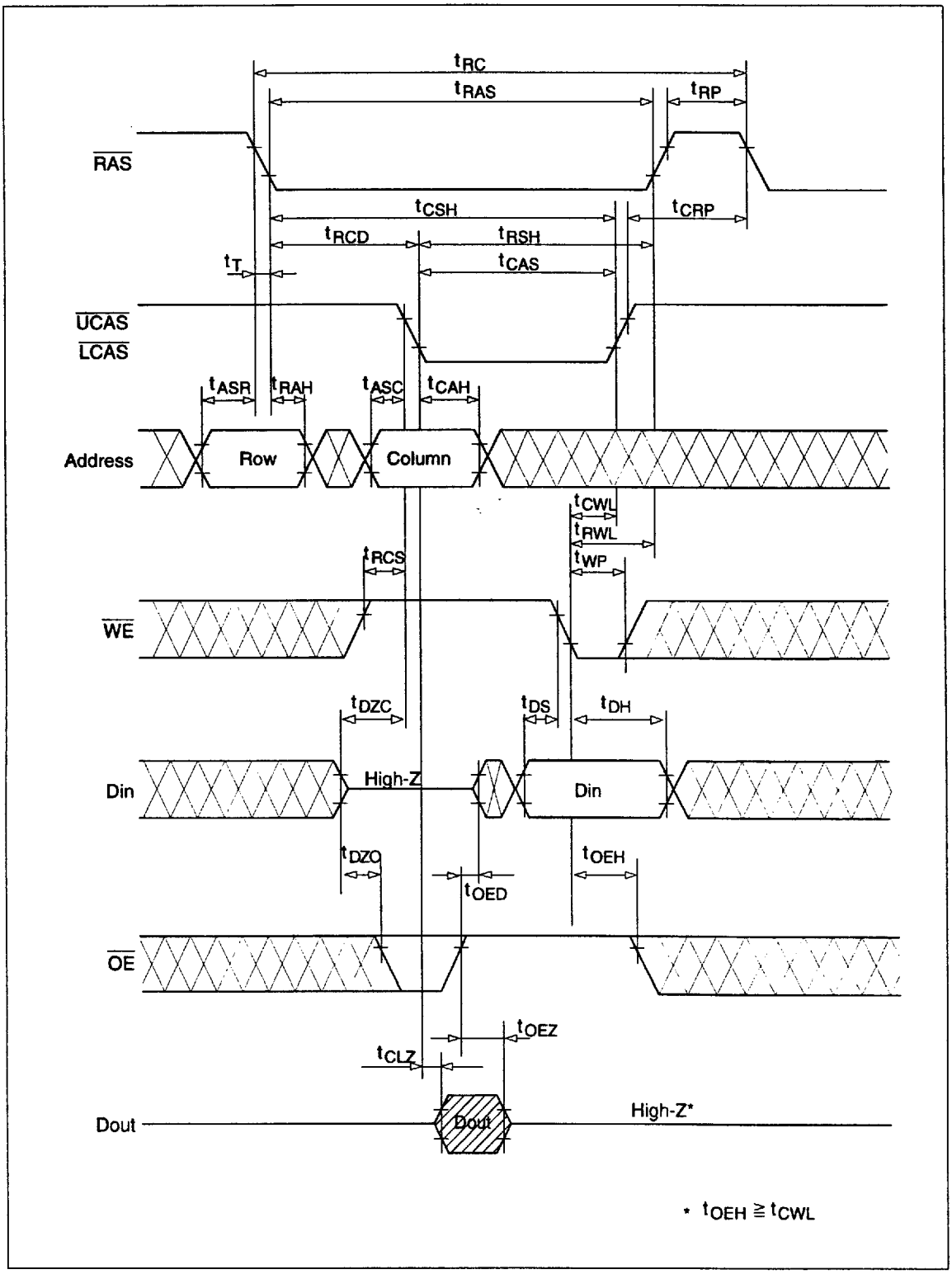
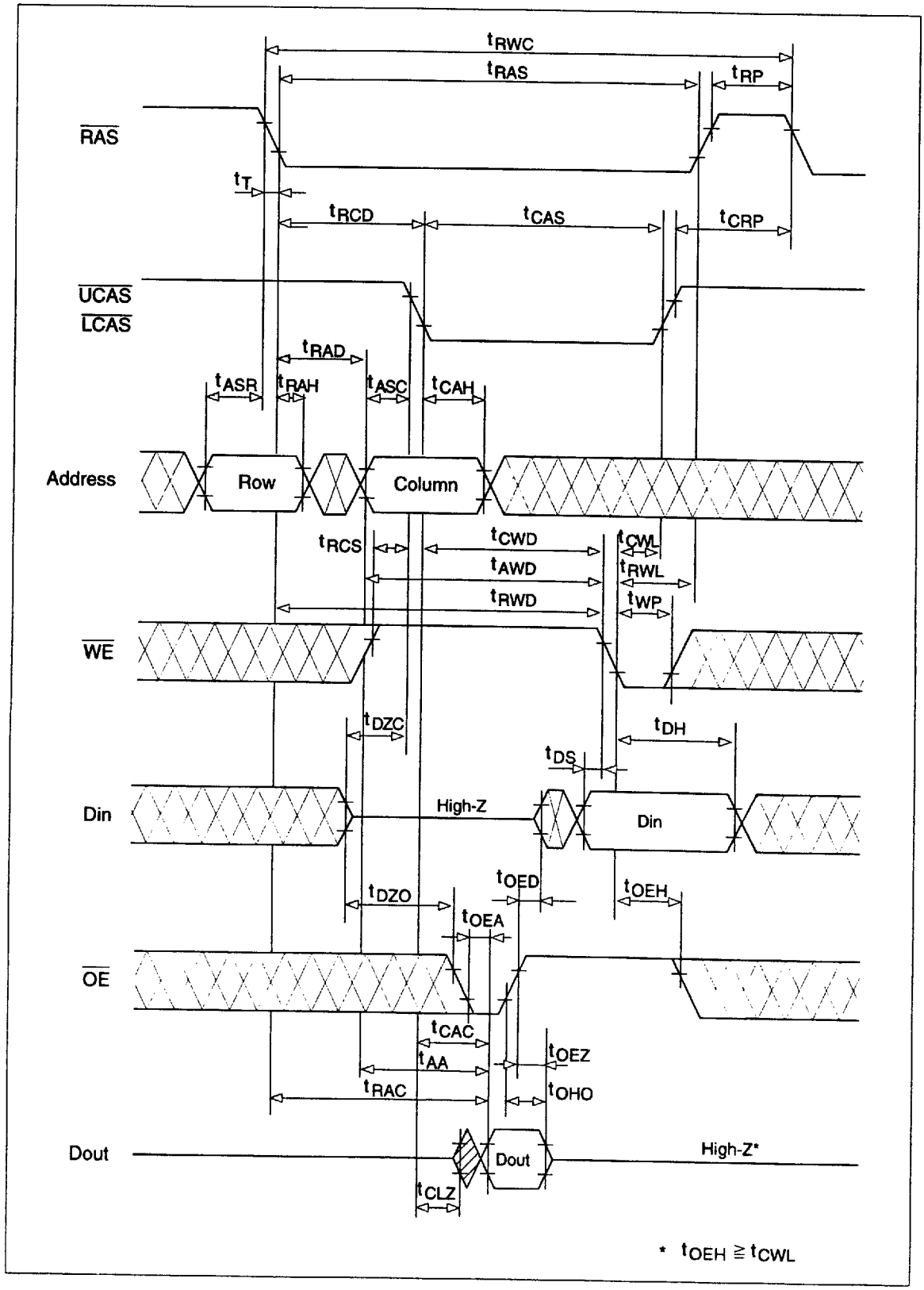
Delayed Write Cycle *19



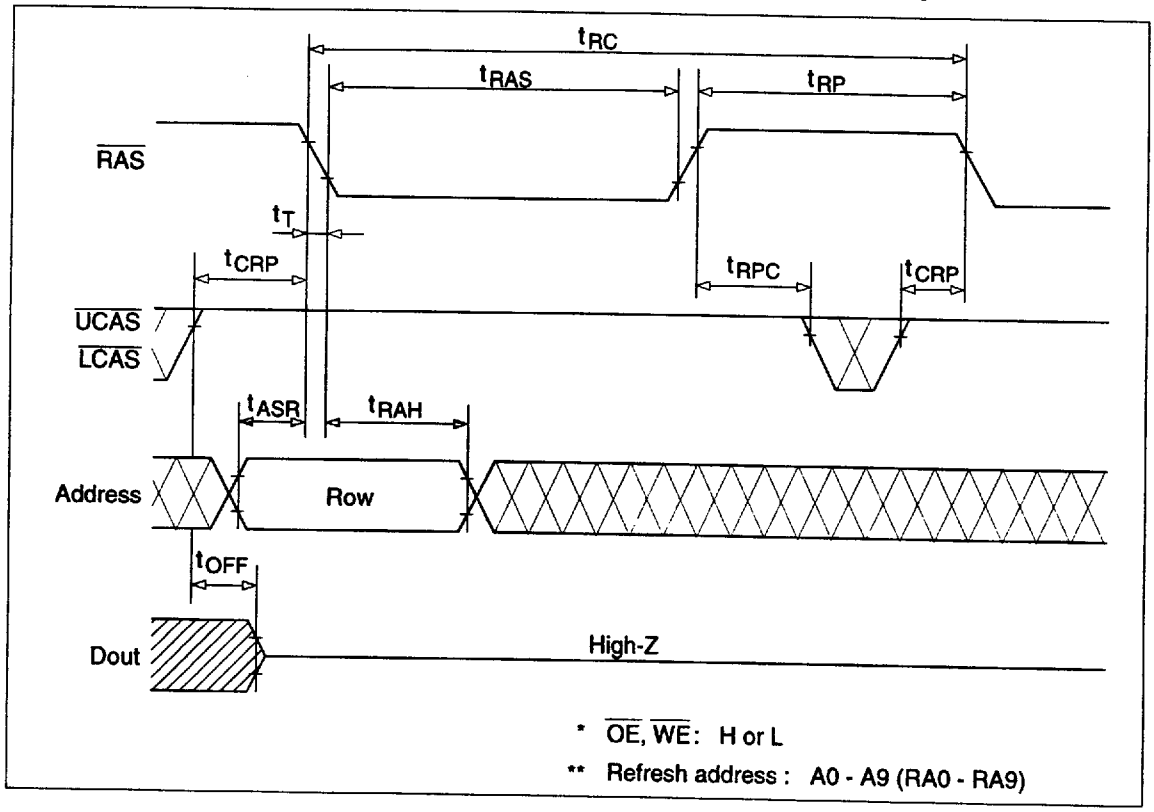
4496203 0026756 151

Read-Modify-Write Cycle *19

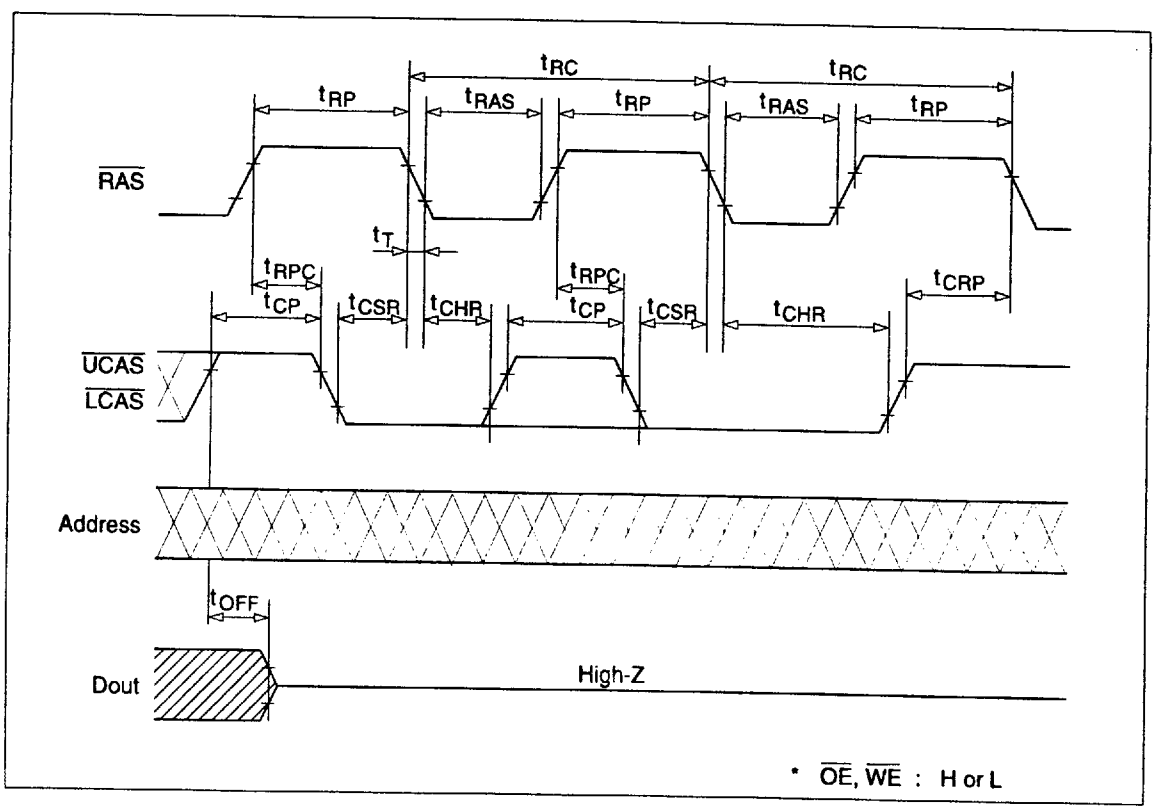


4496203 0026757 098

RAS-Only Refresh Cycle

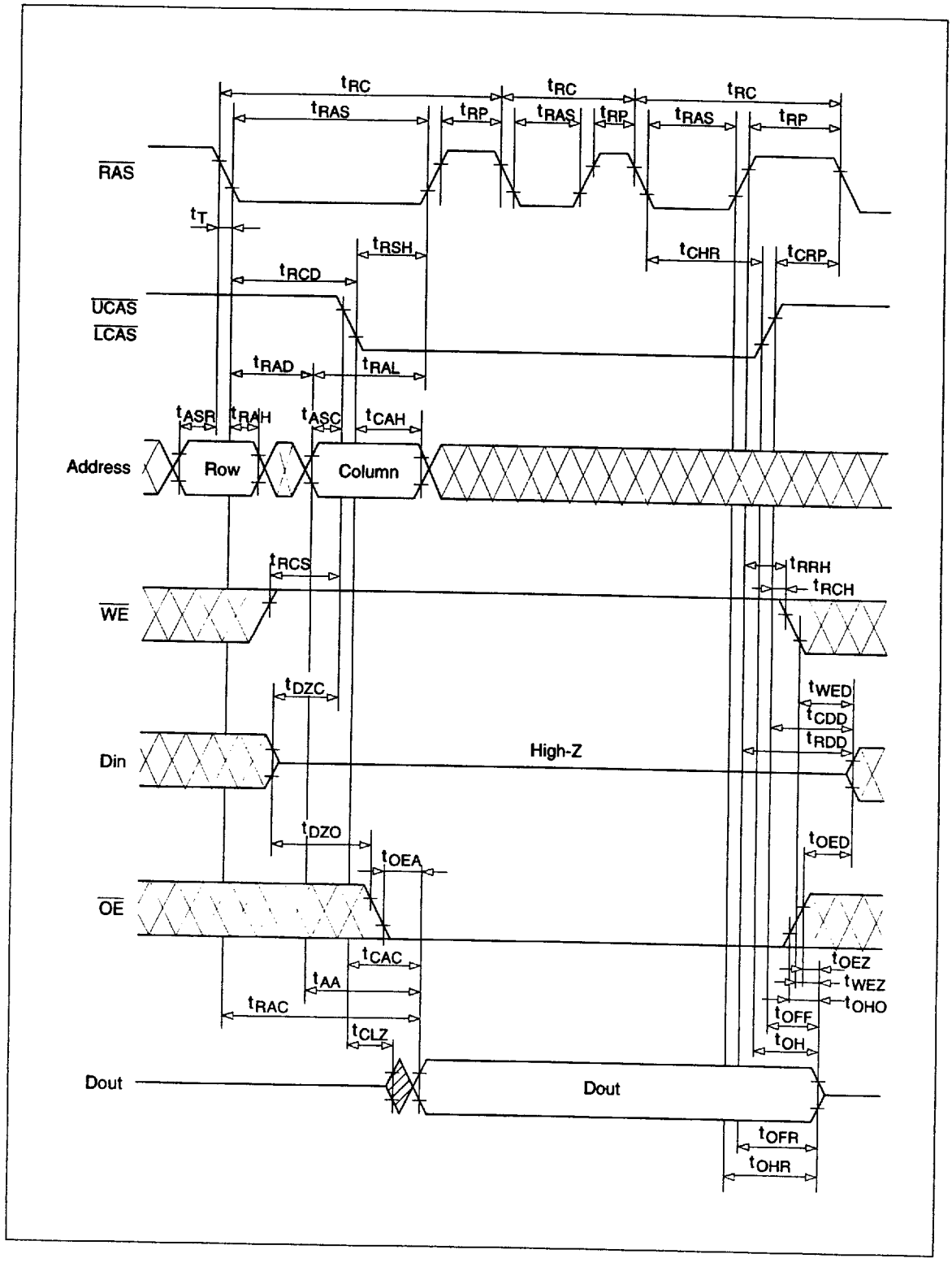


CAS-Before-RAS Refresh Cycle



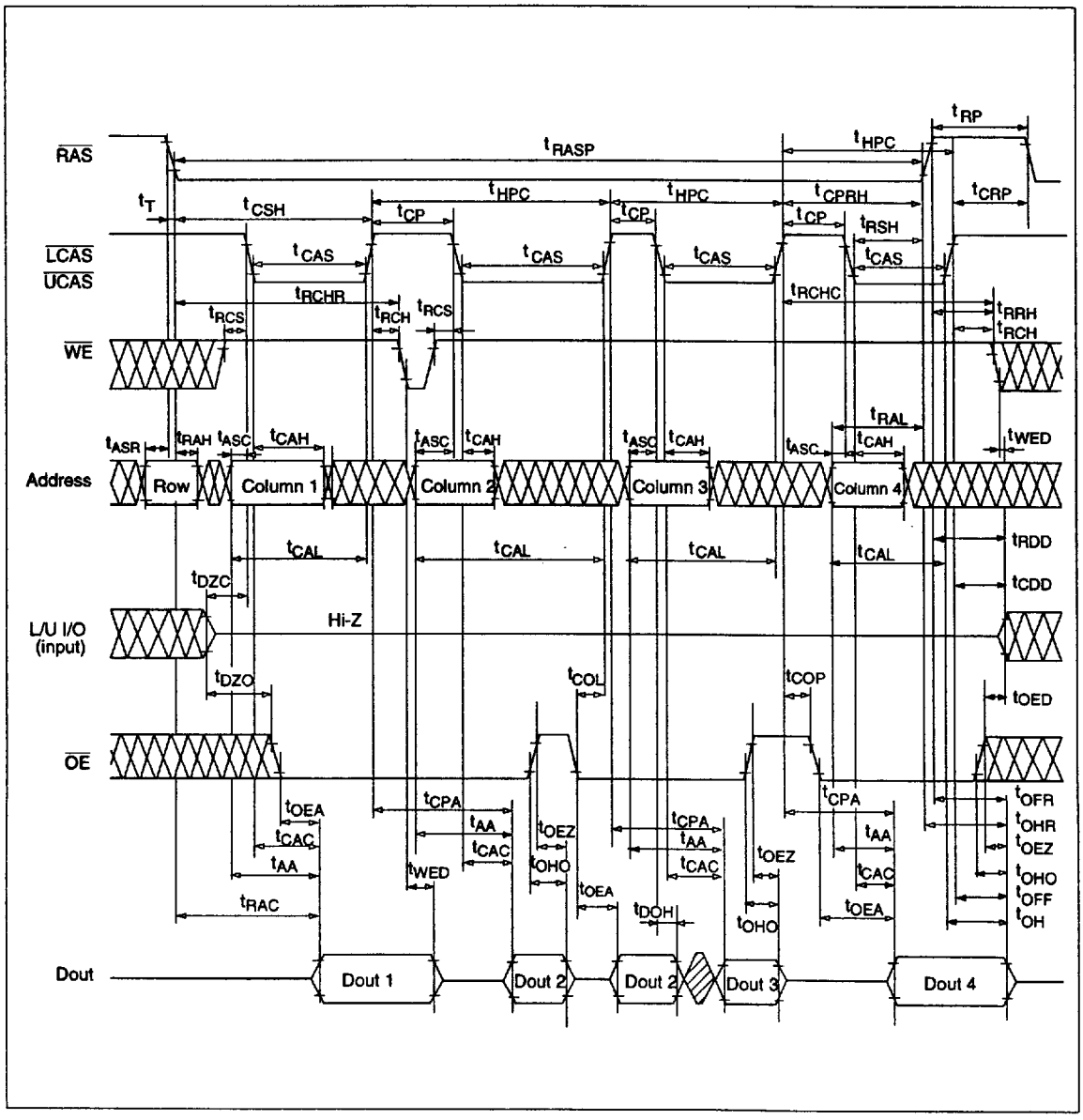
4496203 0026758 T24

Hidden Refresh Cycle



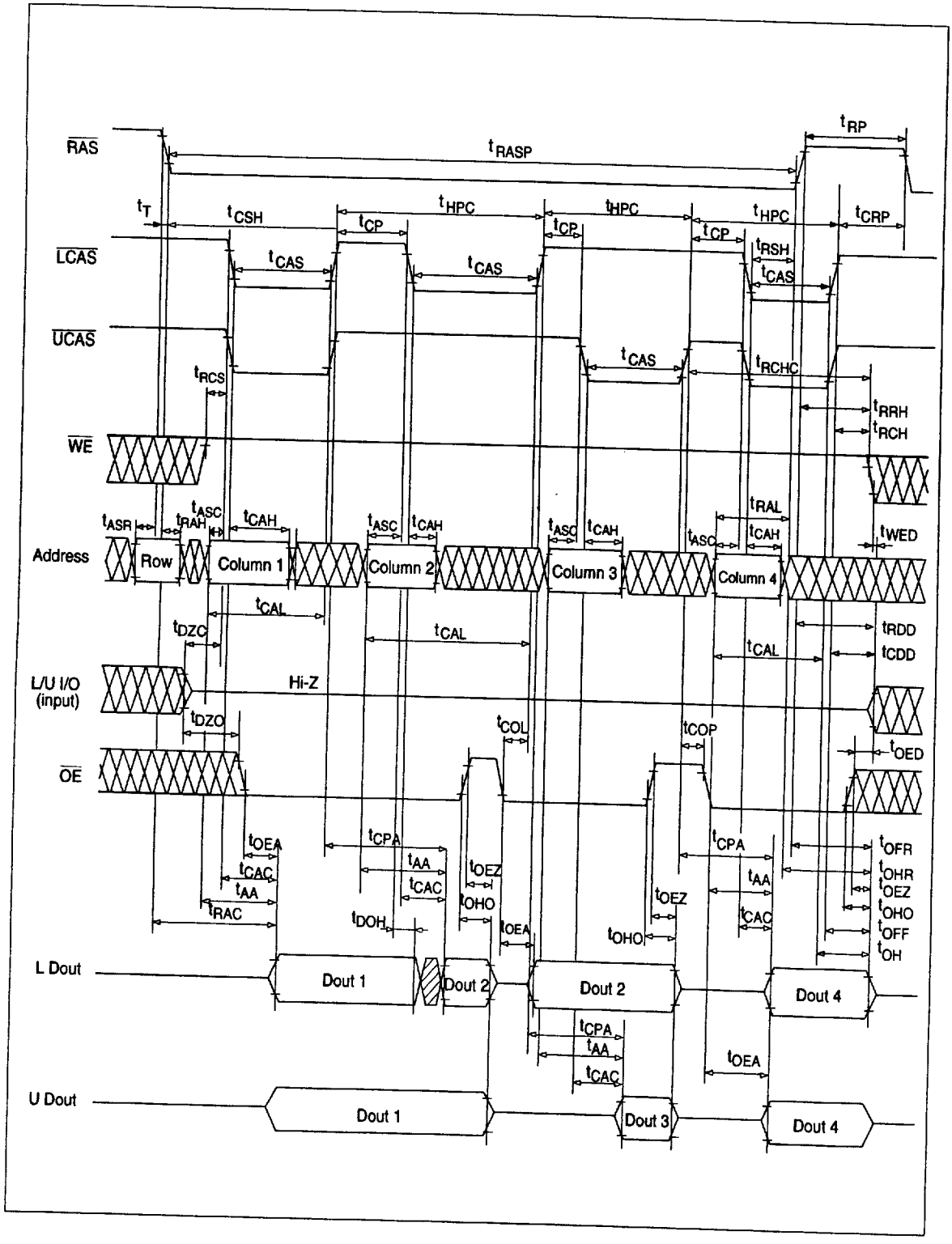
4496203 0026759 960

EDO Page Mode Read Cycle



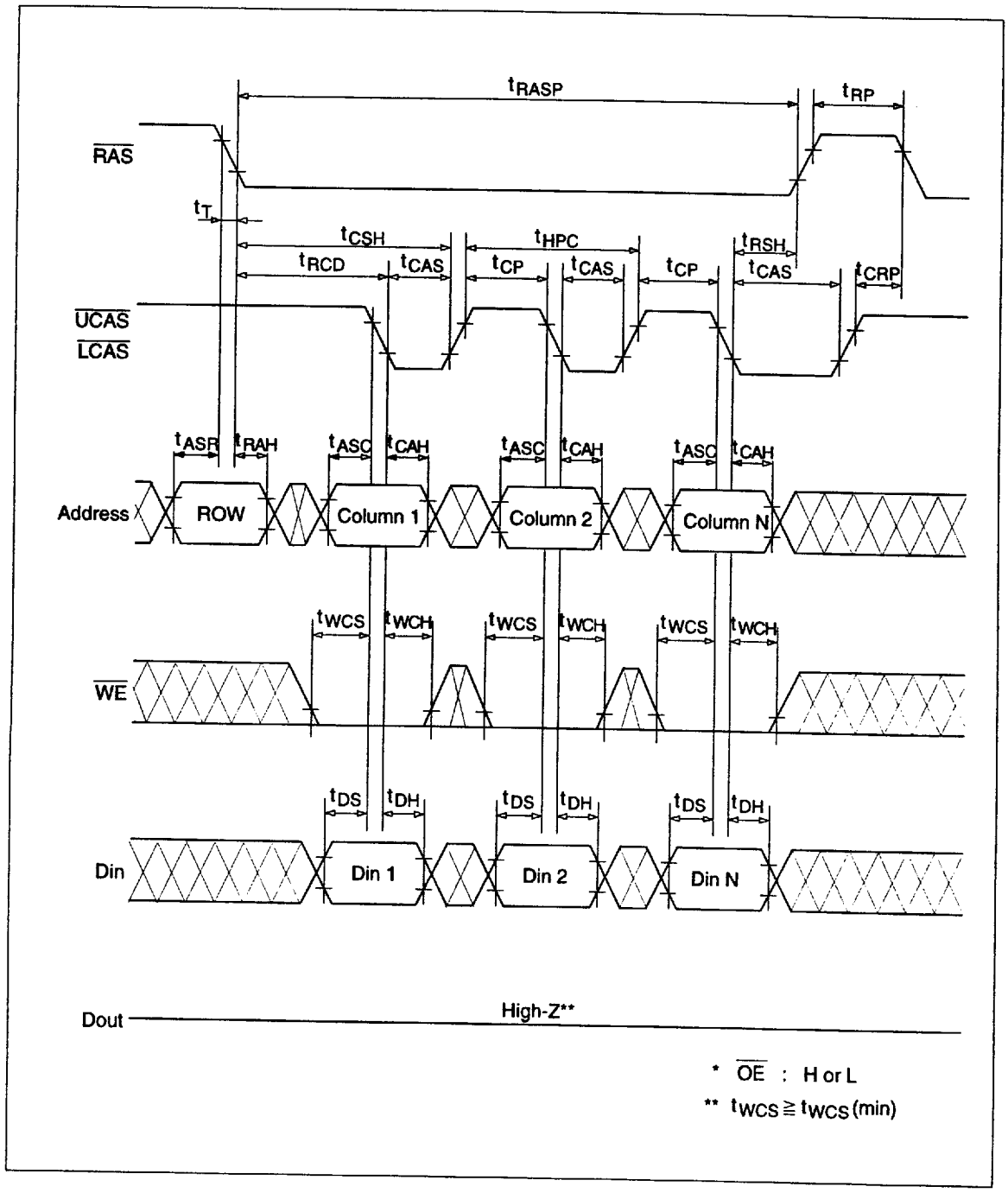
4496203 0026760 682

EDO Page Mode Read Cycle (2$\overline{CAS}$ type)



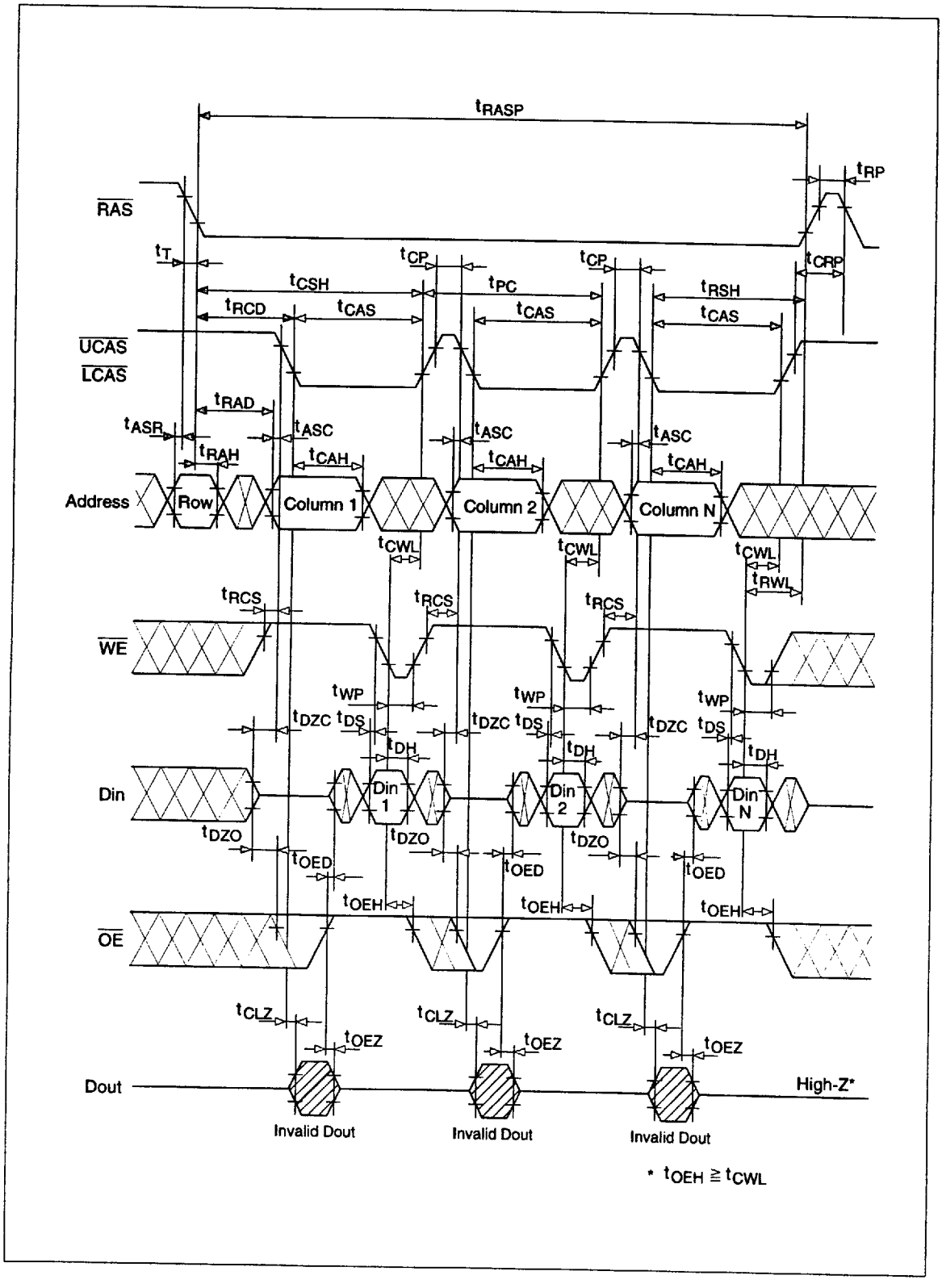
4496203 0026761 519

EDO Page Mode Early Write Cycle



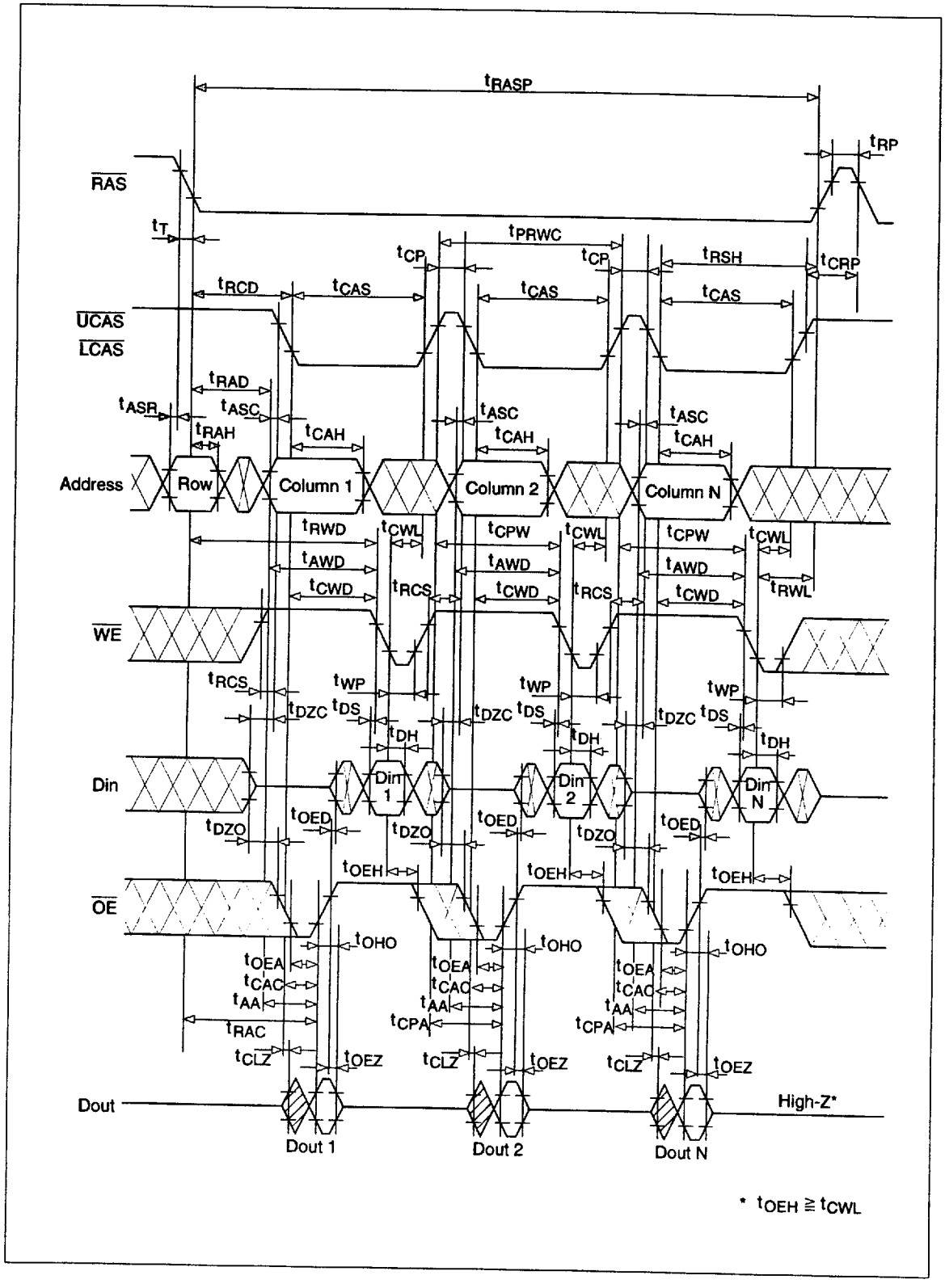
4496203 0026762 455

EDO Page Mode Delayed Write Cycle *19



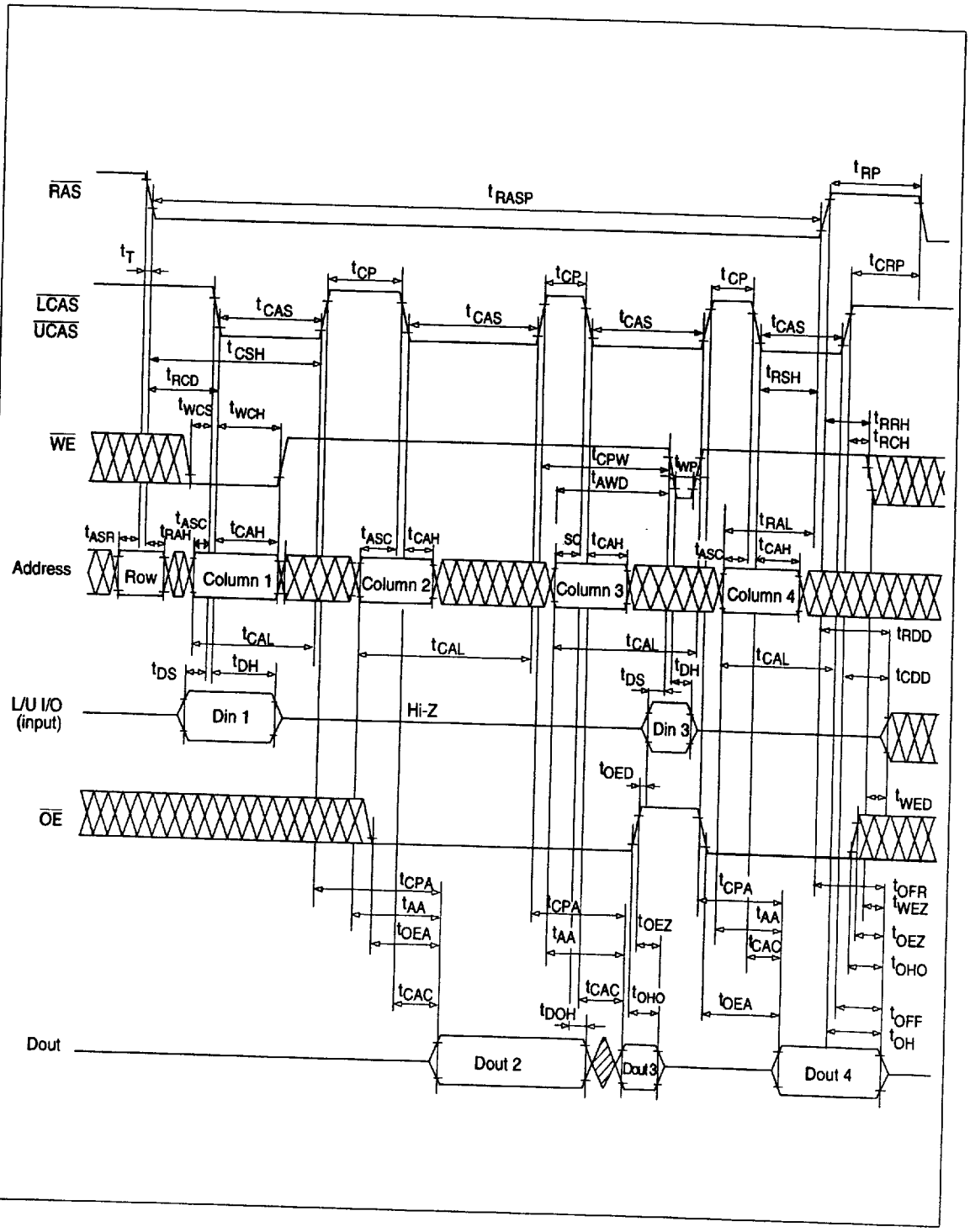
4496203 0026763 391

EDO Page Mode Read-Modify-Write Cycle*19



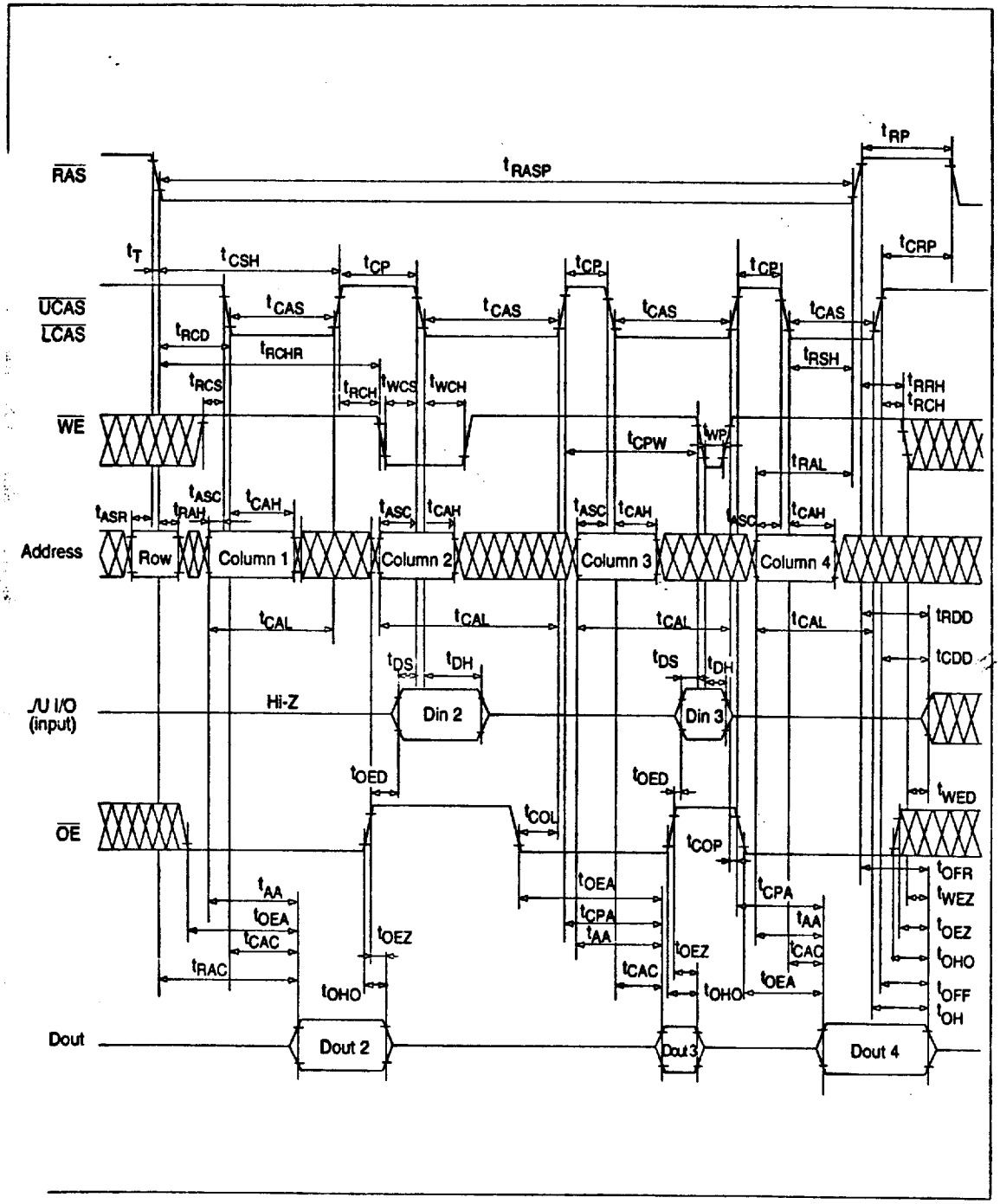
4496203 0026764 228

EDO Page Mode Mix Cycle (1)



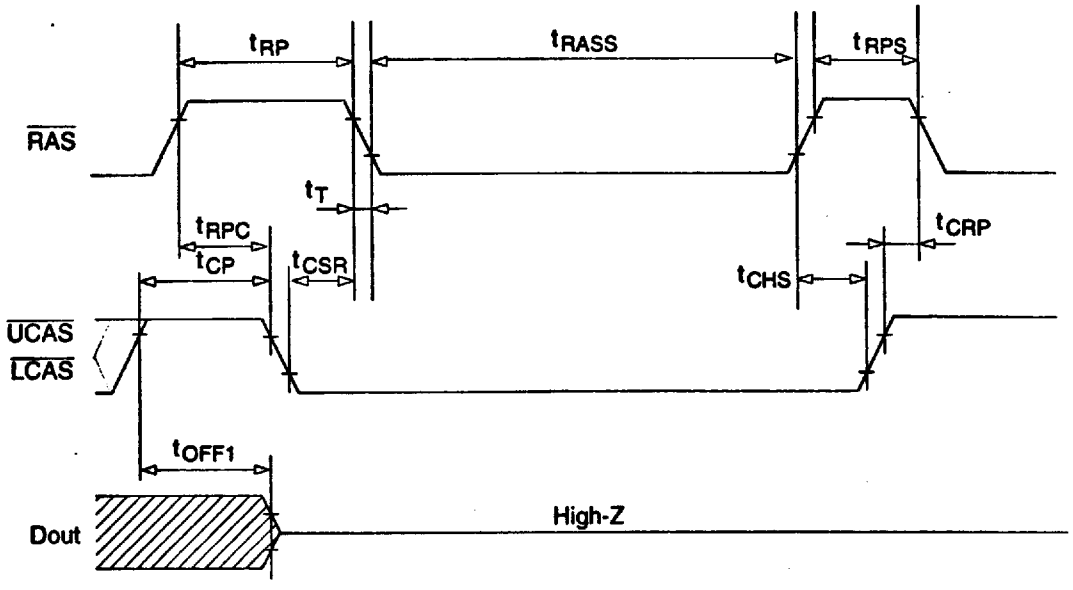
4496203 0026765 164

EDO Page Mode Mix Cycle (2)



4496203 0026766 0T0

Self Refresh Cycle (L-version) *28, 29, 30, 31



*Address, $\overline{OE}$, $\overline{WE}$: H or L

4496203 0026767 T37