DimmDrive Solid State IDE Flash Module with Power Failure Protection* *IDE36*
DimmDrive Solid State IDE Flash Module *IDE33*

FEATURES

- 144 pin SO-DIMMpackage with IDE pinouts
- Plug-and-play solid state disk
- NAND Flash memory technology by SanDisk
- 3.3 V and 5.0 V power supply operation
- 16MB – 2GB memory density
- Low power consumption
- ECC error correction
- 512 Byte Sector compatible to IDE HD Drives
- Supports true IDE mode
- Commercial temperature range 0°C - +70°C
- PFP Power Failure Protection Circuit (IDE36)

POWER BACKUP FEATURES (IDE36)

- Added PFP circuit built in to preserve card integrity during accidental power loss
- PFP circuit may not prevent file/data loss if power failure occurs during a long write operation
- PFP control circuit prevents false operations after power loss
- Improves card integrity in applications with a high risk of power failure
- Minimum power backup time of 10ms

APPLICATIONS

- Embedded systems
- Internet Access Devices
- Set Top Boxes
- WEB Browser
- Routers, Networking
- WEB phones, car PC, DVD, HPC
- Point-of-sale
- Medical and Telcom
- Other applications requiring embedded or solid state storage

* Patent pending

GENERAL DESCRIPTION

The DimmDrive WED7GxxxIDE36 is a high performance single chip flash disk IDE module with Power Failure Protection Circuit available in 144 Pin SO-DIMM package.

The DimmDrive WED7GxxxIDE33 does not have the additional PFP circuit.

The additional circuit provides protection against accidental power loss. This circuit provides an internal power supply and control logic to stop receiving data and complete writing the last sector of data received. This is not intended to be backup for the host system. It will only allow the last sector received to finish writing and no more. It will improve card integrity in applications with a high risk of power failure. The read/write unit is 1 sector (512 bytes) sequential access.

The module is based on SanDisk NAND Flash technology and utilizes 128Mb, 256Mb, 512Mb or 1Gb memory components to provide the maximum in module density.

The DimmDrive WED7GxxxIDE36/33 utilizes a SanDisk Flash ChipSet controller for the SanDisk memory devices. This interface allows a host computer to issue commands to read or write blocks of memory in the Flash memory array. The intelligence to manage the interface protocols, data storage and retrieval as well as ECC, defect handling and diagnostics are controlled by this device. Automatic power management and clock control is handled by the controller as well.

The DimmDrive WED7GxxxIDE36/33 module will have the same functionality and capabilities of an intelligent ATA (IDE) disk drive. Once the device has been configured by the user, it appears to the host as a standard ATA disk drive.

The on-board controller is a highly integrated solution designed to handle all intelligent operations, even the rare cases when new defects arise and need to be mapped out or replaced by a spare. The hardware performs the complicated task of ECC detection and correction and will return good data to the host. The controller manages all defects and errors and makes the Flash memory appear as perfect memory to the host.

The DimmDrive WED7GxxxIDE36/33 module also provides a more cost effective solution to the traditional hard disk media. The module is perfect for applications requiring upgrade ability to higher densities and for those applications with limited space availability and power consumption requirements.

Unlike standard IDE drives, no cables or extra space is required. The module has no moving parts providing significant reduction in power consumption and increasing reliability. Simply insert the module into a standard 144 Pin SO-DIMM socket with IDE pinout and you then have a bootable flash disk.

The DimmDrive WED7GxxxIDE36/33 is available with memory densities of 16MB to 2GB.

MODULE PINOUT

PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL	PIN	SIGNAL
2	GND	38	D11	74	CS0#	110	A2
4	V_{CC}	40	NC	76	NC	112	NC
6	GND	42	D3	78	NC	114	NC
8	NC	44	NC	80	CS1#	116	DASP#
10	D7	46	D12	82	IORD#	118	PDIAG#
12	NC	48	NC	84	IOWR#	120	A1
14	D8	50	D2	86	NC	122	A0
16	NC	52	NC	88	NC	124	IOCS16#
18	D6	54	D13	90	NC	126	V_{CC}
20	NC	56	NC	92	NC	128	GND
22	D9	58	D1	94	NC	130	NC
24	NC	60	NC	96	IRQ	132	NC
26	D5	62	D14	98	CSEL#*	134	NC
28	NC	64	NC	100	RESET	136	NC
30	D10	66	D0	102	IORDY**	138	NC
32	NC	68	NC	104	NC	140	NC
34	D4	70	D15	106	NC	142	NC
36	NC	72	NC	108	NC	144	NC

Notes:

Odd pins are NC (NO CONNECT).

"/" indicates signals active low.

* low for MASTER, high (open) for SLAVE

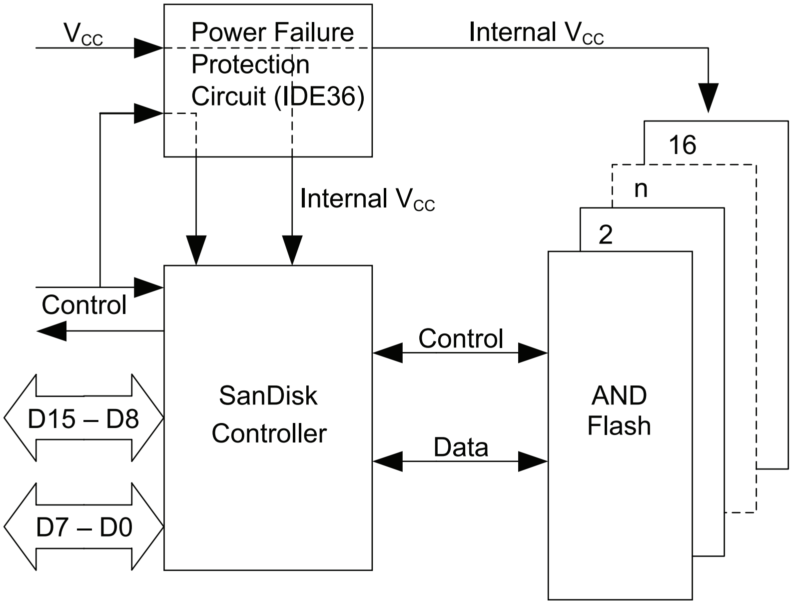
** pulled up

On the NC pins of the module, additional signals not used in the IDE mode may be present.

SIGNAL DESCRIPTION

SIGNAL NAME	DIR	PIN	DESCRIPTION
RESET	I	100	HOST RESET. Reset signal from the host that is active on power up.
D(15-0)	I/O	70,62,54,46,38,30, 22,14,10,18,26,34, 42,50,58,66	HOST DATA. These 16 lines carry the data between the controller and the host. The low 8 lines transfer commands, status and ECC information between the host and the controller.
IOWR	I	84	I/O WRITE. This strobe pulse is used to clock data or commands on the host data bus into the controller. The clocking will occur on the negative to positive edge of the signal (trailing edge).
IORD	I	82	I/O READ. This is a read strobe generated by the host. This signal gates data or status on the host bus and strobes the data from the controller into the host on the low to high transition (trailing edge).
CSEL	I	98	This internally pulled up signal is used to configure this device as a Master or a Slave. When this pin is grounded by the host, this device is configured as a Master. When this pin is high (or open), this device is configured as a Slave.
IRQ	O	96	INTERRUPT REQUEST. This is an interrupt request from the controller to the host, asking for service. The output of this signal is tri-stated when the interrupts are disabled by the host.
IOCS16	O	124	I/O SELECT 16. This open drain output is asserted low by the controller to indicate to the host the current cycle is a16 bit word data transfer.
PDIAG	I/O	118	PASS DIAGNOSTIC. This bi-directional open drain signal is asserted by the slave after anExecute Diagnostic command to indicate to the master it has passed its diagnostics.
A(2-0)	I	110,120,122	HOST ADDRESS. These address lines are used to select the registers within the controller task file.
CS0	I	74	HOST CHIP SELECT 0. This is a chip select signal that is used to select the controller task file.
CS1	I	80	HOST CHIP SELECT 1. This is a chip select signal that is used to select the control and diagnostic register.
DASP	I/O	116	DISK ACTIVE/SLAVE PRESENT. This open drain output signal is asserted low any time the drive is active. In a master/slave configuration, this signal is used by the slave to inform the master a slave is present.
IORDY	O	102	This is an optional signal that is negated when the drive is not ready to respond to a data transfer request. For the module this signal is not used, the pin is pulled up. As long as the host obeys PIO mode 0 or 4 timing, the module is guaranteed to respond properly.
GND		2,6,128	GROUND.
Vcc		4,126	POWER (3.3V – 5V)

FIG. 1 BLOCK DIAGRAM



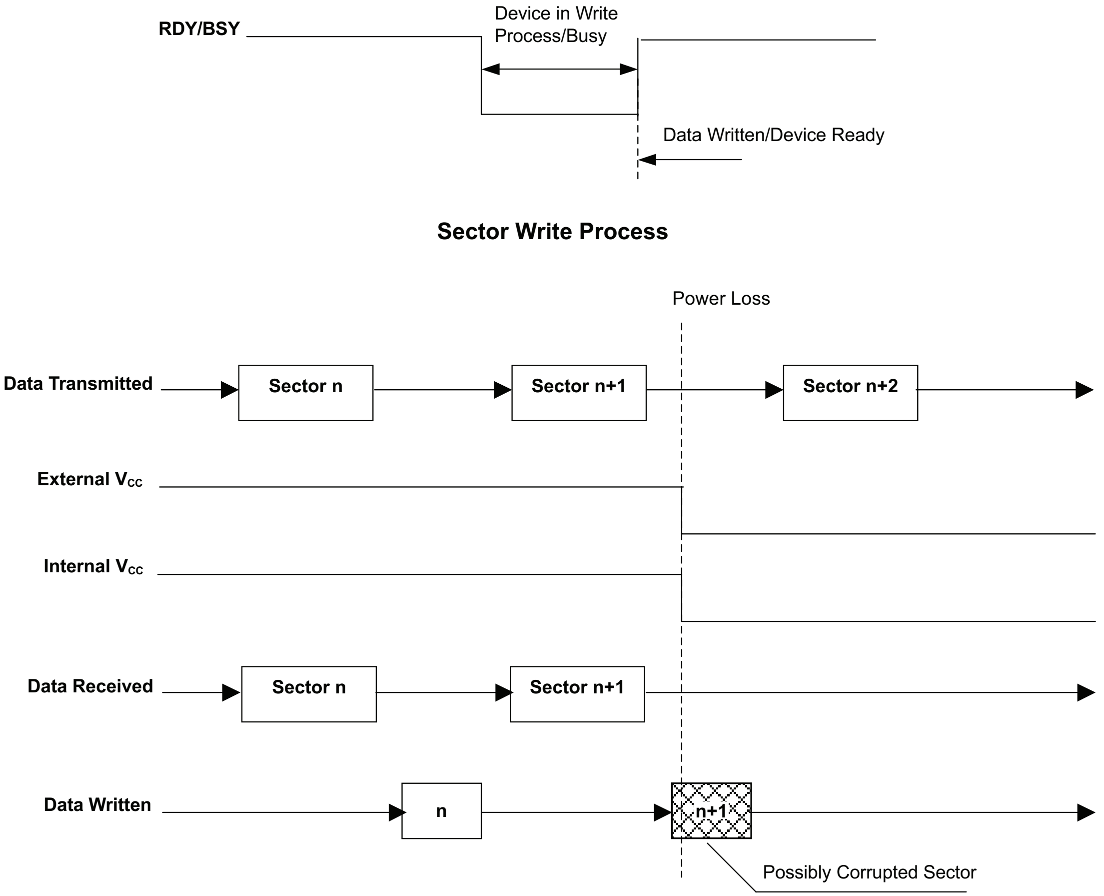
POWER BACKUP TIMING

Shown in the following two figures are the differences in operation between the WED7GxxxIDE33 module, and the WED7GxxxIDE36 module with Power Failure Protection Circuit.

Figure 1 shows how a sector is written to a NAND Flash. The entire sector is received and then is written at one time. The RDY/BSY line stays busy until proper writing of the data is ensured. If power loss occurs before the RDY/BSY line becomes ready again, the module may have correctly written the data, but this is not ensured. Therefore the data may be corrupted.

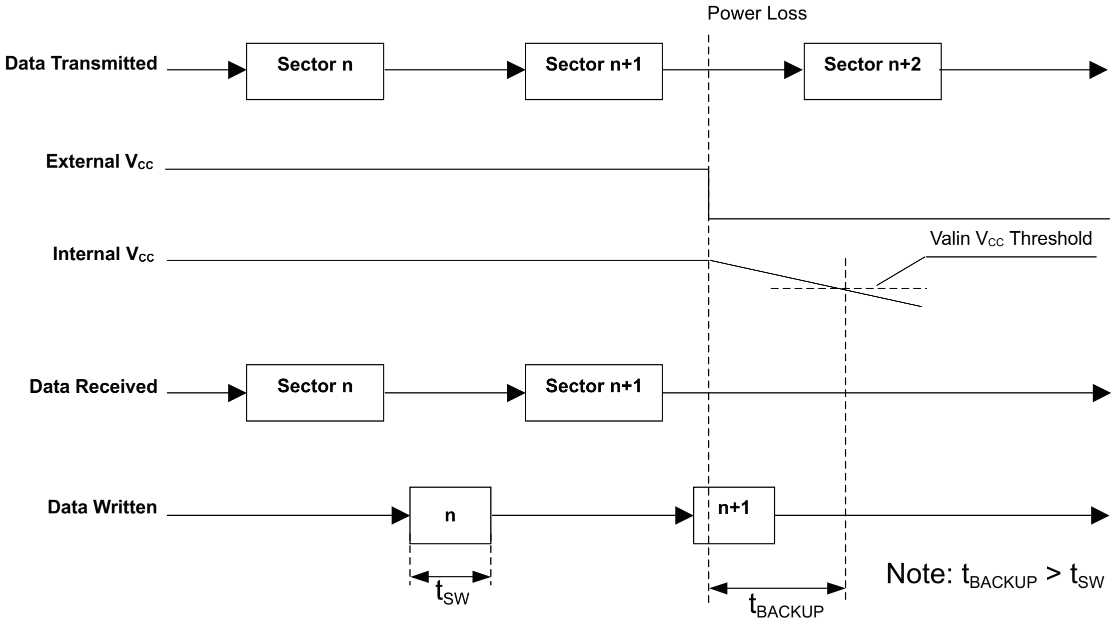
Figure 2 shows the protected module. The power is again lost after the second sector (Sector n+1) is received, but the internal backup power allows the sector to be properly written, and the card completes the write sector operation.

FIG. 2 POWER LOSS WITHOUT POWER FAILURE PROTECTION CIRCUIT



Note: Sector Blocks in these diagrams do not represent a difference with size of data written, between the data received and the data written. This represents the shorter time to write the data than to transmit it.

FIG. 2: POWER LOSS WITH POWER FAILURE PROTECTION CIRCUIT



ENVIRONMENTAL SPECIFICATIONS

Temperature	Operating Non-Operating	0° C to 70° C -25° C to 85° C
Humidity	Operating Non-Operating	8% to 95 %, non-condensing 8% to 95 %, non-condensing
Acoustic Noise		0 dB
Altitude (relative to sea level)	Operating Non-Operating	80,000 feet maximum

POWER REQUIREMENTS

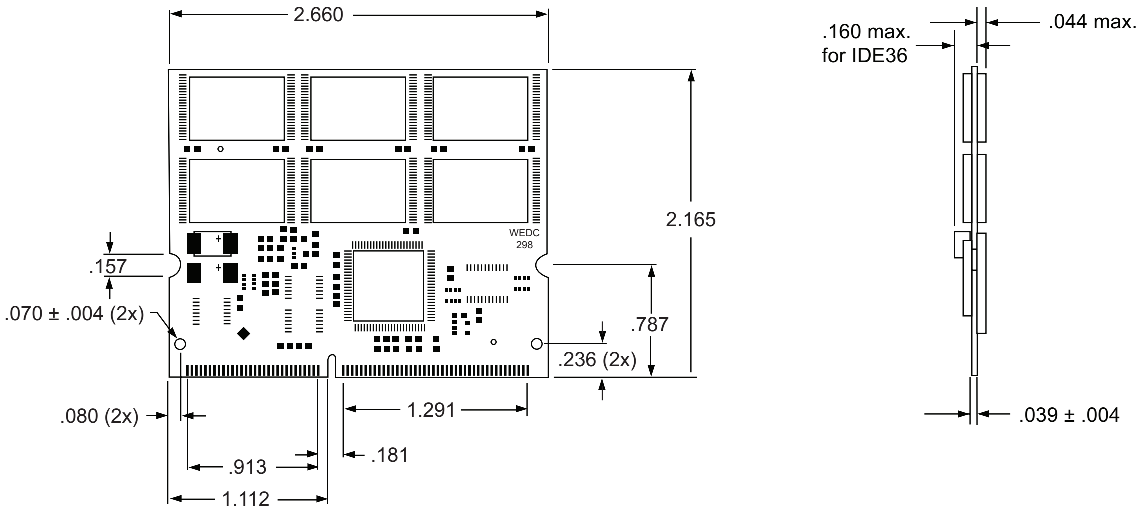
		3.3 V	5 V
DC Input Voltage (V_{CC}) 100 mV max. ripple (p-p)		3.3V +/- 5%	5V +/- 10%
See Notes	Sleep Reading Writing Read/Write Peak	200 µA 21 mA 24 mA 150 mA/50 µs	500 µA 34 mA 34 mA 150 mA/50 µs

Notes:
All values quoted are typical at ambient temperatures and nominal supply voltage unless otherwise stated.
Sleep mode current is specified under the condition that all inputs are at static CMOS levels and in a “Not Busy” operating state.

RELIABILITY AND MAINTENANCE

MTBF (@ 25° C)	> 1,000,000 hours
Preventive Maitenance	None
Data Reliability	<1 non-recoverable error in 10^{14} bits read <1 erroneous correction in 10^{20} bits read
Endurance (commercial temp.)	300,000 erase/program cycles per block typical

PACKAGE



ORDERING INFORMATION–DIMMDRIVE PART NUMBER MATRIX

WED 7 G 256 IDE36 A D C 25

PREFIX

PRODUCT GROUP
7 Flash

SUBSTRATE
F FRA w/Tin leads contact
G FRA w/Gold contact

CAPACITY

016	16MB	416	416MB
032	32MB	448	448MB
048	48MB	480	480MB
064	64MB	512	512MB
080	80MB	576	576MB
096	96MB	640	640MB
112	112MB	704	704MB
128	128MB	768	768MB
144	144MB	832	832MB
160	160MB	896	896MB
176	176MB	960	960MB
192	192MB	1G0	1024MB
208	208MB	1G1	1152MB
224	224MB	1G2	1280MB
240	240MB	1G4	1408MB
256	256MB	1G5	1536MB
288	288MB	1G6	1664MB
320	320MB	1G7	1792MB
352	352MB	1G9	1920MB
384	384MB	2G0	2048MB

CARD FAMILY & VERSION
IDE33 SanDisk based IDE module
IDE36 SanDisk based IDE module with PFP circuit

OPTIONS
A Reset Low (Standard)

PACKAGE
D SO-DIMM; 144

TEMPERATURE RANGE
C Commercial 0°C to +70°C

SPEED
25 250ns