100MHz Differential Twisted-Pair Drivers

The EL5170 and EL5370 are single and triple high bandwidth amplifiers with a fixed gain of 2. They are primarily targeted for applications such as driving twisted-pair lines in component video applications. The inputs signal can be in either single-ended or differential form but the outputs are always in differential form.

The output common mode level for each channel is set by the associated V_{REF} pin, which have a -3dB bandwidth of over 70MHz. Generally, these pins are grounded but can be tied to any voltage reference.

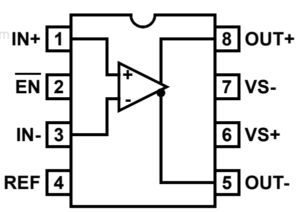
All outputs are short circuit protected to withstand temporary overload condition.

The EL5170 and EL5370 are specified for operation over the full -40°C to +85°C temperature range.

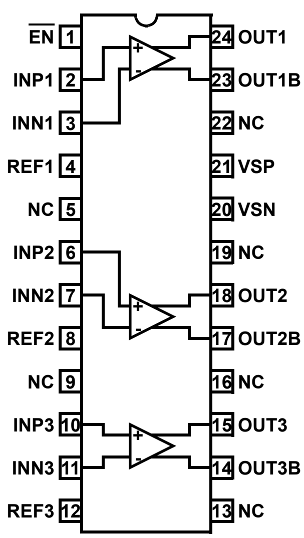
Pinouts

EL5170
(8 LD SO, MSOP)
TOP VIEW

www.DataSheet4U.com



EL5370
(24 LD QSOP)
TOP VIEW



Features

- Fully differential inputs and outputs
- Differential input range ±2.3V typ.
- 100MHz 3dB bandwidth at fixed gain of 2
- 1100V/µs slew rate
- Single 5V or dual ±5V supplies
- 50mA maximum output current
- Low power - 7.4mA per channel
- Pb-free plus anneal available (RoHS compliant)

Applications

- Twisted-pair drivers
- Differential line drivers
- VGA over twisted-pairs
- ADSL/HDSL drivers
- Single ended to differential amplification
- Transmission of analog signals in a noisy environment

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5170IS	5170IS	-	8 Ld SO	MDP0027
EL5170IS-T7	5170IS	7”	8 Ld SO	MDP0027
EL5170IS-T13	5170IS	13”	8 Ld SO	MDP0027
EL5170ISZ (See Note)	5170ISZ	-	8 Ld SO (Pb-Free)	MDP0027
EL5170ISZ-T7 (See Note)	5170ISZ	7”	8 Ld SO (Pb-Free)	MDP0027
EL5170ISZ-T13 (See Note)	5170ISZ	13”	8 Ld SO (Pb-Free)	MDP0027
EL5170IY	g	-	8 Ld MSOP	MDP0043
EL5170IY-T7	g	7”	8 Ld MSOP	MDP0043
EL5170IY-T13	g	13”	8 Ld MSOP	MDP0043
EL5170IYZ (See Note)	BAAVA	-	8 Ld MSOP (Pb-Free)	MDP0043
EL5170IYZ-T7 (See Note)	BAAVA	7”	8 Ld MSOP (Pb-Free)	MDP0043
EL5170IYZ-T13 (See Note)	BAAVA	13”	8 Ld MSOP (Pb-Free)	MDP0043
EL5370IU	EL5370IU	-	24 Ld QSOP	MDP0040
EL5370IU-T7	EL5370IU	7”	24 Ld QSOP	MDP0040
EL5370IU-T13	EL5370IU	13”	24 Ld QSOP	MDP0040
EL5370IUZ (See Note)	EL5370IUZ	-	24 Ld QSOP (Pb-Free)	MDP0040
EL5370IUZ-T7 (See Note)	EL5370IUZ	7”	24 Ld QSOP (Pb-Free)	MDP0040
EL5370IUZ-T13 (See Note)	EL5370IUZ	13”	24 Ld QSOP (Pb-Free)	MDP0040

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage (V_S+ to V_S-) 12.6V
Maximum Output Current. . . . . ±60mA
Storage Temperature Range . . . .-65°C to +150°C
Operating Junction Temperature . . . . +135°C
Recommended Operating Temperature . . . .-40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, T_A = 25°C, V_{IN} = 0V, A_V = 2, R_{LD} = 200Ω, C_{LD} = 1pF, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
AC PERFORMANCE						
BW	-3dB Bandwidth			100		MHz
BW	± 0.1dB Bandwidth			12		MHz
SR	Slew Rate	V_{OUT} = 2V_{P-P}, 20% to 80%	800	1100		V/µs
T_{STL}	Settling Time to 0.1%	V_{OUT} = 2V_{P-P}		20		ns
T_{OVR}	Output Overdrive Recovery time			40		ns
V_{REF}BW (-3dB)	V_{REF} -3dB Bandwidth	A_V =1, C_{LD} = 2.7pF		70		MHz
V_{REF}SR+	V_{REF} Slew Rate - Rise	V_{OUT} = 2V_{P-P}, 20% to 80%		125		V/µs
V_{REF}SR-	V_{REF} Slew Rate - Fall	V_{OUT} = 2V_{P-P}, 20% to 80%		65		V/µs
V_N	Input Voltage Noise	f = 10kHz		28		nV/√Hz
HD2	Second Harmonic Distortion	V_{OUT} = 2V_{P-P}, 1MHz		-79		dBc
HD2	Second Harmonic Distortion	V_{OUT} = 2V_{P-P}, 10MHz		-65		dBc
HD3	Third Harmonic Distortion	V_{OUT} = 2V_{P-P}, 1MHz		-62		dBc
HD3	Third Harmonic Distortion	V_{OUT} = 2V_{P-P}, 10MHz		-43		dBc
dG	Differential Gain at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.14		%
dθ	Differential Phase at 3.58MHz	R_{LD} = 300Ω, A_V = 2		0.38		°
e_S	Channel Separation - For EL5370 only	at f = 1MHz		85		dB
INPUT CHARACTERISTICS						
V_{OS}	Input Referred Offset Voltage			±6	±25	mV
I_{IN}	Input Bias Current (V_{IN}, V_{INB})		-10	-6	-2	µA
I_{REF}	Input Bias Current at REF Pin	V_{REF} = +3.2V	0.5	1.25	3	µA
		V_{REF} = -3.2V	-1	0	+1	µA
Gain	Gain Accuracy	V_{IN} = ±1V	1.98	2	2.02	V
R_{IN}	Differential Input Resistance			300		kΩ
C_{IN}	Differential Input Capacitance			1		pF
DMIR	Differential Mode Input Range		±2.1	±2.3		V
CMIR+	Common Mode Positive Input Range at V_{IN}+, V_{IN}-		3.2	3.4		V
CMIR-	Common Mode Negative Input Range at V_{IN}+, V_{IN}-			-4.5	-4.2	V
V_{REFIN}	Reference Input Voltage Range - Positive	V_{IN}+ = V_{IN}- = 0V	3.4	3.8		V
	Reference Input Voltage Range - Negative			-3.3	-3	V
V_{REFOS}	Output Offset Relative to V_{REF}		-140	60	+140	mV

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $T_A = 25°C$, $V_{IN} = 0V$, $A_V = 2$, $R_{LD} = 200\Omega$, $C_{LD} = 1pF$, unless otherwise specified.

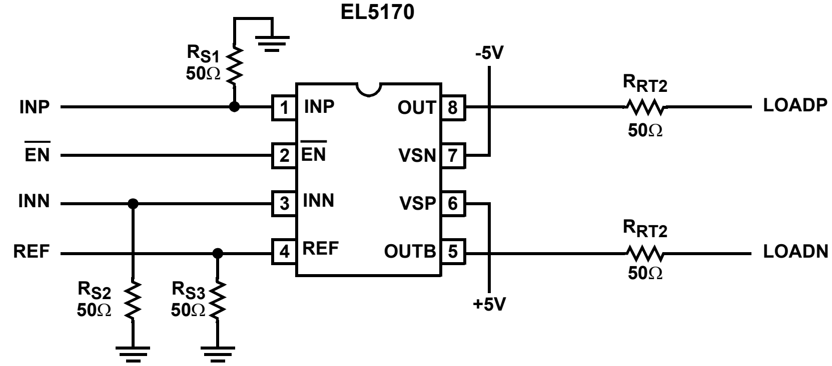
PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
CMRR	Input Common Mode Rejection Ratio	$V_{IN} = \pm 2.5V$	65	84		dB
OUTPUT CHARACTERISTICS						
V_{OUT}	Positive Output Voltage Swing	$R_{LD} = 200\Omega$	3.3	3.6		V
	Negative Output Voltage Swing			-3.3	-3	V
I_{OUT}(Max)	Maximum Output Current	$R_L = 10\Omega$ (EL5170)	±50	±80		mA
		$R_L = 10\Omega$ (EL5370)	±70	±85		mA
R_{OUT}	Output Impedance			60		mΩ
SUPPLY						
V_{SUPPLY}	Supply Operating Range	V_S+ to V_S-	4.75		11	V
$I_{S(ON)}$	Power Supply Current - Per channel		6	7.4	8.4	mA
$I_{S(OFF)}+$	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V (EL5170)	60	80	100	µA
$I_{S(OFF)}-$	Negative Power Supply Current - Disabled		-150	-120	-90	µA
$I_{S(OFF)}+$	Positive Power Supply Current - Disabled	$\overline{EN}$ pin tied to 4.8V (EL5370)	0.5	2	5	µA
$I_{S(OFF)}-$	Negative Power Supply Current - Disabled		-150	-120	-90	µA
PSRR	Power Supply Rejection Ratio	V_S from ±4.5V to ±5.5V (EL5170)	70	83		dB
		V_S from ±4.5V to ±5.5V (EL5370)	65	83		dB
ENABLE						
t_{EN}	Enable Time			200		ns
t_{DS}	Disable Time			1		µs
V_{IH}	$\overline{EN}$ Pin Voltage for Power-up				V_S+ - 1.5	V
V_{IL}	$\overline{EN}$ Pin Voltage for Shut-down		V_S+ - 0.5			V
$I_{IH\text{-}EN}$	$\overline{EN}$ Pin Input Current High - per channel	At $V_{EN} = 5V$		40	50	µA
$I_{IL\text{-}EN}$	$\overline{EN}$ Pin Input Current Low - per channel	At $V_{EN} = 0V$	-6	-3		µA

Pin Descriptions

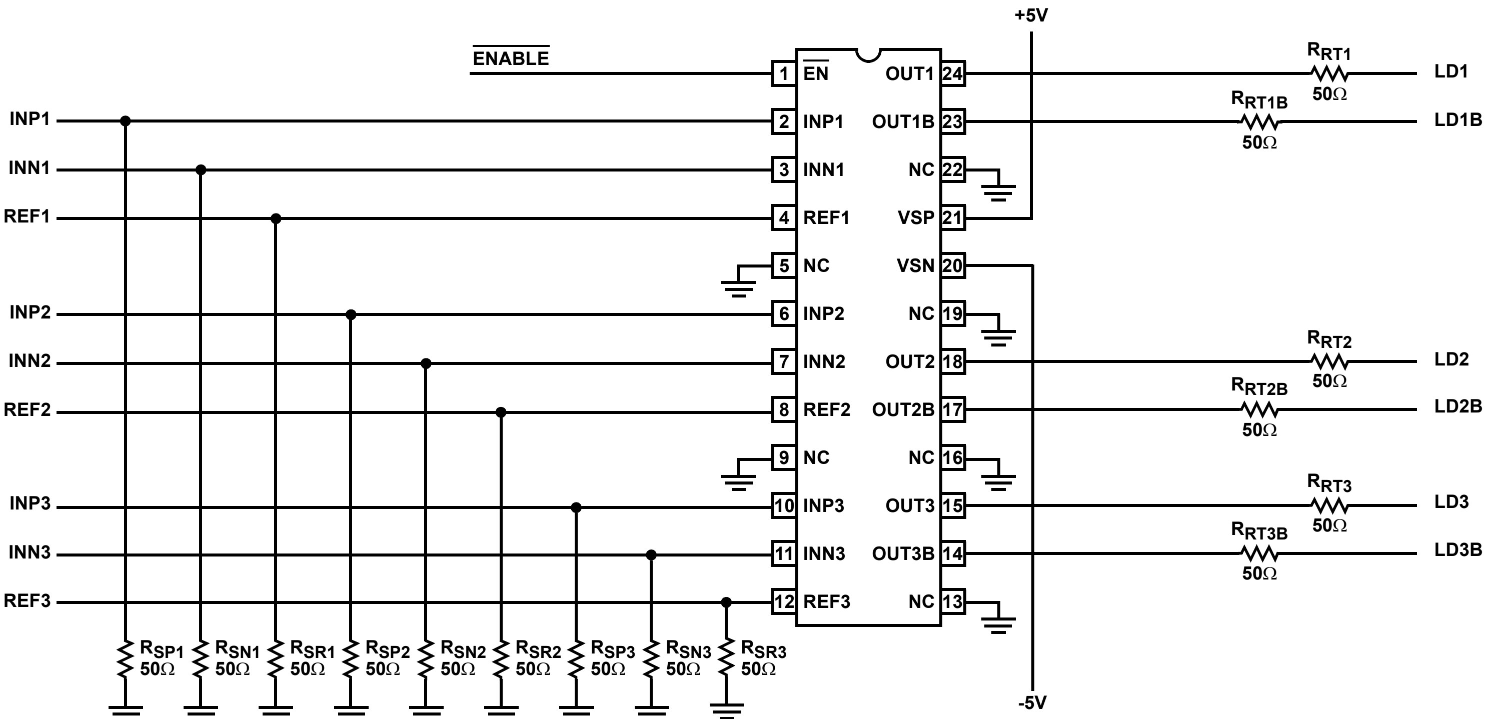
EL5170	EL5370	PIN NAME	PIN FUNCTION
1	2, 6, 10	IN+, INP1, 2, 3	Non-inverting inputs
2	1	$\overline{EN}$	$\overline{\text{Enable}}$
3	3, 7, 11	IN-, INN1, 2, 3	Inverting inputs
4	4, 8, 12	REF1, 2, 3	Reference input, sets common-mode output voltage
5	14, 17, 23	OUT-, OUT1B, 2B, 3B	Inverting outputs
6	21	VS+, VSP	Positive supply
7	20	VS-, VSN	Negative supply
8	15, 18, 24	OUT+, OUT1, 2, 3	Non-inverting outputs
	5, 9, 13, 16, 19, 22	NC	No connects, grounded for best crosstalk performance

Connection Diagrams

EL5170



EL5370



Typical Performance Curves

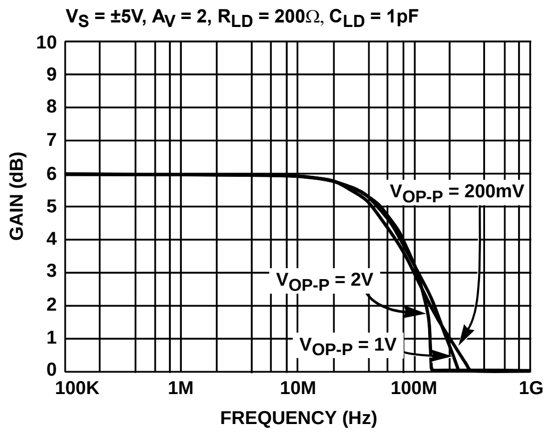


FIGURE 1. FREQUENCY RESPONSE

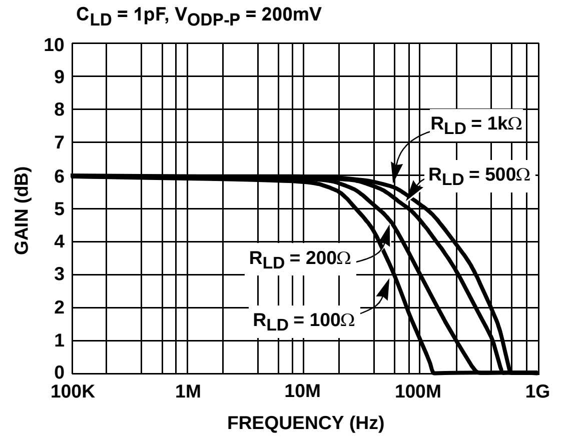


FIGURE 2. SMALL SIGNAL FREQUENCY RESPONSE vs R_{LD}

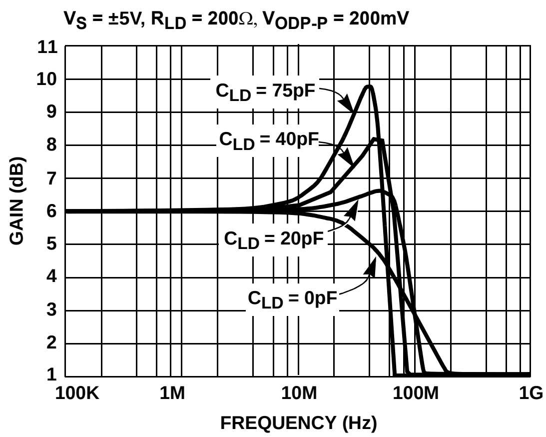


FIGURE 3. SMALL SIGNAL FREQUENCY RESPONSE vs C_{LD}

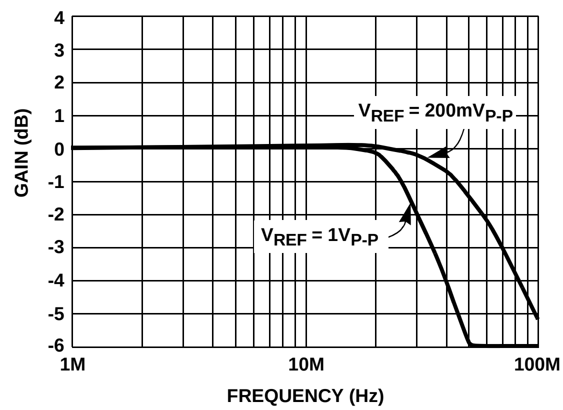


FIGURE 4. FREQUENCY RESPONSE vs V_{REF}

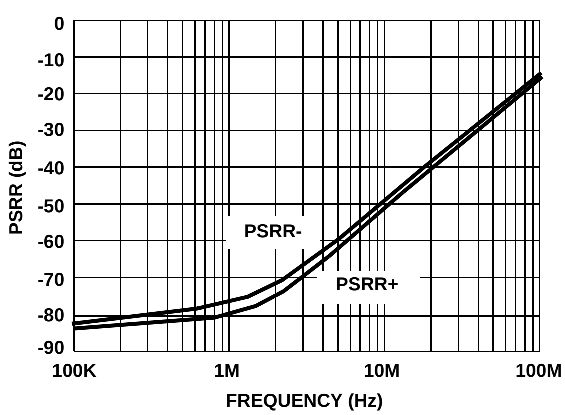


FIGURE 5. POWER SUPPLY REJECTION RATIO vs FREQUENCY

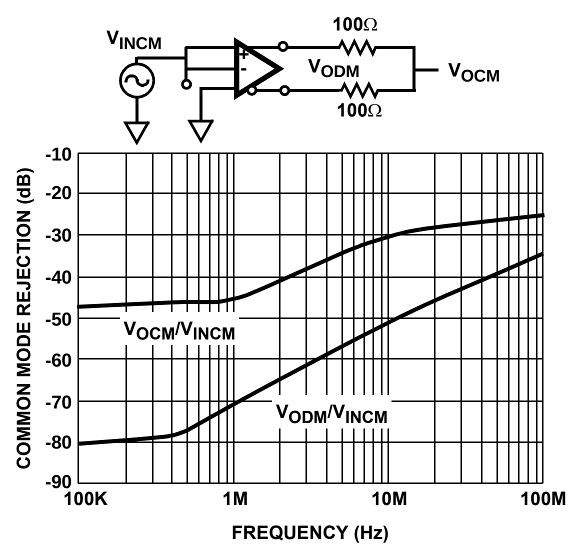


FIGURE 6. COMMON MODE REJECTION vs FREQUENCY

Typical Performance Curves (Continued)

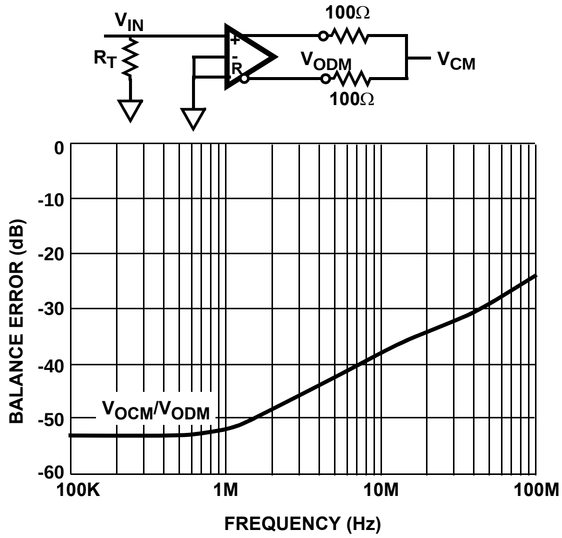


FIGURE 7. DIFFERENTIAL MODE OUTPUT BALANCE ERROR vs FREQUENCY

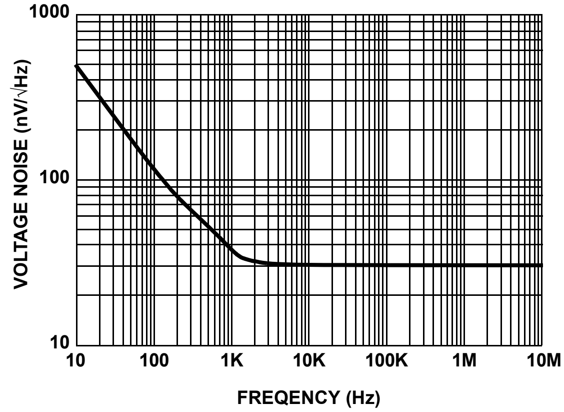


FIGURE 8. INPUT VOLTAGE NOISE vs FREQUENCY

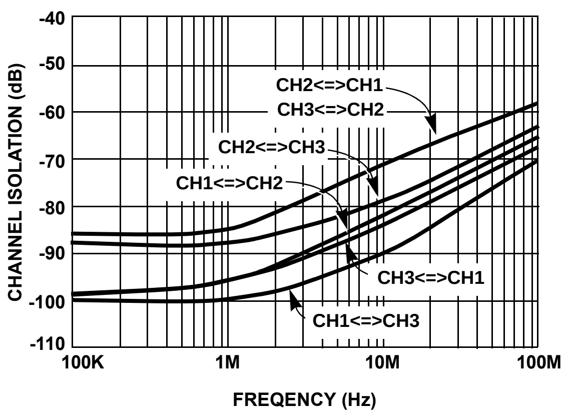


FIGURE 9. CHANNEL ISOLATION vs FREQUENCY

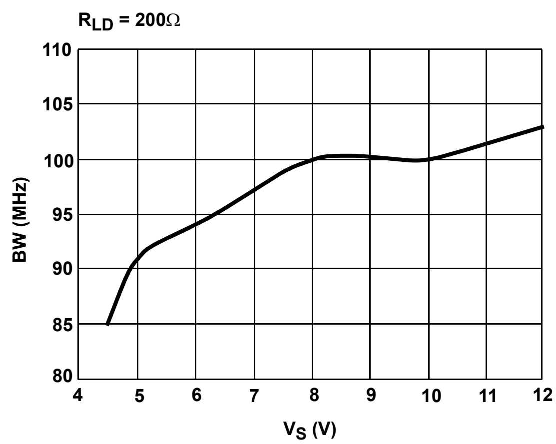


FIGURE 10. BANDWIDTH vs SUPPLY VOLTAGE

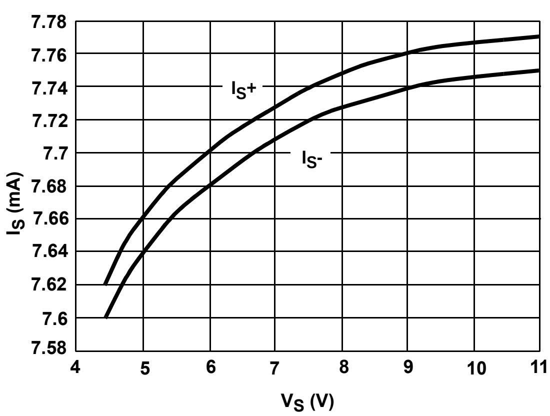


FIGURE 11. SUPPLY CURRENT vs SUPPLY VOLTAGE

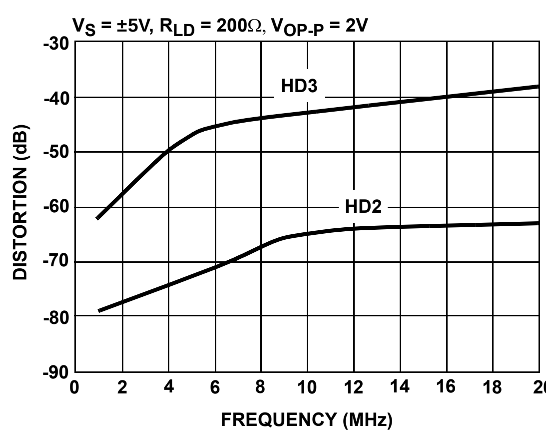


FIGURE 12. HARMONIC DISTORTION vs FREQUENCY

Typical Performance Curves (Continued)

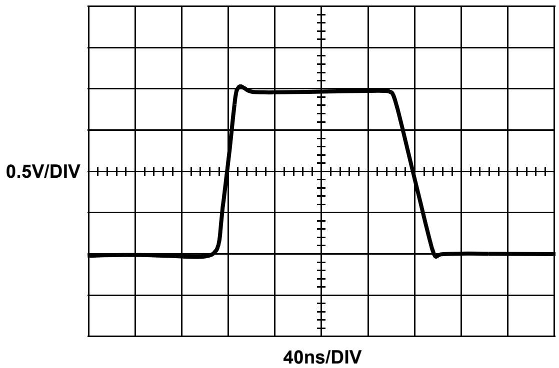


FIGURE 13. V_{COM} TRANSIENT RESPONSE

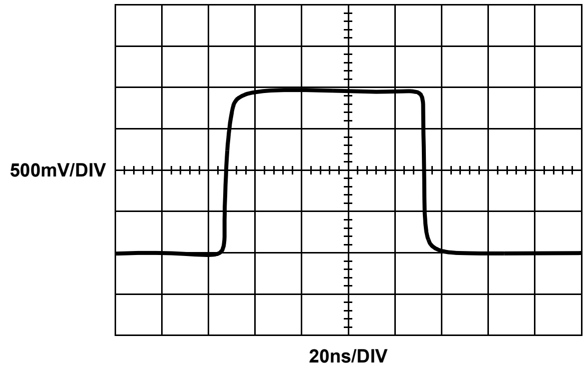


FIGURE 14. LARGE SIGNAL TRANSIENT RESPONSE

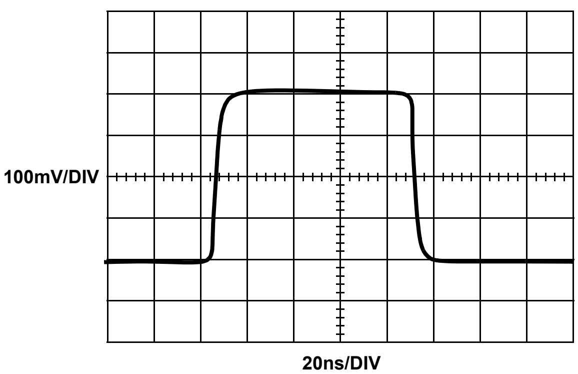


FIGURE 15. SMALL SIGNAL TRANSIENT RESPONSE

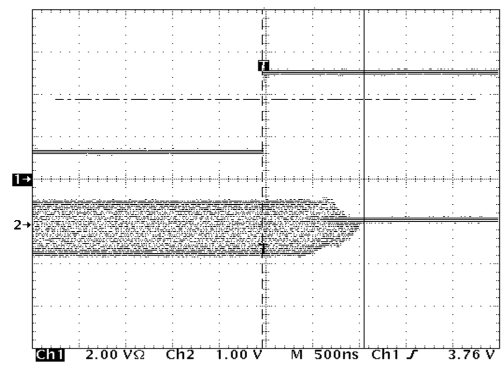


FIGURE 16. DISABLED RESPONSE

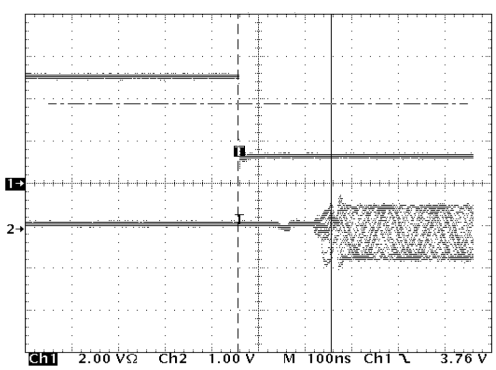


FIGURE 17. ENABLED RESPONSE

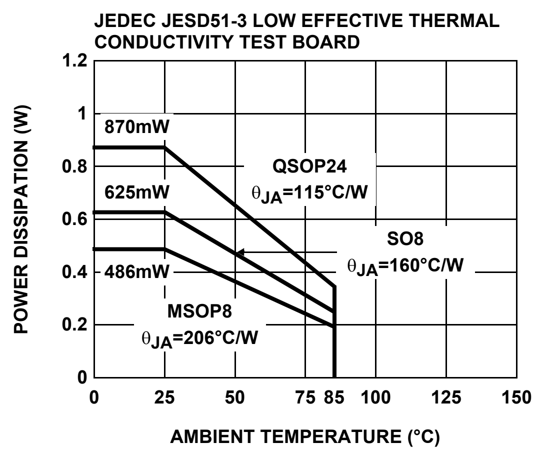


FIGURE 18. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Typical Performance Curves (Continued)

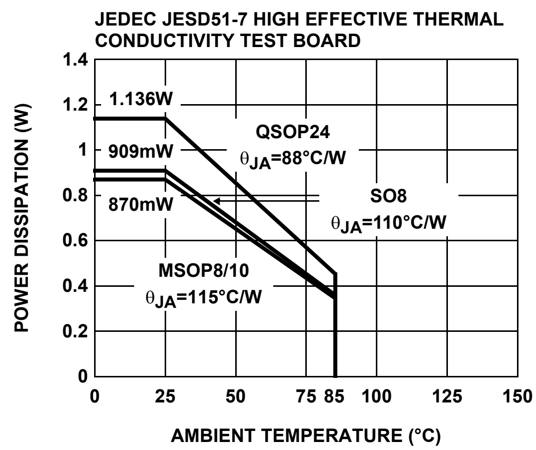
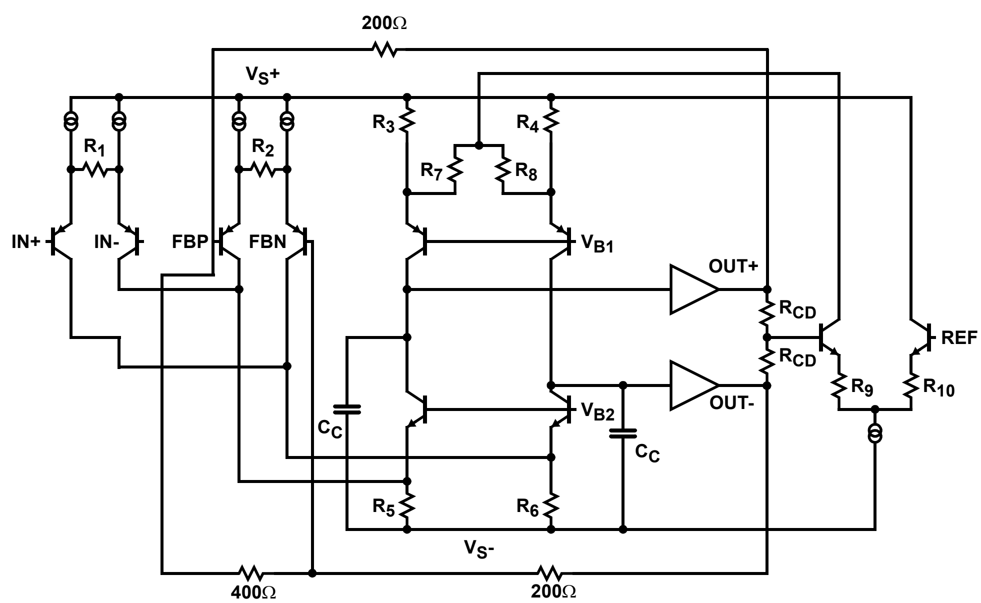


FIGURE 19. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

Simplified Schematic



Description of Operation and Application Information

Product Description

The EL5170 and EL5370 are wide bandwidth, low power and single/differential ended to differential output amplifiers. They have a fixed gain of 2. The EL5170 is a single channel differential amplifier. The EL5370 is a triple channel differential amplifier. The EL5170 and EL5370 have a -3dB bandwidth of 100MHz while driving a 200Ω differential load. The EL5170 and EL5370 are available with a power down feature to reduce the power while the amplifiers are disabled.

Input, Output and Supply Voltage Range

The EL5170 and EL5370 have been designed to operate with a single supply voltage of 5V to 10V or a split supplies with its total voltage from 5V to 10V. The amplifiers have an input common mode voltage range from -4.5V to 3.4V for ±5V supply. The differential mode input range (DMIR) between the two inputs is from -2.3V to +2.3V. The input voltage range at the REF pin is from -3.3V to 3.8V. If the input common mode or differential mode signal is outside the above-specified ranges, it will cause the output signal distorted.

The output of the EL5170 and EL5370 can swing from -3.3V to 3.6V at 200Ω differential load at ±5V supply. As the load resistance becomes lower, the output swing is reduced.

Differential and Common Mode Gain Settings

As shown at the simplified schematic, since the feedback resistors RF and the gain resistor are integrated with 200Ω and 400Ω, the EL5170 and EL5370 have a fixed gain of 2. The common mode gain is always one.

Driving Capacitive Loads and Cables

The EL5170 and EL5370 can drive 75pF differential capacitor in parallel with 200Ω differential load with less than 3.5dB of peaking. If less peaking is desired in applications, a small series resistor (usually between 5Ω to 50Ω) can be placed in series with each output to eliminate most peaking. However, this will reduce the gain slightly.

When used as a cable driver, double termination is always recommended for reflection-free performance. For those applications, a back-termination series resistor at the amplifier's output will isolate the amplifier from the cable and allow extensive capacitive drive. However, other applications may have high capacitive loads without a back-termination resistor. Again, a small series resistor at the output can help to reduce peaking.

Disable/Power-Down

The EL5170 and EL5370 can be disabled and placed their outputs in a high impedance state. The turn off time is about 1µs and the turn on time is about 200ns. When disabled, the amplifier's supply current is reduced to 2µA for I_S+ and 120µA for I_S- typically, thereby effectively eliminating the power consumption. The amplifier's power down can be controlled by standard CMOS signal levels at the ENABLE pin. The applied logic signal is relative to V_S+ pin. Letting the $\overline{EN}$ pin float or applying a signal that is less than 1.5V below V_S+ will enable the amplifier. The amplifier will be disabled when the signal at $\overline{EN}$ pin is above V_S+ -0.5V.

Output Drive Capability

The EL5170 and EL5370 have internal short circuit protection. Its typical short circuit current is ±80mA. If the output is shorted indefinitely, the power dissipation could easily increase such that the part will be destroyed. Maximum reliability is maintained if the output current never exceeds ±60mA. This limit is set by the design of the internal metal interconnect.

Power Dissipation

With the high output drive capability of the EL5170 and EL5370 it is possible to exceed the 125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for the application to determine if the load conditions or package types need to be modified for the amplifier to remain in the safe operating area.

The maximum power dissipation allowed in a package is determined according to:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\Theta_{JA}}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

$$PD = i \times \left(V_S \times I_{SMAX} + V_S \times \frac{\Delta V_O}{R_{LD}}\right)$$

Where:

V_S = Total supply voltage

I_{SMAX} = Maximum quiescent supply current per channel

ΔV_O = Maximum differential output voltage of the application

R_{LD} = Differential load resistance

I_{LOAD} = Load current

i = Number of channels

By setting the two PD_{MAX} equations equal to each other, we can solve the output current and R_{LOAD} to avoid the device overheat.

Power Supply Bypassing and Printed Circuit Board Layout

As with any high frequency device, a good printed circuit board layout is necessary for optimum performance. Lead lengths should be as sort as possible. The power supply pin must be well bypassed to reduce the risk of oscillation. For normal single supply operation, where the V_S- pin is connected to the ground plane, a single 4.7µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor from V_S+ to GND will suffice. This same capacitor combination should be placed at each supply pin to ground if split supplies are to be used. In this case, the V_S- pin becomes the negative supply rail.

For good AC performance, parasitic capacitance should be kept to minimum. Use of wire wound resistors should be avoided because of their additional series inductance. Use of sockets should also be avoided if possible. Sockets add parasitic inductance and capacitance that can result in compromised performance. Minimizing parasitic capacitance at the amplifier's inverting input pin is very important. The feedback resistor should be placed very close to the inverting input pin. Strip line design techniques are recommended for the signal traces.

Typical Applications

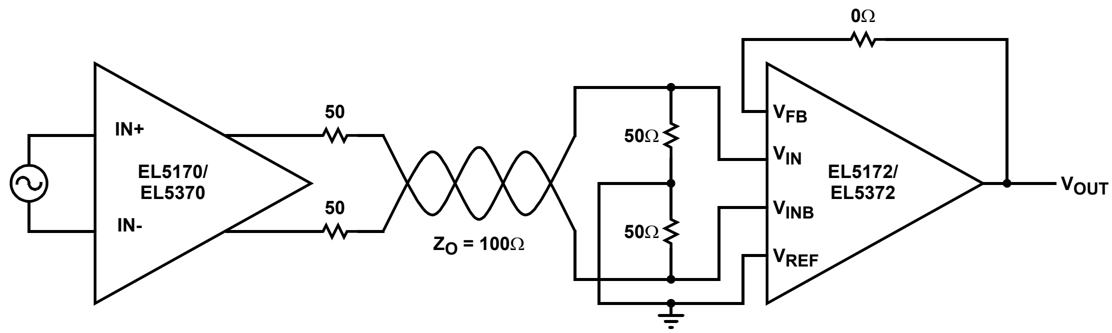


FIGURE 20. TWISTED PAIR DRIVER

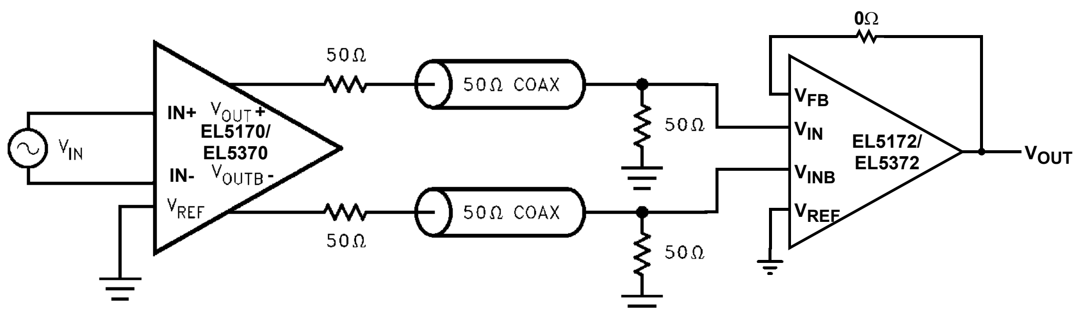


FIGURE 21. DUAL COAXIAL CABLE DRIVER

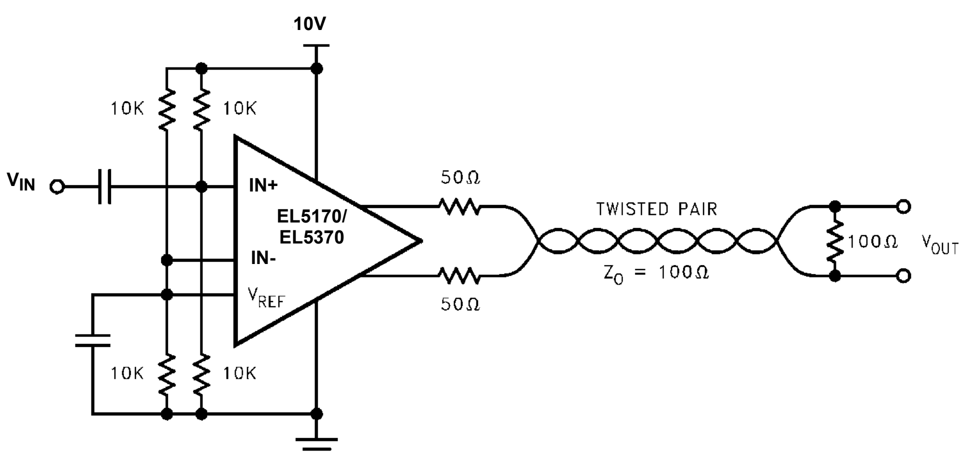


FIGURE 22. SINGLE SUPPLY TWISTED PAIR DRIVER

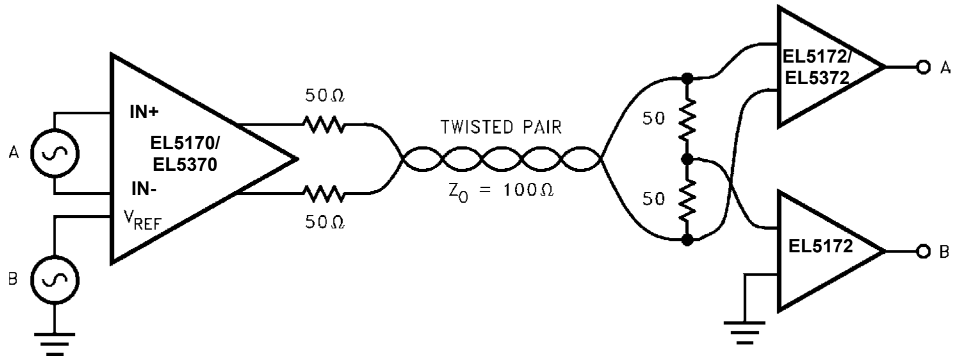
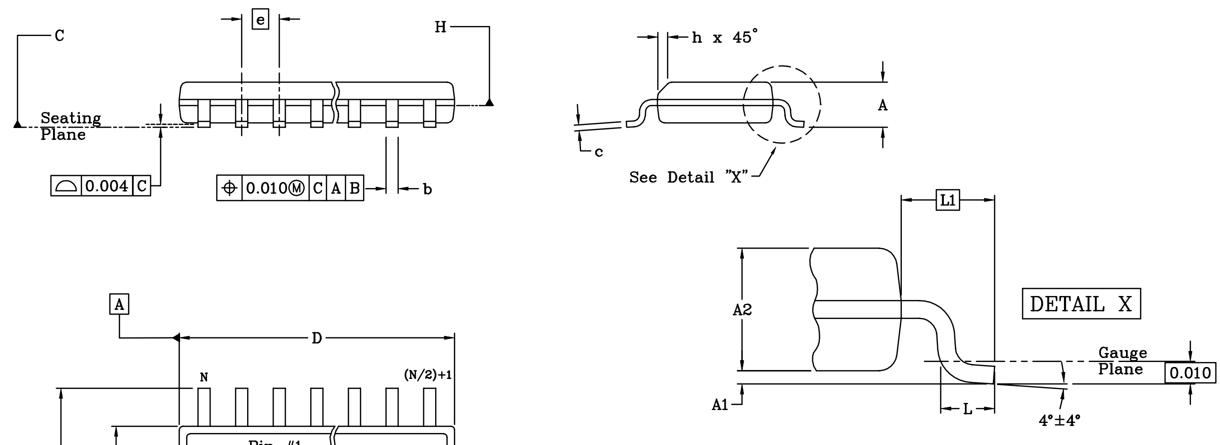
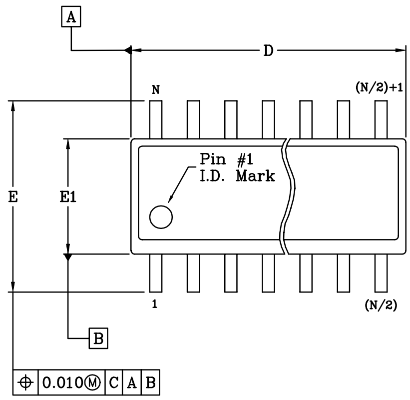


FIGURE 23. DUAL SIGNAL TRANSMISSION CIRCUIT

SO Package Outline Drawing





DIMENSION TABLE

Symbol	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	Tolerance
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX.
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	+/- 0.003
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	+/- 0.002
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	+/- 0.003
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	+/- 0.001
D (1)(3)	0.193	0.341	0.390	0.406	0.504	0.606	0.704	+/- 0.004
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	0.295	0.295	0.295	0.295	+/- 0.004
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	+/- 0.009
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference
N	8	14	16	16	20	24	28	Reference

Drawing #: MDP0027	PACKAGE OUTLINE DRAWING SMALL OUTLINE (SO) PACKAGE FAMILY
Rev: L	
Date: 2/15/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MS-012/013	

Notes:

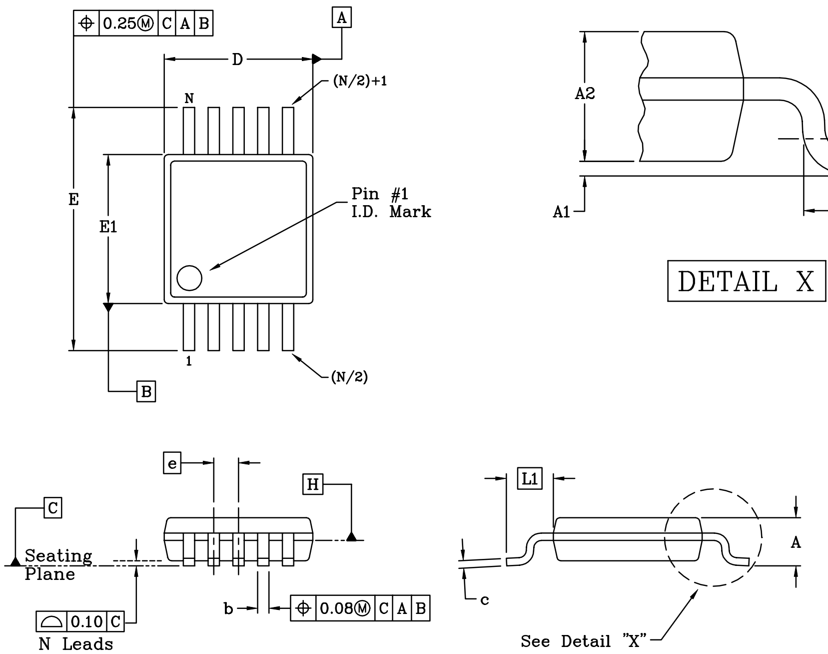
(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

MSOP Package Outline Drawing

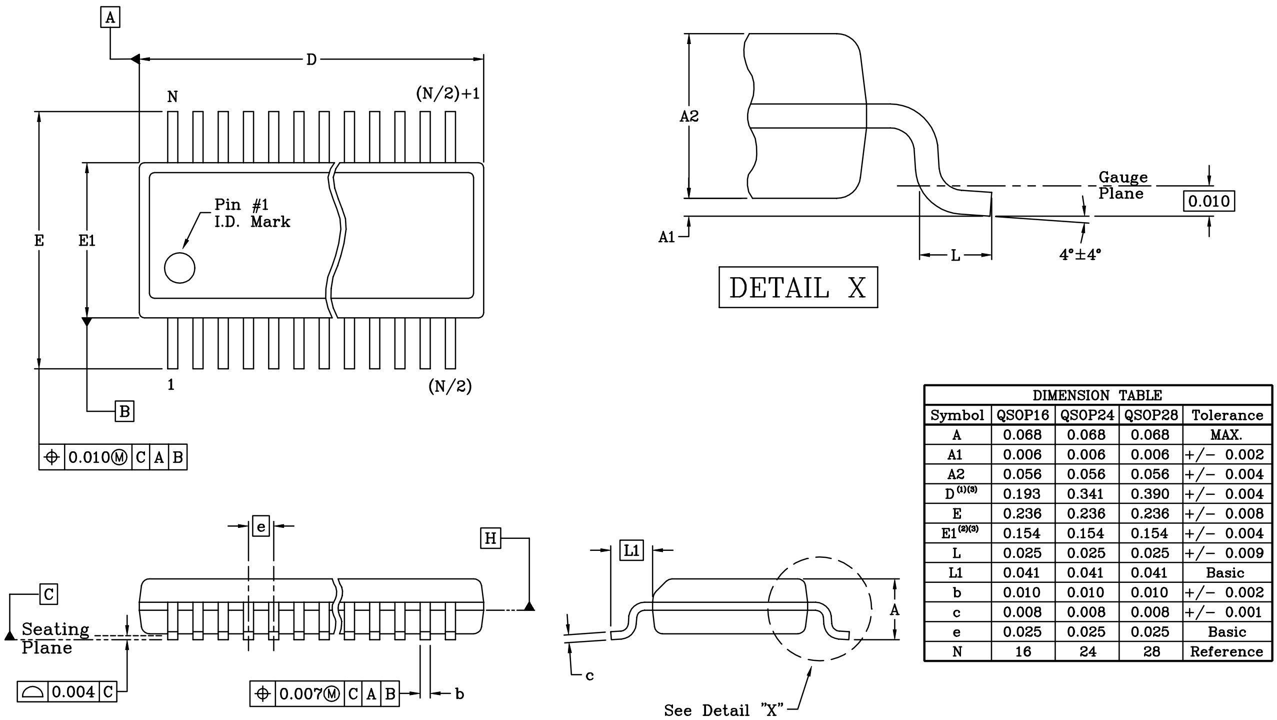


DIMENSION TABLE			
Symbol	MSOP8	MSOP10	Tolerance
A	1.10	1.10	MAX.
A1	0.10	0.10	+/− 0.05
A2	0.86	0.86	+/− 0.09
D (1)(3)	3.00	3.00	+/− 0.10
E	4.90	4.90	+/− 0.15
E1 (2)(3)	3.00	3.00	+/− 0.10
L	0.55	0.55	+/− 0.15
L1	0.95	0.95	Basic
b	0.33	0.23	+0.07/−0.08
c	0.18	0.18	+/− 0.05
e	0.65	0.50	Basic
N	8	10	Reference

Notes:
(1) Plastic or metal protrusions of 0.15 mm maximum per side are not included.
(2) Plastic interlead protrusions of 0.25 mm maximum per side are not included.
(3) Dimensions "D" and "E1" are measured at Datum Plane "H".
(4) Dimensioning and tolerancing per ASME Y14.5M−1994.

Drawing #: MDP0043	PACKAGE OUTLINE DRAWING
Rev: C	MINI SO PACKAGE (MSOP) PACKAGE FAMILY
Date: 6/14/99	
Units: mm	élantec Semiconductor, Inc.
JEDEC Reg: MO−187	HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS

QSOP Package Outline Drawing



DIMENSION TABLE				
Symbol	QSOP16	QSOP24	QSOP28	Tolerance
A	0.068	0.068	0.068	MAX.
A1	0.006	0.006	0.006	+/- 0.002
A2	0.056	0.056	0.056	+/- 0.004
D (1)(3)	0.193	0.341	0.390	+/- 0.004
E	0.236	0.236	0.236	+/- 0.008
E1 (2)(3)	0.154	0.154	0.154	+/- 0.004
L	0.025	0.025	0.025	+/- 0.009
L1	0.041	0.041	0.041	Basic
b	0.010	0.010	0.010	+/- 0.002
c	0.008	0.008	0.008	+/- 0.001
e	0.025	0.025	0.025	Basic
N	16	24	28	Reference

Drawing #: MDP0040	PACKAGE OUTLINE DRAWING QSOP – 0.150" NARROW BODY PACKAGE
Rev: E	
Date: 3/19/01	
Units: Inches	élantec Semiconductor, Inc. HIGH PERFORMANCE ANALOG INTEGRATED CIRCUITS
JEDEC Reg: MO-137	

Notes:

(1) Plastic or metal protrusions of 0.006" maximum per side are not included.

(2) Plastic interlead protrusions of 0.010" maximum per side are not included.

(3) Dimensions "D" and "E1" are measured at Datum Plane "H".

(4) Dimensioning and tolerancing per ASME Y14.5M-1994.

NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at http://www.intersil.com/design/packages/index.asp

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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

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