# Digital Signal-Processing ICs

| Type | Function | Description | Package Number of Pins |
|---|---|---|---|
| ISP9110 | 12-bit Micro-Program Sequencer | 12-bit microprogram sequencer/controller used for high speed execution of microprogram instructions stored in external memory. The ISP9110 is typically used in conjunction with bit slice processor systems and DSP building blocks to control the sequence of execution of instructions stored in microprogram memory, but can also be used in digital systems as a stand-alone control element. | 40 DIP<br>44 PLCC |
| ISP9119 | FIFO RAM Controller | The ISP9119 FIFO RAM Controller (FRC), together with a static RAM array, forms a First-in-First-Out (FIFO) buffer. The ISP9119 FRC, implemented in Harris' 1.5 micron AVLSI CMOS technology, is pin-for-pin compatible with 57/674219. This process allows the ISP9119 to operate at twice the speed, but one tenth the power dissipation of its bipolar counterpart. | 40 DIP<br>44 PLCC |
| ISP9128 | Finite Impulse Response Filter Controller | This 16-bit FIR Filter (FFC) provides all the data, history, storage, and programmable filter cycle control logic required to implement FIR filters of up to 128 filter points. | 64 DIP<br>68 PLCC<br>68 PGA |
| ISP9326 | 32-Bit Floating Point Processor | The ISP9326 is a high-speed floating point processor unit. It performs 32-bit single precision floating point addition, subtraction, and multiplication operations in a single CMOS VLSI integrated circuit using the format specified by the IEEE floating point standard 754. | 144 PGA |
| ISP9520<br>ISP9521 | Multilevel Pipeline Register | The ISP9520 and ISP9521 are multilevel pipeline registers implemented using Harris' 1.5 micron AVLSI CMOS technology. The ISP9520/21 operate at bipolar speeds with one tenth the power dissipation of their bipolar counterparts. The ISP9520 and ISP9521 are pin-for-pin compatible replacements for industry standard multilevel pipeline registers such as the bipolar AM29520 and AM29521. | 24<br>(300-mil)<br>(skinny)<br>DIP |

| Type | Description | | Package Number of Pins* |
|---|---|---|---|
| CDPS100 | CMOS Programmable Digital FIR Filters (39 or 40 tap linear phase filter operation | 20MHz throughput rate. Provides 39/40 tap linear phase or 20 tap arbitrary phase filter, 8-bit input data, 11 bit output data in 2's complement form. Expandable with no speed degradation. | 68-Q |
| CDPS110 | CMOS Least Mean Square (LMS) Adaptive FIR Filter (high-speed 8th order type) | 10MHz clock rate. Expandable to any order in multiples of 8. Eight-bit input data. 12-bit output data in two's complement format. | 68-Q |
| CDPS200 | CMOS Programmable Length FIFO (2 to 1281 sample by 10-bit wide shift register) | DC to 40MHz shift rate: Write or recirculate mode, 10 bits wide. Provides programmable length of 2 to 1281 clock cycles. | 44-Q |

* See interpretation guide and packaging section